Growth Kinetics and Electrical Characteristics of Thermal Silicon Dioxide Grown at Low Temperatures

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ABSTRACT

The oxidation kinetics and electrical characteristics of thermal silicon dioxide grown between 650 and 750°C have been measured and compared to oxides grown at higher temperatures. The majority of the growth occurs in the rapid oxidation regime. The growth rate results agree well with the theory of Massoud, with appropriate low temperature extrapolations. Chlorinated oxidation shows some growth rate enhancement. The interface state density is found to be slightly higher in low temperature oxides, although the difference is mitigated by a hydrogen sinter. The apparent breakdown field of the low temperature oxides is about 16 MV/cm, with a distribution comparable to higher temperature dielectrics. The I-V stressing characteristics of all of the thin oxides are markedly different than those of the thicker oxides. Explanations of the difference and possible mechanisms for the breakdown are presented.

One of the most useful processes in silicon based technology is oxidation. The highly perfect oxide and semiconductor/oxide interface produced by simple thermal oxidation is the basis of metal oxide semiconductor (MOS) transistors and most silicon isolation techniques. Models of the growth kinetics in this regime have been developed for one atmosphere of dry oxygen and nearly one atmosphere of steam. The classic study of this topic resulted in the linearparabolic or Deal-Grove model of oxidation. Additional studies have characterized growth rates for steam at high pressure at temperatures as low as 750°C, and in dry O₂/HCl mixtures temperatures between 900 and 1100°C. These studies have determined that for oxide thicknesses greater than 500 Å, the Deal-Grove model shows good agreement with experimental data. For thin oxides an accelerated growth was seen. This has been attributed to space charge effects, ¹⁻³ to oxide structural effects, ^{4,5} and to stress effects in the oxide. ⁶⁻⁸ One theory that seems to fit experimental data well, describes the thin oxide regime as being due to the growth occurring over a finite depth rather than directly at the surface.9

Virtually all of the oxidation models, including those relating to the thin oxidation regime, are derived from data taken at temperatures above 750°C. Furthermore since most oxides are grown in the temperature range 800-1200°C, oxidation rates at temperatures below 750°C have not been well characterized. Because of the increased importance of both very thin oxides and lower temperature processing, particularly with the advent of metastable IV-IV heterostructures, oxidation at these low temperatures is becoming increasingly interesting. In this paper we will present experimental measurements of the oxidation rates in the temperature range 600 to 750°C and compare these rates to various kinetic models. We will also present electrical characterization of these oxides, and measure the interface state density as a function of the growth temperature. It will be shown that the degradation mechanism for very thin oxides appears different than that for thicker oxides.

Experimental Technique

<100> 4 in. Czochralski silicon wafers were used in this study. The starting material was n-type, with a resistivity of 0.5-2.0 Ω -cm. A thick oxide was first grown on the surface to eliminate surface impurities. The wafers were then etched in 9:1 buffered hydrofluoric acid, rinsed, spun dry, and immediately loaded into the oxidation furnace. Oxidations were carried out in a Thermco 9001 furnace. The wafers were pushed into the furnace at the growth temperature in a nitrogen flow. The furnace was allowed to stabilize for 10 min. Nitrogen was switched off and an oxidizing

cycle was run. This consisted of either 4 standard liters per minute (slm) of oxygen flow or a combined flow of 4 slm of oxygen and 0.2 slm of HCl. Following the completion of the growth cycle, oxygen flow was terminated, and nitrogen flow was reestablished for 10 min. The wafers were then pulled from the furnace and the back side of the wafer was coated with aluminum in an electron beam evaporator for a substrate contact. Finally a photomask was applied to the front, and 2000 Å of aluminum was deposited in a thermal evaporator. The aluminum was lifted off to form the gates of the MOS structures. A final sinter was done at 450°C in an ambient of $10\%\ H_2$ in N_2 .

The oxide thickness was determined electrically and through the use of thin film analytic techniques. Electrical methods assume that the oxides have the same electrical properties as thicker films. For such thin oxides, it was determined experimentally that the capacitance in accumulation was not constant, but instead increased with increasing bias. This effect is due to the finite width of the accumulation layer. The electrons in the layer can be treated to first order as independent. If we assume a triangular well at the surface, the result is the well known Airy function 10

$$\psi_{i}(x) = A_{i} \sqrt{\frac{8\pi^{2}m^{*}q \mathcal{E}}{h^{2}}} \left[x - \frac{E_{i}}{e \mathcal{E}} \right]$$
[1]

where \mathcal{E} is the electric field at the Si/SiO₂ interface, m^* is the effective mass, and E_i is the ith energy level. The average distance of an electron in the ith state is given by $2E_i/3q$ \mathcal{E} .

We have chosen to measure all of our accumulation capacitances at surface potentials of $25\ kT$. The expectation value of the accumulation layer thickness for the corresponding field is about $40\ \text{Å}$. From a capacitive standpoint this corresponds to an equivalent oxide thickness of $13.3\ \text{Å}$, and the capacitance per unit area of the gate is given by

$$C_{\text{gate}}(25 \ kT) = \frac{\epsilon_{\text{ox}}}{t_{\text{ox}} + 13.3 \ \text{Å}}$$
 [2]

As shown in Fig. 1, when this simple quantum correction is taken into account, the optical and electrical measurements are in generally good agreement. This suggests that to a good approximation these thin oxides can be treated as simple SiO_2 layers, without regard to chemical composition gradients. The oxide thicknesses that we report here will be those electrically measured in this manner.

Kinetic Results and Discussion

Figure 2 shows a plot of the experimental growth thickness. All of the wafers show an initial oxide of about 20 Å.

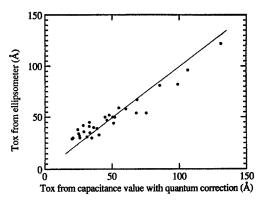


Fig. 1. Scatter plot of capacitive and optical measurements of oxide thickness.

The basic oxidation model is the Deal-Grove equation

$$x_o^2 + Ax_o = B(t + \tau)$$
 [3]

where the initial time τ is given by

$$\tau = \frac{x_i^2 + Ax_i}{B}$$
 [4]

and x_i is the initial oxide thickness. The linear and parabolic rate coefficients follow Arrhenius behavior at high temperature

$$B = 725 \frac{\mu m}{hr} e^{\frac{-1.24 \text{ eV}}{kT}}$$

$$\frac{B}{A} = 5.82 \cdot 10^6 \frac{\mu \text{m}^2}{hr} e^{\frac{-2.00 \text{ eV}}{kT}}$$
[5]

If we extrapolate these equations to the growth conditions the predicted thicknesses are shown as solid lines in Fig. 2. The experimental data lie above the prediction of the Deal-Grove model, even allowing for the native oxide. A growth enhancement mechanism is therefore occurring (or the extrapolated behavior of the oxidation coefficients are incorrect).

The presence of an initially enhanced growth rate has been taken into account by Massoud⁹ by adding two additional terms to the basic Deal-Grove growth rate equation

where L_1 is of order a few angstroms. For all of the measurements taken in this paper $x_0 >> L_1$, and so the second term can be neglected. In this model L_2 is assumed to be an effective thickness over which the oxidation occurs. Mas-

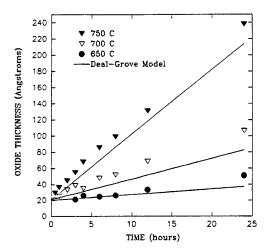


Fig. 2. Comparison of low temperature oxide thickness vs. time and the basic Deal-Grove model.

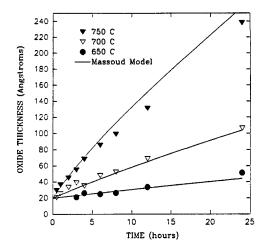


Fig. 3. Comparison of low temperature oxide thickness and the Massoud model.

soud determined C_2 and L_2 by fitting to experimental data in the range of temperatures 800 to 1000°C. Over this temperature range it was determined that for <100> silicon in dry oxygen

$$C_2 \approx 6.57 \cdot 10^{10} \frac{A}{\text{min}} e^{\frac{-2.37 \text{ eV}}{\text{kT}}}$$
 [7]

and L_2 is a constant value of 69 Å. In the limit of short time growth

$$\frac{dx_0}{dt} \approx \frac{B}{A} + C_2 e^{-\frac{x_0}{L_2}}$$
 [8]

This can be solved analytically

$$x_{o} = L_{2} \ln \left[e^{\frac{B \operatorname{tot}}{A \operatorname{L}_{2}}} - \frac{A}{B} C_{2} \right]$$
 [9]

where

$$\tau = \frac{A}{B}L_2 \ln \left[e^{\frac{x_1}{L_2}} + \frac{A}{B}C_2 \right]$$
 [10]

For temperatures of interest, the extrapolated values of A are at least 3 times larger than x_0 for the longest times studies; the linear approximation is therefore allowed. Figure 3 compares the result of extrapolating the linear rate coefficient, L_2 , and C_2 , and inserting these values into Eq. 8, with the experimental data. A better agreement is obtained than for the Deal-Grove model, although some adjustment of the L_2 , and C_2 parameters could certainly improve the fit.

Previous studies have shown that the addition of HCl results in the improvement of threshold stability and dielectric strength. It has also been reported that the addition of HCl increases the oxide growth rate. For <100> silicon Hess and Deal¹¹ reported that for high temperatures the parabolic rate constant increases as a weak exponential at 900°C, which was the lowest temperature studied in sufficient detail to form conclusions. From 0 to 5% HCl, B increased by about 40%. At 900°C the linear rate coefficient increased by a factor of 2 with the addition of 1% HCl and staved constant for higher concentrations. A set of growths was done at 700°C in a 5% HCl in O2 ambient. Figure 4 shows the results. An accelerated growth behavior was observed relative to the runs done in pure oxygen. If we fit this data to the Massoud model and assume that L_2 and τ remain fixed, the result is the solid line through the HCl data. The linear rate coefficient and C_2 are both larger than the corresponding values for nonchlorinated oxides by a factor of 1.8 and 1.2, respectively. The linear rate coefficient is in good agreement with the enhancement projected at low temperature from the data of Hess and Deal.

A chemical analysis was completed on one HCl grown and one dry O_2 grown oxide using SIMS. The measurements were done in a Riber MIQ-156 system with a 50 pA O_{18}^- beam and a 4 kV accelerating voltage. Negative ion

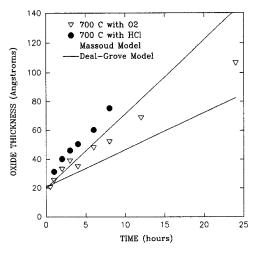


Fig. 4. Growth enhancement at 700°C in a 5% HCl ambient.

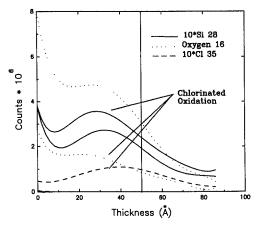


Fig. 5. SIMS profiles of low temperature oxidations. Depth scale inferred from oxide thickness measurement using ellipsometry.

collecting was used. The results are shown in Fig. 5. The depth scale was inferred from the oxide thickness measured using ellipsometry prior to profiling. Although some profile broadening is seen in these conditions, the relative amplitudes of the profiles are instructive. The HCl grown oxide shows considerable Cl incorporation, with a peak near the $\mathrm{Si/SiO_2}$ interface, in general agreement with reports from higher temperature growths. It is not clear whether Cl has become incorporated in the underlying silicon or whether this is a knock-on artifact of the data. Mass 35 (HCl) is only seen at the surface of the oxide grown in pure oxygen. This is believed to be a surface contaminant.

Electrical Results and Discussion

In order to measure the quality of the oxide the capacitors were characterized by breakdown distributions, C-V analysis, and time dependent dielectric breakdown (TDDB). Figure 6 shows a typical breakdown curve for approximately 50 Å thermal oxides grown at 650, 700, 750, and 900°C. The wafers were tested by ramping the positive voltage on the gate electrode, driving the device into accumulation. The capacitors were 400 by 400 μm. Breakdown was taken to occur at the point of an irreversible current increase. Although the breakdown fields appear low, this was found to depend on the gate electrode and post electrode deposition processing. Shown in Fig. 6 are two dielectrics with polysilicon electrodes. These devices showed similar TDDB behavior to the aluminum electrodes unless a high temperature (900°C) sinter is added after polysilicon deposition. In that case the apparent breakdown fields of the devices exceeded 16 MV/cm. This number however fails to take into account the finite width of the accumulation layer. In general we can say that the time dependent dielectric breakdown evaluation of the low tem-

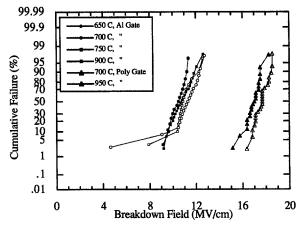


Fig. 6. Breakdown curves for oxides grown at 650, 700, 750, and 900°C with aluminum gates and for oxides grown at 700 and 950°C with polysilicon gates.

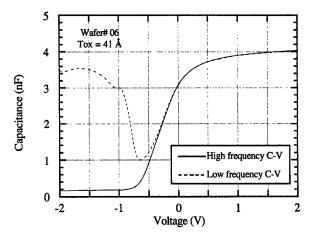


Fig. 7. Typical high and low frequency C-V traces.

perature oxides are comparable to their high temperature counterparts when the same gate electrode is used.

Figure 7 shows 100 Hz and 1 MHz C-V traces of a typical low temperature oxide, prior to hydrogen sintering. Measurements taken at low frequency were done under illumination to ensure true low frequency behavior. Good agreement was seen between the 100 Hz data and true quasi static C-V results. Interface state densities extracted using the Castagne, 12 Berglund, 13 and Terman 14 methods showed good agreement. The interface state density for all four oxides prior to the hydrogen sinter is shown in Fig. 8. The $D_{\rm it}$ of the 900°C oxide was about half that of the lower

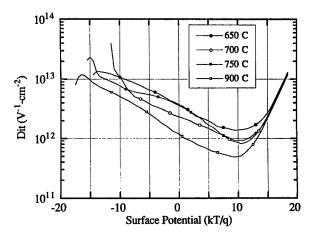


Fig. 8. Interface state density in the bandgap with growth temperature as a parameter.

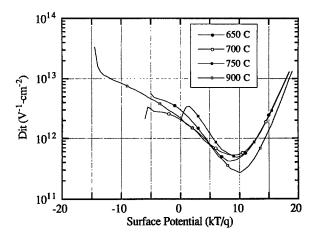


Fig. 9. Interface state density after a hydrogen anneal.

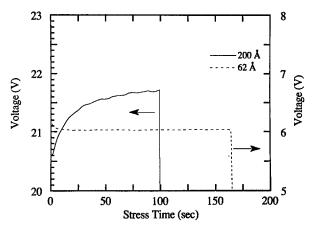


Fig. 10. Constant current stress characteristics of 200 and 62 Å oxides.

temperature oxides. No significant difference is seen between the three low temperature oxides. The addition of the forming gas anneal sharply reduces $D_{\rm it}$ for all four oxides (Fig. 9), but the 900°C oxide remains slightly better than the lower temperature oxides.

To investigate the breakdown mechanism of the thin oxides grown in this study, ramped voltage, constant voltage, and constant current time dependent breakdown (TDDB) measurements were performed on all of the samples. Figure 10 compares constant current stress measurements for 200 and 62 Å oxides. The thick oxide shows an increasing voltage that saturates as the breakdown point is approached. This effect is generally understood to represent negative charge trapping in the bulk of the oxide. ¹⁵ These charges reduce the electric field in the oxide conduction

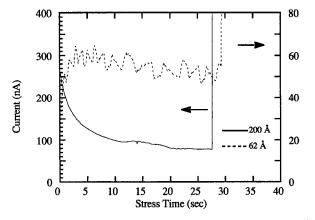


Fig. 11. Constant voltage stress characteristics of 200 and 62 $\mbox{\normalfont\AA}$ oxides.

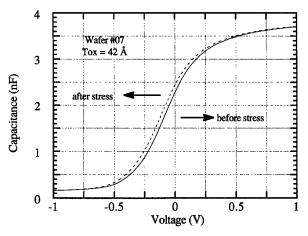


Fig. 12. High frequency C-V characteristic before and after stress.

band and therefore reduce the current flow. On the linear scale the thin oxides show a brief initial peak, then decrease much more slowly than the thicker oxides. No evidence of negative charge trapping is seen for any growth temperature. The constant voltage results are shown in Fig. 11. The stress current through the thick oxide drops by a factor of 3.4 from the initial value. The thin oxide shows a smaller initial increase in the stress current, then decays very slowly.

Figure 12 shows the high frequency C-V curves after constant current stressing of 1.56 µA/cm² for 20 s. A small negative shift corresponding to positive charge trapping is seen. The magnitude of this shift is in good agreement with previous results. 15 It is generally thought that this charge represents trapped holes. In thicker oxides holes are generated primarily by impact ionization. For thin oxides it is much more likely that holes are injected from the gate electrode16 (Fig. 13). After the electrons tunnel into the oxide they thermalize and drift toward the gate electrode. Energetic electrons collected at the gate excite surface plasma oscillations. These decay into hot electron-hole pairs. These energetic holes may then be thermionically emitted over the barrier or tunnel through the barrier into the oxide. Once in the bulk of the oxide they encounter traps. The position of the centroid of these charges is unknown, but due to the thinness of the oxide, it is probably near the

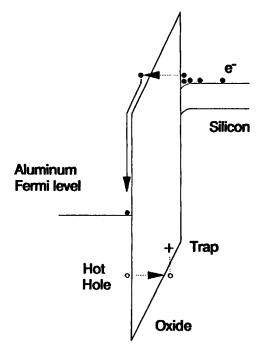


Fig. 13. Band diagram of stress behavior.

center or the trapped holes would tunnel. The appearance of the positive charge suggests that the thin oxides may break down by the same mechanism as thicker oxides: positive feedback of the tunneling current which is caused by barrier narrowing due positive charge accumulation near the substrate. For ultrathin oxides even the center of the dielectric film may be sufficiently near the substrate to effectively contribute to barrier narrowing.

This model of positive charge generation can also be used to explain the observed breakdown results. The morphology of the SiO₂/gate electrode interface strongly influences the hot hole injection rate, and therefore the charge to breakdown. We have found the charge to breakdown figure for these tests to increase by several orders of magnitude if a high temperature anneal is done after gate electrode deposition.¹⁷ Since the aluminum gates cannot tolerate high temperature processing, those breakdown fields were rather low. We believe that the negligible negative charge trapping seen in the constant current and constant voltage TDDB characteristics of the thin oxides is a result of electron tunnel annealing. The distance to either electrode is so short in these devices that electrons readily detrap. Holes associated with positive traps however are much less prone to annealing and therefore build up.

Summary

Silicon wafers were oxidized in the temperature range 650-750°C. The oxidation kinetics were fit to the thin oxide growth model of Massoud et al. 9 Parameters derived from fitting these equations agree with extrapolated values. Low temperature oxides show similar breakdown fields to high temperature oxides. The interface state density of these oxides is slightly higher than our high temperature control oxide, but seems to be independent of oxidation temperature over the range 650-750°C. A shift of the high frequency C-V curves corresponding to a positive charge was seen. This suggests that the breakdown mechanism of the thin oxides may be similar to thicker oxides: hole trapping. It is speculated that the source of these holes is the gate electrode. The I-V characteristics of the time dependent breakdown was qualitatively different for all oxides in the 4070 Å range. This effect is believed to be due to the absence of electron trapping in ultrathin oxides.

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A Kinetic Study of Reactive Ion Etching of Tungsten in SF₆/O₂ RF Plasmas

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ABSTRACT

The reactive ion etching of chemically vapor deposited (CVD) tungsten in SF₆/O₂ plasma has been investigated by means of optical emission spectroscopy, mass spectrometry, and in situ x-ray photoelectron spectroscopy. This study is particularly focused on the etching of WO₃ over W, a native oxide 34-45 Å thick (WO₃) always appearing on the CVD tungsten surface. Actinometry measurements show an excess of atomic fluorine and oxygen relative concentrations during the etching of the WO₃ layer as compared to that of tungsten. Two etch products of tungsten are detected by mass spectrometry: WF₆ and WOF₄. In pure SF₆ plasma, the main etched product of WO₃ and W is WF₆. In SF₆/O₂ (40/60) plasma, WF₆ is the dominant product of the etching of the WO₃ layer and WOF₄ that of W. In situ XPS analyses show the presence of fluorine, oxygen, and sulfur on the etched tungsten surface. The role of these elements in the formation of the two etch products of tungsten is discussed.

Tungsten is currently used as interconnection material for the first metallization level in very large scale integration (VLSI) technology. By reason of its high melting point, its low resistivity, and its high electromigration resistance, tungsten takes precedence of place over aluminum. This metal could be also used as gate material for submicron devices. Reactive ion etching allows fine line pattern definition of interconnect structures to be obtained. Fluori-

nated gases such as CF4 and SF6, mixed with O2, are frequently used in dry etching of tungsten.¹
Previous studies²⁻⁴ have shown the influence of the con-

centration of fluorine and oxygen atoms on the formation of the etched products of tungsten, WF₆ and WOF₄, in the SF₆/O₂ plasmas. However, the detailed mechanism of the formation of the etch products is not well understood. Moreover etching is frequently described in a steady-state