Spring 1-1-2013

Process Variation in Silicon Photonic Devices

Xi Chen
University of Colorado at Boulder, flycanvas@gmail.com

Process Variation in Silicon Photonic Devices

by

Xi Chen

B.S., Peking University, 2006

M.S., University of Colorado Boulder, 2009

A thesis submitted to the

Faculty of the Graduate School of the

University of Colorado in partial fulfillment

of the requirements for the degree of

Doctor of Philosophy

Department of Electrical, Computer and Energy Engineering

2013

This thesis entitled:
Process Variation in Silicon Photonic Devices
written by Xi Chen
has been approved for the Department of Electrical, Computer and Energy Engineering

_____

Prof. Alan Mickelson

_____

Prof. Li Shang

Date _____

The final copy of this thesis has been examined by the signatories, and we find that both the content and the form meet acceptable presentation standards of scholarly work in the above mentioned discipline.

Chen, Xi (Ph.D., Electrical Engineering)

Process Variation in Silicon Photonic Devices

Thesis directed by Prof. Alan Mickelson

The high index contrast of the silicon - silicon dioxide material system allows for dense integration of optical waveguide devices. Possible applications include intra-chip, inter-chip and fiber optic interconnection systems. Optical intra-chip interconnections become more desirable as the complementary metal-oxide-semiconductor (CMOS) circuit density puts ever tighter constraint on on-chip interconnection performance. Board level, rack level and rack-to-rack data center interconnections are ever more constrained by space and bandwidth to which silicon photonic modules may offer an improvement. As fiber optic systems serve smaller and smaller area systems, integrated switching systems that are enabled by silicon photonic devices involving wavelength division multiplexing (WDM) become more desirable.

In this thesis, we firstly take a brief review of the development history of information technology, optical communication and silicon photonics. Secondly we examine the optical performance of an array of photonic devices which are the basic building blocks for silicon photonic circuits. Thirdly we turn the attention to the fabrication related issues. Silicon photonic circuits are prone to the thermal and fabrication induced process variations. We discover the process variation exhibits a "random walk" pattern with spatial extent at wafer scale. Fourthly we propose a simple method to extract fundamental parameters out of fabricated silicon photonic devices. Based on the systemic wafer-scale measurement results, our method combines the advantage of both numerical simulation and simple analytical modeling techniques. Lastly, we propose a variation-aware on-chip interconnect design for multi-core processors. This design adapts to on-chip thermal and process variation effects, pointing to the improvement of wafer-scale fabrication yield and interconnect network communication throughput.

Dedication

To my family.

Acknowledgements

In the journey of my Ph.D. study here in Boulder, I feel so fortunate to have Prof. Alan Mickelson as my academic advisor. Alan introduced me to this fascinating topic of silicon photonics that eventually develops into a thesis. Besides exciting results I discovered in lab through out the years, the process of research could be challenging at times. Alan's wisdom and kindness constantly encourage me to overcome barriers and lead me to greater achievements. I always enjoy the office meeting with Alan and his humor always brings out a little laughter after long serious discussion.

I also would like to extend my sincere gratitude to my thesis committee members: Prof. Dejan Filipovic, Prof. Juliet Gopinath, Prof. Yung-Cheng Lee, Prof. Wounjhang Park and Prof. Li Shang. It has been a great experience to collaborate with them on various projects at different stages of my study and learn from their advices and insights.

My fellow labmates and colleagues have been very supportive to each other's work and I enjoy the positive atmosphere we have at the Guided Wave Optics Lab (GWOL). I would like to express my thankfulness to Dr. Zheng Li, Dr. Moustafa Mohamed, Dr. Hongyu Zhou, Dr. Eric Dudley, Dr. Brian Schwartz, David Espinoza, Jyothi Karri, Jian Wang, Todd Houghton, Keyon Janani, Eric Jacobson and Dr. Yonghao Cui for their direct and indirect contributions to this thesis.

I would like to thank Jim Marcelli and folks at Lightwave Logic Inc. for their support of my research. I would not forget the countless helps from friends in the ECEE administrative office. My appreciation also goes to all the other friends in the ECEE department and at CU.

Finally, I would like to express my deep love to my family for their enormous support and love in my life.

Contents

Chapter

Tables

Table

Figures

Figure

Chapter 1

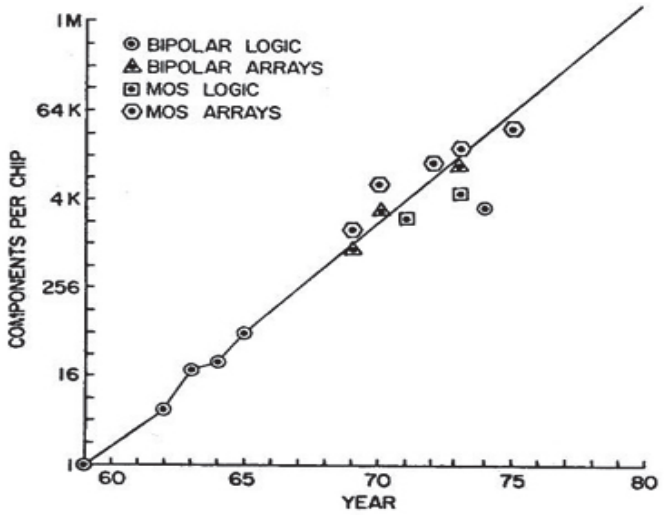
Introduction

1.1 Moore's Law and Beyond

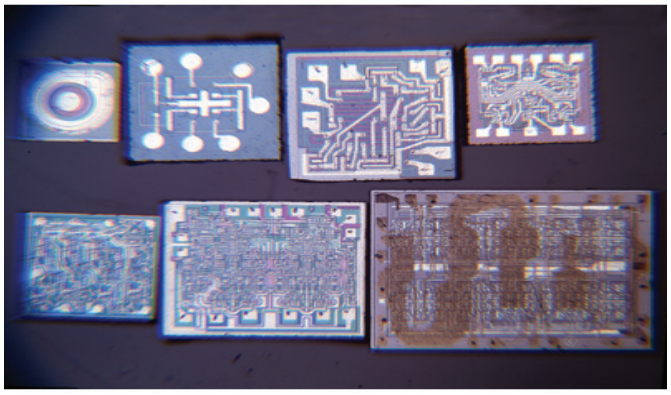
In the modern society, we enjoy daily life with the convenience that advanced communication and computation technologies bring to us. Mobile broadband and high-speed Internet keep people stay connected almost everyday and everywhere around the world. Information is transmitted and shared in the global community at an unimaginable fast rate. Data centers, supercomputing centers and cloud computing service businesses are growing ever faster around the world. Enormous amount of data is generated, stored and processed at every second to meet the society development needs and help accelerate scientific exploration and advancement. All of these activities started with the invention of the Integrated Circuit (IC) technology when Robert Noyce filed the "Semiconductor device-and-lead structure" patent in the late 1950s with engineers from the legendary Fairchild Semiconductor. Ever since, the semiconductor industry began a race for producing IC chips with denser and denser transistor components. From the small-scale integration (SSI) and medium-scale integration (MSI) in 1960s to the very large-scale integration (VLSI) in the 1980s and the modern three-dimensional integrated circuit (3D-IC), each step represents breakthroughs in terms of industry material research and circuit fabrication progress.

One of the driving principles and guidelines enabling higher density integration in the semiconductor industry was defined by Gordon Moore in his 1965 paper [1] where he observed and predicted the number of components in integrated circuits doubles every year since the invention of integrated circuits. A period of eighteen-month later became the industry standard for a doubling

in chip performance and widely known as the “Moore’s Law”.



(a)



(b)

Figure 1.1: (a) Data for the component counts on IC chip during 1960s and 1970s verifies the Moore’s Law. (b) Images of IC chips that were used in constructing the Moore’s Law.[1]

[1] Image (a): courtesy of Intel Corporate. Image (b): courtesy of Fairchild Camera & Instrument Corporation.

Moore's Law has been accurate for half a century. Figure 1.1 illustrates this trend for transistor component counts in the early 1960s and 1970s, together with the images of early IC chips. The semiconductor industry has been striving to keep up with the pace defined by this trend. The critical dimension (the gate length) of transistor on the IC chip is shrunk down from 10-100 μm range in the early IC chips to the current sub-100 nm. The integration density has improved exponentially from the 60 transistors of 1965 as shown in the figure to today's over one billion transistors in an area the size of a fingernail. Decades of research and investment has substantially boosted IC chip's performance while the cost of manufacturing drops down dramatically. At present, the cost of a single transistor on IC chip is estimated to be comparable to that of a printed newspaper character. Information is being generated and shared at a more and more affordable rate around the world.

With the ever glowing demands for information technology and transistor reaching its physical limit for the critical dimension, the concern is that the semiconductor industry would soon meet the end of Moore's Law. A closer examination reveals that there are problems associated with the higher and higher density in IC chip integration. One important issue is that the high power density of IC chips becomes untenable. Take the microprocessor for example. Transistor density growth inherently brings up power usage on chip. Even though the power consumption increment trend slows down, the overall processor power has exponentially grown to over 100 Watts today for high performance microprocessors [2, 3]. The power consumption requirement would limit chip achievable performance and becomes a significant constraint for modern chip design [4]. Power density at some point would reach a level that is beyond the capability of heat extraction [5]. Hot spot on chip would substantially cause issues for the overall on-chip thermal management, leakage current, cooling cost and reliability [6, 7, 8].

The rising constraint towards the on-chip power density changes the approach of processor design in computer system. Over the past few years, multi-core and many-core structures emerged as one way to keep the chip performance scalability alive [9, 10, 11, 12]. Parallel computing is an energy-efficient way to achieve high performance. In this new paradigm, innovations are being

explored on the chip architecture and circuit design towards low power, high efficiency computing domain [13, 14, 15, 16].

1.2 The Electrical Interconnection

The idea of parallel computing in multi-core and many-core microprocessor on a single chip began to thrive since IBM delivered the first general-purpose non-embedded multi-core processor, the POWER4, in 2001 [17]. In these systems, while chip performance can be enhanced with multiple processor cores, chip size also grows. One of the interesting and challenging problems is the wiring and latency issue in the on-chip interconnection, that is, how to build effective communication channels among cores and chips without sacrifices on delays. Solving the problem on wiring delay is equally important as improving transistor's switching speed, as wiring delay gradually becomes a dominant issue that hampers efficiently utilizing each clock cycle in microprocessor [18]. On-chip communication turns into a key performance bottleneck. For instance, the total on-chip wire length is estimated to be more than 2 km/cm^2 [19]. The global interconnect latency in the traditional on-chip electrical interconnect is not scaled down as the technology node evolves. On contrary, wire delay is worsen with technology scaling. Global interconnect delay is continuously increasing [20]. It becomes a problem that signals cannot travel across the entire die within a global clock cycle. Although introducing copper wire [21] and low-κ dielectric insulators [22] would help reduce delay, the problems are multi-fold. With increment in chip complexity for more functionality, local interconnect wire density grows exponentially. At global interconnect level, aggressive use of repeaters and buffers leads to increased chip area and power consumption. Studies showed that an average of 50% power is consumed in the on-chip interconnect [23]. Cross-talk becomes serious with increasing cross-coupling capacitances between electrical interconnects on the same metal layer [24]. Under these circumstances, interconnect solution that can provide low latency, high sustained bandwidth and low energy consumption is mostly desired for the multi-core and many-core systems.

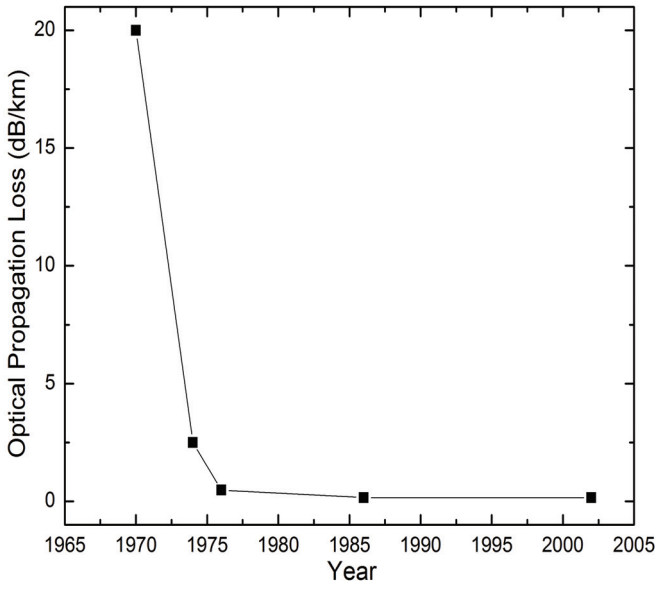


Figure 1.2: The reduction of fiber optical propagation loss over the years.

1.3 The Optical Interconnection

In parallel with the development of microprocessor chips in the past half a century, the optical interconnection technology revolution has experienced many important milestones over the years. The size of optical communication devices evolves from the large long-haul communication form factor towards the integrated on-chip small form factor.

The development of fibers and modern optical devices began around 1960 and continues strongly today. The first mile stone was undoubtedly the invention of the "Light Amplification by Stimulated Emission of Radiation" (Laser) by T.H. Maiman at Hughes Research Laboratories in the early 1960s. Laser immediately distinguished itself from other light sources by the exceptional property of highly spatial and temporal coherence. The ability of providing high radiances and low divergence over long propagation distance set laser as the ideal light source for optical telecommunication.

The second milestone was the development of low-loss optical fiber in the 1970s. The idea of using glass fiber to transmit optical communication signals can be dated back to Alexander Graham Bell's "Photophone" [25]. However, like many other inventions, fiber communication

had to experience a long waiting time before better glass appeared and low-cost electronics became available. K.C. Kao and G.A. Hockham showed that, in their 1966 paper, it was possible to decrease the attenuation in optical fiber down to a few dB/km by eliminating impurity ions [26]. As a transmission medium, glass fiber is immune to electromagnetic interference. This discovery opened up the opportunity for the telecommunication industry to develop long-haul optical communication link and the possibility of replacing bulky copper telephone lines with thin glass fibers. Since then, the refinement of glass fiber had never stopped. Figure 1.2 plots the progress on fiber propagation reduction over the years. From Corning Glass Works's 20 dB/km in 1970 [27] to Sumitomo Electric's 0.1484 dB/km in 2002 [28], the loss reduction advanced with emergence of new generations of technology. Currently, the fiber optical loss is approaching the theoretical limits. Because of its superior merits of low loss, low power consumption and high bandwidth, glass fiber gradually became the standard medium to carry large information capacity over long-haul telecommunication transmission. Kao was awarded the Nobel Prize in Physics in 2009 for this discovery.

In the 1980s, long-haul telephone links were deployed, thanks to the development of single-mode fiber. Single-mode fiber, operated together with 1300 nm laser source, was incorporated into the national telecommunication backbone by carriers across the United States. The Northeast Corridor system started to link Washington D.C. and New York together in 1983. New generation of single-mode fiber system with a 1550 nm laser wavelength operation window demonstrated feasibility of transmitting at even longer distance for the submarine cable operation. The first transatlantic fiber system, TAT8, started its operation in 1988. The third milestone was established when the optical fiber amplifier was invented. Erbium-doped fiber amplifier (EDFA) eliminated the need for installing electro-optic repeaters in the long-haul communication. It further reduced the cost of fiber operation and lifted the economic development barrier for the fiber-optic communication. The telecom industry was then well on its development high way.

Similar to the concept of parallel computing in the microprocessor world, wavelength division multiplexing (WDM) was firstly introduced in the 1970s [29]. WDM is a technology that allows a number of different optical signals (channels) to be transmitted simultaneously in a single fiber

by using multiple laser wavelengths. The idea of WDM was advocated by telecom carriers, as it enabled them to upgrade the bandwidth capacity without overhauling the infrastructure that was already installed. In the 1990s, high capacity WDM systems with up to 80 channels were delivered to the market, capable of carrying terabit/second of information. Fiber-optic technology entered the "Tera-era". With the maturing of the WDM technology, fiber-optic communication presents itself as a viable solution that possesses the merits of low loss, low latency and high bandwidth. As multi-core and many-core microprocessor chips reach the bottleneck in interconnection, the obvious question is can the fiber-optic communication technology be utilized in the microprocessor on-chip interconnection?

1.4 Silicon Photonics

The equivalent question is can the fiber-optic communication system be transformed and fabricated in a form of optical integrated circuit? The concept of "integrated photonics" was firstly introduced around 1970 [30, 31, 32]. An integrated photonic circuit should be able to facilitate the interaction between electrons and photons, using advanced fabrication technique to control the flow of photons on chip. It should contain the counterparts of microwave components that have functions of generating, splitting, coupling, filtering, switching, multiplexing, de-multiplexing and detecting light signals in the on-chip circuit. When this concept is mingled with the semiconductor fabrication technology, a more specific form of "integrated photonics" is born. That is "silicon photonics", using silicon integrated circuit to control the flow of photons. The pioneer works on silicon photonics were conducted by R. Soref in the 1980s and 1990s [33, 34]. The idea of creating cost-effective silicon photonic complementary metal-oxide-semiconductor (CMOS) hybrid "superchip" was investigated. These fundamental research works explored basic on-chip photonic components, including silicon waveguiding structures, silicon electro-optic effects and related fabrication techniques, etc. The results demonstrated the feasibility for the CMOS compatible photonic on-chip communication.

With the rapid development of information technology, silicon is the most studied semiconductor material on earth. Intrinsic silicon has an indirect bandgap of 1.11 eV at room temperature,

therefore it is transparent to wavelengths longer than 1100 nm in the near infrared (NIR) region. The absorption loss in silicon material is minimum for the telecommunication wavelength window of 1300 nm and 1550 nm. This is one of the advantages that helps accelerate the mergence of photonics and electronics. Meanwhile, silicon waveguides can be conveniently fabricated on the Silicon-on-Insulator (SOI) wafer. Although the wafer material of choice is different from those used for IC chips, the fabrication process is still virtually the same. The process is CMOS compatible. Without too much modification, silicon photonic devices can be produced in a CMOS foundry. Moreover, with the 130 nm or more advanced lithography technology tools available, single-mode silicon waveguide with several hundred nanometers width can be patterned on SOI wafer. Single-mode silicon waveguide prevents modal dispersion and its core size is about 1000 times smaller than that of a single mode fiber, due to the high index contrast in the forming waveguide of silicon and silica interfaces. Fabrication advancement in 2004 by Vlasov [35] lowered the propagation loss in silicon waveguide to a few dB/cm. Even though the loss factor seems high comparing with the optic fiber, silicon photonics deals with signal transmission at chip scale and a few dB/cm becomes acceptable within several millimeters. At this point, silicon photonic integration became practical.

Although silicon has an indirect bandgap that does not seem to promote light emitting, heterogeneous epitaxy of germanium on silicon creates opportunities for on-chip laser. Lasing from electrically pumped n-type Germanium-on-Silicon Fabry-Perot cavities was observed [36]. Meanwhile, solid-state off-chip laser components, such as amplified spontaneous emission (ASE) source, superluminescent light emitting diode (SLED) and supercontinuum source that provide superior bandwidth and power, are widely available in the market. These off-chip laser devices when coupled via fibers are capable of providing the wavelength spectrum required for the on-chip WDM components. Germanium-on-Silicon heterostructure also emerged as the preferred photodiode for high speed light detection in silicon photonic circuits [37, 38]. Silicon photonic foundries such as IMEC [39] and LETI [40] of ePIXfab/EuroPractice [41, 42] already started offering on-chip germanium photodetector as a feature in their wafer shuttle runs. Concurrently, optical modulators that convert electrical and optical signals were created. Silicon photonic crystal waveguide modula-

tor [43], p-n junction modulator [44] and silicon/electro-optic polymer hybrid modulator [45] looked promising for the on-chip integration. Therefore, the answer to the question at the beginning of this section is YES. Silicon photonic research is moving towards realizing a complete integrated on-chip optoelectronic system. The miniaturization of the optical telecommunication system into the integrated circuit form would deeply revolutionize this ecosystem and further reduce production cost. Silicon photonics is on the horizon of being a matured next generation technology.

In the past, the high cost of the optical interconnection technology could only be justified for the long-haul transmission. Optical interconnect could only be found in the long distance telecommunication backbone. Recently, with the advancement of photonic integration technology, optical interconnect gradually migrates to shorter and shorter communication regions, such as metropolitan area networks (MANs), local area networks (LANs) and Network on chip (NoC). Silicon photonic technology has emerged and will play an important role in speeding up this revolution. No matter for the short distance off-chip communication or for the multi-core and many-core on-chip interconnection, the advantages of optical interconnect over electrical interconnect is apparent. Optical interconnect brings high bandwidth, lower power consumption and lower latency to the communication link [46, 47, 48]. The demand for optical interconnect to replace electrical interconnect is growing stronger. The positive economy benefit and impact of silicon photonics are increasingly being recognized. An initial silicon photonics market starts to surface. Cisco bought silicon-photonics startup Lightwire and Mellanox purchased Kotura. All these moves indicate that in the current telecom and datacom markets, industry leaders and dominant players sense the opportunity in silicon photonics and adjust their strategic market alignment in order to keep the edge for future growth.

1.5 Statement of the Research

The interconnection problem is power dissipation and latency of the interconnection. The interconnection between cores is necessary because cores are necessary. Multiple cores became necessary when the circuit density on the standard size die became so great that the only way

designers knew how to harness the computing resources was by limiting the transistors to processor cores that were already understood. No one knows how to layout transistors all over the die and still be able to use them. These cores will continue to generate just as much heat as the transistors within them no matter how they are interconnected. There are references made in our work to architectures where 30% or more of the chip dissipation is in the interconnect [23, 49]. This was not the case in rack to rack interconnects where we were clearly told that the interconnection dissipates negligible heat compared to the processors on a board, on a backplane or in a rack. Not all multicore processor architectures generate so much heat in the interconnect. The problem may become worse with the increasing number of cores.

The voltage and current required by metal stripe circuits do not scale well with size of stripes and frequency of transmission. An important measurement of interconnect system stability is the system receiver signal-to-noise ratio (SNR). The SNR is quantified by

$$\mathrm{SNR} = \frac{P_{\mathrm{rec}}}{N_r + N_x} \tag{1.1}$$

where P_{rec} is the signal level received at detector, N_r is the receiver noise generated by thermal noise, shot noise and dark current noise, and N_x is the crosstalk noise. The receiver noise N_r is proportional to the detection bandwidth. That is to say, the signal power must increase at least linearly with bandwidth to preserve the SNR. As circuits become denser and wires size shrinks down, electrical interconnect wires are packed closer together, the capacitance per unit length increases as size decreases ($C = \varepsilon A/d$ where separation distance d decreases). The resistance per unit length increases with decreasing size ($R = \rho L/S$ where wire cross-section area S shrinks down). The total resistance and capacitance increase with length of the interconnection. Because the RC time constant increases, the electronic noise (Johnson noise) increases in the circuits. This raises the crosstalk noise N_x at the receiver, therefore more power must be applied to the interconnect to preserve the SNR.

To reduce latency in long wires, the length of interconnections can be kept shorter by using

repeaters in the lines [50]. However, repeaters require more power be dissipated and it may end up with the increased total power overhead. Another solution that is being tested is use of only nearest neighbor connections in order to support packet situation. Packet-switching network moves data in small blocks (pocket) based on the destination of each block. Data will be reassembled into normal sequence once the block is received. This will increase power dissipation but more importantly leads to an exponential increase in latency, due to runtime multihop data buffering, resource arbitration and link contention [51].

A broadcast interconnection solves latency as well as power dissipation problems. Broadcast avoids long copper wire and transmits data at light speed. This would greatly reduce latency. Meanwhile, silicon optical waveguide strongly confines propagation waves and has excellent power efficiency. Our results show significantly power dissipation reduction can be achieved in photonic broadcast design [52]. However, a broadcast interconnection may not improve performance as much as is necessary to justify such a disruptive technology. A silicon photonic broadcast subnetwork on top of CMOS circuit would require hybrid integration of both technologies. CMOS circuit production has high yield but silicon photonic fabrication technology is yet mature. Silicon photonic hybrid integration has to demonstrate orders of magnitude in performance improvement for further hybrid integration development. In many cases, more communication layers may be necessary, for example, the broadcast layer may be employed to circuit interconnect channels for large scale node-to-node data transfer that is not so latency critical as short burst synchronization messages. The broadcast layer can be used for transferring latency-critical global synchronization messages in the critical path of system performance, while circuit switching layer is setup for large scale data transfer.

To fully utilize the advantage of deploying broadcast interconnect, it is of interest to see whether broadcast communication theme could eliminate the switching layer in between sender and receiver which causes most of the latency and consumes significant portion of the on-chip power. If silicon photonic WDM technology applied to the broadcast interconnect could be able to create enough separate channels for all the nodes in the network, there would be no need to

use circuit switching. It is also in the research interest to investigate what can be achieved for broadcast interconnect with today's technology.

1.5.1 The Vision

The importance of silicon photonics has drawn widespread interests in the academia and research community. The effort by our team at the Guided Wave Optics Lab (GWOL) of the University of Colorado Boulder started in 2008 under the NSF "EMT-NANO" project[2] . We focused on designing and characterizing components for the next generation silicon photonic interconnect in the multi-core and many-core environment. This thesis comes out of my effort in participating the "EMT-NANO" project and related on-going projects[3] .

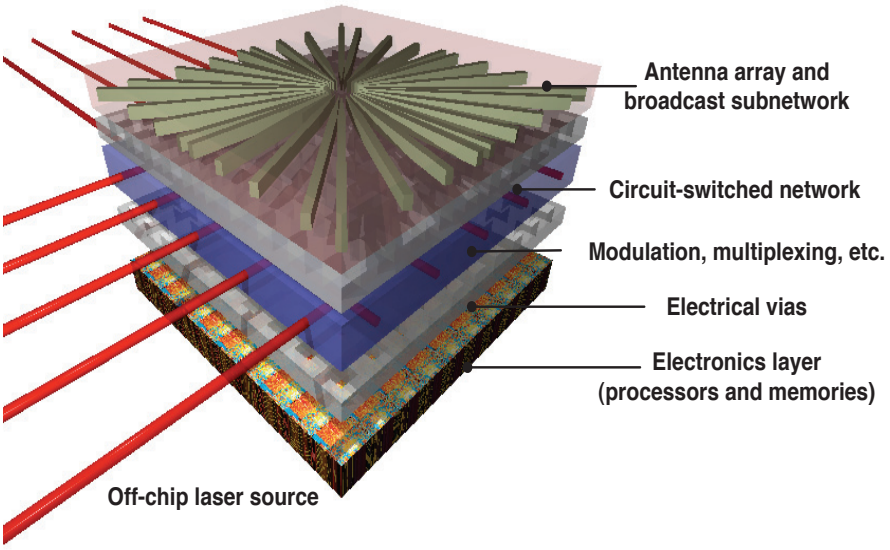


Figure 1.3: A schematic plot of 3D-IC network design. Off-chip light source is connected to an on-chip silicon photonic layer that modulates and multiplexes/demultiplexes the light signals. A CMOS electronic control layer at the bottom is connected to the silicon photonic layer through electrical vias. The processed signals is switched and broadcast using antenna array and broadcast subnetwork.

Our research direction has been guided under one silicon photonic broadcast optical intercon-

[2] National Science Foundation (NSF) Award #CCF-0829950 — EMT-NANO: Broadcast Optical Interconnects for Global Communication in Many-Core Chip-Multiprocessor.

[3] Part of the content in this thesis is from the papers listed in Section 1.5.2 that I have published or that is under review.

nection architecture. Figure 1.3 is a depiction of the architecture we envisioned. The whole system is a 3D hybrid integration of SOI silicon photonic layer and CMOS electronics layers. The system is capable of light detecting, modulating, multiplexing/demultimplaxing, switching and broadcasting. At the bottom sit the multi-core and many-core processors and memories, the control units. This layer connects the middle silicon photonic layers through electrical vias. Broadband light source is sliced into many channels and routed via photonic circuit-switching network. The processed light signal is sent out via the top antenna array and broadcast subnetwork layer. WDM technique is fully deployed in this 3D on-chip network. Together, this architecture addresses the latency, bandwidth and power efficiency issues that nest in traditional electrical interconnect network.

1.5.2 List of Publications and Origins of Contribution

GWOL team worked collectively on the "EMT-NANO" project. Our work has resulted in many journal and conference publications over the course of the project. In this section, I include these publications and describe the origins of contribution.

1.5.2.1 Journal Publications

J1 X. Chen, M. Mohamed, Z. Li, L. Shang, and A. R. Mickelson, "Process variation in silicon photonic devices," **Appl. Opt.**, vol. 52, no. 31, pp. 7638–7647, Nov 2013.

Contribution: The wafer-scale process variations on devices of interest are characterized and analyzed. Chen carried out the experiments and wrote the manuscript; co-authors edited the manuscript.

J2 X. Chen, Z. Li, M. Mohamed, L. Shang, and A. R. Mickelson, "Parameter extraction from fabricated silicon photonic devices (in review)," **Appl. Opt.**, 2013.

Contribution: A simple method is proposed to determine effective indices of fabricated devices and a calibrated T-matrix model is presented for device of interest. Chen finished the analysis and wrote the manuscript; co-authors edited the manuscript.

J3 H. Zhou, X. Chen, D. Espinoza, A. Mickelson, and D. Filipovic, "Nanoscale optical dielectric rod antenna for on-chip interconnecting networks," **Microwave Theory and Techniques, IEEE Transactions on**, vol. 59, no. 10, pp. 2624–2632, 2011.

Contribution: A new on-chip optical dielectric rod antenna array is simulated, fabricated and analyzed. Zhou designed the antenna and wrote the manuscript; Chen did physical and optical characterization of the fabricated antenna design and wrote the manuscript on experiment; Espinoza did polymer coating for the antenna; Mickelson and Filipovic edited the manuscript.

J4 D. Espinoza, X. Chen, M. Mohamed, H. Zhou, E. Dudley, W. Park, D. Filipovic, and A. Mickelson, "Nanometric polymer coatings for silicon on insulator circuits," in **Proc. SPIE 8173, Photonics 2010: the 10th International Conference on Fiber Optics and Photonics**, Aug 2011, p. 81730H.

Contribution: The effect of polymer coating on variety of silicon photonic devices is investigated. Espinoza and Mickelson wrote the manuscript. Espinoza did polymer coating and part of microscope imaging; Chen did optical characterization of the devices of interest, part of microscope imaging and writing the manuscript on optical measurement; co-authors edited the manuscript.

J5 M. Mohamed, Z. Li, X. Chen, L. Shang, and A. Mickelson, "Reliability-aware design flow for silicon photonics on-chip interconnect (in press)," **Very Large Scale Integration (VLSI) Systems, IEEE Transactions on**, no. 99, Oct 2013.

Contribution: A reliability-aware design flow to address variation-induced reliability issues is proposed and analyzed. Mohamed and Li did analysis and wrote the manuscript; Chen provided physical and optical characterization data of the devices of interest and built T-matrix models; co-authors edited the manuscript.

J6 Z. Li, M. Mohamed, X. Chen, E. Dudley, K. Meng, L. Shang, A. Mickelson, R. Joseph,

M. Vachharajani, B. Schwartz, and Y. Sun, "Reliability modeling and management of nanophotonic on-chip networks," **Very Large Scale Integration (VLSI) Systems, IEEE Transactions on**, vol. 20, no. 1, pp. 98–111, 2012.

Contribution: Run-time techniques are proposed to address on-chip system variation in photonic network. Li and Mohamed did analysis and wrote the manuscript; Chen provided physical and optical characterization data of the devices of interest; co-authors edited the manuscript.

J7 Z. Li, M. Mohamed, X. Chen, A. Mickelson, and L. Shang, "Device modeling and system simulation of nanophotonic on-chip networks for reliability, power and performance," in **Proceedings of the 48th Design Automation Conference**, ser. DAC '11. New York, NY, USA: ACM, 2011, pp. 735–740.

Contribution: A novel modeling and simulation methodology is proposed for silicon photonic network that is affected by process and thermal variations. Li and Mohamed did analysis and wrote the manuscript; Chen provided physical and optical characterization data of the devices of interest and built T-matrix models; co-authors edited the manuscript.

J8 Z. Li, M. Mohamed, X. Chen, H. Zhou, A. Mickelson, L. Shang, and M. Vachharajani, "Iris: A hybrid nanophotonic network design for high-performance and low-power on-chip communication," **J. Emerg. Technol. Comput. Syst.**, vol. 7, no. 2, pp. 8:1–8:22, Jul 2011.

Contribution: An Iris topology is proposed for silicon photonic on-chip network. Li and Mohamed did analysis and wrote the manuscript; Chen provided physical and optical characterization data of the devices of interest; co-authors edited the manuscript.

J9 Z. Li, M. Mohamed, H. Zhou, L. Shang, A. Mickelson, D. Filipovic, M. Vachharajani, X. Chen, W. Park, and Y. Sun, "Global on-chip coordination at light speed," **Design Test of Computers, IEEE**, vol. 27, no. 4, pp. 54–67, 2010.

Contribution: Multi-core chip interconnect and broadcasting concept with silicon photonics are discussed and analyzed. Li and Mohamed did analysis and wrote the manuscript; Zhou designed the antenna; Chen provided physical and optical characterization data of the devices of interest; co-authors edited the manuscript.

1.5.2.2 Conference Publications

C1 X. Chen, D. Espinoza, E. Dudley, Z. Li, M. Mohamed, Y. Cui, W. Park, L. Shang, and A. Mickelson, "Polymer-clad silicon on insulator slot modulator," in **Advanced Photonics**. Optical Society of America, 2011, p. IMB7.

Contribution: A polymer-clad slot waveguide with FIB deposited electrodes for phase modulator is fabricated and investigated. Chen did physical and optical characterization of the devices of interest and wrote the manuscript on introduction and fabrication and measurement; Espinoza did polymer coating; Dudley did simulation work and wrote the manuscript on design; Cui did FIB deposition work; co-authors edited the manuscript.

C2 X. Chen, Z. Li, M. Mohamed, L. Shang, and A. Mickelson, "Matrix analysis of nanophotonic devices," in **Photonics 2010: the 10th International Conference on Fibre Optics and Photonics**, Guwahati, India, Dec 2010.

Contribution: T-matrix modeling technique is proposed for silicon photonic devices. Chen did the analysis and wrote the manuscript; co-authors edited the manuscript.

C3 X. Chen, M. Mohamed, B. Schwartz, Z. Li, L. Shang, and A. Mickelson, "Racetrack filters for nanophotonic on-chip networks," in **Integrated Photonics Research, Silicon and Nanophotonics and Photonics in Switching**. Optical Society of America, 2010, p. ITuB5.

Contribution: Three different-order racetrack resonators are fabricated and analyzed. Chen did physical and optical characterization of the fabricated devices and wrote the manuscript

on theory and experiment; Mohamed analyzed and wrote the manuscript on numerical simulation; co-authors edited the manuscript.

C4 D. Espinoza, X. Chen, H. Zhou, D. Filipovic, and A. Mickelson, "Nano-photonic antennas propagation through a polymer medium," in **Photonics 2010: the 10th International Conference on Fibre Optics and Photonics**, Guwahati, India, Dec 2010.

Contribution: The on-chip antenna propagation with polymer cladding is investigated. Espinoza did polymer coating and wrote the manuscript; Chen provided physical and optical characterization data of the devices of interest; Zhou designed the antenna; co-authors edited the manuscript.

C5 M. Mohamed, Z. Li, X. Chen, A. Mickelson, and L. Shang, "Modeling and analysis of micro-ring based silicon photonic interconnect for embedded systems," in **Proceedings of the seventh IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis**, ser. CODES+ISSS '11. New York, NY, USA: ACM, 2011, pp. 227–236.

Contribution: Analytical models are developed and calibrated for widely used passive and doped micro-ring resonators. Mohamed and Li did analysis and wrote the manuscript; Chen provided physical and optical characterization data of the devices of interest and built T-matrix models; co-authors edited the manuscript.

C6 M. Mohamed, Z. Li, X. Chen, L. Shang, A. Mickelson, M. Vachharajani, and Y. Sun, "Power-efficient variation-aware photonic on-chip network management," in **Low-Power Electronics and Design (ISLPED), 2010 ACM/IEEE International Symposium on**, 2010, pp. 31–36.

Contribution: Run-time management solution, inter-channel hopping, wavelength tuning and routing are proposed for silicon photonic network that is affected by variations. Mohamed and Li did analysis and wrote the manuscript; Chen provided physical and optical

characterization data of the devices of interest; co-authors edited the manuscript.

C7 M. Mohamed, Z. Li, E. Dudley, X. Chen, L. Shang, W. Park, and A. Mickelson, "Adiabatic couplers for linear power division," in **Advanced Photonics**. Optical Society of America, 2011, p. IMD6.

Contribution: A silicon photonic adiabatic 3dB coupler is designed and fabricated. Mohamed designed the structure and wrote the manuscript; Chen provided physical and optical characterization data of the device of interest; co-authors edited the manuscript.

1.6 Thesis Outline and Origins of Contribution

1.6.1 Thesis Outline

The work presented in this thesis focuses on the fabrication and characterization related issues in silicon photonic technology.

Chapter 1 examines the development trend for microprocessor and the potential problems for on-chip electrical interconnect. A brief history of optical communication is introduced and the emergence of silicon photonic technology for on-chip interconnect application is discussed. The scope of our research on silicon photonics is presented.

Chapter 2 introduces the wafer-scale fabrication for silicon photonic devices and describes our in-house photonic measurement testbed for device optical characterization. The majority of the content focus on the discussion of several fundamental silicon photonic devices, namely grating coupler, micro-ring and racetrack resonator, directional coupler, optical on-chip antenna array and photonic crystal. Their operation mechanisms and optical transfer functions are explained.

Chapter 3 presents the characterization work of the wafer-scale process and thermal variations in three classes of devices including micro-ring, racetrack and directional coupler. Measurement results on thermal variation verify the accuracy of the measurements. Process variation shows a uniformly wafer-scale "random walk" pattern across the devices. The results provide a quantitative base for fabrication-yield-aware design.

Chapter 4 talks about phenomenological modeling of using T-matrix to describe fabricated photonic devices. It shows that the effect of process and thermal variations which exist in the fabricated devices can be well expressed in the effective index. A simple method that combines Comsol full wave simulation and analytical models is presented for extracting the effective index out of fabricated photonic devices. T-matrix with calibrated effective index values displays excellent fitting result for the optical measurements.

Chapter 5 introduces a variation-aware on-chip broadcast interconnect design for multi-core processor. This design utilizes the demonstrated WDM micro-rings and any-one-to-all antenna array to create broadcasting channels. With the cluster design of micro-rings, it shows this architecture can be realized with today's technology.

Chapter 6 concludes this topic.

1.6.2 Origins of Contribution

In Chapter 1, Section 1.1 to Section 1.4 are the review of literature. Section 1.5 to Section 1.6 are my original work.

In Chapter 2, the operation mechanism of the antenna in Section 2.4.4.2 and the introduction of the photonic crystal in Section 2.4.5.1 are written by Prof. Alan Mickelson in our publication [J4] of Section 1.5.2.1 and adapted in this thesis. The rest of sections are my original work.

Chapter 3 to Chapter 6 are my original work. Prof. Alan Mickelson, Dr. Zheng Li and Dr. Moustafa Mohamed help edit the contents in Chapter 3 and Chapter 4.

Chapter 2

Fabrication, Measurement and Design Characterization of Silicon Photonic Devices

2.1 Introduction

For the interconnection network of the multi-core and many-core systems, one of the great advantages of silicon photonics is that it offers on-chip wavelength division multiplexing (WDM) technology. Silicon photonics technology brings the WDM from the long-haul optical telecommunication to the chip scale. The use of WDM enables bidirectional communications. It can increase the bandwidth capacity by a large factor, depending on how many wavelength channels are deployed simultaneously. It addresses the bandwidth constraint in current on-chip communication network at ease.

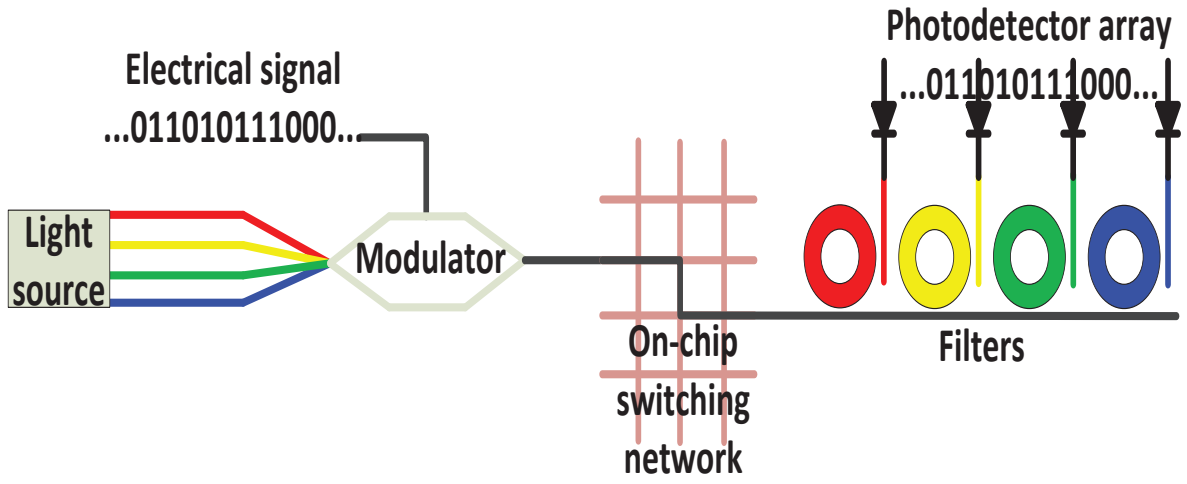


Figure 2.1: A schematic diagram of a silicon photonic on-chip WDM network.

A complete WDM functioning link is comprised of a broadband light source, demultiplexer and multiplexer units at the transmitter side, waveguide with multiple routes that compose of the WDM network, demultiplexer unit at the receiver side. Figure 2.1 illustrates the idea of a silicon photonc on-chip WDM network. When the broadband light signal is off-chip, it can be delivered to the on-chip waveguide via grating coupler. The signal is then split into many wavelength channels by the demultiplexer at the transmitter. Each wavelength passes through individual electro-optic (EO) modulation device and the electrical digital information is transformed into the optical information via EO conversion. All the modulated wavelengths are combined and broadcast out at the multiplexer unit. At the receiving end, the demultiplexer unit would slice the wavelength bundle into separate wavelength channels for the detectors. On-chip germanium detector is oftentimes used for high-speed detection. At the destinations, signals are amplified and processed individually by CMOS circuit components.

In this chapter, we will discuss the basic components of a WDM link in the silicon photonic on-chip network. Our effort focuses on the passive devices. In Section 2.2, the wafer-scale fabrication is introduced. In Section 2.3, the details of our in-house measurement setup is described. In Section 2.4, several key photonic device components are introduced and their optical performance is characterized.

2.2 Fabrication

All silicon photonic devices used in our study were fabricated at ePIXfab [41] during the period 2009-2012. ePIXfab offers a standard CMOS-compatible photonic foundry process where the 8-inch Silicon-on-Insulator (SOI) wafer (Soitech) is adopted as the standard substrate. The functional layers of the wafer are comprised of a 220-nm ($\pm$3.5 nm) crystalline silicon layer on top of a 2-μm buried silicon oxide layer. The silicon oxide layer is sufficiently thick to reduce optical leakage through the substrate. Deep UV lithography of 193 nm line is used in fabricating our designs. The wafers that we measure are diced into repeated units (dies) across the wafer. The lithography exposure is flashed in steps of increasing/decreasing dosage across the columns from

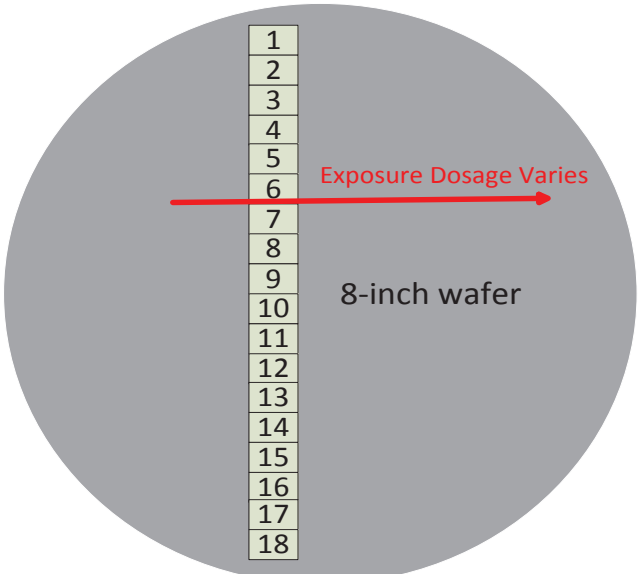


Figure 2.2: Schematic depiction of an 8-inch wafer that details the vertical cells (repeated dies) of a single column. The lithographic exposure was swept horizontally such that each column received a different exposure, but each cell within a column received nominally the same exposure.

left to right, as depicted in Figure 2.2. As a result, different columns consist of devices with slightly different physical dimensions for a single design. Only one column contains the desired physical dimensions of our design. Our optical measurement characterization is focused on this particular column. Within one column, the devices of each design repeated on the dies receive a fixed amount of exposure dosage and have nominally same physical dimensions. The size of each die on the wafer from LETI ([40] an ePIXfab/EuroPractice [42] facility) is smaller than those of wafers from IMEC ([39] another ePIXfab/EuroPractice facility). There are, therefore, more dies in one single column on the LETI wafer. The number of dies per column can reach up to 28 dies on the LETI wafer and 19 dies on the IMEC wafer depending on the location on the wafer. Moreover, within one die, devices are laid out row by row with 25 μm separation distance vertically in between.

2.3 Measurement Apparatus and Its Use

All the device measurements are carried out in-house using the apparatus depicted in Figure 2.3. The system employs a broadband super luminescent light emitting diode (SLED) light

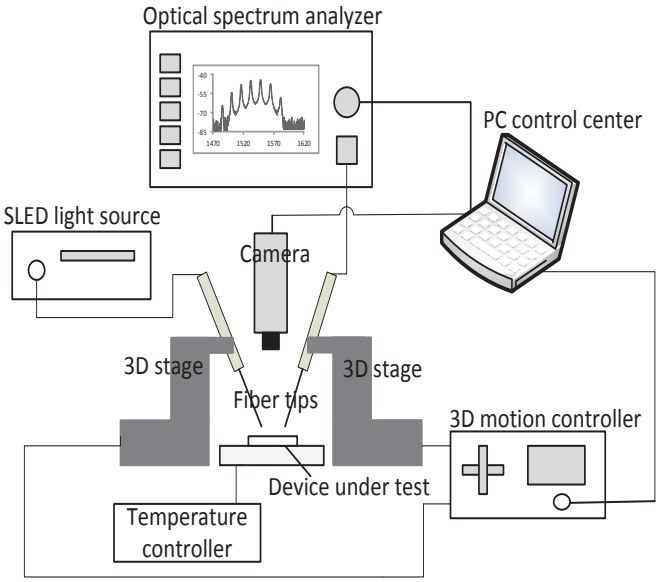


Figure 2.3: Schematic of the in-house measurement setup. The set-up is comprised of a SLED light source, an optical spectrum analyzer, two single mode fibers that couple light to and from the photonic chips, two sub-micron accurate 3D motion controllers, a visible camera that monitors the fiber movement and a temperature controlled sample stage.

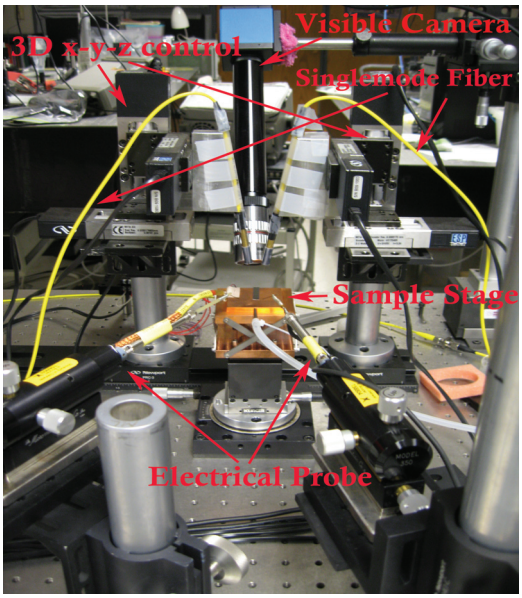


Figure 2.4: Photo of the in-house measurement setup. It shows the physical images of the key components of the setup.

source whose wavelength range is 1480-1600 nm. The photonic chip is placed on a temperature controlled sample stage. A single mode fiber delivers the light signal to the photonic chip where

light is coupled into device through a grating coupler located at one end of each device. The grating coupler is optimized for passing transverse electric (TE) modes where E-field is parallel to the grating grooves. After passing through the device, light is coupled out through another TE-mode grating coupler into an optical spectrum analyzer (OSA) via the second single mode fiber. The maximum resolution of the OSA is 80 pm throughout the wavelength range of 600-1700 nm. The fiber movements are precisely controlled by two 3D motion controllers which are capable of sub-micrometer adjustment. A visible camera is used to monitor the movement of the two fiber tips. Two probes are used to apply electrical signals to the photonic chip where necessary. Figure 2.4 displays the physical image of the setup in our lab.

2.4 Design Characterization of Silicon Photonic Devices

In this section, we take a closer look at the silicon photonic devices that are found in a WDM communication link. These components include grating coupler, waveguide, micro-ring, racetrack, directional coupler, broadband antenna and photonic crystal.

2.4.1 Grating Coupler

2.4.1.1 Introduction

In order to characterize and operate a silicon photonic, light signal has to be efficiently delivered to the device. Recently, on-chip light source has been demonstrated in experiment [36, 53, 54]. However, before the on-chip light source technology produces matured reliable products, the silicon photonics development depends on off-chip light source as the light signal generator. How to effectively couple light into a silicon waveguide becomes an interesting and challenging problem. Oftentimes it becomes crucial to the success of a photonic circuit design when the power budget is tight. One straightforward way of coupling light into a silicon waveguide is end-fire coupling [55, 56]. In the end-fire coupling setup, the efficiency coupling depends on the spatial overlap of a free-space Gaussian beam in fiber and a bound waveguide mode. Focusing lens is

regularly implemented to help increase the overlap therefore to get higher efficiency. The setup could be bulky and not flexible. The other issue with end-fire coupling is that it requires a clean and well-cut waveguide end-face. It usually involves wafer cleaving and polishing. It complicates the post-process procedures and lower the yield.

One way to get around these troubles is to use grating coupler as the coupling mechanism. Grating coupler allows out-of-plane coupling. That is, launching the mode via vertical coupling instead of horizontal coupling. Grating coupler can be fabricated on the SOI wafer via standard CMOS technology and resembles periodic structures on the surface. With grating coupler, a waveguide mode can be excited by a free-space beam when the Bragg condition is satisfied. The vertical coupling eliminates the wafer cleaving process. Fiber that delivers the light signal can move above wafer for coupling and presents an advantage for fast wafer testing process. Grating coupler is convenient in use and becomes a standard in silicon photonic technology [57].

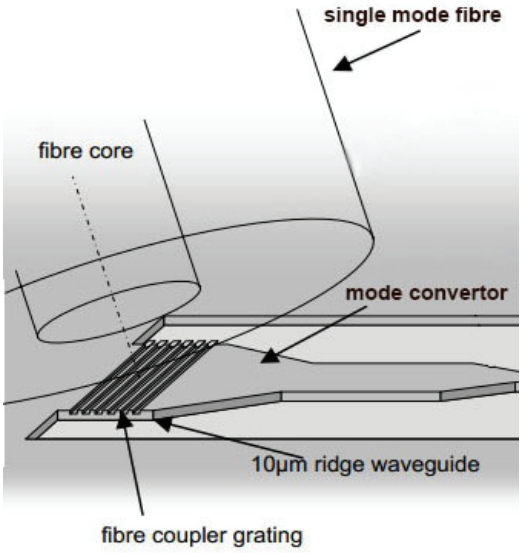


Figure 2.5: A schematic setup of a single-mode fiber to grating coupler. The core diameter of a sing mode fiber is about 10 μm. The grating coupler area on waveguide is comparable to this size.[1]

[1] Image credit: ePIXfab, "Silicon photonics platform: building a vertical fibre coupling setup", Dec. 2006.

2.4.1.2 Coupling Mechanism

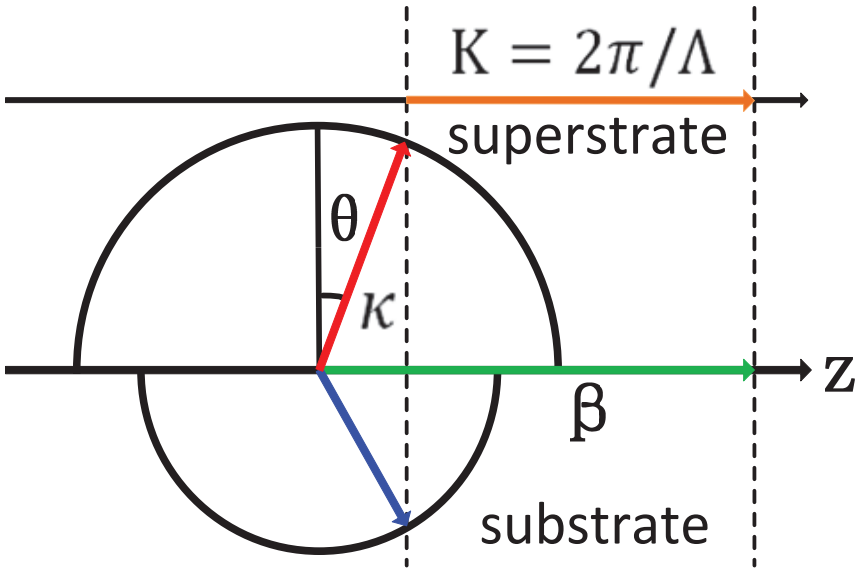


Figure 2.6: The Bragg condition for grating coupling mechanism. θ and κ are the coupling angle and the wave vector of the incident beam. Λ is the grating period. β is the propagation constant for the waveguide mode.

Figure 2.5 displays the fiber-to-grating setup where the core of a single-mode fiber is aligned to the area of grating coupler. The area of the grating coupler is comparable to that of the fiber core end-face. Once a waveguide mode is excited, it passes through a low loss taper waveguide region in order to be converted to a single mode of the input wavelength. The Bragg condition for the grating coupler can be written in the following form:

$$\kappa \sin(\theta) n_{\text{sup}} + mK = \beta, \qquad m = 1, 2, 3... \tag{2.1}$$

where $\kappa = 2\pi/\lambda$ is the wave number of the input wavelength, θ is the incident angle with respect to the surface normal, n_{sup} is the refractive index of the superstrate, m is the grating diffraction number, $K = 2\pi/\Lambda$ in which Λ is the grating period and β is the propagation constant of the excited waveguide mode. $\beta = 2\pi n_{\text{eff}}/\lambda$ where n_{eff} is the effective index of the grating coupler. The Bragg condition for first order diffraction grating is plotted in Figure 2.6. $m = 1$ in this case.

2.4.1.3 Characterization

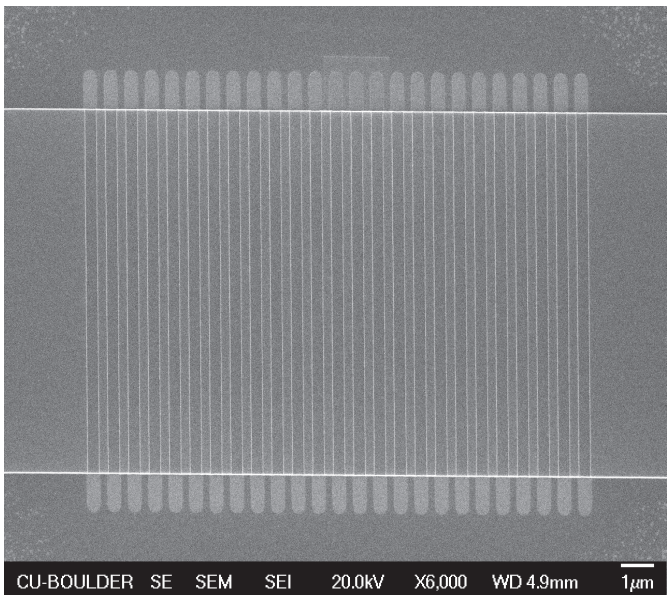


Figure 2.7: A scanning electron microscope image of a grating coupler that was fabricated at the ePIXfab. The area size of the grating coupler is about 10 μm $\times$ 15 μm.

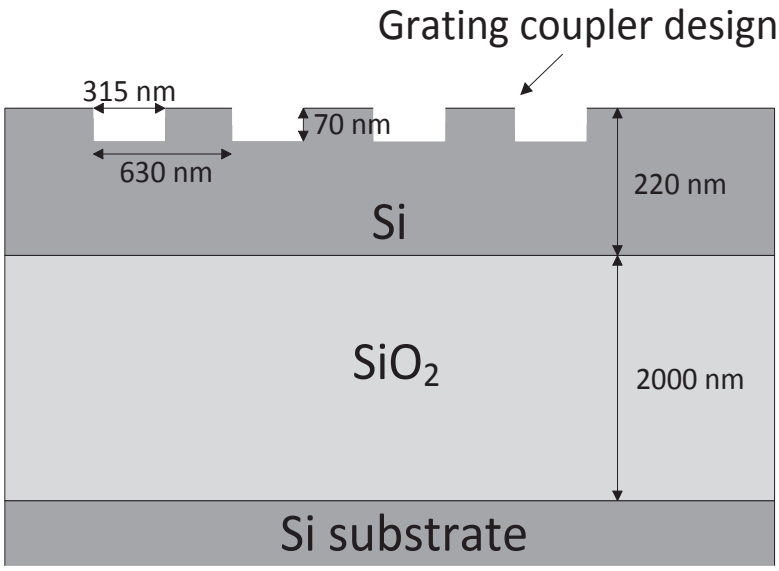


Figure 2.8: Schematic of the cross-section view of the grating coupler design on the SOI wafer. The SOI wafer is comprised of a silicon substrate, a 2-μm thick silicon dioxide insulating layer buried under a 220-nm silicon device layer. In the grating coupler area, the grating groove is shallow-etched about 70 nm down the surface.The trench width is around 315 nm and the pitch width is about 630 nm in total.

Our silicon photonic devices which were fabricated at the ePIXfab all have standard grating coupler. Figure 2.7 shows a scanning electron microscope (SEM) image of a fabricated grating coupler. The width of the grating coupler region is 10 μm and the length of the region is about 15 μm. Figure 2.8 depicts the cross-section view of the grating coupler design on the SOI wafer. The grating coupler is fabricated on the 220-nm silicon layer. The grating groove is etched 70 nm down the surface. The grating coupler design is optimized for the operation in the wavelength range of 1550 nm - 1560 nm where its groove trench width is about 315 nm with a total pitch width of 630 nm. The grating coupler acts as a polarization filter. This specific design couples the TE polarized light well into the grating with 10° of incident angle. TE polarization is defined as the direction parallel with the grating grooves. Maintaining TE polarization in waveguide and device is specially convenient for polarization sensitive devices and applications.

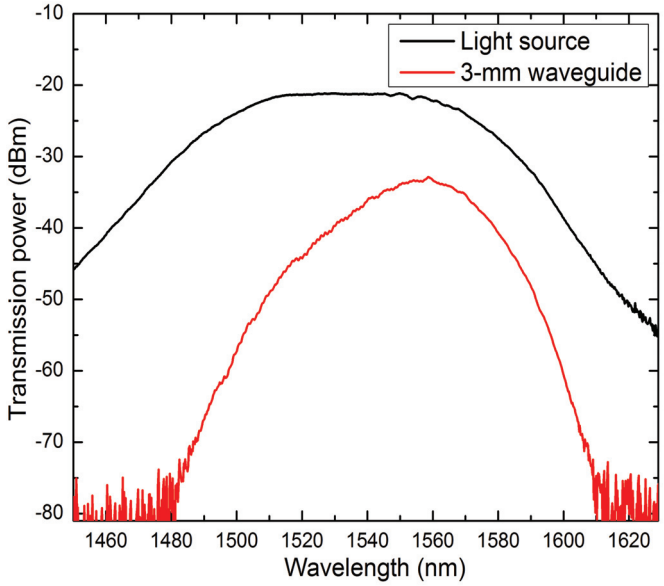


Figure 2.9: Grating coupler efficiency measurement. The black curve shows the input light source spectrum and power level. The red curve is the output light spectrum and corresponding power after passing through a 3-mm long bare waveguide with two grating couplers at both ends. The maximum transmission peak is at around 1560 nm.

We characterized the coupling efficiency of grating coupler in our lab. Figure 2.9 displays the measurement result. The input light source spectrum and power was captured by the OSA directly from a SLED light source. The light power was coupled into a 3-mm long bare waveguide on one

end firstly via a grating coupler and then coupled out via a second identical grating coupler on the other end of the waveguide. The output power spectrum was recorded by the OSA. As shown in the plot, the maximum transmission peak is at around 1560-nm wavelength. The power loss for the maximum transmission is about -10 dB. The ePIXfab standard waveguide propagation loss is about 2.5 dB/cm. A 3-mm long waveguide contributes about -0.75 dB loss. Therefore, the coupling efficiency for a single grating coupler is about 30 % at the optimized wavelength.

2.4.2 Ring Resonator

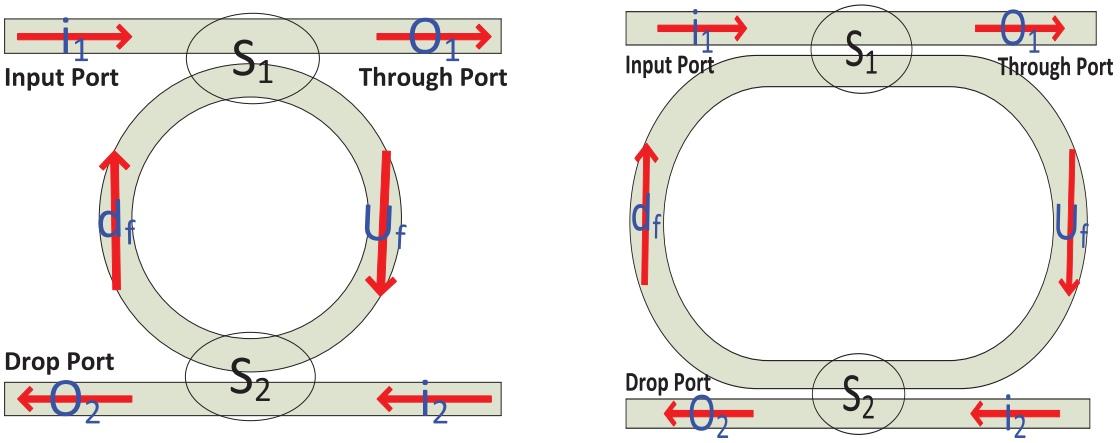
2.4.2.1 Introduction

One of the important functions of a WDM system is enabling switching and routing different wavelength channels. In a silicon photonic WDM system, this function can be realized by using variety of ring resonators designs, such micro-ring and racetrack resonators. Due to its resonant structure, ring resonator is a wavelength-selective device. It can be used to slice a broadband spectrum into WDM channels for downstream processing. By using silicon photonic ring resonator, efficient on-chip wavelength add-drop filters [58, 59] and optical network switches [60, 61] have been demonstrated. Moreover, ring resonator can realize high speed modulator with proper doping level inside its waveguide structures [62, 63, 64]. Ring resonator is versatile in terms of on-chip wavelength-selective functionality.

Another attractive feature of ring resonator for the integrated photonics is that its size can be very compact. A salient feature of the SOI waveguide is its high-index contrast between the waveguide interface materials with 3.48 for silicon, 1.45 for silicon dioxide and 1 for air. High-index contrast allows strong confinement of optical mode inside waveguide, therefore enabling extremely compact ring resonator devices. Micro-ring resonators with radii less than 2 μm were produced [65, 66]. The small foot print of ring resonator promotes high-density photonic device integration. Although tight waveguide bending induces optical radiation loss, balancing between bending loss and device size offers photonic circuit architect more flexibility. Ring resonator generates more and

more interest in silicon photonic device design.

2.4.2.2 Operation Principle



(a) Micro-ring resonator

(b) Racetrack resonator

Figure 2.10: Schematics of two kinds of ring resonator. S_1/S_2 are the coupling regions, i_1/i_2 are the input ports, O_1/O_2 are the output ports in the devices and d_f/U_f are the connecting ports in the resonance structures.

In general, ring resonator is a four-port device that consists of a circular resonant cavity and two coupling waveguides. Figure 2.10 illustrates two kinds of ring resonator: micro-ring resonator and racetrack resonator. They both have two input ports i_1/i_2 and two output ports O_1/O_2. The design difference lies in the coupling region. Micro-ring resonator has a circular ring that is point-coupled to its adjacent waveguides as displayed in Figure 2.10(a), whereas in racetrack resonator as shown in Figure 2.10(b), the coupling region is elongated into two straight lines parallel with the neighboring waveguides. Optical waves inside the input waveguides are evanescently coupled to the resonant cavity and travel round trips inside the cavity. Resonance condition is satisfied when the phase shift of the coupled waves built up inside the cavity equals $2\pi m$ where m is an integer. Resonant waves are then coupled out through the output ports. Comparing with the micro-ring resonator, racetrack resonator provides longer coupling length, allowing for broader spectral responses.

For a ring resonator, its resonant wavelength λ_{res} is defined as:

$$\lambda_{\text{res}} m = L n_{\text{eff}}, \qquad m = 1, 2, 3... \tag{2.2}$$

where L is the circumference of the ring resonant cavity, n_{eff} is the effective index of the ring cavity waveguide, and m is an integer. It means a resonant wavelength is selected when the optical length of the ring structure equals to a number of times the specific wavelength and the rest of wavelengths are suppressed by the cavity.

Another important parameter for a ring resonator is the free spectral range (FSR). It is defined as the wavelength spacing between adjacent resonant wavelengths and can be approximated as:

$$\text{FSR} = \lambda_{\text{res(m)}} - \lambda_{\text{res(m}-1)} \cong \frac{\lambda_{\text{res}}^2}{n_g L}, \tag{2.3}$$

where $\lambda_{\text{res(m)}}$ and $\lambda_{\text{res(m}-1)}$ represent adjacent wavelengths, L is the circumference of the ring resonant cavity, n_g is the group index which takes into account the wavelength dispersion in waveguide. n_g can be expressed as:

$$n_g = n_{\text{eff}} - \lambda_{\text{res}} \frac{dn_{\text{eff}}}{d\lambda} \tag{2.4}$$

The FSR is inversely proportional to the circumference of the ring resonant cavity. The smaller the circumference is, the larger the FSR will be.

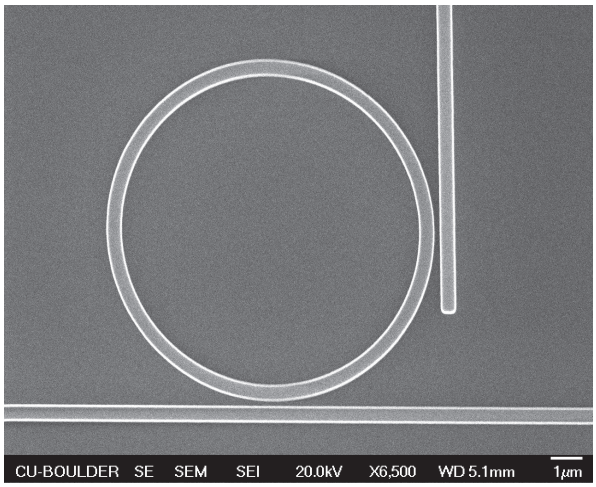
The full width at half maximum (FWHM) is commonly used to describe the width of a resonance. It is given by the distance between two wavelengths points where it reaches the half of resonance power on wavelength spectrum. Associated with this parameter, finesse F and quality factor Q are two key characteristics of the ring resonator performance, which are defined as:

$$F = \frac{\text{FSR}}{\text{FWHM}} \tag{2.5}$$

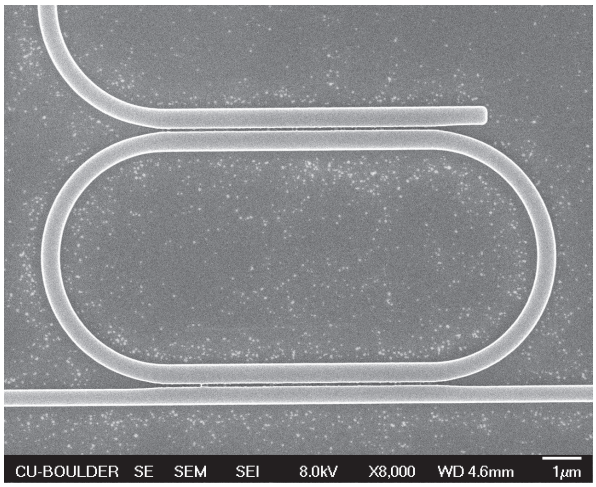
$$Q = \frac{\lambda_{\text{res}}}{\text{FWHM}} \tag{2.6}$$

The sharpness of the resonance can be characterized by the FWHM. Therefore, finesse F is a measure of the sharpness of the resonances with respect to the spacing in between and quality factor Q is a measure of the sharpness of the resonance with respect to the center wavelength. Quality factor Q can also be regarded as the stored energy inside the cavity divided by the optical power loss per round trip and it is oftentimes used to quantify the amount of losses inside the cavity.

2.4.2.3 Characterization



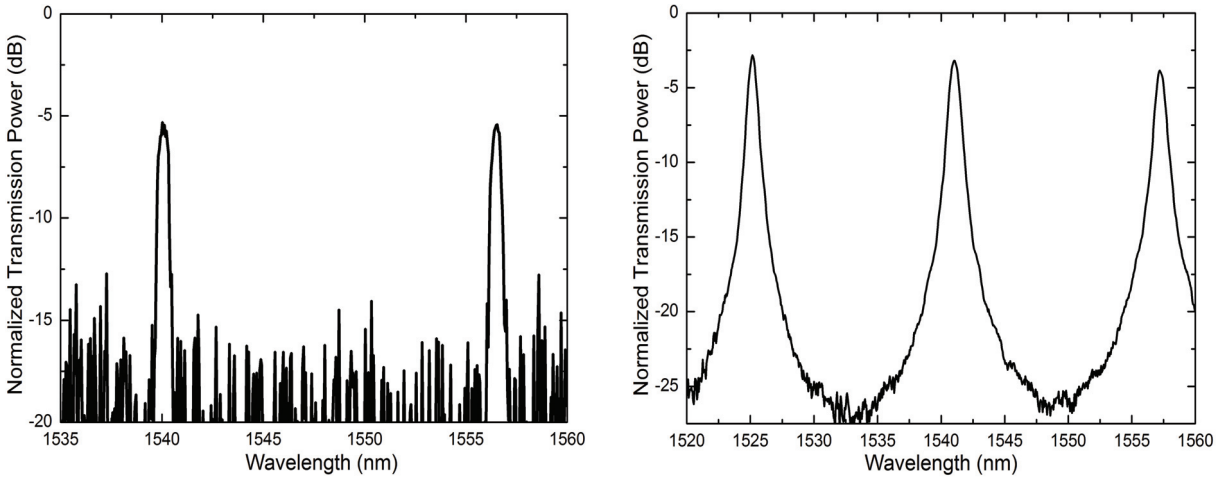
(a) Micro-ring resonator. The radius of the cavity is 4.975 μm and the coupling gap is 200 nm.



(b) Racetrack resonator. The coupling length is 7 μm, the bending radius is 3 μm and the coupling gap is 130 nm.

Figure 2.11: SEM images of fabricated ring resonators. The waveguide dimension in the structures is 450 nm (width) $\times$ 220 nm (height).

Figure 2.11 displays the SEM images of a micro-ring and a racetrack of our designs. These devices were fabricated in the ePIXfab wafer shuttle runs. In Figure 2.11(a), the micro-ring has a cavity with a radius of 4.975 μm and a coupling gap of 200 nm on both input and output sides. The racetrack, shown in Figure 2.11(b), has a coupling length of 7 μm, a bending radius of 3 μm



(a) Micro-ring resonator.

(b) Racetrack resonator.

Figure 2.12: Optical transmission measurement of the ring resonators in Figure 2.11.

and a coupling gap of 130 nm. The waveguide dimension in these structures is 450 nm (width) × 220 nm (height).

We measured the optical performance of these devices in our lab. The measurements were carried out at room temperature. We tested the broadband spectrum response of the devices. As illustrated in Figure 2.12(a), the micro-ring has a FSR of 16.52 nm and a FWHM of about 0.56 nm. Therefore, its finesse F is about 29.5. Its quality factor Q is about 2735.39 at the resonance of 1540.03 nm and 2764.74 at the resonance of 1556.55 nm.

The measurement result of the racetrack is plotted in Figure 2.12(b). The racetrack has a FSR of about 16.02 nm and a FWHM of about 0.9 nm. Accordingly, its finesse F is about 17.8. Its quality factor Q is about 1694.62 at the resonance of 1525.16 nm, 1712.25 at the resonance of 1541.03 nm and 1730.22 at the resonance of 1557.20 nm.

Both devices have similar circumferences, so their FSRs are close to each other. Comparing with the micro-ring, the racetrack apparently have a large FWHM. This is due to the fact that the racetrack has elongated coupling region. The longer coupling region enables broader bandwidth. Racetrack provides an extra dimension in design space when a wide passband (spectral width) and a controllably low finesse are needed.

2.4.3 Directional Coupler

2.4.3.1 Introduction

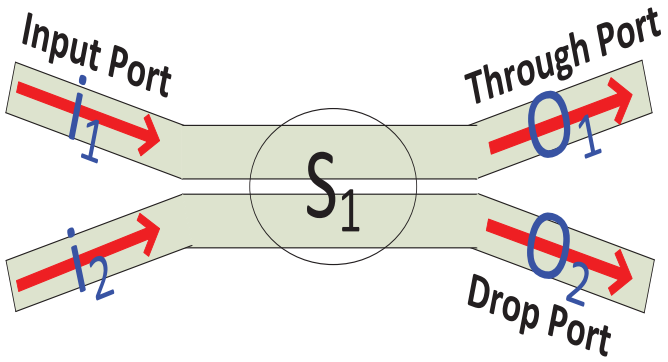
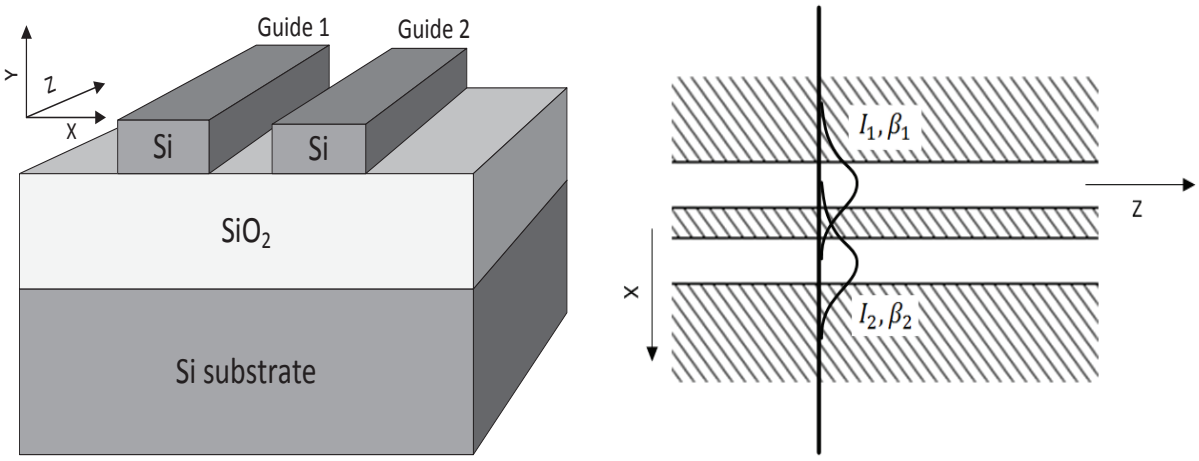


Figure 2.13: Schematic of a directional coupler. S_1 is the coupling region, i_1/i_2 are the input ports, O_1/O_2 are the output ports.

Optical power that travels inside a waveguide can be coupled to another adjacent waveguide by its evanescent field. This interaction happens in the so-called directional coupler. It is one of the essential components in integrated optical interconnect and widely found in fiber and integrated optics [67, 68, 69]. Directional coupler has been used in coupling and splitting lights between waveguides, creating different communication channels. For instance, filter/switch design such as Mach-Zehnder interferometer (MZI) utilizes and relies heavily on the concept of directional coupler. A directional coupler is two distant waveguides that are brought together and run in parallel with a fixed gap in between for a distance of coupling length. Then the two arms of the directional coupler separate as shown in Figure 2.13. Unlike the micro-ring and racetrack structures in which the wavelength resonance is created by the fundamental optical mode, the wavelength-selective directional coupler operates by different mechanism. Two fundamental (even and odd) modes propagate in the structure, creating beat for broadband wavelength input spectrum.

2.4.3.2 Transmission Characteristics



(a) Cross-sectional view. Two coupling waveguides are parallel with each other. The middle SiO_2 insulating layer is 2 μm thick. The top device layer is 220 nm thick.

(b) Top view. Coupling mode I_1 is interacting with mode I_2. Their propagation constants are β_1 and β_2 respectively.

Figure 2.14: Schematic of mode coupling in SOI directional coupler structure.

Figure 2.14 shows a basic configuration of a directional coupler. Its optical transmission mechanism can be interpreted by the coupled mode theory. Figure 2.14(a) plots the cross-sectional view of the coupler. On the SOI wafer, the distance between two parallel waveguides influences the mode coupling. As displayed in Figure 2.14(b), when the gap is small enough so that the evanescent field tails of the two confined modes overlap with each other, power coupling occurs.

According to the coupled mode theory, the electrical field of the propagating mode in the coupling region can be expressed as:

$$\begin{aligned} E(x,y,z) &= E_1(z)I_1(x,y)e^{-j\beta_1 z} + E_2(z)I_2(x,y)e^{-j\beta_2 z} \\ &= A_1(z)I_1(x,y) + A_2(z)I_2(x,y) \end{aligned} \tag{2.7}$$

where $I_1(x,y)$ and $I_2(x,y)$ are the unperturbed normalized mode field profile. The power flow in each waveguide is $P_1(z)=|A_1(z)|^2$ and $P_2(z)=|A_2(z)|^2$. The coupled-mode equations are written in the following forms:

$$\frac{dA_1(z)}{dz} = (-j\beta_1 - \frac{\alpha}{2})A_1(z) - j\kappa A_2(z), \tag{2.8}$$

$$\frac{dA_2(z)}{dz} = (-j\beta_2 - \frac{\alpha}{2})A_2(z) - j\kappa A_1(z), \tag{2.9}$$

where α is the loss coefficient and κ is the coupling coefficient. Solving Equation 2.8 and Equation 2.9 with an initial condition of $A_1(0) = 1$ and $A_2(0) = 0$, the power flow in each waveguide is:

$$P_1(z) = |A_1(z)|^2 = \cos^2(\kappa z)\exp(-\alpha z), \tag{2.10}$$

$$P_2(z) = |A_2(z)|^2 = \sin^2(\kappa z)\exp(-\alpha z), \tag{2.11}$$

As shown in the above equations, the power flow interaction in both waveguides exhibits a sine square shape of profile.

2.4.3.3 Characterization

Figure 2.15 shows the SEM image of a part of directional coupler of our design. It was also fabricated at ePIXfab. This directional coupler has a coupling region of 1063 μm which is too long for the SEM to capture the whole structure. The coupling gap is 130 nm. The waveguide height of the two coupling guides is 220 nm and the width is the foundry standard 450 nm. We characterized this directional coupler in our lab. The optical transmission measurement of this structure at room temperature is plotted in Figure 2.16. An extinction ratio of more than 15 dB is achieved in this design. The FSR is about 6.2 nm and the bandwidth is about 3.1 nm. Its wide bandwidth can be deployed in a wide passband filter in the WDM design.

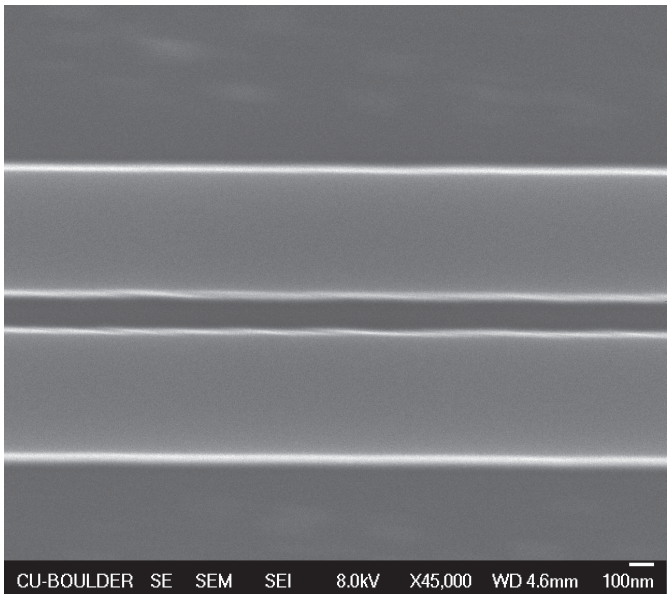


Figure 2.15: A SEM image of part of a directional coupler that was fabricated at the ePIXfab. The coupling region is 1063 μm with a coupling gap of 130 nm. The waveguide size of the two coupling guides is 220 nm (Height) $\times$ 450 nm (Width).

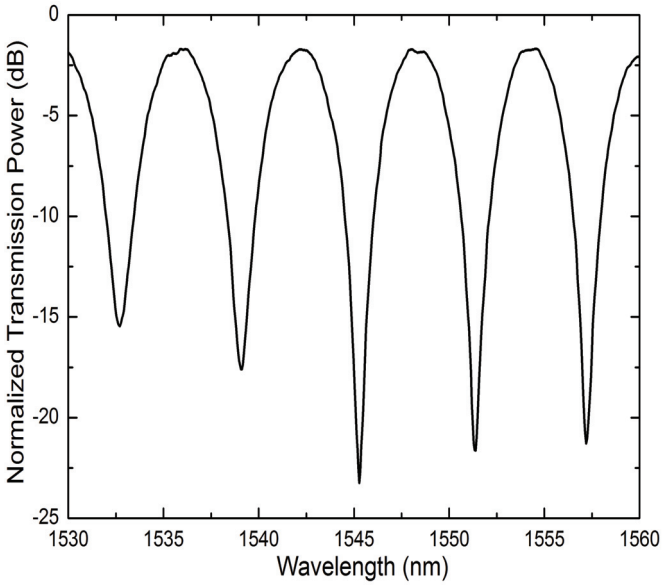


Figure 2.16: Optical transmission measurement of the directional coupler in Figure 2.15.

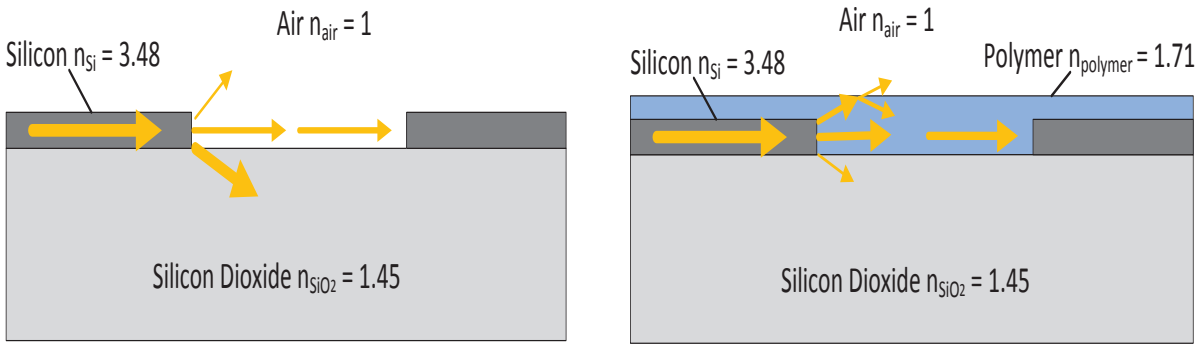
2.4.4 Optical Antenna

2.4.4.1 Introduction

The multi-core and many-core on-chip interconnection requires a significant amount of latency-critical, multi-cast traffic to enable transmission of bandwidth-demanding data. To enable such

interconnection, the optical network must support both broadcast and large numbers of channels of wavelength division multiplexing (WDM) for bandwidth. Broadcast requires one to many transmissions. Devices that perform such function are generally referred to as antennas. Antennas are crucial parts of our visionary on-chip architecture in Section 1.5.1. The bare SOI antennas have one issue that etched silicon waveguide antennas would radiate into their upper and lower cladding layers. In order to increase throughput, polymer top layer coating can be deployed to replace the air upper cladding. Polymer layer increases the index contrast of the materials that surround wave-guiding layer, therefore creating better confinement for the propagating optical mode. In this section, we design and demonstrate a highly efficient polymer-coated antenna device for the on-chip communication network.

2.4.4.2 Operation Mechanism

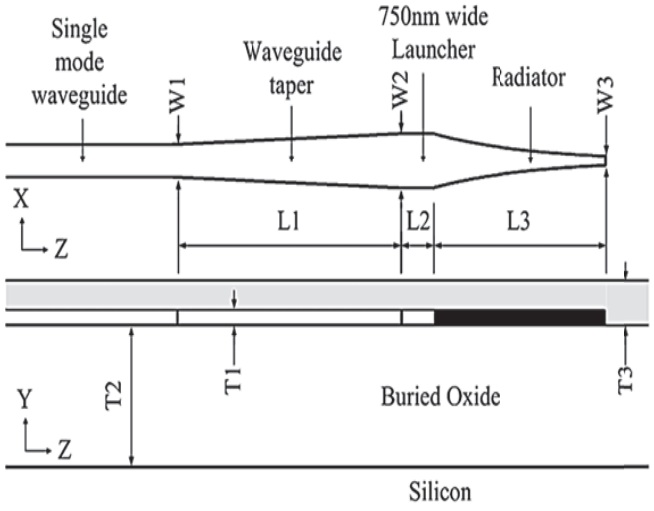


(a) (b)

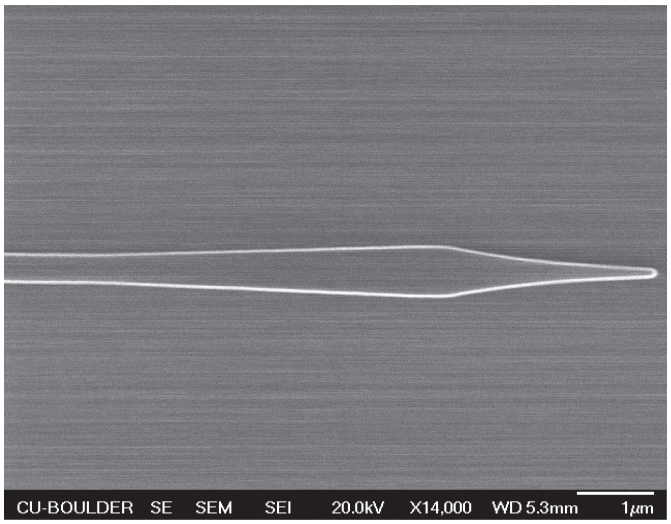
Figure 2.17: A pair of diagrams that illustrate the functionality of power overlay for in-plane antennas. (a) Illustration of the propagation of a wave from a diffraction antenna output. The higher index of the silicon dioxide (silica) with respect to air causes a significant portion of the radiated light to propagate downward into the silica (SiO_2). (b) When the SOI substrate is coated with a polymer with index higher than silica, the radiated light may be effectively guided in the horizontal direction when the dimensions of the guide are single mode at the operating wavelength.

Figure 2.17 displays how polymer improves power transmission efficiency of the SOI antenna pairs. A coated polymer with refractive index (in our case of polyimide with index of refraction $n \approx 1.71$) higher than that of silicon dioxide ($n \approx 1.45$) operates as a slab waveguide between the

silica (silicon dioxide) substrate and the air above. As shown in Figure 2.17(b), the polymer coating serves as a 2D transmission medium for light emitted by the on-chip dielectric antenna. A free-space antenna that uses air as a 3D transmission medium satisfies a three dimensional Friis equation with the field falling off as $1/r^2$ in the antenna far field, where r is the source to receiver distance. The



(a)



(b)

Figure 2.18: The SOI optical rod antenna design and fabrication. (a) Plot of the top and side views. The design values are: L1 = 4 μm, L2 = 0.5 μm, L3 = 3 μm, W1 = 0.45 μm, W2 = 0.75 μm, W3 = 0.13 μm, T1 = 0.22 μm, T2 = 2 μm, T3 = 0.5 μm. (b) A SEM image of a fabricated SOI antenna design.

two dimensional Friis equation exhibits a $1/r$ dependence. Concentrating the radiated power in a planar layer, then, enhances the on-chip transmission between antennas. The case of SOI is still more severe than free space because of the silicon dioxide (silica) substrate. Without the polymer layer, a significant fraction of the transmitted power radiates downward into the silica layer to be further refracted into the silicon substrate rather than guided in the polymer layer, as illustrated in Figure 2.17(a). Figure 2.18(a) shows a schematic of a single SOI optical rod antenna of our design. It comprises of a single mode waveguide that carries optical waves, a waveguide taper that tapers to a 750 nm-wide antenna launcher and a radiator tip. This antenna is designed to operates at optimally with a 500-nm thick polyimide overlay (T3 = 500 nm) [70]. Finite integration technique (FIT) code CST [71] and finite element method (FEM) code HFSS [72] are used in the numerical modeling for validation. Excellent agreements are obtained.

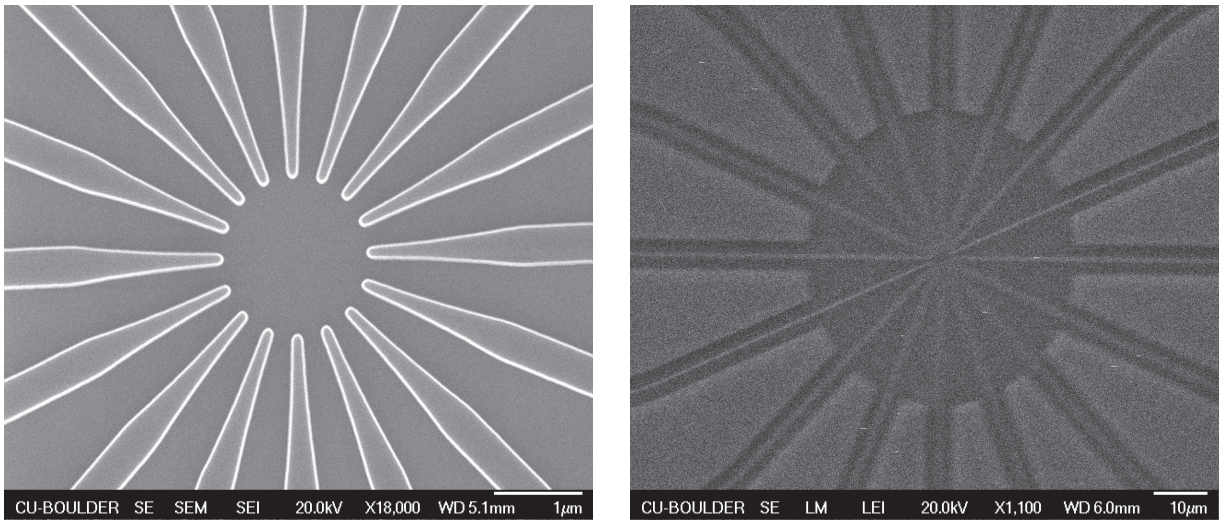
Geometry parameters	Design value (μm)	Fabrication value (μm)	Variation percentage
L3	3.00	2.74	8.7%
W1	0.45	0.38	15.6%
W2	0.75	0.67	10.7%
W3	0.13	0.09	30.8%
Antenna tip	Rectangular	Round	N/A

Table 2.1: Fabrication induced variations on the antenna geometry.

We fabricated this antenna design at the ePIXfab. Figure 2.18(b) displays the SEM image of a fabricated antenna design on SOI wafer. Fabricated induces certain process variations on the designed geometry of the antenna. A comparison between the geometry parameters before and after fabrication is listed in Table 2.1. Parameters are noted in Figure 2.18(a). The antenna dimension variation is about 8.7% in length and 10.7% in width. The largest fabrication induced variation happened at the antenna tip where the fabricated tip is shrunk by around 30.8%. The designed rectangular shape of tip is rounded after fabrication. Note that the 193-nm lithography tool is deployed in the ePIXfab wafer shuttle run at current stage and the minimum allowed linewidth is 120 nm for this lithography technology node. The design value for the antenna tip is 130 nm

which is very close to the minimum allowed linewidth. The closer it is to the 120 nm, the more likely higher fabrication variation is introduced, due to etching process and mask error [73]. The waveguide was shrunk by 15.6% in this case.

2.4.4.3 Characterization



(a) (b)

Figure 2.19: SEM images of a 16-antenna any-one-to-all circular array before and after polymer coating.(a) Before polymer coating. The design of individual antenna is the same as what is shown in Figure 2.18(a). The distance between two opposite antennas is 1.42 μm. (b) After polymer coating. A layer of 500-nm thick polyimide (n = 1.71) is coated onto the antenna array. Polyimide infiltrates well in the device layer and there is no obvious defect found. The blurring image is due to the poor electron conductivity of the polyimide.

Figure 2.19 display the SEM images of a fabricated 16-antenna any-one-to-all array without and with polymer coating. The waveguides are designed to be operated as diffraction antennas. The waveguides are arranged to form a circular structure. The waveguide terminations radiate their guided light and receive light radiated from the other waveguide terminations into their waveguide mode. Each of these antennas is connected to a port of the chip through a waveguide. These ports are equipped with grating couplers which couple light beam from a single-mode fiber into the SOI waveguides. Polyimide was conveniently processed and coated onto the antenna array for a thickness of 500 nm. Figure 2.19(b) illustrates the coating quality of such polymer layer. There

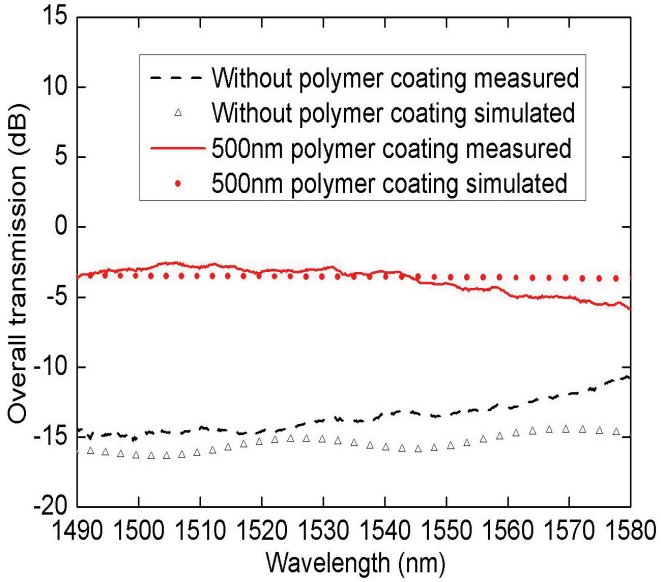


Figure 2.20: Comparison between the simulated and the measured results of the 16-antenna any-one-to-all array without and with 500-nm thick polyimide coating. The simulated and measured show remarkable agreement for all wavelengths below 1550 nm in the same wavelength regime where the transmitted power improvement is greater than 10 dB.

were no obvious coating defects such as bubbles or holes found in the polymer.

The results of spectral throughput measurements carried out on the 16-antennas circular array without and with a 500-nm thick polyimide layer are depicted in Figure 2.20 alongside simulation results. The quantity plotted on the vertical axis is the sum of the power output of each of the antennas. The agreement between theory and simulation is quite good except near the upper reaches of the wavelength sweep above 1550 nm. The total summed received signal improvement is greater than 10 dB for all wavelengths less than 1550 nm.

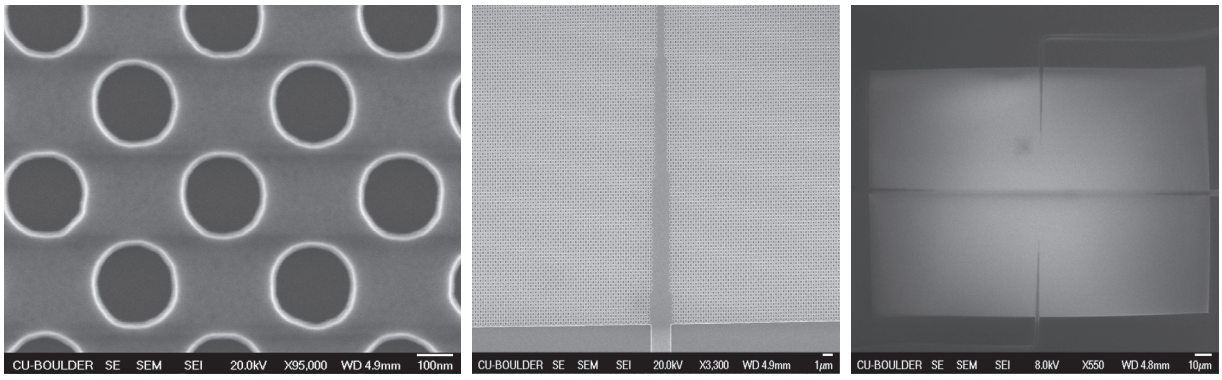
2.4.5 Photonic Crystal

2.4.5.1 Introduction

A photonic crystal (PC) is a periodic, dispersive structure. Periodic dielectric loading in one, two or three dimensions can provide spatial and spectral manipulation of light. The large index contrast in high index material makes silicon on insulator (SOI) a promising platform for

compact periodic structures. Two dimensional PCs that consist of rows of holes in SOI promise to provide a flexible and versatile platform for spatial and spectral manipulation of guided light in silicon photonic circuits. Most PC devices are passive devices that have been specifically designed to perform a certain function. Such passive PC structures lack post fabrication tunability. Process variation during fabrication or operating-point drift may render such devices unusable. Tunability is desirable. Active tuning schemes using electrical [74], thermal [75] or mechanical [76] means have been proposed. In this section, we demonstrate a simpler, more robust method for tuning the optical properties of a photonic crystal. We selectively fill the void nanostructures of the photonic crystal with the polymeric material whose refractive index may be varied during the polymer formulation.

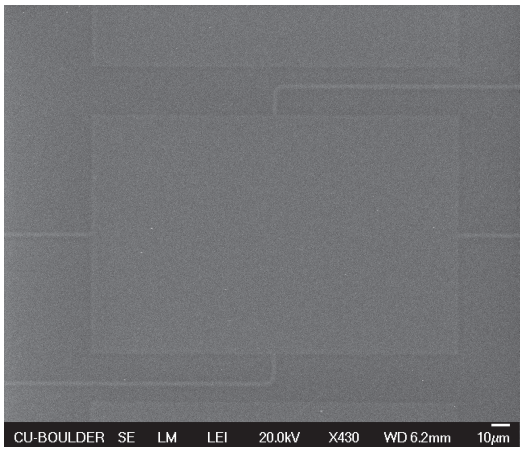
2.4.5.2 The Structure and Polymer Tuning Characterization



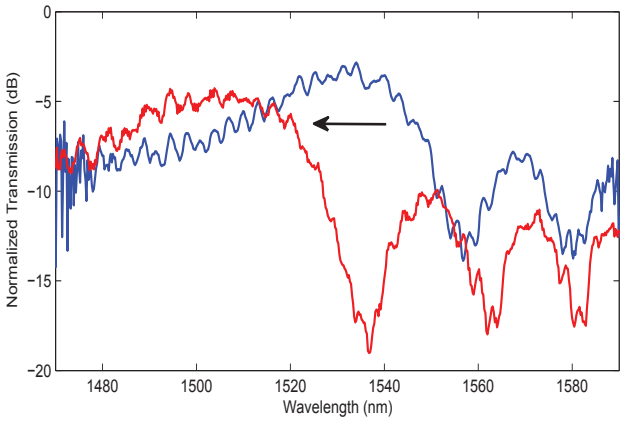
(a) (b) (c)

Figure 2.21: SEM images of a photonic crystal waveguide structure. (a) Zoomed-in image of the periodic hole array. The diameter of the hole is 220 nm. (b) Image of the waveguide path in the photonic crystal. Waveguide is formed with a designed 'defect' path in the periodic structure. (c) Complete view of the fabricated photonic crystal waveguide design. The waveguide is in the middle row.

Several SEM images of the PC structure for coating are shown in Figure 2.21. The lattice constant of this PC is 500 nm with a hole diameter of ∼220 nm as illustrated in Figure 2.21(a). More complex PC structures can be generated simply by modulating the row spacings and hole sizes. The device pictured was fabricated by ePIXfab as was the any-one-to-all antenna array. The holes in the untuned PC are etched into the silicon after masking, using the silica layer as the etch



(a)



(b)

Figure 2.22: SEM image of the polymer coated photonic crystal waveguide and measurement results of its transmission characteristics before and after polymer turning. (a) Image shows the top surface of the photonic crystal waveguide with a 1.2-μm thick polyimide overlay. The coating is good that no obvious polymer defect is observed. (b) Transmission property of the photonic crystal waveguide before (blue curve) and after (red curve) polymer coating. The arrow indicates the spectrum shift.

stop. In the foundry fabricated device voids are filled with air. The surrounding silicon then is the 220-nm thick silicon on silica. The PC pattern is organized into a rectangular lattice with a single row defect waveguide through the center, as depicted in Figure 2.21(b) and Figure 2.21(c).

We coated the PC waveguide with a 1.2-μm thick polyimide overlay. Figure 2.22(a) shows the coated device. The structure is somewhat obscured by the thickness of the polymer layer. There is no obvious polymer defect observed in inspection, indicating good coating quality of the film. The optical transmission behavior of the device is determined by the refractive indices of the constituent materials. By using processes such as doping chromophores and bleaching, the refractive index of the top layer polymer can be engineered. It provides a convenient way to achieve controlling and tuning the transmitting functionality of the PC waveguide. Spectral transmission measurements were performed on the photonic crystal structure. As shown in Figure 2.22(b), filling the holes of the PC shifts the transmission spectrum of the waves that enter the left port in Figure 2.22(a) and exit at the right. The measured transmission spectra shows a shift in their transmission minima and maxima due to polymer loading. A notable point is that the coated polymer exhibits almost

the same transmission maximum (within 1 dB). As the PC structure is a self collimating structure in which the light traverses through a large number of the holes, the transmission is meanwhile a good measure of the polymer quality.

2.5 Conclusion

Silicon photonic technology holds promises for the on-chip WDM communication. Individual photonic device's optical performance and its fabrication are key to the success of further development. In this chapter, we introduce the wafer-scale fabrication for silicon photonic devices and the device measurement setup. We characterize a grating coupler which enables light coupling in and out of photonic devices. The maximum coupling efficiency of such coupler is around 30%. We introduce the designs of micro-ring and racetrack resonators. With elongated coupling region, racetrack presents better coupling than the micro-ring resonator. The bandwidth of the racetrack is about 0.9 nm whereas the bandwidth of the micro-ring is about 0.6 nm. We investigate the optical property of a directional-coupler which has a coupling region of 1063 μm. A extinction ratio of 15 dB is achieved in this design. We realize an optical 16-antenna any-one-to-all array. With the assistance of sub-micron polymer coating, this array exhibits superior broadband broadcasting functionality. We also test the optical tuning in a polymer-coated photonic crystal structure. In the device characterization process, we come to notice that the optical performance of fabricated photonic devices can be influenced by the process and thermal induced variations. These variation effects are investigated in Chapter 3.

Chapter 3

Process Variation in Silicon Photonic Devices

3.1 Introduction

Silicon-on-insulator (SOI) technology enables fabrication of high index contrast optical devices on silicon substrates. High index contrast allows for high optical integration density. An SOI system-on-a-layer holds promise for on-chip interconnections [77]. The yield of the silicon complementary metal-oxide-semiconductor (CMOS) circuits to be interconnected is high, generally greater than 90%. In order for the SOI to be viable for on-chip interconnection, not only must the SOI yield be as high as the CMOS yield, but the yield of monolithically-produced, optically-interconnected structures must be comparable to the CMOS yield and the methods of controlling run time variations must be compatible. Here we consider the first part of this problem, that of the process variation of standalone SOI circuits given the tacit assumption that process variation defines the yield for given a set of system requirements. We discuss the relation between yield and process variation elsewhere [78]. Here we focus on the salient features of the process variation data. We will see that for the values of quantities of interest in this paper, the locations of maxima and minima on measured optical transmission as a function of wavelength curves drift in value with distance. We will see that the drift can be characterized by a linear growth in the variance of a sample of values. The process variation we observe for rings and racetracks is roughly 1.33 nm^2/cm and 0.33 nm^2/cm for directional couplers.

To characterize wafer-scale process variation, we have characterized a variety of silicon-on-insulator (SOI) photonic devices on four wafers fabricated through the ePIXfab program [41]. We

have chosen to quantify thermal drift and process variation through measurement of the wavelength dependent optical transmission (transfer function) of fabricated micro-rings, racetrack resonators and directional couplers. Our work expands on earlier work by Selvaraja [79] on racetracks, Mach-Zehnder and grating couplers and by Zortman [80] on micro disk resonators. We have extracted maxima and minima from the measured transfer functions in order to quantify how features drift with respect to temperature (thermal drift) and vary with respect to position (process variation).

Before analyzing the process variation data, we determined the effect of thermal variation on transfer function features and effective index. That is, we measured transfer functions for a number of components on different dies in different columns and rows of the wafer while controlling the substrate temperature. We then tracked features (maxima and minima of the transfer functions) as we varied the effective substrate temperature. The magnitude of the effects of the thermal variation on effective index that we observe (the features on the transfer function of a 5 μm-radius micro-ring resonator drifts at the rate of 78.5 pm/°C) is in agreement with what others report in the literature [81, 82, 83, 84, 85, 86, 87, 88, 89]. The measurements indicate that thermal drift is independent of position on the wafer. This indicates that thermal tuning could be used as a method for mitigating process variation and runtime drift as has been discussed extensively elsewhere [90, 91] where the power overhead for this operation acceptable. We do not consider such mitigation techniques further in this work but instead concentrate on the salient features of process variation.

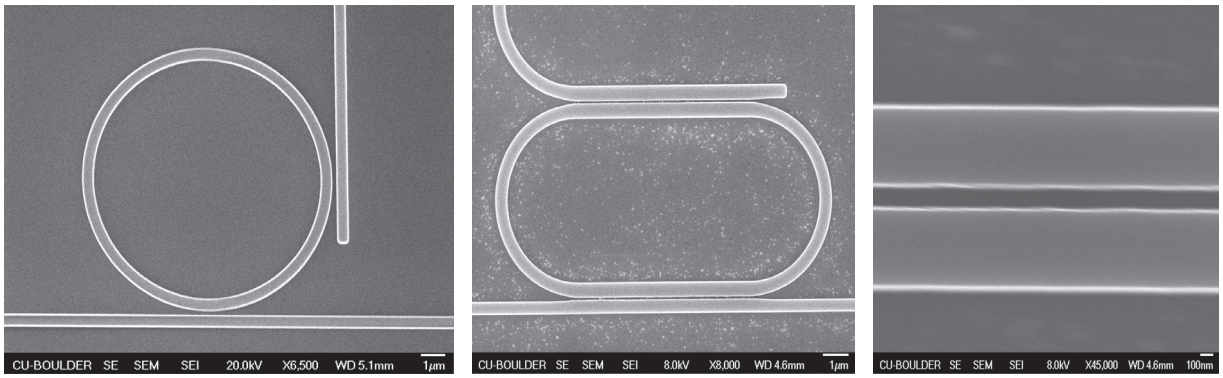
Room temperature data taken on various devices in various rows and columns of the wafer data indicate that values of transfer function features of interest vary across the wafer. It is the variance of arrays of values within a given spatial extent that we have come to refer to as process variation. In the work here, the spatial extent that we use is the number of rows in a given column of a wafer. We have generally swept the exposure dosage across the columns. The dosage then within the rows of a column is constant. Much as in Brownian motion where the standard deviation (distance travelled) increases as the square root of the time, we find that the standard deviation of the sample of values increase as the square root of the number of rows included in the sample

of values. That is to say, the variance is linear in the spatial extent. We note that in the extent of the linear variation of variance, the magnitude which is on the order of something greater than 1 nm^2/cm is in agreement with the values obtained by Selvaraja [79] for both intra-die and inter-die process variations.

Selvaraja [79, 92, 93] also correlated process variation with wafer-scale silicon layer thickness. We do not have the capability to make such measurements to the required precision to quantitatively consider this effect. We do note that in these previous works as well as in our own, the drifting non-uniformity also appears to vary from wafer to wafer. Indeed, the shape of the slowly varying component that we extract from the data differs from those of Selavaraja. Selvaraja points out that if the form of the slowly varying component is known a priori then the drift can be compensated by varying the fabrication conditions on that wafer. The analysis we use in this work could be used to aid in such a compensation scheme. We caution that such a scheme could be involved if each wafer need be treated independently. More study is necessary.

The question of yield requires discussion of the function of the chip and the tolerances that are allowed at the system level. These system requirements will differ with the interconnection scheme [51, 52, 94, 95, 96] as well as any variation mitigation approach employed [90, 91]. SOI system-on-a-chip also holds promise for multi-chip interconnection that again would require a completely different set of system specifications and, therefore, a still different definition of yield. Network function and system analysis are beyond the scope of this work but are treated in another work that is in press [78].

The chapter is organized as follows. In Section 3.2, we discuss the test structures that we employed for this study and how the measurements were performed on these structures. Thermal variation is discussed in this section. In Section 3.3, we present the wafer-scale measurement results and characterize the process variation. A Markovian nature of variation pattern is observed. In Section 3.4, similarities and differences between our results and other works are analyzed.



(a) (b) (c)

Figure 3.1: SEM images of the 450 nm × 220 nm waveguide structures of interest including (a) a micro-ring resonator with radius of 4.975 μm and 200 nm coupling gap, (b) a racetrack resonator with the coupling length of 7 μm, bend radius of 3 μm and 130 nm coupling gap, and (c) a section of the coupling region of a directional coupler with coupling length is 1063 μm and 130 nm gap.

3.2 Test Structures and Their Measurement

The devices that comprise our test array were introduced in Section 2.4.2 and Section 2.4.3. They are reiterated in this section for convenience. The characteristics of the wafers on which the devices were fabricated and the measurement setup were described in Section 2.2 and Section 2.3. Our measurements throughout the process consist of determining the wavelength dependent transmission of given devices. The wavelength-dependent transmission that we will generally call the transmission function will exhibit characteristic features such as maxima and minima. The maxima of the transfer function of micro-ring and racetrack resonators as well as the minima of the transmission function for directional couplers will sometimes be referred to as resonant wavelengths in what follows. We compare our measurements made with those made with other apparati by determining the effect of substrate temperature on measurement result. That is, we measure the transfer function (transmitted power as a function of wavelength) as parameterized by substrate temperature. We find that our measurements agree with those in the literature. Throughout the paper, we unify our measurement data for rings, racetracks and directional coupler devices that we measure through use of effective index theory. That is, the wavelength transfer function of each device is dependent on the effective index (propagation constant) of the fundamental mode of

that device [97]. We can calculate these mode indices to any level of approximation that we wish using available software. We complete this section by determining effective index as a function of substrate temperature. We find that calculations of the effective device index based on the change of substrate temperature recover the observed wavelength transfer functions. More discussion of use of analytical transfer function models to extract more data from measurements as well as to make predictions of device performance is introduced in Chapter 4.

3.2.1 The Fabricated Devices

Our process variation data are based upon wafer-scale measurements of a variety of types of devices. These representative device types include micro-ring, racetrack, and directional coupler. However, due to the fabrication variation, the dimensions of each design vary across all the dies within the same column on wafer. Scanning electron microscope (SEM) images of some fabricated devices are shown in Figure 3.1. Figure 3.1(a) depicts the micro-ring resonator with a radius of 4.975 μm. The coupling gap in the micro-ring is 200 nm and the waveguide width are uniformly designed to be 450 nm. Figure 3.1(b) illustrates a racetrack resonator whose coupling length is 7 μm in both arms and bending radius is 3 μm in the two semicircles. Its coupling gap is 130 nm and waveguide width is 450 nm. Figure 3.1(c) displays a part of the coupling section of a directional coupler. The coupling length of this structure is 1063 μm which is too long for the SEM to capture without sacrificing resolution. The coupling gap is 130 nm, the same as that of the racetrack resonator of Figure 3.1(b) and the waveguide width is 450 nm. These devices were designed, simulated, laid out, measured and the measurements analyzed in our lab.

We carried out process and thermal variation measurements using our fiber testing platform that is introduced in Section 2.3. For thermal variation measurements, the temperature can be accurately controlled in the range of 25°C - 50°C. Each chip to be measured is placed in the sample holder that is equipped with a temperature controller. The heating starts at a controlled lab room temperature of 25°C and the heating step is set at 5°C increment. The transfer function data at each heating step is taken once the temperature has stabilized.

Process variation measurements were performed on both the LETI and the IMEC wafers. Light coupling to the devices is controlled and optimized by a computer-aided automation program. Manual intervention is reduced to the minimum possible. The SLED light source maintains constant power during the measurements and the wavelength spectrum is stable. Once the photonic devices are fabricated, their optical performance can only be influenced by temperature fluctuation under our lab testing condition. The measurement temperature is controlled to be at 25 °C for process variation measurements.

3.2.2 Measurements and Analysis of Wavelength Dependent Transmission

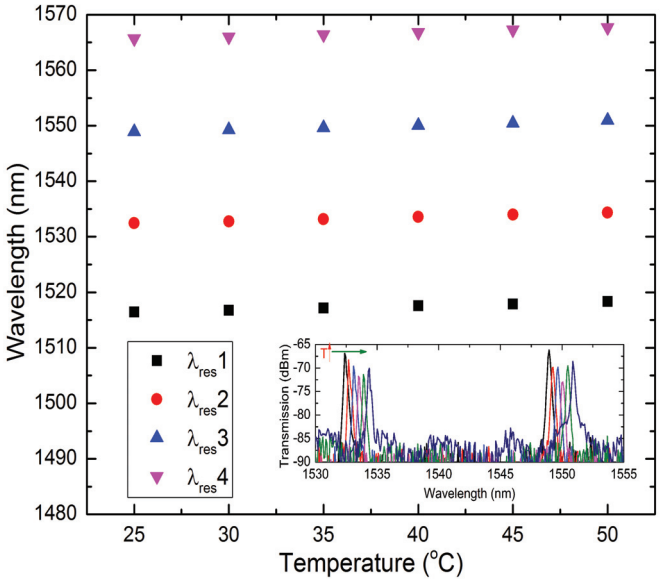


Figure 3.2: Study of the variation of 4 maximum transmission wavelengths of the 4.975-μm-radius micro-ring in Figure 3.1(a) at 6 temperatures in the range of 25°C - 50°C. The inset shows a regime of transmission function that includes 2 peaks at all of the temperatures.

We carried out measurements of the wavelength dependent optical transmission (transfer function) as we varied the substrate temperature in the range from 25°C - 50°C, that is, a realistic fluctuation range for operation of a silicon processor [98]. The devices employed were micro-ring, racetrack and directional coupler as illustrated in Figure 3.1. The thermal drift measurement results for the 4.975-μm-radius micro-ring in a wavelength-division multiplexer (WDM) structure appear

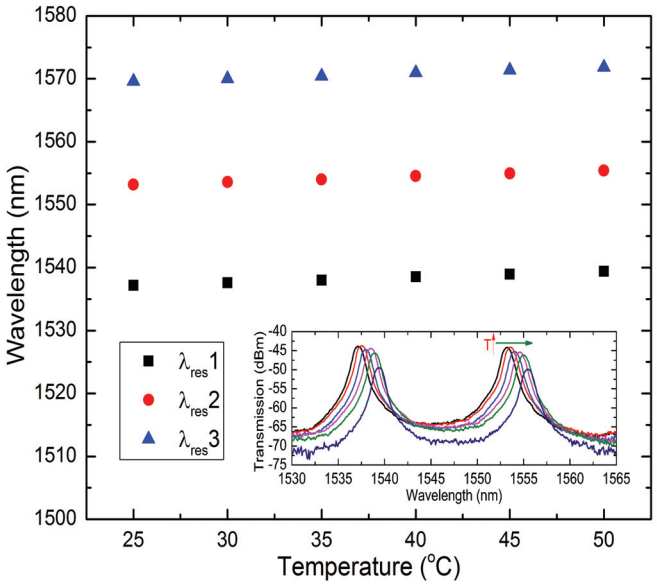


Figure 3.3: Study of the variation of 3 maximum transmission wavelengths of the racetrack of Figure 3.1(b) at 6 temperatures in the range of 25°C - 50°C. The inset shows a regime of transmission function that includes 2 peaks at all of the temperatures.

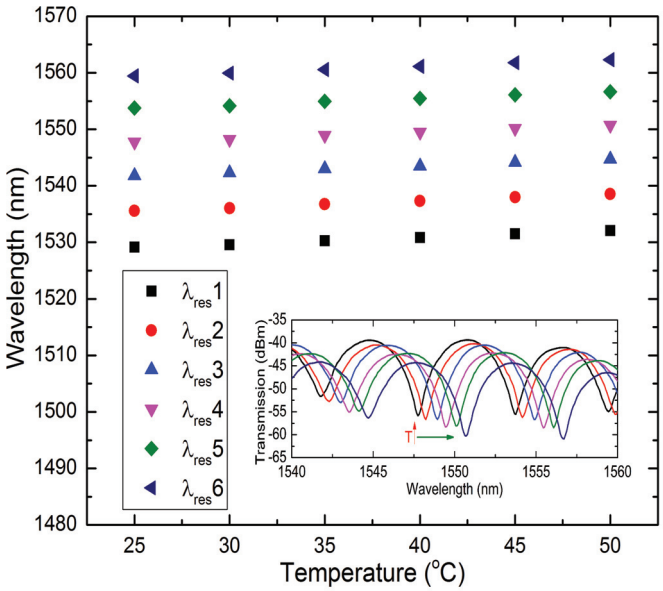


Figure 3.4: Study of the variation of 6 minimum transmission wavelengths of the directional coupler of Figure 3.1(c) at 6 temperatures in the range of 25°C - 50°C. The inset shows a regime of transmission function that includes 3 minima at all of the temperatures.

in Figure 3.2, for the racetrack in Figure 3.3 and for the directional coupler in Figure 3.4.

The micro-ring structure exhibits wavelength drift of ∼78.5 pm/°C in our measurement. We

obtain a wavelength drift of roughly 89.7 pm/°C for the racetrack resonator. These values are in agreement with the thermal drift values on similar structures cited in other works, which range from 90 pm/°C - 110 pm/°C [81, 82, 83]. These values are also in agreement with effective index variation that can be approximated from the thermal-optical coefficient $\sim 1.86\times10^{-4}(K^{-1})$ [85, 98] for silicon. As shown in Figure 3.4, the measured selected wavelength drift for a 1063-μm directional coupler is around 116.4 pm/^{o}C. We are aware of no values in the literature to compare to.

All of these resonant devices function as Fabry-Perot resonators. A selected wavelength, λ_{sel} varies with effective index according to:

$$m\lambda_{\text{sel}} = L_c n_{\text{eff}}(\lambda_{\text{sel}}) \tag{3.1}$$

where L_c is the length of the curved path for the micro-ring structure [99, 100] and

$$m\lambda_{\text{sel}} = L_c n^c_{\text{eff}}(\lambda_{\text{sel}}) + L n^s_{\text{eff}}(\lambda_{\text{sel}}) \tag{3.2}$$

for the racetrack where L_c and L are the lengths of the curved and straight regions of the racetrack, n^c_{eff} and n^s_{eff} are the effective indices of the corresponding regions. The difference in the effective indices of this two regions is significant and can reach up to a value of 0.03 [101, 102]. There are two modes, an even and an odd, in the directional coupler [103, 104], such that

$$m\lambda_{\text{sel}} = 2L(n^e_{\text{eff}}(\lambda_{\text{sel}}) - n^o_{\text{eff}}(\lambda_{\text{sel}})) \tag{3.3}$$

where L is the length of the coupling structure in directional coupler. n^e_{eff} and n^o_{eff} are the effective indices for the even and odd modes in the structure. In the above models, m is the m^{th} mode number and λ_{sel} is a selected (meaning with a fixed m) wavelengths. Each selected wavelength has a unique effective index value $n_{\text{eff}}(\lambda_{\text{sel}})$. Further discussion will be given to the modeling in Chapter 4. On-chip thermal variation affects the effective index n_{eff} of corresponding devices,

thereby affecting the wavelength drift. Through the measurements on thermal variation effect, we verify our measurement and analysis methodology.

3.3 Measurement and Analysis to Determine Process Variation

In this section, we present room temperature measurements of transfer functions for micro-rings, racetracks and directional couplers. An analysis of the measurement data indicates that the wavelength variance of a given transfer function feature calculated on a set spatially adjacent measurement points exhibits a variance that depends linearly on the spatial extent of the sample. That is, the difference in the mean value of wavelength of, for example, a minima of the transfer function of directional coupler at two different locations on a wafer increases with the distance between the devices. The dependence on the distance between the devices is the same as the dependence of as the mean deviation of a random walk would vary with the number of steps taken. It is also comparable to the mean deviation of the distance from its original stationary location that a particle exhibiting Brownian motion would display with very small steps. This Markovian nature (memoryless) of the magnitude of the process variation indicates that a number of processes are contributing to the process variation underlying this effect. As will taken up again the discussion, this observation is in agreement with other process variation studies.

3.3.1 Micro-ring

The measurements were carried out on a four-ring WDM structure as shown in Figure 3.5. The wafer was fabricated at LETI under the ePIXfab [41] shuttle program. As shown in Figure 3.6, we measure wavelength dependent transfer functions on 12 of the 14 dies in the upper half of a 28 die column (see, for example, the schematic of an 18 die column in Figure 2.2). The most salient features of the transfer function (see the inset of Figure 3.6) are the transmission peaks that we will variously refer to as resonant wavelengths or transfer function maxima. We logged the intensities, wavelengths and rows of two peak wavelengths per transfer function for the twelve dies, that is, for 94 discrete wavelengths (two data points lost due to fabrication defects). Figure 3.6 is a scatter

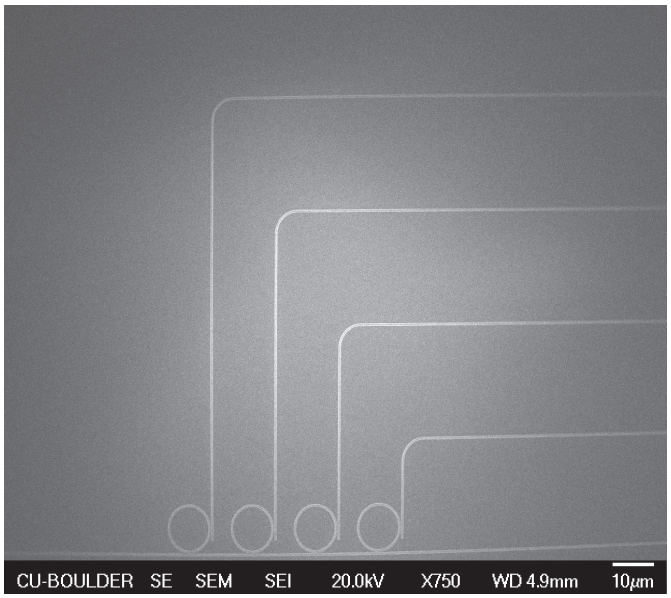


Figure 3.5: A SEM image of a wavelength-division multiplexer (WDM'er) that consists of four micro-ring resonators with 200-nm gaps and 450-nm waveguides. From left to right, the radii of the micro-rings are 4.975 μm, 4.995 μm, 5.015 μm and 5.035 μm, respectively.

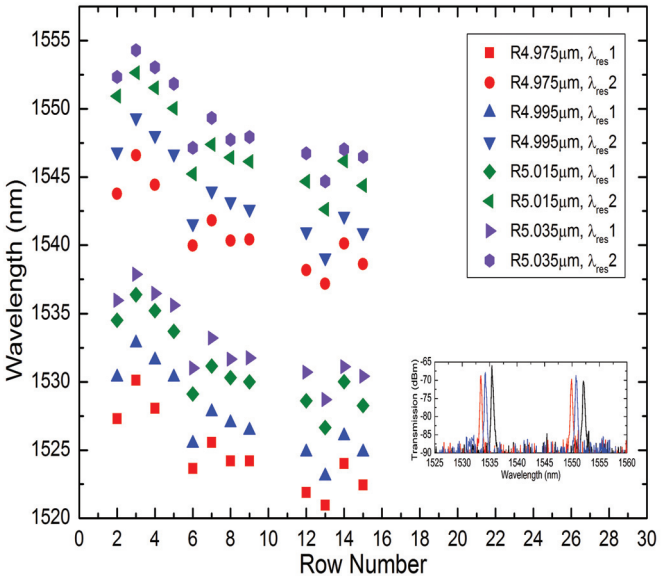


Figure 3.6: A scatter plot containing two of the maximum transmission wavelengths of each of the four transmission functions of the WDM device of Figure 3.5 realized on 12 dies of a 28 die column (for example, see the layout of the 18 die column of Figure 2.2). The inset shows the measured transfer function for this design realization on 3 adjacent dies.

plot of wavelength versus die location (in units of row number) for the two wavelengths on each of the four transfer functions per each nominally equivalent device (one per die) for each of the

12 dies. The scatter plot contains a total of 94 wavelengths. The smaller the row number is, the closer it is to the wafer edge. The measured peak wavelengths tend to increase in the direction of the wafer edge, at least, between rows 13 to 3. The average drift in wavelength from rows 13 to 3 is ∼9.64 nm. The average drift of peak wavelength between two adjacent dies is ∼1.78 nm for the 4.975-μm ring, ∼1.95 nm for the 4.995-μm ring, ∼1.92 nm for the 5.015-μm ring and ∼1.73 nm for the 5.035-μm ring.

The data indicates that the 8 sets of 11-12 points per set are highly correlated. Equation 3.1 indicates that this should be the case. That is, the free spectral range (FSR) in nm is given by

$$\mathrm{FSR} = \frac{\lambda_0^2}{n_g L} \tag{3.4}$$

where λ_0 is the center wavelength, n_g is the group index and L the circumference is roughly 31.4 m. The FSR which is about 16.5 nm is, therefore, larger than the drift range in nm of the data for a given m value on a given measurement set across the wafer. We can then identify m values in the data from following the measurement points from die to die. For racetracks and directional couplers, the FSR is not so large and some care must be made to determine if the wavelength features have the same interpretation on different devices in different rows. Here, we can assume that we know which points go together for the microrings. We would then expect the pattern we obtain where the highest wavelength points correspond to the lowest m value for the smallest ring and the lowest wavelength points correspond to the largest m value for the largest ring.

Here, we associate the drift with a random process. Indeed, one can make a sequence of groupings from 2 up to 12 points. One can further combine all of the 94 points after the mean of each of the 8 (2 m values for each of 4 rings per WDM) is subtracted out. We start by grouping the points in rows 8 and 9 together. We then group 7, 8, 9 and 11 together and then successively add two more points to the grouping until we have included all 12 points. We carry this out for each of the 8 (2 m values times four individual rings), subtracting out the mean value for each and then plotting the variance of the group of points as a function of the spatial length of the association.

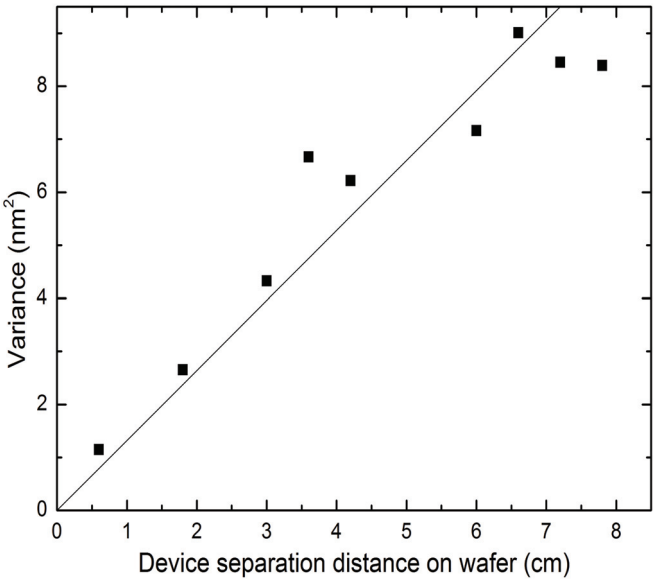


Figure 3.7: A plot of the variance of transmission wavelength peaks of the WDM structures over the device separation distance on wafer.

The result is as in Figure 3.7. As can be seen from the plot, the variance increases to roughly 8 nm^2 over 6 cm. One could then define the process variation to be 1.3 nm^2/cm. We will see that this number varies with device. We would imagine that this figure of merit also varies with processing conditions, being lower for higher resolution lithography and more meticulously fabricated SOI wafers by using advanced techniques, such as wafer-scale device density control [105], corrective wafer etching technology proposed in [79, 93]. This improvement per processing condition needs to be further investigated.

3.3.2 Racetrack

An example racetrack for the nominal design studied here is shown in Figure 3.1(b). This nominal design is comprised of 3 μm radius bends, coupling length of 7 μm, and waveguide width of 450 nm with a coupling gap of 130 nm. The wafer was fabricated at IMEC. We choose to study the wafer column where the fabricated devices have physical dimensions closest to our design. This column contains 18 dies. The inset of Figure 3.8 shows a wavelength regime of 3 transfer functions, each containing 2 peak wavelengths. We extracted 5 peak wavelengths, all lying in the range of 1490

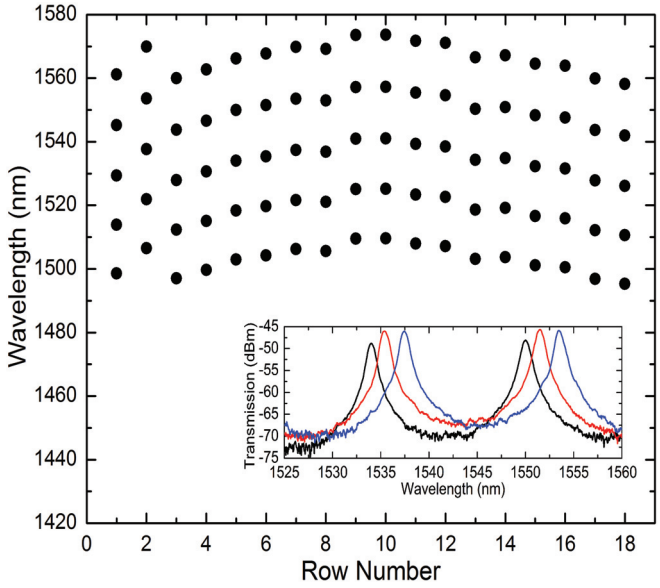


Figure 3.8: A scatter plot of 5 wavelength peaks of each of 18 transfer functions. The 18 transfer functions represent one per device of Figure 3.1(b) where these devices are repeated per die where there is one die per row for each of the 18 rows of a column of a wafer as depicted in Figure 2.2. Die (row) 1 and die (row) 18 are located at the edges of the wafer. The inset shows the wavelength dispersion of two peaks of three transfer functions on three adjacent dies.

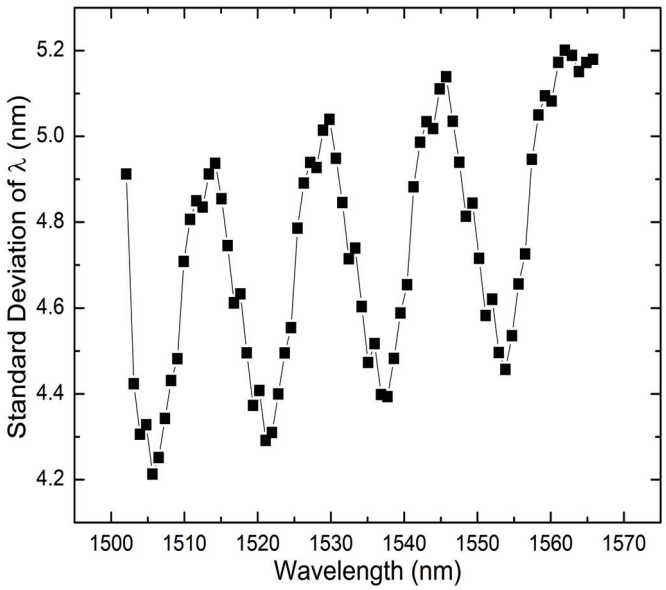


Figure 3.9: Plot of the standard deviation versus mean of each set of 18 consecutive wavelengths that can be constructed from the scatter data of Figure 3.8.

nm-1580 nm from each of the 18 dies that we studied, one each per row of the 18-row column. A scatter plot of the 90 points of this data is displayed in Figure 3.8. In the case of the micro-ring,

the FSR exceeded the drift. That is not the case here for this nominal racetrack design. Rather than pick a special sets of wavelengths across the rows, we instead use each set of 18 adjacent wavelengths. The mean and standard deviation of each of these sets are plotted in Figure 3.9. One would assume that the oscillation exhibited on the plot is due to different sets containing wavelengths with different m values from Equation 3.2. The upward trend of the values at the top and bottom of the oscillation indicates that the deviation of the data is wider at longer wavelength as seems apparent from the plot of Figure 3.8. The oscillation indicates that different groupings have different variances.

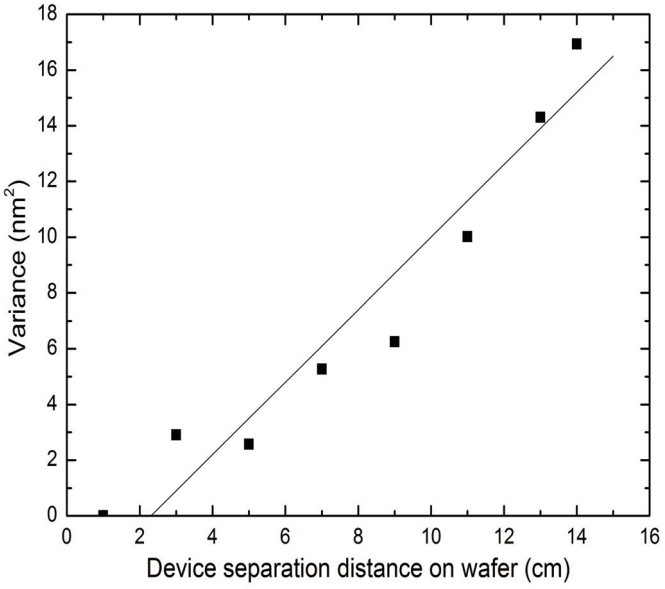


Figure 3.10: A plot of the variance of transmission wavelength peaks of the racetrack structures over the device separation distance on wafer.

Again, we test to see how the magnitude of the variance changes with the number of rows included. We do not include the values that are in rows 1 and 2 in the calculations as we see that the trend there is broken as we might expect trends to be broken near the edges of the wafer. The results are displayed in Figure 3.10. Again, we note that the variance is linear in the number of rows included in the averaging. Here the process variation, as defined by the increase of variance per cm is of the order of 1.3 nm^2/cm. That is, for 8 cm, the standard deviation is $\sqrt{10.5}$ nm or a little bit more than 3 nm.

3.3.3 Directional Coupler

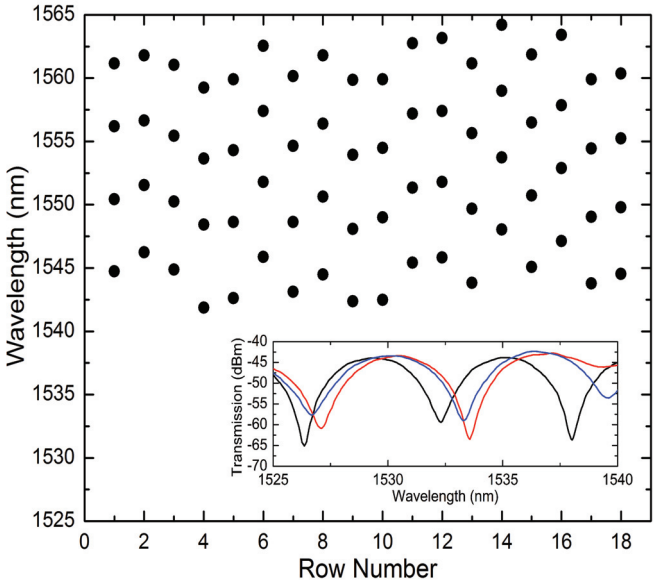


Figure 3.11: A scatter plot of the four adjacent minima of directional coupler transfer functions. The measured transfer functions are realizations of the device Figure 3.1(c) (nominal dimensions of the device: coupling length 1063 μm, waveguide width 450 nm and coupling gap of 130 nm) repeated one per die, one die per row of an 18 column row as per Figure 2.2. Die 1 and die 18 are located at the edges of the wafer. The inset indicates the minima located between 1525 nm and 1540 nm of three transfer functions.

Here we present measurements of the transfer function of a directional coupler. Figure 3.1(c) which depicts a portion of the coupling region of a directional coupler of our nominal design. This device was fabricated at IMEC on the same wafer as that with the racetrack design. We carry out the optical measurements on the same 18 dies which contain the racetrack and directional couplers. Figure 3.11 illustrates the optical measurement results of this directional coupler on all 18 dies. The wavelengths selected by each device are extracted and the drift pattern reveals the process variation across the wafer.

The FSR of this directional coupler is small compared with the average wavelength drift across wafer as was the case for the racetrack of the last section. Rather than assume that we can select the data that goes with an m value of Equation 3.3, we instead plot the standard deviations as a function of wavelength for all the possible sets of the minimum wavelength features in which

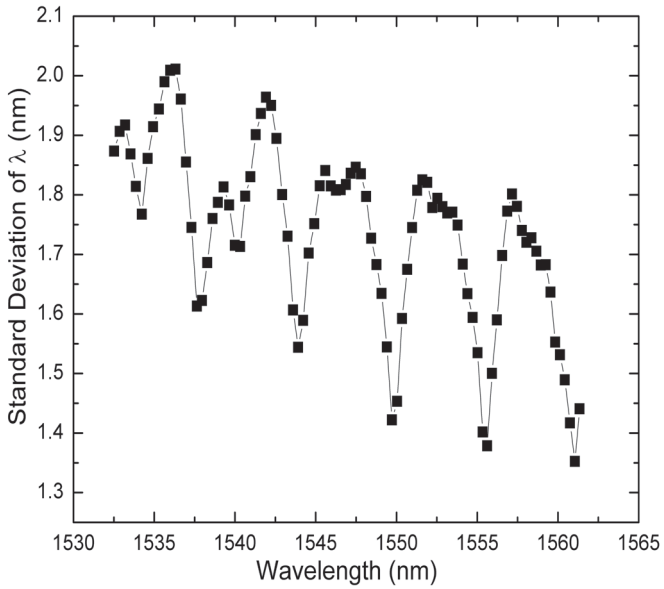


Figure 3.12: A plot of standard deviation (STD) versus mean value for each possible grouping of 18 adjacent wavelength data points of Figure 3.11.

all of the measured values are adjacent to each other. The results of this exercise are compiled in Figure 3.12.

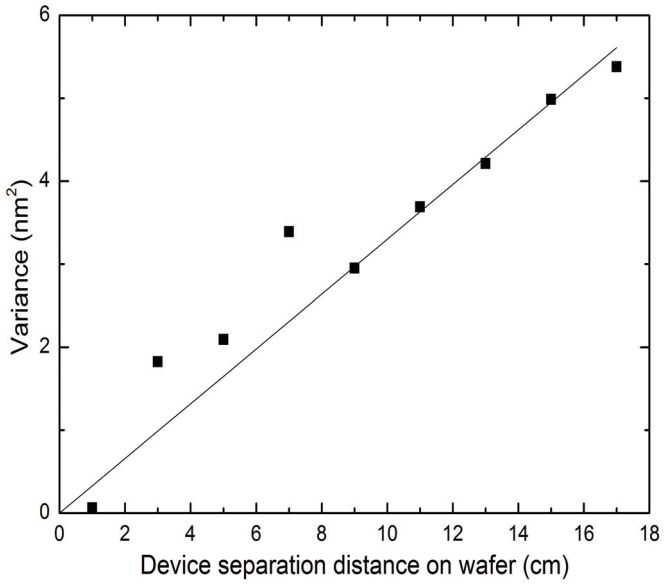


Figure 3.13: A plot of the variance of transmission wavelength minima of the directional couplers over the device separation distance on wafer.

As with the ring and racetrack, we again test for variation with spatial location. The results

are displayed in Figure 3.13. Again, the variance is nearly a straight line that has slope of 0.33 nm^2/cm. This variance is a quarter of that for the micro-rings and racetracks.

3.4 Discussion

Device	Thermal Variation	Process Variation
Micro-ring	78.5 pm/°C	1.3 nm^2/cm
Racetrack	89.7 pm/°C	1.3 nm^2/cm
Directional Coupler	116.4 pm/°C	0.33 nm^2/cm

Table 3.1: Summary of the thermal and local process variation of the fabricated devices.

The salient feature of our investigation was the uncovering of a seemingly simple relation between the distance between devices on the wafer and the standard deviation about the mean of the value of key features on the transfer function. The drift variance values are summarized in Table 3.1. It have been noted in the literature that a key feature such as a resonant wavelength will shift about 2 nm in response to a 1 nm shift in silicon layer thickness and 1 nm due to a 1 nm shift in lithographic linewidth. These relations are not empirical but can be simulated using the relation between resonance wavelength for a given device and effective index of the waveguiding sections of a guided wave device, that is, a micro-ring, racetrack or directional coupler, in particular.

The relation between distance and difference in response is not limited to our data or to the wafer scale. We note that Selvaraja et al. [79] found that the process variation for a ring resonator was roughly 1.5 nm^2/cm and that for a Mach-Zehnder was roughly 2 nm^2/cm whether within a die or between dies (Tables III and IV of [79]), although these figures were slightly smaller when the spacings were on the order of a few microns.

3.5 Conclusion

Thermal and process variations alter the wavelength response of silicon photonic devices. These effects can not be known until fabrication, making it costly to design systems. In this chapter,

we study these variation effects towards various photonic devices and reconstruct the first order statistics of the measurement data sets. We statistically analyze the shift in resonant wavelengths of micro-rings and racetracks, and the peak transmission wavelengths of directional couplers. We observe a thermal drift rate in the range of 80 pm/$^{\circ}C$-90 pm/$^{\circ}C$ in the micro-ring and racetrack, which generally agrees with the values in the literature. A thermal drift of around 110 pm/$^{\circ}C$ is found for a 1.063 mm-long directional coupler. Analysis of the variation of the optical responses of the room temperature devices is used to determine the process variation. We find that if we form successive arrays of values of a quantity of interest (peak wavelength of a transfer function) at a single device at some point on the wafer and then increase the size of the array by including values of devices at ever greater distances from the original, the variance of values of the successive arrays increase linearly with the linear extent of the sample. That is, the process variation exhibits a "random walk" pattern with spatial extent. Expressing the process variation in units of variance per length, we find our measured values agree with others in the literature, that is, the process variation are circa 1 nm^2/cm.

Our analysis points in the direction of fabrication/design optimization and this work provides a quantitative base for fabrication-yield-aware design. As photonic fabrication technology evolves, fabrication uniformity improves. We believe quantifying the variations for wavelength-selective devices such as the micro-ring, racetrack and directional coupler at any current technology node is the necessary step towards bridging the gap between photonic device/circuit design and its fabrication.

Chapter 4

Parameter Extraction from Fabricated Silicon Photonic Devices

Silicon photonics has potential as a technology for future interconnection networks [106]. The high index contrast of silicon with its native oxide facilitates miniaturization of photonic devices. The well-developed design and fabrication techniques for the complementary metal-oxide-semiconductor (CMOS) circuits have been widely applied to design and fabrication of silicon photonics [107, 108, 109]. Most of the components necessary for optical communication system have been demonstrated in silicon photonics including waveguides [35], rings [110, 111], couplers [112, 113], modulators [45, 114, 115, 116], switches [117, 118, 119, 120, 121], wavelength division multiplexers (WDM) [122, 123] and integrated photodetectors [124]. The only desirable (but non-essential) component missing is the silicon light source that has been demonstrated but remains hopelessly impractical for system use [125, 126].

A major problem with silicon photonics is the sensitivity of components to process variation [79, 127]. Simulations of components made during the design phase, previous to layout, may agree well qualitatively with the measured characteristics of fabricated devices but still exhibit significant quantitative disagreement. The problem does not lie with the accuracy of simulation tools. Computer intensive tools abound, including beam propagation method (BPM) [128], finite-difference time-domain method (FDTD) [129] and finite element method (FEM) [130]. However, these tools are only as accurate as the data input to them. The most ubiquitous of silicon photonics device performance measurements are the transmission as a function of wavelength (transmission function) measurements. The most salient features of such measurements are sharp spectral features

such as wavelength resonances exhibited as peaks or dips in spectral response. Rules of thumb for spectral sensitivity of such features to variations in device dimension are that 1 nm of silicon waveguide width variation creates about 1 nm resonant wavelength drift and 1 nm of silicon layer thickness variation is responsible for 2 nm resonant wavelength drift [92]. As present day optics spectrum analyzers are generally accurate to 80 pm or less, 0.1 nm dimensional variations will show up on transmission function plots. The nanometric size dimensional variations that lead to the smallest observable experimental variation generally lie at or below the limits of measurement technology. If the inputs to the simulation tools are inaccurate, then the outputs will be inaccurate. The problem is that unmeasurable uncertainties in input result in easily measurable variation in output.

Were it possible to extract all of the dimensions of waveguides, rings and other devices from comparison of simulation and measurement, all of our fabrication problems would be tractable. An easily constructed feedback loop could be used to correct any and all fabrication errors. Such is not the case due to the curse of dimensionality [131, 132, 133]. The waveguide varies not only in width but also in thickness and further, the waveguide's thickness and width are not constant with propagation distance. For a ring, add in the necessity to know the radius of curvature, the details of the region of coupling. Surface roughness compounds all problems. One dimensional measurement data is not sufficient to fully specify a parameter space of a multiplicity of dimensions. However, all of the devices that are in use in silicon photonics depend on the effective index of the structure and the effective index, in turn, depends on all of the dimensions of the structure that the effective index describes. A first step to parameter extraction could well be the determination of the value of effective index of a given device as a function of wavelength, that is, a dispersion curve.

In this chapter, we use a simple analytical models in combination with Comsol simulations to determine the effective index dispersion curves of micro-ring resonators, racetrack resonators and directional couplers over the complete wavelength regime of experimental interest, that is, throughout the S and C bands of the third telecommunications window about 1550 nm. All of these devices are ones of interest in photonic device research [134, 135]. The linearity of the

effective index with wavelength curves that we determine for each of the experimental cases is a first measure of their correctness. That the extracted effective index curves when used in a simple analytical model (here the T-matrix) recovers the experimental data in qualitative detail is the definitive measure of the applicability of the approach.

This chapter is organized as follows: In Section 4.1, we first discuss the effective index of refraction and how it relates to the waveguide parameters. We briefly discuss a description of wavelength dependent transmission. This naturally leads to a discussion of more detailed models for the devices that we are placing attention on in this work, namely, micro-rings, racetracks and directional couplers. We then illustrate the efficacy of using the effective index to describe devices by using the effective index to track the effective of temperature variation on wavelength dependent transmission. In Section 4.2, we present examples where effective indices were extracted from measurement data for micro-rings, racetracks and directional couplers that had been laid out over the surface of actual fabricated wafers.

4.1 Modeling Framework

The focus of this chapter is on determining how two devices of nominally identical design parameters that are measured to have different transfer characteristics do actually differ. We cannot determine all of the device dimensions directly from length measurements to the accuracy necessary to predict wavelength dependent transmission to the accuracy with which we can make those spectral measurements. The effective index of refraction of a device, however, is a representation of a device that will differ when transfer characteristics differ. The transfer matrix, or T-matrix, of a device depends on the effective index of refraction and a few phenomenological parameters that can be fit from measurement. As we will soon see, we can extract a wavelength dependent effective index of refraction from measurement by judicious use of the T-matrix together with more accurate modeling software. Such dispersion curves then do model the devices with the accuracy necessary to differentiate devices of nominally identical fabrication parameters.

In this section, we discuss our approach to determining dispersion relations, that is, the

wavelength dependent effective index, $n_{\text{eff}}(\lambda)$, from wavelength dependent transmission data. We first discuss the effective index of refraction and the factors upon which it depends. We then discuss the T-matrix description of wavelength dependent transmission. Such a simplified S-matrix provides a framework in which experimental data can be described by phenomenological equations. Those phenomenological equations prominently display the effective index in device descriptions and in the equations that describe interconnection of the devices. The dependence of salient features (sharp peaks and troughs of wavelength dependent transfer functions) on the effective index is then discussed for the three devices of interest, the micro-ring and racetrack resonators and the directional coupler. To demonstrate the efficacy of effective index as a descriptive tool, predictions of the variation of effective index with temperature are used in transfer matrices to accurately predict measured transmission results for rings, racetracks and directional couplers.

4.1.1 The Effective Index of Refraction

The phase progression in free space propagation of monochromatic electromagnetic fields is governed by the free space propagation constant $k_0 = \frac{2\pi}{\lambda}$ where λ is the wavelength, related to the frequency, f, by the speed of light in vacuum, c, through $\lambda = \mathrm{c}f$. Propagation of a monochromatic electromagnetic waves in a homogeneous, isotropic material with an index of refraction $n(\lambda)$ is also characterized by λ and f of the monochromatic wave but where the proportionality is through the phase velocity of propagation in the medium, $v_{ph} = \frac{\mathrm{c}}{n(\lambda)}$. Unidirectional guided wave propagation of waves is characterized by an eigenvalue equation for the propagation constant, β, of a wave that is characterized by the effective index of the medium as defined by $n_{\text{eff}}(\lambda) = \beta/k_0$.

A usual method of experimentally characterizing a silicon photonic (or other) optical device, is by measuring the optical transmission of the device as a function of wavelength. This measured transmission function generally contains salient wavelength features such as sharp peaks or dips in the transmission as a function of wavelength. A selected peak or dip may then be associated with a selected wavelength that we denote by λ_{sel}. Clearly, the value of the selected feature is a function of the waveguides and coupling structures that make up the guided wave structure of

the silicon photonic device. These waveguides and coupling structures are defined by the effective indices of refraction. In the simple devices that we consider here, the ring, the racetrack and the directional coupler, we can say that the propagation is dependent on a composite effective index of the structure and the ways that the bends and coupling regions modify that effective index as a function of position within the structure of interest. One can then generally write that

$$\lambda_{\text{sel}} = f(n_{\text{eff}}), \tag{4.1}$$

that is, the specific location of the selected feature in wavelength space is dependent on detailed structure of the silicon photonic device.

The effective index of a device is influenced and determined by a multitude of factors. Any structural variation causes change in the effective index. The uniformity of the silicon layer on silicon-on-insulator (SOI) wafer [136], plasma dry etching pattern uniformity across wafer [92, 137], optical lithography and photoresist development uniformity [92] all will effect the physical dimensions of a device. As far as functional dependence is concerned, though, the primary dependence of the effective index as a function of wavelength is on width, height, bending radius and coupling gap as expressed by

$$n_{\text{eff}}(\lambda) = f(w, t, R_c, g, \lambda; T), \tag{4.2}$$

where w is the channel width, t is the thickness of the silicon layer, R_c is the radius of curvature of any waveguide bend and g is the width of any coupling gap. The temperature, T, dependence has been factored out as the effect of temperature is independent of the other effects, that is, a drift in temperature will result in a drift in effective index that is essentially independent of the values of the other parameters affecting effective index [81, 87]. We will demonstrate the fact in an upcoming section where we will also verify that temperature variation causes shift of 90 pm/°C - 110 pm/°C [81, 83, 138] in the wavelength dependent features in a typical ring resonator. Temperature

variation of as much as ±15°C can occur in usual operation of CMOS [98]. That is to say thermal variation per degree C is roughly equivalent to a change of 0.1 nm in a channel width. A 10°C change in temperature is equivalent to a 1 nm change in dimension of a characteristic width. The difference between temperature and dimension is that the change in temperature will always have the same effect whereas the width, height, bending radius and coupling inextricably intertwined.

4.1.2 Wavelength Dependent Transmission

The T-matrix [139, 140, 141, 142, 143] is a method to characterize the wavelength dependent transmission of a single or multi-port photonic device when the reflections from the device ports can be safely ignored. Otherwise a full S-matrix would be required [144, 145, 146]. For the wavelength selective devices such as micro-rings, racetracks and directional couplers, T-matrix can be expressed in the generic form

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} r & -it \\ -it & r \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix}, \tag{4.3}$$

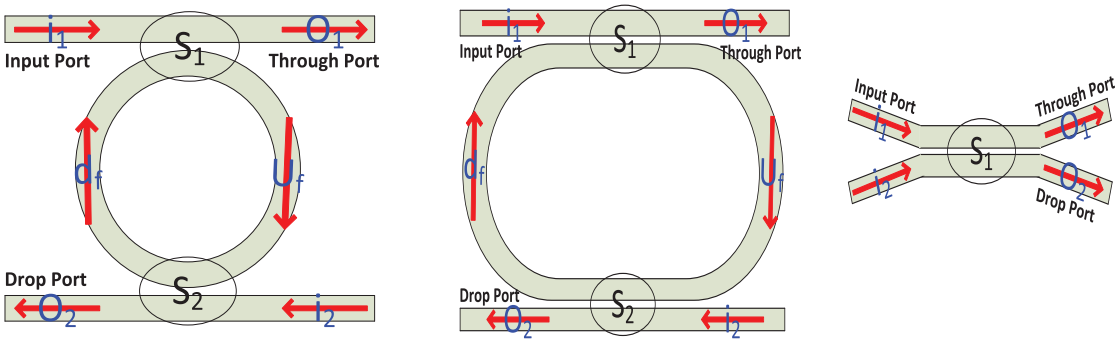
where **a** and **b** are the vectors of the input and output mode amplitudes. The squared magnitudes of the components of **a** and **b** vectors are the modal powers and the t and r are the transfer coupling coefficients. If the device is lossless, then the associated T-matrix is unitary and unimodular [140] and therefore $|t|^2 + |r|^2 = 1$. This is never precisely the case although often the differential loss between ports is small and one can approximate propagation through devices as having a common loss factor of $\exp(-\Gamma)$ where Γ is an overall loss factor.

Propagation through a system can be represented by multiplication of the individual T-matrices of the components and waveguides comprising the system. That is, one can always obtain an overall n x m T-matrix for any system with m inputs and n outputs from multiplying the matrices of individual components comprising the system. We saw above the generic form of the matrix for rings, racetracks and directional couplers. A waveguide is characterized by a scalar T-matrix that relates the scalar a (input) and b (output) for a single mode waveguide by

$$b = \exp\left[-\alpha L + i \cdot 2\pi n_{\text{eff}} L/\lambda\right] a, \tag{4.4}$$

where α is the loss factor and L is the effective propagation length. It is usual that rings, racetracks and directional couplers are comprised of waveguides of the same nominal characteristics of the connecting waveguides and therefore that the waveguide and component would share an $n_{\text{eff}}(\lambda)$ to begin with. The component, though, will generally consist of combination of straight and curved sections sections as well as coupler coupled as illustrated in Figure 4.1.

4.1.3 Models for Wavelength-Selective Devices



(a) Micro-ring resonator (b) Racetrack resonator (c) Directional Coupler

Figure 4.1: Schematic depictions of the devices of interests. S_1 and S_2 are the coupling regions, i_1 and i_2 are the input ports and o_1 and o_2 are the output ports in the devices.

The devices we are considering appear schematically in Figure 4.1. The plots were introduced in Section 2.4.2 and Section 2.4.3. They are reiterated in this section for convenience. The micro-ring and racetrack resonators are resonant devices. Resonant wavelengths separated by (almost) regular wavelength intervals are the most salient of features on the wavelength dependent transmission curves for these devices. One says that each pair of adjacent resonant wavelengths is separated by a **free spectral range** (FSR). The resonant wavelengths are determined by the condition that the phase, $\Phi(\lambda)$, in propagating one complete cycle inside of the device satisfies $\Phi = 2m\pi$ where m is an integer. The separation between the $(\text{m+1})^{st}$ and m^{th} resonances is the

m^{th} free spectral range (FSR). The FSR is generally given with dimensions of frequency. Here we will use primarily wavelength ranges where the simple relation $d\lambda = -\frac{cdf}{f^2}$ can be used to convert. For the micro-ring, the m-relation can be expressed in the form

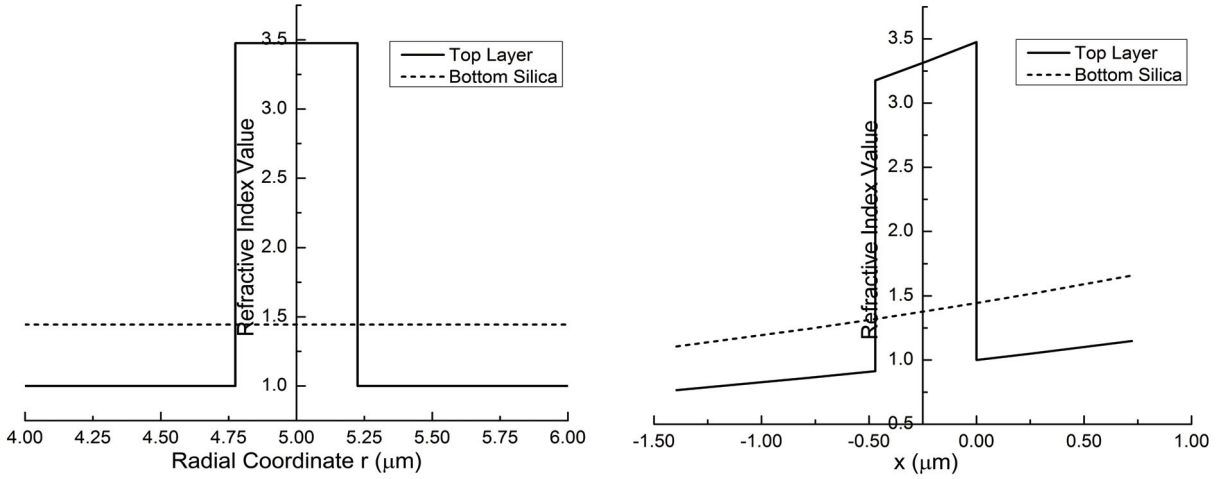
$$m\lambda_{\text{sel}} = L_c n^{\text{c}}_{\text{eff}}(\lambda_{\text{sel}}) \tag{4.5}$$

whereas for the racetrack, the m-relation is

$$m\lambda_{\text{sel}} = L_c n^{c}_{\text{eff}}(\lambda_{\text{sel}}) + L n^{s}_{\text{eff}}(\lambda_{\text{sel}}) \tag{4.6}$$

where the L_c is the length of the curved path, L the length of the straight path, $n^{c}_{\text{eff}}(\lambda_{\text{sel}})$ and $n^{s}_{\text{eff}}(\lambda_{\text{sel}})$ are the effective indices in the curved and straight regions. The effective index of a waveguide flowing a circular path can be approximated from a two-dimensional conformal mapping [147, 148]. The correction is significant as will be discussed in the next section and is seen for the specific case of a racetrack in Figure 4.9. Conformal mapping technique is an accurate and straightforward method to take into account of the bending radius effects in structure, where curved waveguide with constant radius is transformed into an equivalent straight waveguide with modified waveguide width and exponentially redistributed refractive index. Conformal mapping technique naturally takes bending loss into consideration. Figure 4.2 illustrates the idea of conformal mapping by showing the transformation of a 5 μm-radius silicon waveguide circle with 450 nm width into its equivalent straight waveguide. The effective index of the waveguide circle can be obtained by simulating the equivalent structure in the numerical mode solver.

The directional coupler has different principle of operation. The coupling region has two modes that we will refer to as an even and an odd mode. The transmission as a function of wavelength of a given port will show a sharp feature whenever the accumulated phase difference $\Delta\Phi = m\pi$. Although the terminology is not commonly in use, we will call the distance between the $(\text{m}+1)^{st}$ and m^{th} depressions as the free spectral range (FSR). The m-relation here can be expressed as



(a) Refractive index values showing in the radial coordinates of the bend.

(b) Conformal mapping transformed refractive index values in the estimated straight waveguide.

Figure 4.2: Cross-sectional distribution of the refractive index in the bending structure before and after using conformal mapping technique. The bending radius is 5 μm and the width of the waveguide is 450 nm. Top layers consist of air and silicon. Bottom layer is silica.

$$m\lambda_{\text{sel}} = 2L(n^{e}_{\text{eff}}(\lambda_{\text{sel}}) - n^{o}_{\text{eff}}(\lambda_{\text{sel}})) \tag{4.7}$$

where L is the length of the coupling region and n^{e}_{eff} and n^{o}_{eff} are the effective indices for the even and odd modes in the structure. Each selected wavelength has a unique effective index value $n_{\text{eff}}(\lambda_{\text{sel}})$. A part of the complexity of finding the correct effective index from the measured curve is finding the correct m value. We will use a full wave mode solver (specifically in our case, Comsol) in order to determine mode indices over the complete space of possible parameter variations to determine the m-value. This will be discussed at length in the next sections.

4.1.4 Sample Preparation

All devices used in our study were fabricated at ePIXfab [41] during the period 2009-2012. ePIXfab offers a standard CMOS-compatible photonic foundry process where the 8-inch SOI wafer (Soitech) is adopted as the standard substrate. Much more discussion of the wafers and measurements is given in Section 2.2 and Section 2.3.

4.1.5 Tracking Thermal Variations with Effective Index

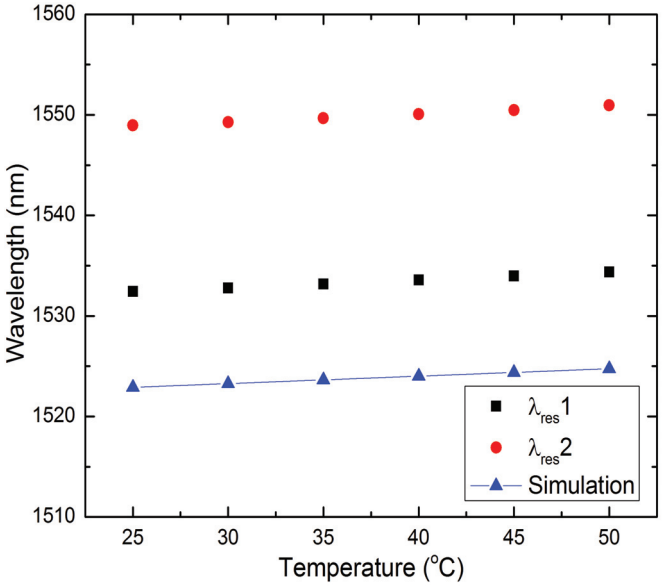


Figure 4.3: Thermal variation measurement and numerical modeling results of the micro-ring described in Figure 4.1(a). The temperature range is 25°C - 50°C. $\lambda_{res}1$ and $\lambda_{res}2$ are the measured resonant wavelengths. The measured thermal drift rate of 78.5 pm/°C closely agrees with the simulation result of 74.2 pm/°C.

We performed a set of thermal drift measurements on a set of selected devices in order to demonstrate the independence of thermal variation from process variations. For the calculations of this section, we use fabrication values to determine room temperature effective index value and then the temperature variation of the waveguide layer to track the effective index as a function of temperature. We will find that we can track the effective index but cannot a priori calculate the initial value of the effective index.

The thermal-optical coefficient of silicon can be expressed as $\sim 1.86 \times 10^{-4} (K^{-1})$ [85, 98]. This bulk index variation does not apply especially well to SOI layers. An experimentally verified model for the variation of index of an SOI structure is given by [149] as

$$\frac{\partial n}{\partial T} = A + BT + CT^2, \tag{4.8}$$

where A = 9.48 × 10^{-5}, B = 3.47 × 10^{-7}, and C = -1.49 × 10^{-10}. The dimensions of the

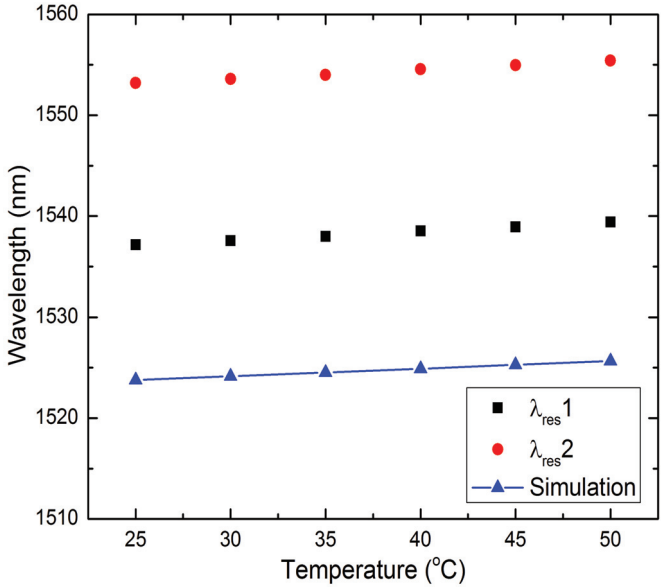


Figure 4.4: Thermal variation measurement and numerical modeling results of the racetrack described in Figure 4.1(b). The temperature range is 25°C - 50°C. $\lambda_{res}1$ and $\lambda_{res}2$ are the measured resonant wavelengths. The measured thermal drift rate is 89.7 pm/°C whereas the simulation result shows a drift rate of 75.2 pm/°C.

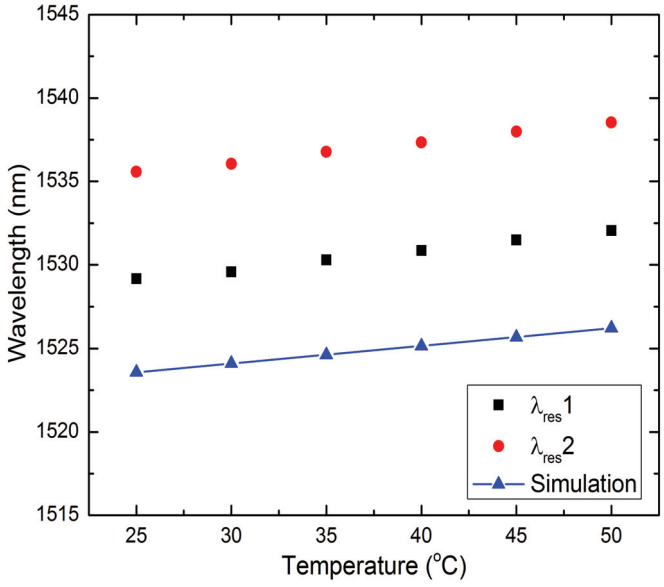


Figure 4.5: Thermal variation measurement and numerical modeling results of the directional coupler described in Figure 4.1(c). The temperature range is 25°C - 50°C. $\lambda_{res}1$ and $\lambda_{res}2$ are the measured resonant wavelengths. The measured thermal drift rate is 116.4 pm/°C and the numerical simulation shows a drift rate of about 105.8 pm/°C.

expression are per °C. We used this relation in the mode solver Comsol in order to generate a

thermally affected effective index curve. We carried out measurements in the temperature range of 25°C - 50°C. This temperature range is within the realistic temperature fluctuation range for the on-chip environment [98]. We then compared the calculated and measured values. The variation of resonant wavelength as a function of temperature and the fits to these curves bases on the effective index curves calculated with Equation 4.8 are given in Figures 4.3 - 4.5.

Figure 4.3 shows the comparison of the thermal variation drift results on this micro-ring structure in the range of 25°C - 50°C between measurement and Comsol simulation modeling. The measured drift rate is 78.5 pm/°C, whereas the simulation gives a thermal drift rate of 74.2 pm/°C. The comparison reveals that our numerical device model in Comsol is accurate and the slight difference in drift rates is within the accuracy of our measurement setup. In the same temperature range, we obtain a thermal resonance wavelength drift of about 89.7 pm/°C for the racetrack resonator. Figure 4.4 displays the results on thermal variation measurement and its corresponding numerical simulation results. The numerical simulation indicates a drift rate of 75.2 pm/°C for the same structure. The mismatch in drift rates is within 0.16°C in terms of temperature measurement error. This discrepancy is probably caused by our temperature controllers 0.1°C accuracy. Considering the measurement error, our calibration method is considered accurate for modeling the racetrack. Figure 4.5 plots both measurement data and simulation results on the thermal variation for the directional coupler in the same 25°C - 50°C as the micro-ring and racetrack. As shown in the figure, we obtain a thermal drift of 116.4 pm/°C in measurement, whereas the simulation reveals a drift rate of 105.8 pm/°C. The discrepancy between the two results are about 0.09°C in terms of temperature measurement error. Within the measurement accuracy of the temperature controller, this comparison demonstrates our numerical model is credible in the directional coupler case.

4.2 Extracting Effective Index from Experimental Data

In this section we describe the extraction of effective index dispersion curves from experimental data for the micro-rings, racetracks and directional couplers. The experimental data was taken

on a significant number of devices laid out and fabricated on wafers fabricated in the ePIXfab [41] shuttle process at the IMEC [39] and LETI [40] facilities. More discussion of the wafers is given in Chapter 3. A full wave mode solver (Comsol) is used to generate effective index values over the complete range of parameter variation that the foundry deems possible from post fabrication run measurements. A phenomenological model (T-matrix) is used to select a set of simulated values that may correspond to the measured wavelength dependent transmission. The effective index dispersion curve is then determined by fitting the remaining parameter, the coupling of the ring to input and output (actually a single parameter when conservation of power flow). The extracted effective index is linear in wavelength over the limited range of wavelengths considered (as it effective index should be far enough from material resonances and mode cutoffs) and the fits to the experimental curves are quite accurate.

4.2.1 Micro-ring

A micro-ring resonator is a four-port device as shown in Figure 4.1(a). In a more complete model than the generic form of Equation 4.3, the resonator is modeled as a Fabry-Perot etalon [150]. A more refined T-matrix than that of Equation 4.3 is given by

$$\begin{pmatrix} b_1 \\ d_f \end{pmatrix} = \begin{pmatrix} r_1 & -it_1 \\ -it_1 & r_1 \end{pmatrix} \begin{pmatrix} a_1 \\ e^{i\Phi/2}e^{-\alpha l/2}u_f \end{pmatrix}, \tag{4.9}$$

$$\begin{pmatrix} u_f \\ b_2 \end{pmatrix} = \begin{pmatrix} r_2 & -it_2 \\ -it_2 & r_2 \end{pmatrix} \begin{pmatrix} e^{i\Phi/2}e^{-\alpha l/2}d_f \\ a_2 \end{pmatrix}, \tag{4.10}$$

where a_1 and a_2 are the input ports, b_1 and b_2 are the output ports, d_f is the downward stream in the ring, and u_f is the upward stream in the ring as shown in the plot. r_1 and t_1 are the coupling coefficients from the input stream into the ring, with t_1 being the coupling amplitude. r_2 and t_2 are the coupling coefficients from the ring to output stream. α is the loss per unit length in the ring resonator. $\alpha = 1/(Q * L)$ where Q factor is measured by λ_{res}/FWHM from experiment data. L is the propagation distance. Φ is the phase progression of one round trip in the ring, which can

be expressed as $\Phi = 2\pi n_{\text{eff}} \times L/\lambda$, where n_{eff} is the effective index and λ is the wavelength in free space.

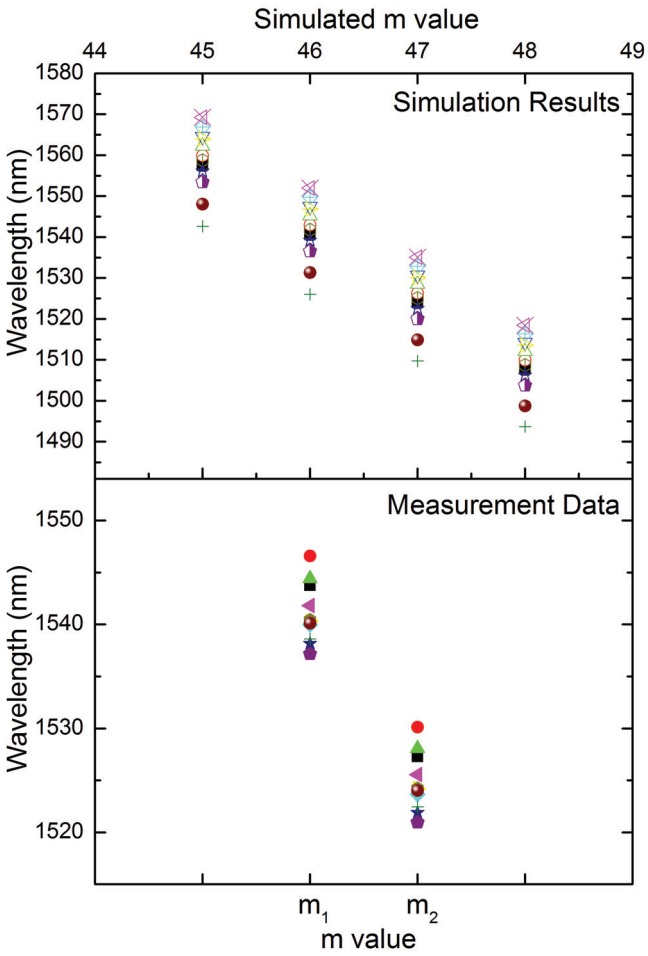


Figure 4.6: Illustration of the process to find the mode number m from the measured resonant wavelengths and simulation. The simulations are carried out using foundry wafer-scale variation data as appears in the upper panel whereas the lower panel is the measurement data. Comparing the plots, we determine $m_1 = 46$ and $m_2 = 47$.

The foundry generally supplies the user with values of the relevant range over which the width and thickness varied during the fabrication run. We can use these values to generate a set of wavelength signatures using a full wave mode solver such as Comsol if we know the index of the silicon and silicon dioxide throughout the wavelength region of interest. The wavelength dependent approximations we have used are given by [102]

$$n_{\mathrm{Si}}(\lambda) = 3.4277 + \frac{0.1104}{\lambda^2} + \frac{0.041}{\lambda^4}, \tag{4.11}$$

$$n_{\mathrm{SiO_2}}(\lambda) = 1.4213 + \frac{0.0856}{\lambda^2} - \frac{0.0735}{\lambda^4}, \tag{4.12}$$

We obtain the fabrication variation information from the IMEC [92]. We implement the variation data into a micro-ring of our design. The nominal design of this micro-ring has a waveguide width of 450 nm, a coupling gap of 200 nm and a radius of 4.975 μm. We carry out a series of simulations to study the resonant wavelength drift under fabrication variation. As shown in the top plot of Figure 4.6, we can see that the resonant wavelength values cluster together for different mode numbers. The clustering results from the total variation of fabrication parameters being sufficiently small compared to an FSR. Calculating the effective index value as given in Equation 4.5 requires that we know the m-value of the mode. The clustering allows us to determine the m-value by the following logic. In the bottom plot of Figure 4.6 is the wafer-scale measurement data of two resonant wavelength group of the same micro-ring on different dies. By comparing the clustered resonant wavelength signatures, it is clear in this case that the m-values are 46 and 47 for the corresponding resonant wavelengths of the device.

Knowing the m-value, we can find n_{eff} from the relation

$$m\lambda_{\mathrm{res}} = 2\pi \left(R + \frac{w}{2}\right) n_{\mathrm{eff}}^{\mathrm{c}}, \tag{4.13}$$

where R is the radius defined from the center of the ring to the center of the ring waveguide and w is the width of the ring waveguide. R+w/2 is the outer radius of the micro-ring. We adopt the outer radius in this equation is that the mode profile shifts away from the center of the waveguide to the outer edge due to tight bending [102, 151]. It results in the dispersion curve of Figure 4.7. Similar methodology is applied to the racetrack and directional coupler and the results will be discussed further in the next two sections.

In order to test the effective index results against experiment, we need to find the goodness of fit of the effective index of Figure 4.7 to the experimental data of Figure 4.8. To carry this

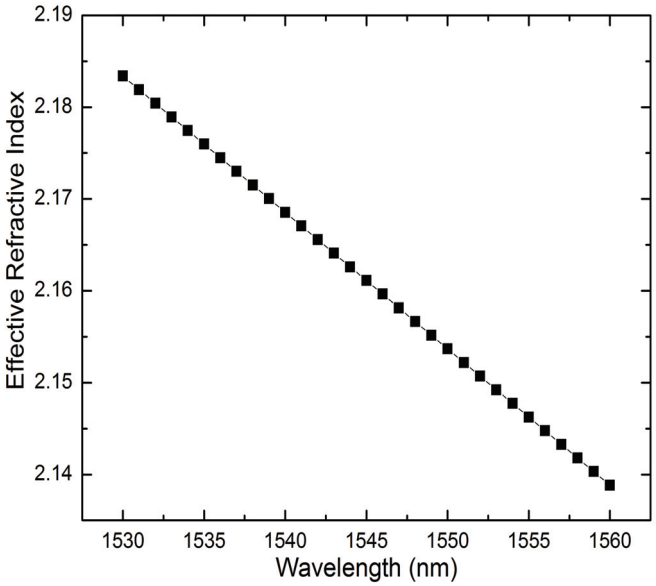


Figure 4.7: Effective index dispersion curves extracted from measured data for a micro-ring (450 nm waveguide width, coupling gap 200 nm, radius of 4.975 μm) as sketched in Figure 4.1(a).

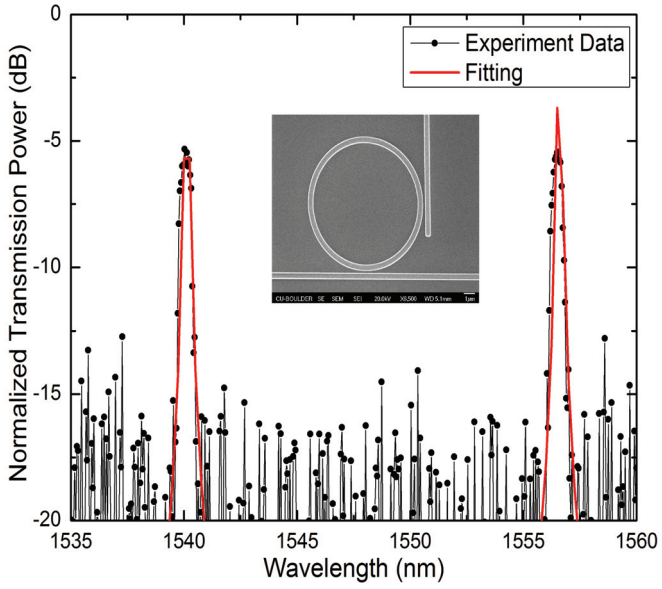


Figure 4.8: Optical transmission measurement of a micro-ring and its corresponding numerical model fitting. The inset shows the scanning electron microscope (SEM) image of the fabricated structure. The radius of the micro-ring is 4.975 μm. Its waveguide width is 450 nm and the gap width is 200 nm.

out we still need values for the other free parameters of Equations 4.9 and 4.10. The α can be determined from the measured Q. Power flow conservation (matrix unitarity) requires that the r

and t of Equation 4.3 satisfy $|r|^2 + |t|^2 = 1$. A fit with $|r|^2 = 0.29$ gives the result that appears in Figure 4.8. The fit is quite good.

4.2.2 Racetrack Resonator

A racetrack resonator consists two parts as shown in Figure 4.1(b), where the coupling region comprises of straight waveguides and the curved structure which is similar to that of the micro-ring. The length of the straight waveguide controls the coupling. A racetrack resonator can the be modeled as micro-ring resonator with improved coupling coefficient. The T-matrix is shown in Equations 4.9 and 4.10.

We calibrate the effective index dispersion curve for the racetrack model following the same steps described in Section 4.2.1. We first analyze the wafer-scale variation data for the racetrack of our interest, then obtain the fitted effective index dispersion curves using our proposed analysis technique. The racetrack has a bending radius of 3 μm and a straight coupling region of 7 μm. The coupling gap is 130 nm on both input and output sides of the structure. Its waveguide width is 450 nm. A single effective index dispersion curve can describe micro-ring in its circular waveguide. However, racetrack contains straight waveguide coupling regions and curved waveguide regions. The effective index dispersion in the straight waveguide is different from that of the curved waveguide region in the structure. The mode solver is coded differently and computes for resonance modes that obey Equation 4.6 which is expressed as:

$$m\lambda_{\text{res}} = 2\pi \left(R + \frac{w}{2}\right) n^c_{\text{eff}} + 2L n^s_{\text{eff}}, \tag{4.14}$$

where R is the radius defined from the center of the ring to the center of the ring waveguide. w is the width of the ring waveguide. L is the length of the straight coupling region. Figure 4.9 depicts the fitted n^c_{eff} and n^s_{eff} dispersion curves.

Figure 4.10 contains an inset SEM image of the fabricated racetrack resonator. We calibrate the racetrack T-Matrix model using the same steps described in Section 4.2.1. The two effective

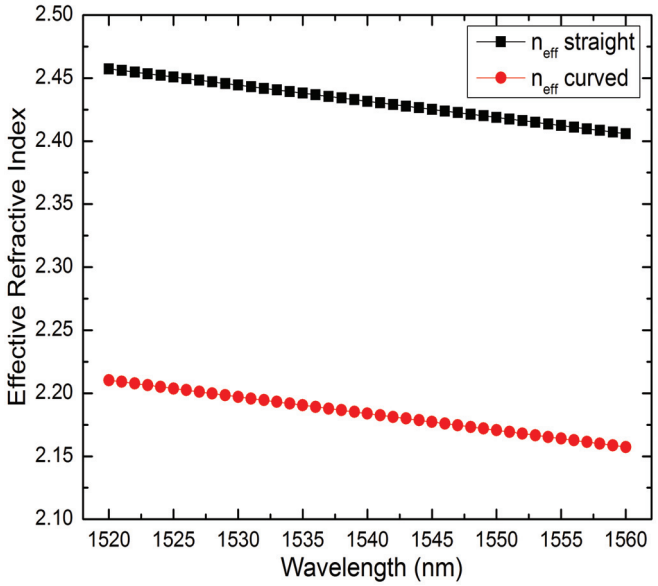


Figure 4.9: Effective index dispersion curves for the straight region (n^s_{eff}) and the curved region (n^c_{eff}) extracted from measured data for a racetrack (450 nm waveguide width, coupling gap 130 nm for 7 μm, bending radius of 3 μm) as sketched in Figure 4.1(b).

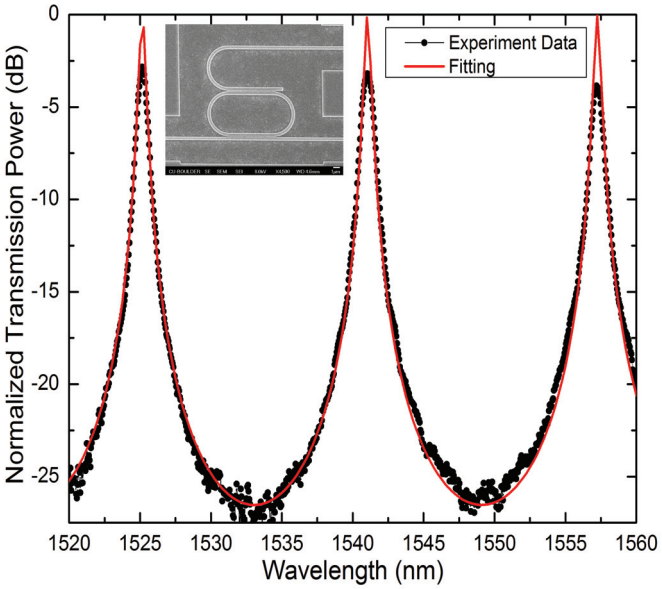


Figure 4.10: Optical measurement of a racetrack and its corresponding numerical model fitting. The SEM image shows the fabricated structure. Its bending radius is 3 μm and coupling length is 7 μm, with a coupling gap of 130 nm. The waveguide width is 450 nm.

index dispersion curves in Figure 4.9, together with $t^2 = 0.09$, $r^2 = 0.91$, are applied into its T-matrix model Equations 4.9 and 4.10 for fitting the optical response of the device with experiment

data. Figure 4.10 shows that the numerical fitting is well overlapping on top of the measurement optical data. The racetrack T-matrix is well calibrated after these steps and we are able to obtain accurate fittings as shown in the figure. In this calibrated racetrack T-matrix model, the coupling transmission coefficient t = 0.3. Comparing with the micro-ring's 0.17 of the transmission coefficient t, it is obvious that the coupling of racetrack is enhanced by implementing a straight waveguide coupling section in the device.

4.2.3 Directional Coupler

Directional coupler may also find use in integrated optical interconnects. A directional coupler consists of two separated waveguides that are brought together and run in parallel with a fixed gap in between for a distance of coupling length. The two arms of the directional coupler appear in Figure 4.1(c). Two modes (even and odd) propagate in the structure. The beating of the modes leads to the mode transfer behavior of the individual modes [152].

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} r & -it \\ -it^* & r^* \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{4.15}$$

where b_1 and b_2 are the outputs. a_1 and a_2 are the inputs. r is the **reflected** energy coefficient and t is the **transmitted** energy coefficient. r^* and t^* are the complex conjugates. The coefficients r and t of master equation Equation 4.3 are defined as [153]:

$$r = \cos(Z\sqrt{\kappa^2 + \delta^2}) + i\frac{\delta}{\sqrt{\kappa^2 + \delta^2}}\sin(Z\sqrt{\kappa^2 + \delta^2}), \tag{4.16}$$

$$t = \frac{\kappa}{\sqrt{\kappa^2 + \delta^2}}\sin(Z\sqrt{\kappa^2 + \delta^2}), \tag{4.17}$$

where Z is the coupling length and κ is the coupling coefficient. $\delta = \triangle\beta/2$ where $\triangle\beta$ is the difference between the propagation constants of the even and odd modes of each input wavelength in the coupling region.

The directional coupler of our design has a coupling length is 1063 μm with a coupling gap of 130 nm. The waveguide width of both coupling arms is 450 nm. We follow the same steps in Section 4.2.1. The mode solver looks for modes that obey Equation 4.7. We fit the difference between the effective index values of the even and odd modes $\triangle n_{\text{eff}}^{e-o}$ by comparing simulation results of resonance wavelength with experiment data. Figure 4.11 shows the dispersion curve of $\triangle n_{\text{eff}}^{e-o}$ for this directional coupler.

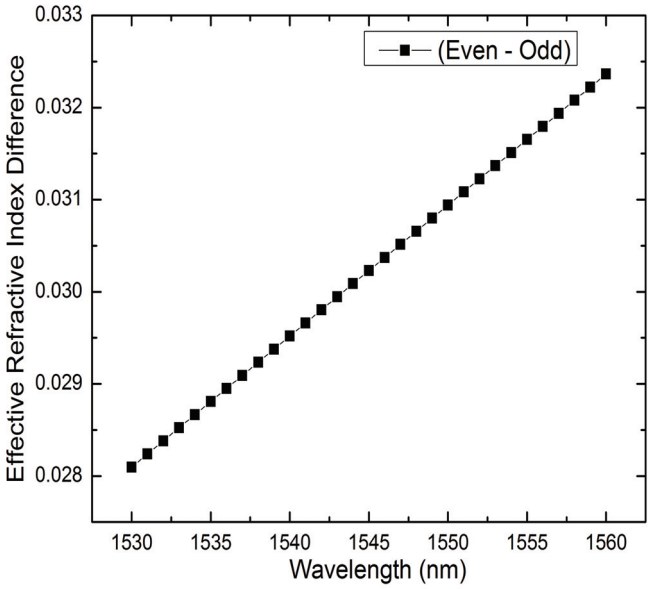


Figure 4.11: Effective index dispersion curves for $n_{\text{eff}}^{e} - n_{\text{eff}}^{o}$ extracted from measured data for a direction coupler (450 nm waveguide width, 130 nm coupling gap and 1063 μm coupling length) as sketched in Figure 4.1(c).

The inset of Figure 4.12 shows an SEM image of the device. This device is too long to be captured in one SEM image with enough resolution. This zoomed-in image displays a partial section of the device. We found that the relation between coupling length and physical straight waveguide length of coupling region L is Z = aL where a is the length factor. For instance, for this specific directional coupler, we used the coupling coefficient $\kappa = 8.842\times10^{-5}$ and the length factor a = 3.375 to achieve the fit in Figure 4.12.

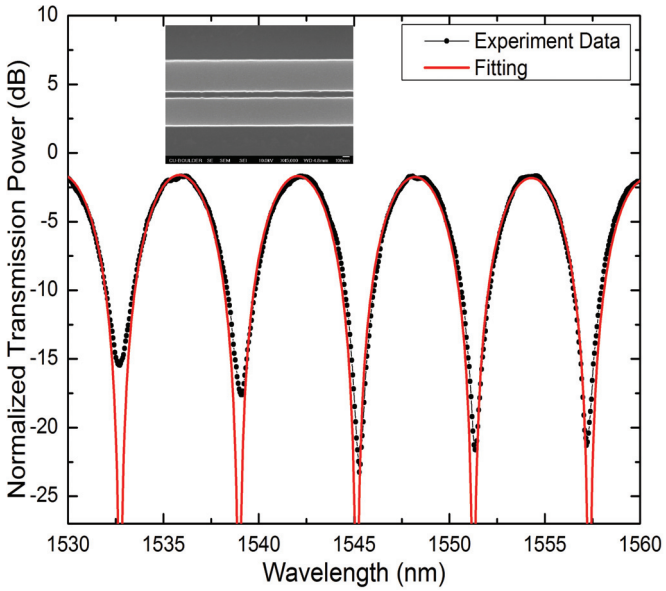


Figure 4.12: Optical measurement of a directional coupler and its corresponding numerical model fitting. The SEM image shows a part of the coupling region of the fabricated structure. Its coupling length is 1063 μm with a coupling gap of 130 nm. The waveguide width is 450 nm.

4.3 Conclusion

Process variation is always present in fabrication. SOI devices are no exception. At present our optical needs for SOI greatly exceed our ability to make physical measurements at the nanoscale. That is, dimensional changes below our measurement accuracy measurably affect wavelength dependent optical transmission. In this chapter, we demonstrate that effective index dispersion curves display sufficient sensitivity to differentiate between nominally identical designs that exhibit measurable differences in optical transmission. The dispersion of the effective index of a device then forms a bridge between dimensional and optical measurement. We further demonstrate how the dispersion of the effective index can be extracted from measurement data using a combination of full wave analysis and phenomenological models. Our methodology is used to obtain effective index curves for micro-rings, racetracks, and directional couplers. The effective index curves can be used to place limits on the magnitude of process variation.

Chapter 5

Variation-Aware On-chip Interconnect

5.1 Introduction

As Moore's Law approaches the physical limitation, on-chip high power density, high wire latency and transmission bandwidth constraints gradually become serious bottlenecks for single-core processor development. The on-chip multi-core architecture provides a new way for boosting processor performance. However, as core number increases, challenge lies in the interconnect communications among cores inside the processor. Electrical interconnect may still be able to handle 64-core architecture [10]. Beyond that, the bus-based electrical interconnect on-chip networks will quickly be saturated with an increase in the number of cores and become impractical [154]. Study shows that silicon photonic interconnect could offer orders of magnitude improvement over electrical interconnect [77].

Silicon photonic technology brings promise to the on-chip interconnect but its fabrication is not yet mature. Silicon photnic devices are prone to variation effects. In Chapter 3 and Chapter 4, we discussed the process and thermal variations in silicon photonic devices. The process variation in various devices exhibits a "random walk" pattern with a variance of around 1 nm^2/cm across wafer. The thermal variation has a drift rate of circa 0.1 nm/°C. For a realistic on-chip environment, the temperature fluctuation is in the range of ±15°C [98]. Wavelength channel of fabricated silicon photonic devices can drift as much as 2 nm under these influences. Due to limitations on the current fabrication technology and silicon material's large intrinsic thermal optical effect, these variation effects cannot be easily eliminated and could be problematic for high-performance

multi-core systems. For instance, high-throughput on-chip systems requires that communication channels are aligned on both sides of transmitter and receiver. Wavelength drifts in silicon photonic interconnect caused by on-chip fabrication or/and thermal fluctuation would create misalignment in each passband or cross-talk induced by channel overlapping. It would decrease the overall system signal-to-noise ratio and degrade throughput and effectiveness of the communication network [90].

Therefore, addressing the wavelength drift problem in silicon photonic devices in the multi-core system interconnect is the key towards the future development and success of the silicon photonic technology. In this section, we discuss one solution for interconnecting 2^n (n being an integer) cores of a multi-core processor using only photonic broadcast topology. The advantage of this solution is by removing circuit-switching layer in the electronics layer, data path is simplified and latency could be greatly reduced. The latency-critical global coordination message and the non-latency-critical data can be transmitted simultaneously in the broadcast layer. We propose a variation-aware interconnect design that is adapted to the on-chip variation effects without losing transmission information. Without trying to eliminate fabrication imperfection, we show that our design of silicon photonic on-chip interconnect can be realized with today's fabrication technology.

5.2 The Design

In Section 1.5.1, we introduced our silicon photonic broadcast optical interconnect architecture. Here, we incorporate the variation-aware design into this architecture. The structure comprises of a 3D silicon photonics and CMOS electronics hybrid integration design. In this structure, its top layer contains broadband any-one-to-all circular antenna array (Figure 2.19) and silicon photonic devices as the broadcasting and interconnect layer. Its bottom layer consists of CMOS processor cores and electronics. Our focus is the top silicon photonic layer. We use a 4-core processor as an example in this section. The on-chip process and thermal variations in silicon photonic devices issues are addressed locally at the individual optical node.

Figure 5.1 illustrates our idea. In this schematic plot, a 4-core processor unit contains an electronics layer and an optical broadcast layer. The electronics layer where the 4 cores are located

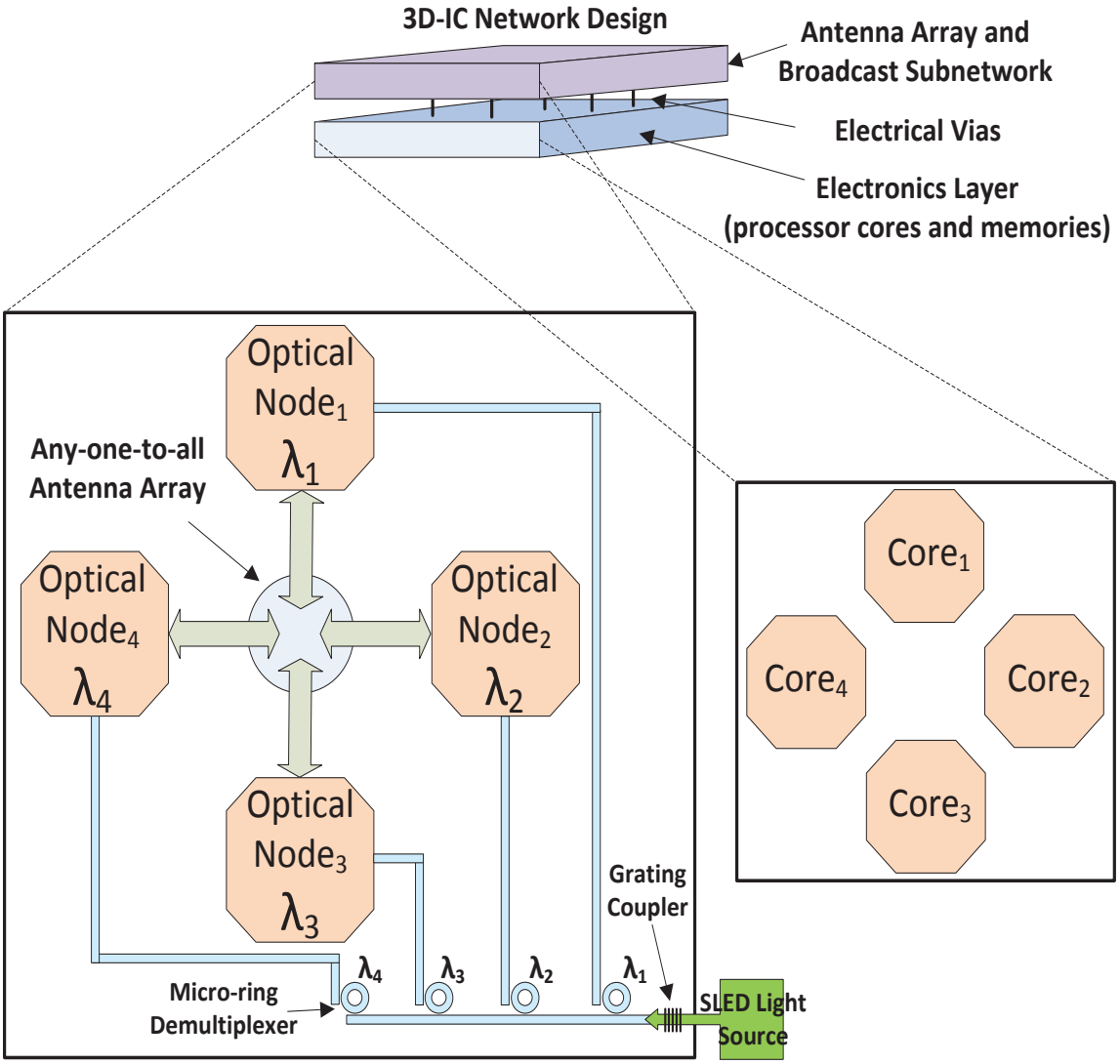


Figure 5.1: A schematic plot of an optical interconnect topology with 4 nodes designed for a 4-core processor. The electronics layer where the 4 cores are located is connected with the broadcast subnetwork using conventional electrical vias. In the plot, core_n is connected to optical node_n (n = 1, 2, 3, 4). In the broadcast layer, each optical node is assigned with a single wavelength communication channel (λ_1 - λ_4) that is provided by demultiplexing a off-chip SLED light source using micro-ring array. Each of the 4 optical nodes communicates to the rest of nodes via any-one-to-all optical antenna array by WDM technology. The optical signal from other nodes are received, converted locally and sent back to the bottom electronics layer.

is connected to the top broadcast layer by conventional electrical vias. The optical nodes in the broadcast layer are interconnected via a any-one-to-all optical antenna array. The performance of this kind of antenna array is discussed in detail in Section 2.4.4. Each optical node is assigned

with a single wavelength communication channel. We use silicon micro-ring resonator to create WDM channels. It is a versatile wavelength filtering device [134, 155, 156]. Meanwhile, micro-ring has small food print and can be operated at high speed [64]. The broadband spectrum of a off-chip superluminescent light emitting diode (SLED) light source is demultiplexed by a micro-ring array to provide these communication channels. The SLED proves to be a cost-effective and reliable light source solution and provides wide wavelength bandwidth that can be sliced into many WDM channels for different optical nodes on the chip. A hypothetical SLED wavelength spectrum is illustrated in the top plot of Figure 5.3. In this example, 4 micro-rings are designed to produce 4 WDM channels λ_1 - λ_4 for the 4 optical nodes. Their channel bandwidth is 1 nm in this design. The on-chip process variation exists in fabrication. For the micro-ring design, the wafer-scale variance is $\sim$1.3 nm^2/cm. These 4 micro-rings are placed adjacent to each other, therefore a channel spacing of 2 nm would be adequate to cover the on-chip process variation and safely protects the WDM channels from overlapping induced by the variation. The middle plot of Figure 5.3 depicts such idea. 4 wavelength channels for the 4 cores are produced by filtering the SLED source input and individually marked as λ_1 - λ_4 in the plot. By using wavelength division multiplexing (WDM) technology, each of the 4 optical nodes exchanges information with the rest of nodes via the antenna array. In one node, the optical signals from other nodes are received and converted by on-chip photodetectors and sent to the bottom layer of CMOS electonic circuity.

Figure 5.2 shows the variation-aware design in a single optical node. A laserless design is implemented for the silicon photonic communication layer at the optical node level. The optical node contains a transmitter section and a receiver section. In the transmitter section, an input waveguide delivers the demultiplexed SLED light signals to an elecro-optic (EO) modulator. The modulator is implemented in each WDM channel for converting electrical stream into optical modulation stream. Various high speed devices have been demonstrated to realize the on-chip EO modulation functionality, including silicon-organic hybrid Mach-Zehnder interferometric (MZI) modulator [45, 116, 157, 158] and doped silicon PN junction modulator [62, 159, 160]. The modulated optical signal is then sent to the any-one-to-all antenna array via a 2 $\times$ 1 multimode

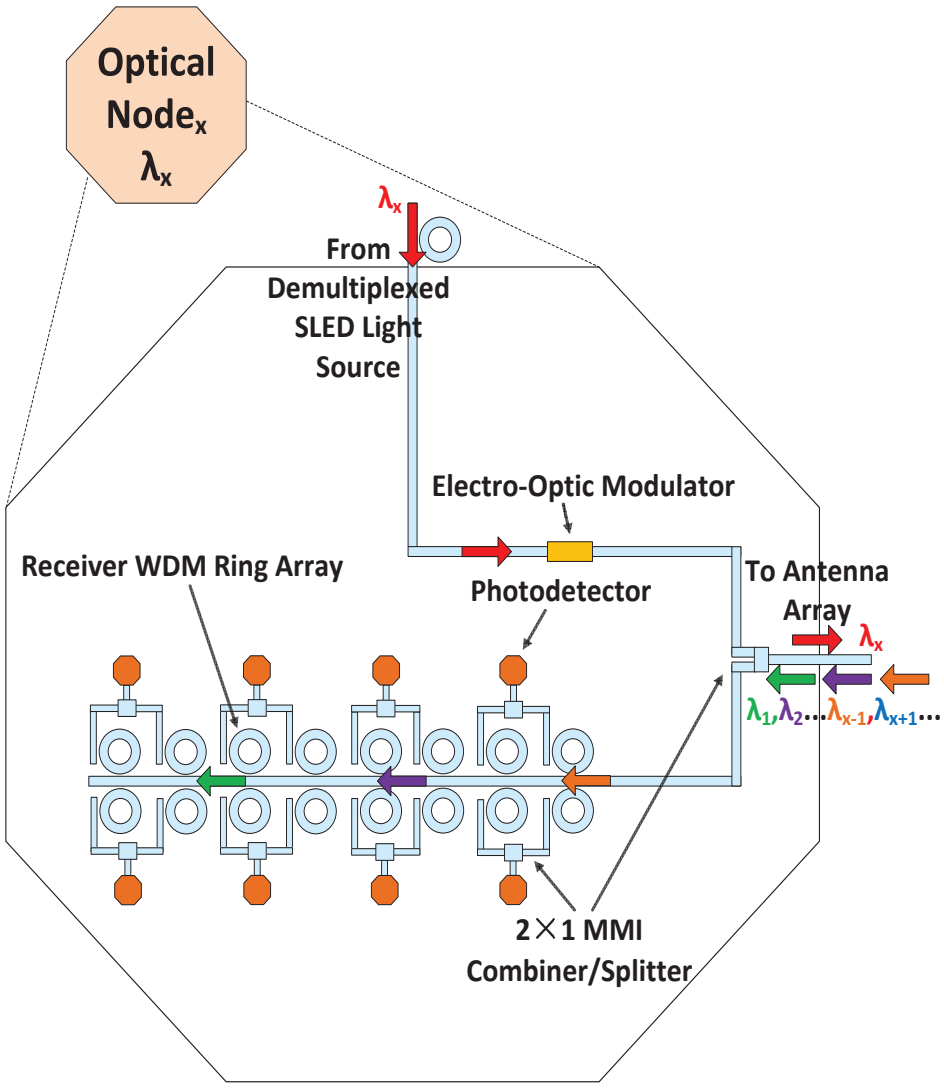


Figure 5.2: A schematic of our proposed variation-aware silicon-organic hybrid design at the optical node level. This communication layer above the processor core contains (a) an input waveguide that provides the demultiplxed SLED light signal to the on-chip electro-optic modulator, (b) an electro-optic modulator that converts electrical information stream into optical information stream, (c) a 2×1 MMI combiner that feeds the optical signal to a any-one-to-all circular antenna array and delivers the signal from the antenna array back to the receiver unit, (d) a variation-aware receiver WDM array of 16 rings that produces many more channels which would cover and compensate channel process and thermal variation drifts in the sender channel groups from other optical nodes, (e) photodetector that receives from two rings and converts optical signals into electrical signals, and sends the signals back to the bottom electronics that processes the information by well-known algorithms.

interferometer (MMI) combiner which is also used as the input port for the receiver section.

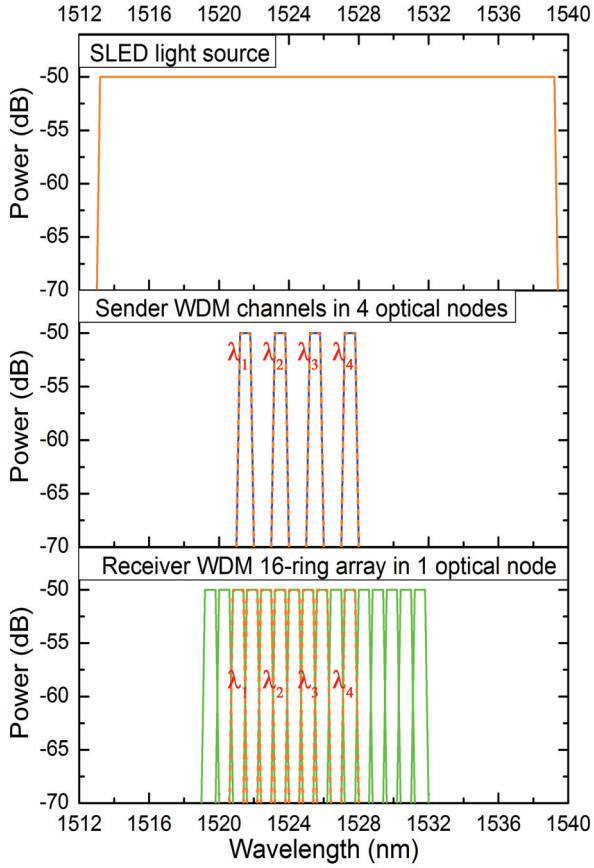


Figure 5.3: A hypothetical wavelength spectrum plot of the SLED light source, the sender WDM channels in 4 optical nodes and the WDM 16-ring array in 1 optical node in Figure 5.2. The channel spectra of the sender and receiver WDM ring arrays drift due to on-chip process and thermal variations. For instance, as it is shown in the plot, the sender channels drift to the left and the receiver channels drift to the right. The design philosophy is to produce enough channels on receiver sides to compensate for the variation drift.

In the receiver section, the design philosophy is that the receiver has many more channels than the transmitter does in order to capture all the transmitted signals, regardless the process and thermal variation. Figure 5.2 shows a receiver WDM array of 16 rings with photodetector for every 2 rings. The 16 wavelength channels produced by rings are designed so that neighboring channels overlap with each other to some extent. The channel bandwidth is 1 nm in this design, same as that of the demultiplexing rings for the SLED source. This design creates a seamless receiving channel array for the transmitted signals. The die size of a modern multi-core processor is about 2 cm $\times$ 2 cm. Due to the fabrication imperfection, the maximum variance among the transmitter

rings and the receiver rings is about 2.6 nm^2/cm which corresponds to a maximum variation of 1.6 nm. 16 channels of the receiver ring array take a bandwidth wide enough to compensate a whole variation range so that all the transmitted signals are guaranteed to be received by some of photodetectors in the group. The bottom plot of Figure 5.3 displays such idea. The green curves are the channels produced by the 16 rings. For instance, the whole receiving channels drift to the right (longer wavelength) due to variation, however from left to right channel 3 and 4 (λ_1), 5, 6 and 7 (λ_2), 8 and 9 (λ_3), 11 (λ_4) in the receiving channel array are still able to pick up the transmitted signals from all the optical nodes. The electronics processes the signals obtained and converted by photodetectors with well-known algorithms [121, 127]. Micro-ring structure offers compact foot print. Take the 5-μm radius micro-ring as an example. For this 16-ring array, the total area is about 1.6×10^{-5} cm^2.

5.3 Demonstration of the WDM Channels

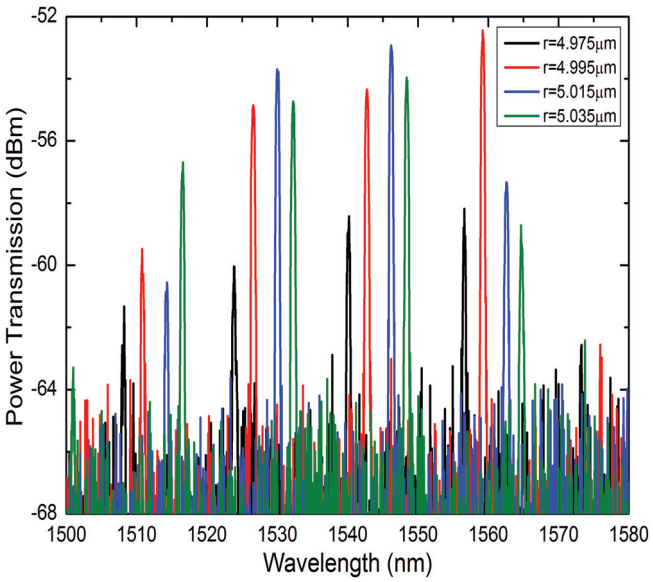


Figure 5.4: A plot of wavelength spectra of the 4-channel WDM device in Figure 3.5. The black, red, blue and green curves are generated by the rings with radii of 4.975 μm, 4.995 μm, 5.015 μm and 5.035 μm respectively. The bandwidth of each channel is about 0.6 nm and the guard band is about 1.4 nm.

We produced a 4-channel WDM ring array, as shown in Figure 3.5, to demonstrate the

concept. The radii of this group of rings are 4.975 μm, 4.995 μm, 5.015 μm and 5.035 μm respectively from left to right. These rings have a waveguide width of 450 nm and a coupling gap of 200 nm uniformly. Figure 5.4 plots the spectra performance of this 4-channel WDM device. A SLED light source is passed through the device and 4 wavelength channels are generated with guard bands in between neighboring channels. The bandwidth of each channel is about 0.6 nm with a guard band of ∼1.4 nm on each side (2 nm spacing). It is worth noting that due to variations, the spacing between these channels are not equal as displayed in the plot. The guard band protects channels from overlapping.

5.4 Scalability

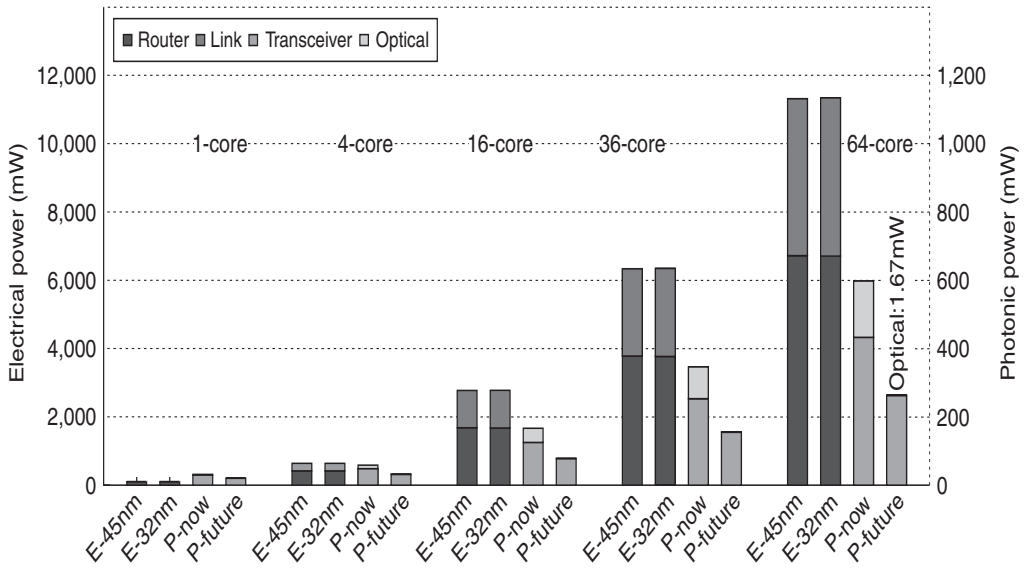


Figure 5.5: Comparison of power consumption of the broadcasting by electrical and photonic interconnect links. The advantage of photonic broadcasting interconnect over electrical links starts to show with processors that have four and more cores [52]. (E: electrical; P: photonic.)

The heating sinking of today's lowest end multicore chip multiprocessors is 1 cm x 1 cm limiting the lowest performance of today's multicore processors to four cores. More advanced heat sinking allows today's higher end standard die size (2 cm x 2 cm) chip processors to contain 16 cores. It is expected that the usual increases in chip density attributable to Moore's law through

the industry wide semiconductor roadmap collaborations will result in high end multicore chip multiprocessors possessing 1024 cores on the usual 2 cm x 2 cm die by 2022. This statement does not address increases that may come about due to advances in wafer scale integration. The advantage of silicon photonic broadcast interconnect over electrical wire would be more apparent with high-density integration of cores. Figure 5.5 compares the power consumption between electrical and photonic interconnect links. With 4 and more cores in processors, the power consumption growth rate with core numbers is much smaller in the photonic broadcast network than in the electrical wires.

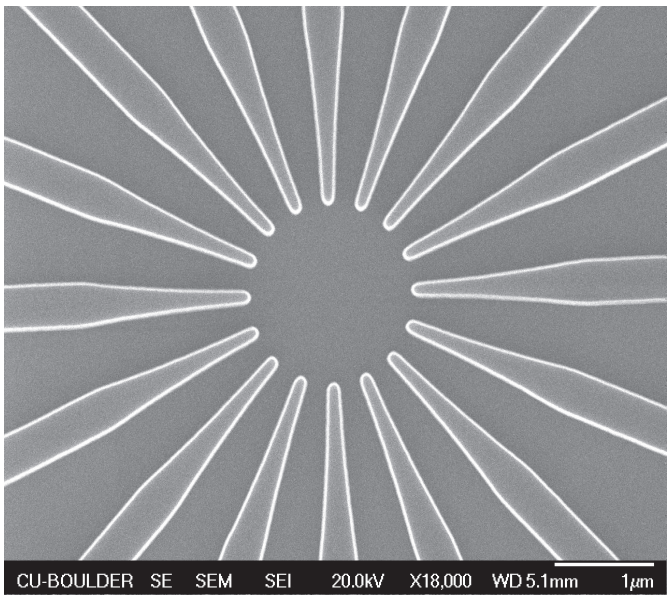


Figure 5.6: The SEM image of a fabricated 16-antenna any-one-to-all array. The diameter of the circle where antenna tips are located is 1.6 μm.

Our silicon photonic variation-aware on-chip interconnect design can be scaled up with the core numbers as the technology evolves. As the key component of the design, the any-one-to-all antenna array enables communications among cores inside the processor. We have produced the 16-antenna array (Figure 5.6) and the 32-antenna array (Figure 5.7). These antenna arrays are able to deliver the SLED power to each channel without introducing much optical loss. A cascaded structure of these antenna arrays creates means for interconnecting 1024 cores in the near future. Its broadcasting topology and WDM multi-wavelength capability simplify network wire connection

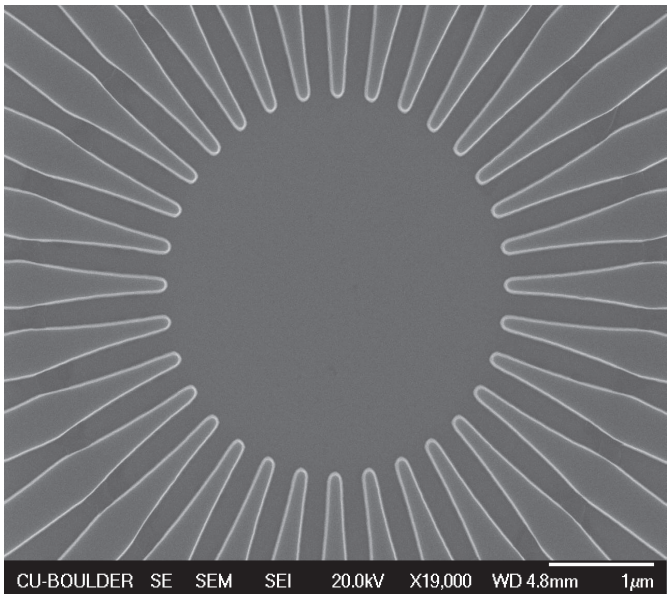


Figure 5.7: The SEM image of a fabricated 32-antenna any-one-to-all array. The diameter of the circle where antenna tips are located is 2.8 μm.

and avoid signal across-talk.

One of the current limitations for the scalability of our broadcast design is the spectrum width of the SLED light source. For instance, the spectrum width of the SLED light source can reach up to 190 nm [161]. We use 2 nm spacing to separate wavelength channels for the cores in a 2 cm x 2 cm area. Only as much as 95 cores can fit in the broadcast multi-core design. At present, supercontinuum light source would be one candidate for providing broader light spectrum. There are commercially available supercontinuum light sources [162] and over 4000 nm bandwidth of mid-IR supercontinuum light source has been demonstrated [163]. The other limitation is the magnitude of the wafer-scale process variation associated with the current fabrication technology. ePIXfab uses 130 nm technology node for the wafer fabrication and the variance is about 1 nm^2/cm across the wafer. In the foreseeable future, if the more advanced technology node, such as the state-of-the-art 22 nm, is applied to the silicon photonic fabrication, the wafer-scale variance would be reduced to several times smaller. For example, a 6-times reduction in wafer-scale variation would means that up to 570 cores can be fit in the design using the 190-nm SLED spectrum bandwidth.

Foot print is not a concern for the cluster of micro-ring design. As for the receiver section

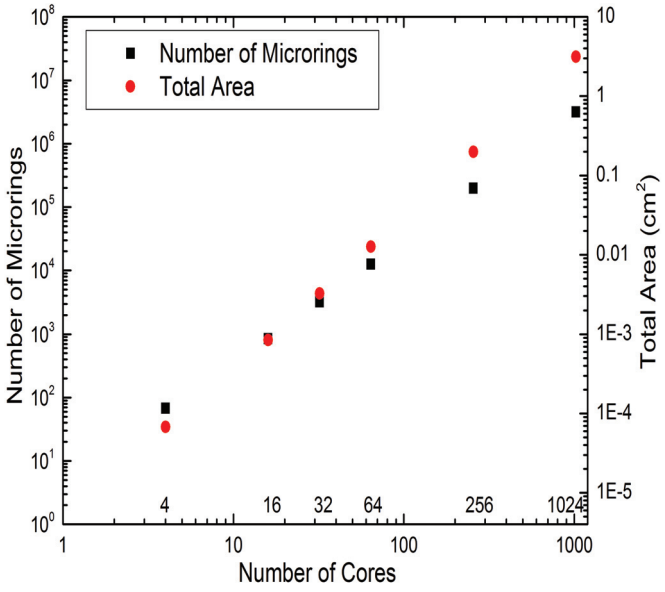


Figure 5.8: The estimation of micro-ring quantity and corresponding foot print for a series of processor designs with 2^n (n being integer) cores. The radius of the micro-ring is about 5-μm.

in a single optical node, due to the small foot print of the micro-ring, it would not be a problem for the receiver micro-ring array to accommodate 1024 wavelength channels. For instance, with a 5-μm radius micro-ring design and 3 rings for a channel spacing to adapt to variation effect, it would take 3069 micro-rings to form the receiver section which corresponds to an area of roughly 3.069×10^{-3} cm^2. Figure 5.8 shows the estimation of the total number of micro-ring and the foot print needed for a series of processor designs with different core numbers. In the 2 cm x 2 cm 1024-core processor, the total micro-rings take about 3 cm^2 area size of the top optical communication layer in the 3D broadcast infrastructure.

5.5 Conclusion

Silicon photonic devices are affected by thermal and fabrication induced process variations. These variations cannot be eliminated easily with the limitation of current fabrication technology. However, with certain design strategy, there is way to overcome these variation effects in the photonic circuity. In this chapter, we propose and discuss a variation-aware on-chip interconnect design for multi-core processors that adapts to the wafer-scale thermal and process variation. We

note that a way of using rings to losslessly distribute the light to the on-chip modulators would be to first separate the light into high wavelength and low wavelength and then subdivide again (repeatedly) in to high and low wavelength. We utilize closely packed micro-ring resonator array to create WDM channels that cover the on-chip wavelength drift range. At the sacrifice of some device foot print, adapting to variations in device designs would be highly feasible to increase the fabrication yield. We demonstrate the WDM concept using a 4-ring silicon photonic structure.

This design addresses the variation problems induced by fabrication and enables on-chip optical communication inside the multi-core processor. For each optical channel, a 1-nm information bandwidth can handle over 100 Gb/s modulation rate. The bandwidth limitation on the interconnect is lifted. Comparing with the traditional electrical interconnect, it also decreases the communication latency and lowers the power consumption in high-density processor core integration. More importantly, our design of silicon photonic on-chip broadcast network can be realized with today's fabrication technology.

Chapter 6

Conclusion

Nowadays, the amount of data in the modern information society has been exploding. New data centers are being built almost everywhere around the world. Cloud computing becomes the new buzzword. We enter a time that has been coined by the term "Big Data Era". The market demand for high performance computing is growing exponentially. To meet this market demand challenge, the semiconductor industry moves from the single-core architecture to the multi-core and many-core architecture in the new generations of processor development. The multi-core and many-core architecture could boost the computing power of a processor with increment of core numbers, however the on-chip interconnection is the key that determines the success of this architecture. As the technology node evolves, traditional electrical interconnect in the multi-core and many-core microprocessor is approaching bottlenecks for the on-chip power, latency and bandwidth. The emergence of silicon photonic technology brings hope for new development direction towards larger scale and higher efficient computing domain. It is of our interest to investigate the feasibility of silicon photonic circuits for the on-chip interconnect application.

In this thesis, we examine the optical performance of the devices that are the fundamental building blocks for silicon photonic circuits. These devices are fabricated at the European foundry ePIXfab. With 30% optimized coupling efficiency, the grating coupler is capable of bringing off-chip light source in and out of functional photonic devices. Before reliable on-chip light source is invented, grating couple plays an irreplaceable role as the input/output (I/O) interface for the silicon photonic circuits. Meanwhile, micro-ring, racetrack are wavelength selective devices which are widely used as

on-chip WDM filters, switches and modulators. Directional coupler is commonly seen in the Mach-Zehnder structures. We demonstrate an optical 16-antenna any-one-to-all array. It is one of the key elements in our proposed 3D hybrid silicon photonic broadcast optical interconnection architecture. Incorporated with polymer coating, this antenna array exhibits superior all-direction transmission properties in the telecommunication wavelength window. We note that polymer coating also can be utilized for optical tuning in the photonic crystals.

We fabricate several wafers of devices using the ePIXfab wafer shuttle runs. Wafer-scale optical measurements indicate that silicon photonic devices are prone to fabrication induced process variations. Devices of same design and fabrication parameters have different optical performance if they are located at different places on the wafer. Research shows that silicon photonic devices are highly sensitive to the variation of overall waveguide width and height. 1 nm of silicon waveguide width variation creates about 1 nm resonant wavelength drift and 1 nm of silicon layer thickness variation produces about 2 nm resonant wavelength drift. Many factors contribute to this problem, including silicon layer thickness uniformity, optical lithography accuracy, dry etching uniformity and photo mask errors, etc. Although advanced optical lithography node and more meticulous fabrication technique would alleviate the process variation, it would not eliminate the problem. By analyzing the wafer-scale measurement data, we discover that the wafer-scale process variation exhibits a "random walk" pattern. That is, the variance of wavelength variation drifts linearly with the separation distance of the devices. The variance is circa 1 nm^2/cm across wafers. This discovery would help photonic device designer come up with design strategy that can adapt to such variation magnitude at wafer-scale fabrication. We note that silicon photonic devices are also prone to the thermal variation due to silicon material's high thermal-optical sensitivity. For instance, the magnitude of thermal variation is in the range of 0.1 nm/°C for a ring resonator with 5-μm radius. We find that directional coupler has remarkable thermal-optical stability at the sacrifice of device foot print.

Due to its sub-nanometer scale, it is hard to track the on-chip process variation of fabricated silicon photonic device with physical measurement tools, such as scanning electron microscope

(SEM). Without an accurate structure description of the final fabricated device, numerical simulations of components can only agree qualitatively with the measured characteristics of fabricated devices but still exhibit large quantitative disagreement. In order to resolve this obstacle, we introduce a method that combines both analytical and numerical modeling. We find that the effective index of refraction of a device is a representation of a device that will differ when transfer characteristics differ. Phenomenological models that are built by our method can be used to extract the dispersion curves that define the effective index of refraction as a function of wavelength for silicon photonic devices. We test our method on three different classes of devices, namely, micro-ring resonators, racetrack resonators and directional couplers. The results coming out of the phenomenological models are made plausible by the linearity of the extracted dispersion curves with wavelength over the wavelength regime of interest (S and C bands) and the use of the determined effective indices to reconstruct the measured transmission as a function of wavelength curves in close agreement with experiment. The extracted effective indices can be used to place limits on the actual fabricated values of waveguide widths, thicknesses, radii of curvature and coupling gaps. The results indicate that our method is accurate towards tracking both on-chip process and thermal variations.

Comparing with traditional electrical interconnect, an 3D silicon photonic on-chip broadcast interconnect offers superior advantages in power, bandwidth and latency. In the wake of the wafer-scale process and thermal variation effect, we propose a variation-aware on-chip broadcast interconnect design for multi-core processor. In the broadcast layer, it contains off-chip super luminescent light emitting diode (SLED) source which is a reliable and cost-effective light source solution to date, wavelength division multiplexing (WDM) sender micro-ring array that creates wavelength channels for the optical nodes, and broadband any-one-to-all antenna array. Inside an optical node, there is a high-speed electro-optic (EO) modulator, a group of silicon micro-rings that forms the WDM receiver array, and on-chip high-speed photodetectors. The key idea of this design is to utilize a large number of silicon micro-rings to accommodate on-chip variations using today's technology. Although it sacrifices device foot print to some extent, it is a viable solution to address

current variation problems for the silicon photonic on-chip interconnect architecture.

Over the last two decades, silicon photonics has gradually grown out of its infancy and the stage is set for this disruptive photonic technology to overcome the barriers. The outcome of our NSF "EMT-NANO" project paves the road for exciting future development in the silicon photonic circuits.

Bibliography

[1] G. E. Moore, "Cramming more components onto integrated circuits," Electronics, vol. 38, no. 8, pp. 114–117, Apr. 1965.

[2] M. Horowitz and W. Dally, "How scaling will change processor architecture," in Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International, 2004, pp. 132–133 Vol.1.

[3] W. Huang, K. Rajamani, M. R. Stan, and K. Skadron, "Scaling with design constraints: predicting the future of big chips," IEEE MICRO, vol. 31, no. 4, pp. 16–29, JUL-AUG 2011.

[4] V. G. Oklobdzija, "Architectural tradeoffs for low power," Intl. Symp. on Computer Architecture, June 1998.

[5] N. Leavitt, "Will power problems curtail processor progress?" Computer, vol. 45, no. 5, pp. 15–17, 2012.

[6] M. Stan, K. Skadron, M. Barcella, W. Huang, K. Sankaranarayanan, and S. Velusamy, "Hotspot: A dynamic compact thermal model at the processor-architecture level," Microelectronics Journal, vol. 34, no. 12, pp. 1153–1165, DEC 2003, 8th IEEE International Workshop on Thermal Investigations of ICs and Systems (THERMINIC 2002), MADRID, SPAIN, OCT 01-04, 2002.

[7] A. Coskun, T. Rosing, K. Whisnant, and K. Gross, "Temperature-aware MPSoC scheduling for reducing hot spots and gradients," in Design Automation Conference, 2008. ASPDAC 2008. Asia and South Pacific, 2008, pp. 49–54.

[8] R. Jayaseelan and T. Mitra, "Temperature aware scheduling for embedded processors," in VLSI Design, 2009 22nd International Conference on, 2009, pp. 541–546.

[9] U. Nawathe, M. Hassan, L. Warriner, K. Yen, B. Upputuri, D. Greenhill, A. Kumar, and H. Park, "An 8-core 64-thread 64b power-efficient SPARC SoC," in Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International, 2007, pp. 108–590.

[10] S. Bell, B. Edwards, J. Amann, R. Conlin, K. Joyce, V. Leung, J. MacKay, M. Reif, L. Bao, J. Brown, M. Mattina, C.-C. Miao, C. Ramey, D. Wentzlaff, W. Anderson, E. Berger, N. Fairbanks, D. Khan, F. Montenegro, J. Stickney, and J. Zook, "Tile64 - processor: a 64-core SoC with mesh interconnect," in Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International, 2008, pp. 88–598.

[11] D. Wendel, R. Kalla, R. Cargoni, J. Clables, J. Friedrich, R. Frech, J. Kahle, B. Sinharoy, W. Starke, S. Taylor, S. Weitzel, S. Chu, S. Islam, and V. Zyuban, "The implementation of power7™: A highly parallel and scalable multi-core high-end server processor," in Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International, 2010, pp. 102–103.

[12] T. Fischer, S. Arekapudi, E. Busta, C. Dietz, M. Golden, S. Hilker, A. Horiuchi, K. Hurd, D. Johnson, H. McIntyre, S. Naffziger, J. Vinh, J. White, and K. Wilcox, "Design solutions for the bulldozer 32nm SOI 2-core processor module in an 8-core CPU," in Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2011 IEEE International, 2011, pp. 78–80.

[13] N. Aggarwal, P. Ranganathan, N. P. Jouppi, and J. E. Smith, "Configurable isolation: building high availability systems with commodity multi-core processors," in ISCA '07: Proceedings of the 34th annual international symposium on Computer architecture. New York, NY, USA: ACM, 2007, pp. 470–481.

[14] G. Loh, "3D-stacked memory architectures for multi-core processors," in Computer Architecture, 2008. ISCA '08. 35th International Symposium on, 2008, pp. 453–464.

[15] B. Nimer and H. Koc, "Improving reliability through task recomputation in heterogeneous multi-core embedded systems," in Technological Advances in Electrical, Electronics and Computer Engineering (TAEECE), 2013 International Conference on, 2013, pp. 72–77.

[16] N. Miura, Y. Koizumi, E. Sasaki, Y. Take, H. Matsutani, T. Kuroda, H. Amano, R. Sakamoto, M. Namiki, K. Usami, M. Kondo, and H. Nakamura, "A scalable 3D heterogeneous multi-core processor with inductive-coupling thruchip interface," in Cool Chips XVI (COOL Chips), 2013 IEEE, 2013, pp. 1–3.

[17] POWER4, http://en.wikipedia.org/wiki/POWER4.

[18] M. Flynn, P. Hung, and K. Rudd, "Deep-submicron microprocessor design issues," IEEE MICRO, vol. 19, no. 4, pp. 11–22, JUL-AUG 1999, 2nd Cool Chips Symposium, KYOTO, JAPAN, APR 26-27, 1999.

[19] S. Pasricha and N. Dutt, "Trends in emerging on-chip interconnect technologies," IPSJ Transactions on System LSI Design Methodology, vol. 1, pp. 2–17, Aug. 2008.

[20] D. Sylvester and K. Keutzer, "A global wiring paradigm for deep submicron design," Trans. Comp.-Aided Des. Integ. Cir. Sys., vol. 19, no. 2, pp. 242–252, Nov. 2006.

[21] P. C. Andricacos, C. Uzoh, J. O. Dukovic, J. Horkans, and H. Deligianni, "Damascene copper electroplating for chip interconnections," IBM Journal of Research and Development, vol. 42, no. 5, pp. 567–574, 1998.

[22] T. Schiml, S. Biesemans, G. Brase, L. Burrell, A. Cowley, K. Chen, A. Von Ehrenwall, B. Von Ehrenwall, P. Felsner, J. Gill, F. Grellner, F. Guarin, L. Han, M. Hoinkis, E. Hsiung, E. Kaltalioglu, P. Kim, G. Knoblinger, S. Kulkarni, A. Leslie, T. Mono, T. Schafbauer, U. Schroeder, K. Schruefer, T. Spooner, D. Warner, C. Wang, R. Wong, E. Demm, and P. Leung, "A 0.13 /spl mu/m CMOS platform with Cu/low-k interconnects for system on chip applications," in VLSI Technology, 2001. Digest of Technical Papers. 2001 Symposium on, 2001, pp. 101–102.

[23] K. Ramani, N. Muralimanohar, and R. Balasubramonian, "Microarchitectural techniques to reduce interconnect power in clustered processors," in In Proc. of the Workshop on Complexity Effective Design, 2004.

[24] C. Duan and A. Tirumala, "Analysis and avoidance of cross-talk in on-chip buses," in Proceedings of the The Ninth Symposium on High Performance Interconnects, ser. HOTI '01. Washington, DC, USA: IEEE Computer Society, 2001, pp. 133–.

[25] Photophone, http://en.wikipedia.org/wiki/Photophone.

[26] K. Kao and G. Hockham, "Dielectric-fibre surface waveguides for optical frequencies," Electrical Engineers, Proceedings of the Institution of, vol. 113, no. 7, pp. 1151–1158, 1966.

[27] F. Kapron, D. Keck, and R. D. Maurer, "Radiation losses in glass optical waveguides," Applied Physics Letters, vol. 17, no. 10, pp. 423–425, 1970.

[28] K. Nagayama, M. Kakui, M. Matsui, T. Saitoh, and Y. Chigusa, "Ultra-low-loss (0.1484 db/km) pure silica core fibre and extension of transmission distance," Electronics Letters, vol. 38, no. 20, pp. 1168–1169, 2002.

[29] O. Delange, "Wide-band optical communication systems: Part II–Frequency-division multiplexing," Proceedings of the IEEE, vol. 58, no. 10, pp. 1683–1690, 1970.

[30] S. E. Miller, "Integrated optics: An introduction," Bell System Technical Journal, vol. 48, no. 7, p. 20592069, Sep. 1969.

[31] J. Goell and R. Standley, "Integrated optical circuits," Proceedings of the IEEE, vol. 58, no. 10, pp. 1504–1512, 1970.

[32] P. K. Tien, "Light waves in thin films and integrated optics," Appl. Opt., vol. 10, no. 11, pp. 2395–2413, Nov. 1971.

[33] R. A. Soref and B. Bennett, "Electrooptical effects in silicon," Quantum Electronics, IEEE Journal of, vol. 23, no. 1, pp. 123–129, 1987.

[34] R. A. Soref, "Silicon-based optoelectronics," Proceedings of the IEEE, vol. 81, no. 12, pp. 1687–1706, 1993.

[35] Y. Vlasov and S. McNab, "Losses in single-mode silicon-on-insulator strip waveguides and bends," Opt. Express, vol. 12, no. 8, pp. 1622–1631, Apr 2004.

[36] R. E. Camacho-Aguilera, Y. Cai, N. Patel, J. T. Bessette, M. Romagnoli, L. C. Kimerling, and J. Michel, "An electrically pumped germanium laser," Opt. Express, vol. 20, no. 10, pp. 11 316–11 320, May 2012.

[37] L. Chen and M. Lipson, "Ultra-low capacitance and high speed germanium photodetectors on silicon," Opt. Express, vol. 17, no. 10, pp. 7901–7906, May 2009.

[38] L. Vivien, A. Polzer, D. Marris-Morini, J. Osmond, J. M. Hartmann, P. Crozat, E. Cassan, C. Kopp, H. Zimmermann, and J. M. Fédéli, "Zero-bias 40Gbit/s germanium waveguide photodetector on silicon," Opt. Express, vol. 20, no. 2, pp. 1096–1101, Jan 2012.

[39] IMEC, http://www.imec.be.

[40] LETI, http://www-leti.cea.fr.

[41] ePIXfab, http://www.epixfab.eu.

[42] EuroPractice, http://www.europractice.com.

[43] Y. Jiang, W. Jiang, L. Gu, X. Chen, and R. T. Chen, "80-micron interaction length silicon photonic crystal waveguide modulator," Applied Physics Letters, vol. 87, no. 22, p. 221105, 2005.

[44] F. Y. Gardes, D. J. Thomson, N. G. Emerson, and G. T. Reed, "40 Gb/s silicon photonics modulator for TE and TM polarisations," Opt. Express, vol. 19, no. 12, pp. 11 804–11 814, Jun 2011.

[45] L. Alloatti, D. Korn, R. Palmer, D. Hillerkuss, J. Li, A. Barklund, R. Dinu, J. Wieland, M. Fournier, J. Fedeli, H. Yu, W. Bogaerts, P. Dumon, R. Baets, C. Koos, W. Freude, and J. Leuthold, "42.7 Gbit/s electro-optic modulator in silicon technology," Opt. Express, vol. 19, no. 12, pp. 11 841–11 851, Jun 2011.

[46] I. Chlamtac, A. Ganz, and G. Karmi, "Purely optical networks for terabit communication," in INFOCOM '89. Proceedings of the Eighth Annual Joint Conference of the IEEE Computer and Communications Societies. Technology: Emerging or Converging, IEEE, 1989, pp. 887–896 vol.3.

[47] D. Miller, "Rationale and challenges for optical interconnects to electronic chips," Proceedings of the IEEE, vol. 88, no. 6, pp. 728–749, 2000.

[48] M. Haurylau, G. Chen, H. Chen, J. Zhang, N. A. Nelson, D. H. Albonesi, E. G. Friedman, and P. M. Fauchet, "On-chip optical interconnect roadmap: Challenges and critical directions," Selected Topics in Quantum Electronics, IEEE Journal of, vol. 12, no. 6, pp. 1699–1705, 2006.

[49] Y. Hoskote, S. Vangal, A. Singh, N. Borkar, and S. Borkar, "A 5-GHz mesh interconnect for a teraflops processor," Micro, IEEE, vol. 27, no. 5, pp. 51–61, 2007.

[50] R. Ho, J. Gainsley, and R. Drost, "Long wires and asynchronous control," in Asynchronous Circuits and Systems, 2004. Proceedings. 10th International Symposium on, 2004, pp. 240–249.

[51] Z. Li, M. Mohamed, X. Chen, H. Zhou, A. Mickelson, L. Shang, and M. Vachharajani, "Iris: A hybrid nanophotonic network design for high-performance and low-power on-chip communication," J. Emerg. Technol. Comput. Syst., vol. 7, no. 2, pp. 8:1–8:22, Jul. 2011.

[52] Z. Li, M. Mohamed, H. Zhou, L. Shang, A. Mickelson, D. Filipovic, M. Vachharajani, X. Chen, W. Park, and Y. Sun, "Global on-chip coordination at light speed," Design Test of Computers, IEEE, vol. 27, no. 4, pp. 54–67, 2010.

[53] K. Yu, A. Lakhani, and M. Wu, "Nanoscale light sources for on-chip optical interconnects," in Optical Internet (COIN), 2010 9th International Conference on, 2010, pp. 1–3.

[54] Y. Zhang, M. Khan, Y. Huang, J. Ryou, P. Deotare, R. Dupuis, and M. LonCar, "Photonic crystal nanobeam lasers," Applied Physics Letters, vol. 97, no. 5, p. 051104, 2010.

[55] H. P. Hsu, A. F. Milton, and W. K. Burns, "Multiple fiber end fire coupling with single-mode channel waveguides," Applied Physics Letters, vol. 33, no. 7, pp. 603–605, 1978.

[56] M. Haruna, Y. Segawa, and H. Nishihara, "Nondestructive and simple method of optical-waveguide loss measurement with optimisation of end-fire coupling," Electronics Letters, vol. 28, no. 17, pp. 1612–1613, 1992.

[57] D. Taillaert, W. Bogaerts, P. Bienstman, T. Krauss, P. van Daele, I. Moerman, S. Verstuyft, K. De Mesel, and R. Baets, "An out-of-plane grating coupler for efficient butt-coupling between compact planar waveguides and single-mode fibers," Quantum Electronics, IEEE Journal of, vol. 38, no. 7, pp. 949–955, 2002.

[58] B. Little, S. Chu, P. Absil, J. Hryniewicz, F. Johnson, F. Seiferth, D. Gill, V. Van, O. King, and M. Trakalo, "Very high-order microring resonator filters for WDM applications," Photonics Technology Letters, IEEE, vol. 16, no. 10, pp. 2263–2265, 2004.

[59] X. Luo, J. Song, Q. Fang, X. Tu, T.-Y. Liow, M. Yu, and G.-Q. Lo, "Thermal-tunable microring resonator-based WDM optical receiver for on-chip optical interconnect," in Photonics Global Conference (PGC), 2012, 2012, pp. 1–3.

[60] B. Lee, A. Biberman, N. Sherwood-Droz, C. Poitras, M. Lipson, and K. Bergman, "High-speed 2 × 2 switch for multiwavelength silicon-photonic networks-on-chip," Lightwave Technology, Journal of, vol. 27, no. 14, pp. 2900–2907, 2009.

[61] H. L. R. Lira, S. Manipatruni, and M. Lipson, "Broadband hitless silicon electro-optic switch for on-chip optical networks," Opt. Express, vol. 17, no. 25, pp. 22 271–22 280, Dec 2009.

[62] F. Y. Gardes, A. Brimont, P. Sanchis, G. Rasigade, D. Marris-Morini, L. O'Faolain, F. Dong, J. M. Fedeli, P. Dumon, L. Vivien, T. F. Krauss, G. T. Reed, and J. Martí, "High-speed modulation of a compact silicon ring resonator based on a reverse-biased pn diode," Opt. Express, vol. 17, no. 24, pp. 21 986–21 991, Nov 2009.

[63] J. C. Rosenberg, W. M. Green, S. Assefa, T. Barwicz, M. Yang, S. M. Shank, and Y. A. Vlasov, "Low-power 30 Gbps silicon microring modulator," in CLEO:2011 - Laser Applications to Photonic Applications. Optical Society of America, 2011, p. PDPB9.

[64] X. Xiao, H. Xu, X. Li, Y. Hu, K. Xiong, Z. Li, T. Chu, Y. Yu, and J. Yu, "25 Gbit/s silicon microring modulator based on misalignment-tolerant interleaved PN junctions," Opt. Express, vol. 20, no. 3, pp. 2507–2515, Jan 2012.

[65] M. S. Nawrocka, T. Liu, X. Wang, and R. R. Panepucci, "Tunable silicon microring resonator with wide free spectral range," Applied Physics Letters, vol. 89, no. 7, p. 071110, 2006.

[66] Q. Xu, D. Fattal, and R. G. Beausoleil, "Silicon microring resonators with 1.5-μm radius," Opt. Express, vol. 16, no. 6, pp. 4309–4315, Mar 2008.

[67] E. A. J. Marcatili, "Dielectric rectangular waveguide and directional coupler for integrated optics," Bell System Technical Journal, vol. 48, no. 7, p. 20712102, Sep 1969.

[68] A. Weierholt and S. Neegard, "Theory of directional couplers including transition region phase shifts," Quantum Electronics, IEEE Journal of, vol. 26, no. 7, pp. 1227–1233, 1990.

[69] W. Shi, X. Wang, C. Lin, H. Yun, Y. Liu, T. Baehr-Jones, M. Hochberg, N. A. F. Jaeger, and L. Chrostowski, "Silicon photonic grating-assisted, contra-directional couplers," Opt. Express, vol. 21, no. 3, pp. 3633–3650, Feb 2013.

[70] H. Zhou, X. Chen, D. Espinoza, A. Mickelson, and D. Filipovic, "Nanoscale optical dielectric rod antenna for on-chip interconnecting networks," Microwave Theory and Techniques, IEEE Transactions on, vol. 59, no. 10, pp. 2624–2632, 2011.

[71] CST Microwave Studio, http://www.cst.com.

[72] HFSS, http://www.ansys.com.

[73] A. Wong, R. A. Ferguson, and S. Mansfield, "The mask error factor in optical lithography," Semiconductor Manufacturing, IEEE Transactions on, vol. 13, no. 2, pp. 235–242, 2000.

[74] K. Busch and S. John, "Liquid-Crystal photonic-band-gap materials: The tunable electromagnetic vacuum," Phys. Rev. Lett., vol. 83, pp. 967–970, Aug 1999.

[75] K. Yoshino, Y. Shimoda, Y. Kawagishi, K. Nakayama, and M. Ozaki, "Temperature tuning of the stop band in transmission spectra of liquid-crystal infiltrated synthetic opal as tunable photonic crystal," Applied Physics Letters, vol. 75, no. 7, pp. 932–934, 1999.

[76] W. Park and J.-B. Lee, "Mechanically tunable photonic crystal structure," Applied Physics Letters, vol. 85, no. 21, pp. 4845–4847, 2004.

[77] R. Beausoleil, P. Kuekes, G. S. Snider, S.-Y. Wang, and R. S. Williams, "Nanoelectronic and nanophotonic interconnect," Proceedings of the IEEE, vol. 96, no. 2, pp. 230–247, 2008.

[78] M. Mohamed, Z. Li, X. Chen, L. Shang, and A. Mickelson, "Reliability-aware design flow for silicon photonics on-chip interconnect," IEEE Transactions of Very Large Scale Integration System (in press), 2013.

[79] S. Selvaraja, W. Bogaerts, P. Dumon, D. Van Thourhout, and R. Baets, "Subnanometer linewidth uniformity in silicon nanophotonic waveguide devices using CMOS fabrication technology," Selected Topics in Quantum Electronics, IEEE Journal of, vol. 16, no. 1, pp. 316 –324, jan.-feb. 2010.

[80] W. A. Zortman, D. C. Trotter, and M. R. Watts, "Silicon photonics manufacturing," Opt. Express, vol. 18, no. 23, pp. 23 598–23 607, Nov 2010.

[81] C. Nitta, M. Farrens, and V. Akella, "Addressing system-level trimming issues in on-chip nanophotonic networks," in High Performance Computer Architecture (HPCA), 2011 IEEE 17th International Symposium on. IEEE Computer Society, Feb 2011, pp. 122 –131.

[82] C. Qiu, J. Shu, Z. Li, X. Zhang, and Q. Xu, "Wavelength tracking with thermally controlled silicon resonators," Opt. Express, vol. 19, no. 6, pp. 5143–5148, MAR 14 2011.

[83] B. Guha, B. B. C. Kyotoku, and M. Lipson, "CMOS-compatible athermal silicon microring resonators," Opt. Express, vol. 18, no. 4, pp. 3487–3493, Feb. 15 2010.

[84] S. Manipatruni, R. K. Dokania, B. Schmidt, N. Sherwood-Droz, C. B. Poitras, A. B. Apsel, and M. Lipson, "Wide temperature range operation of micrometer-scale silicon electro-optic modulators," Opt. Lett., vol. 33, no. 19, pp. 2185–2187, Oct 2008.

[85] G. Cocorullo and I. Rendina, "Thermo-optical modulation at 1.5 mu m in silicon etalon," Electronics Letters, vol. 28, no. 1, pp. 83–85, JAN 2 1992.

[86] I. Kiyat, A. Aydinli, and N. Dagli, "Low-power thermooptical tuning of SOI resonator switch," IEEE Photonics Technology Letters, vol. 18, no. 1-4, pp. 364–366, JAN-FEB 2006.

[87] M. W. Pruessner, T. H. Stievater, M. S. Ferraro, and W. S. Robinovich, "Thermo-optic tuning and switching in SOI waveguide Fabry-Perot microcavities," Opt. Express, vol. 15, no. 12, pp. 7557–7563, June 2007.

[88] J. Teng, P. Dumon, W. Bogaerts, H. Zhang, X. Jian, M. Zhao, G. Morthier, and R. Baets, "Athermal SOI ring resonators by overlaying a polymer cladding on narrowed waveguides," in Group IV Photonics, 2009. GFP '09. 6th IEEE International Conference. IEEE, Sep. 2009, pp. 77–79.

[89] Y. Kokubun, S. Yoneda, and S. Matsuura, "Temperature-independent optical filter at 1.55 μm wavelength using a silica-based athermal waveguide," Electronics Letters, vol. 34, no. 4, pp. 367–369, 1998.

[90] M. Mohamed, Z. Li, X. Chen, L. Shang, A. Mickelson, M. Vachharajani, and Y. Sun, "Power-efficient variation-aware photonic on-chip network management," in Low-Power Electronics and Design (ISLPED), 2010 ACM/IEEE International Symposium on, aug. 2010, pp. 31 –36.

[91] Z. Li, M. Mohamed, X. Chen, E. Dudley, K. Meng, L. Shang, A. Mickelson, R. Joseph, M. Vachharajani, B. Schwartz, and Y. Sun, "Reliability modeling and management of nanophotonic on-chip networks," Very Large Scale Integration (VLSI) Systems, IEEE Transactions on, vol. 20, no. 1, pp. 98 –111, jan. 2012.

[92] S. K. Selvaraja, "Wafer-scale fabrication technology for silicon photonic integrated circuits," Ph.D. dissertation, Ghent University, Ghent, Belgium., 2011.

[93] S. K. Selvaraja, E. Rosseel, L. Fernandez, M. Tabat, W. Bogaerts, J. Hautala, and P. Absil, "SOI thickness uniformity improvement using wafer-scale corrective etching for silicon nano-photonic device," in Proceedings of the 2011 annual symposium of the IEEE Photonics Benelux Chapter, P. Bienstman, G. Mortier, G. n. Roelkens, and M. Verbist, Eds. IEEE Photonics Society, 2011, pp. 289–292.

[94] Z. Li, D. Fay, A. Mickelson, L. Shang, M. Vachharajani, D. Filipovic, W. Park, and Y. Sun, "Spectrum: A hybrid nanophotonicelectric on-chip network," in Design Automation Conference, 2009. DAC '09. 46th ACM/IEEE, 2009, pp. 575–580.

[95] Z. Li, J. Wu, L. Shang, A. R. Mickelson, M. Vachharajani, D. Filipovic, W. Park, and Y. Sun, "A high-performance low-power nanophotonic on-chip network," in Proceedings of the 14th ACM/IEEE international symposium on Low power electronics and design, ser. ISLPED '09. New York, NY, USA: ACM, 2009, pp. 291–294.

[96] Z. Li, M. Mohamed, X. Chen, A. Mickelson, and L. Shang, "Device modeling and system simulation of nanophotonic on-chip networks for reliability, power and performance," in Design Automation Conference (DAC), 2011 48th ACM/EDAC/IEEE, june 2011, pp. 735 –740.

[97] K. Chiang, "Effective-index method for the analysis of optical waveguide couplers and arrays: an asymptotic theory," Journal of Lightwave Technology, vol. 9, no. 1, pp. 62 –72, jan 1991.

[98] Y. Vlasov, W. M. J. Green, and F. Xia, "High-throughput silicon nanophotonic wavelength-insensitive switch for on-chip optical networks," Nature Photonics, vol. 2, no. 4, pp. 242–246, APR 2008.

[99] B. Little, S. Chu, H. Haus, J. Foresi, and J. P. Laine, "Microring resonator channel dropping filters," Lightwave Technology, Journal of, vol. 15, no. 6, pp. 998–1005, 1997.

[100] W. Bogaerts, P. D. Heyn, T. V. Vaerenbergh, K. D. Vos, S. K. Selvaraja, T. Claes, P. Dumon, P. Bienstman, D. V. Thourhout, and R. Baets, "Silicon microring resonators," Laser & Photon. Rev., vol. 6, p. 4773, 2012.

[101] C. T. Shih and S. Chao, "Simplified numerical method for analyzing TE-like modes in a three-dimensional circularly bent dielectric rib waveguide by solving two one-dimensional eigenvalue equations," J. Opt. Soc. Am. B, vol. 25, no. 6, pp. 1031–1037, Jun 2008.

[102] M. Masi, R. Orobtchouk, G. Fan, J.-M. Fedeli, and L. Pavesi, "Towards a realistic modelling of ultra-compact racetrack resonators," Lightwave Technology, Journal of, vol. 28, no. 22, pp. 3233 –3242, nov.15, 2010.

[103] Q. Wang, G. Farrell, and T. Freir, "Effective index method for planar lightwave circuits containing directional couplers," Optics Communications, vol. 259, no. 1, pp. 133–136, MAR 1 2006.

[104] L. Cao, A. Elshaari, A. Aboketaf, and S. Preble, "Adiabatic couplers in SOI waveguides," in Conference on Lasers and Electro-Optics. Optical Society of America, 2010, p. CThAA2.

[105] S. Selvaraja, K. De Vos, W. Bogaerts, P. Bienstman, D. Van Thourhout, and R. Baets, "Effect of device density on the uniformity of silicon nano-photonic waveguide devices," in LEOS Annual Meeting Conference Proceedings, 2009. LEOS '09. IEEE, 2009, pp. 311–312.

[106] C. Batten, A. Joshi, J. Orcutt, A. Khilo, B. Moss, C. W. Holzwarth, M. A. Popovic, H. Li, H. I. Smith, J. L. Hoyt, F. X. Kaertner, R. J. Ram, V. Stojanovic, and K. Asanovic, "Building many-core processor-to-DRAM networks with monolithic CMOS silicon photonics," IEEE Micro, vol. 29, no. 4, pp. 8–21, JUL-AUG 2009.

[107] J. Leuthold, C. Koos, W. Freude, L. Alloatti, R. Palmer, D. Korn, J. Pfeifle, M. Lauermann, R. Dinu, S. Wehrli, M. Jazbinsek, P. Gunter, M. Waldow, T. Wahlbrink, J. Bolten, H. Kurz, M. Fournier, J.-M. Fedeli, H. Yu, and W. Bogaerts, "Silicon-organic hybrid electro-optical devices," Selected Topics in Quantum Electronics, IEEE Journal of, vol. 19, no. 6, pp. 3 401 413–3 401 413, 2013.

[108] M. Hochberg and T. Baehr-Jones, "Towards fabless silicon photonics," Nature Photonics, vol. 4, no. 8, pp. 492–494, AUG 2010.

[109] R. Soref, "Mid-infrared photonics in silicon and germanium," Nature Photonics, vol. 4, no. 8, pp. 495–497, AUG 2010.

[110] Q. Xu and M. Lipson, "All-optical logic based on silicon micro-ring resonators," Optics Express, vol. 15, no. 3, pp. 924–929, FEB 5 2007.

[111] S. Xiao, M. H. Khan, H. Shen, and M. Qix, "Compact silicon microring resonators with ultra-low propagation loss in the C band," Opt. Express, vol. 15, no. 22, pp. 14 467–14 475, Oct 2007.

[112] H. Yamada, T. Chu, S. Ishida, and Y. Arakawa, "Optical directional coupler based on Si-wire waveguides," Photonics Technology Letters, IEEE, vol. 17, no. 3, pp. 585–587, 2005.

[113] Y. jun Quan, P. de Han, Q. jiang Ran, F. ping Zeng, L. peng Gao, and C. hua Zhao, "A photonic wire-based directional coupler based on SOI," Optics Communications, vol. 281, no. 11, pp. 3105 – 3110, 2008.

[114] M. Hochberg, T. Baehr-Jones, G. Wang, J. Huang, P. Sullivan, L. Dalton, and A. Scherer, "Towards a millivolt optical modulator with nano-slot waveguides," Opt. Express, vol. 15, no. 13, pp. 8401–8410, Jun 2007.

[115] D. Thomson, F. Gardes, J.-M. Fedeli, S. Zlatanovic, Y. Hu, B.-P. Kuo, E. Myslivets, N. Alic, S. Radic, G. Mashanovich, and G. Reed, "50-Gb/s silicon optical modulator," Photonics Technology Letters, IEEE, vol. 24, no. 4, pp. 234–236, 2012.

[116] R. Palmer, L. Alloatti, D. Korn, P. Schindler, M. Baier, J. Bolten, T. Wahlbrink, M. Waldow, R. Dinu, W. Freude, C. Koos, and J. Leuthold, "Low power Mach-Zehnder modulator in silicon-organic hybrid technology," Photonics Technology Letters, IEEE, vol. 25, no. 13, pp. 1226–1229, 2013.

[117] J. V. Campenhout, W. M. Green, S. Assefa, and Y. A. Vlasov, "Low-power, 2×2 silicon electro-optic switch with 110-nm bandwidth for broadband reconfigurable optical networks," Opt. Express, vol. 17, no. 26, pp. 24 020–24 029, Dec 2009.

[118] M. Yang, W. M. J. Green, S. Assefa, J. V. Campenhout, B. G. Lee, C. V. Jahnes, F. E. Doany, C. L. Schow, J. A. Kash, and Y. A. Vlasov, "Non-blocking 4×4 electro-optic silicon switch for on-chip photonic networks," Opt. Express, vol. 19, no. 1, pp. 47–54, Jan 2011.

[119] B. G. Lee, C. L. Schow, A. V. Rylyakov, J. V. Campenhout, W. M. J. Green, S. Assefa, F. E. Doany, M. Yang, R. A. John, C. V. Jahnes, J. A. Kash, and Y. Vlasov, "Demonstration of a digital CMOS driver codesigned and integrated with a broadband silicon photonic switch," J. Lightwave Technol., vol. 29, no. 8, pp. 1136–1142, Apr 2011.

[120] A. Rylyakov, C. Schow, B. Lee, W. M. J. Green, S. Assefa, F. Doany, M. Yang, J. Van Campenhout, C. V. Jahnes, J. Kash, and Y. Vlasov, "Silicon photonic switches hybrid-integrated with CMOS drivers," Solid-State Circuits, IEEE Journal of, vol. 47, no. 1, pp. 345–354, 2012.

[121] Y. Xu, J. Yang, and R. Melhem, "Tolerating process variations in nanophotonic on-chip networks," in Proceedings of the 39th Annual International Symposium on Computer Architecture, ser. ISCA '12. Washington, DC, USA: IEEE Computer Society, 2012, pp. 142–152.

[122] A. Liu, L. Liao, Y. Chetrit, J. Basak, H. Nguyen, D. Rubin, and M. Paniccia, "Wavelength division multiplexing based photonic integrated circuits on silicon-on-insulator platform," Selected Topics in Quantum Electronics, IEEE Journal of, vol. 16, no. 1, pp. 23–32, 2010.

[123] S. Assefa, S. Shank, W. Green, M. Khater, E. Kiewra, C. Reinholm, S. Kamlapurkar, A. Rylyakov, C. Schow, F. Horst, H. Pan, T. Topuria, P. Rice, D. Gill, J. Rosenberg, T. Barwicz, M. Yang, J. Proesel, J. Hofrichter, B. Offrein, X. Gu, W. Haensch, J. Ellis-Monaghan, and Y. Vlasov, "A 90nm CMOS integrated nano-photonics technology for 25Gbps WDM optical communications applications," in Electron Devices Meeting (IEDM), 2012 IEEE International, 2012, pp. 33.8.1–33.8.3.

[124] L. Vivien, J. Osmond, D. Marris-Morini, P. Crozat, E. Cassan, J. Fedeli, S. Brision, J. F. Damlencourt, V. Mazzochi, D. Van Thourhout, and J. Brouckaert, "European helios project: Silicon photonic photodetector integration," in Group IV Photonics, 2009. GFP '09. 6th IEEE International Conference on, 2009, pp. 10–12.

[125] M. T. Hill, Y.-S. Oei, B. Smalbrugge, Y. Zhu, T. De Vries, P. J. Van Veldhoven, F. W. M. Van Otten, T. J. Eijkemans, J. P. Turkiewicz, H. De Waardt, E. J. Geluk, S.-H. Kwon, Y.-H. Lee, R. Notzel, and M. K. Smit, "Lasing in metallic-coated nanocavities," Nature Photonics, vol. 1, no. 10, pp. 589–594, OCT 2007.

[126] H.-G. Park, C. J. Barrelet, Y. Wu, B. Tian, F. Qian, and C. M. Lieber, "A wavelength-selective photonic-crystal waveguide coupled to a nanowire light source," Nature Photonics, vol. 2, no. 10, pp. 622–626, OCT 2008.

[127] F. Wang, G. Keskin, A. Phelps, J. Rotner, X. Li, G. K. Fedder, T. Mukherjee, and L. T. Pileggi, "Statistical design and optimization for adaptive post-silicon tuning of MEMS filters," in Proceedings of the 49th Annual Design Automation Conference, ser. DAC '12. New York, NY, USA: ACM, 2012, pp. 176–181.

[128] M. Koshiba, "Time-domain beam propagation method applied to nonlinear photonic crystal waveguide devices," in Integrated Photonics Research and Applications/Nanophotonics for Information Systems. Optical Society of America, 2005, p. ITuD1.

[129] A. Olyaee and F. T. Hamadani, "Compound FDTD method for silicon photonics," AIP Advances, vol. 1, no. 3, SEP 2011.

[130] D. M. H. Leung, N. Kejalakshmy, B. M. A. Rahman, and K. T. V. Grattan, "Rigorous modal analysis of silicon strip nanoscale waveguides," Opt. Express, vol. 18, no. 8, pp. 8528–8539, Apr 2010.

[131] R. E. Bellman, Dynamic Programming. Princeton, New Jersey, U.S.A.: Princeton University Press, Mar 1957.

[132] R. Bellman, Adaptive control processes - A guided tour. Princeton, New Jersey, U.S.A.: Princeton University Press, 1961.

[133] J. P. Rust, "Using randomization to break the curse of dimensionality," Econometrica, vol. 65, no. 3, pp. 487–516, May 1997.

[134] W. Bogaerts, P. Dumon, D. V. Thourhout, D. Taillaert, P. Jaenen, J. Wouters, S. Beckx, V. Wiaux, and R. G. Baets, "Compact wavelength-selective functions in silicon-on-insulator photonic wires," Selected Topics in Quantum Electronics, IEEE Journal of, vol. 12, no. 6, pp. 1394 –1401, nov.-dec. 2006.

[135] M. Ferrera, L. Razzari, D. Duchesne, R. Morandotti, Z. Yang, M. Liscidini, J. E. Sipe, S. Chu, B. E. Little, and D. J. Moss, "Low-power continuous-wave nonlinear optics in doped silica glass integrated waveguide structures," Nature Photonics, vol. 2, no. 12, pp. 737–740, Dec. 2008.

[136] C. Maleville and C. Mazuré, "Smart-cut® technology: from 300 mm ultrathin SOI production to advanced engineered substrates," Solid-State Electronics, vol. 48, no. 6, pp. 1055 – 1063, 2004.

[137] K. Cheng, "Improving front side process uniformity by back-side metallization," in CS MANTECH Conference, Boston, Massachusetts, USA, 2012.

[138] C. Qiu, J. Shu, Z. Li, X. Zhang, and Q. Xu, "Wavelength tracking with thermally controlled silicon resonators," Opt. Express, vol. 19, no. 6, pp. 5143–5148, Mar 2011.

[139] R. Grover, V. Van, T. A. Ibrahim, P. P. Absil, L. C. Calhoun, F. G. Johnson, J. V. Hryniewicz, and P.-T. Ho, "Parallel-cascaded semiconductor microring resonators for high-order and wide-FSR filters," J. Lightwave Technol., vol. 20, no. 5, p. 872, May 2002.

[140] J. Poon, J. Scheuer, S. Mookherjea, G. Paloczi, Y. Huang, and A. Yariv, "Matrix analysis of microring coupled-resonator optical waveguides," Opt. Express, vol. 12, no. 1, pp. 90–103, JAN 12 2004.

[141] J. K. S. Poon, J. Scheuer, and A. Yariv, "Wavelength-selective reflector based on a circular array of coupled microring resonators," Photonics Technology Letters, IEEE, vol. 16, no. 5, pp. 1331–1333, 2004.

[142] X. Zhang, D. Huang, and X. Zhang, "Transmission characteristics of dual microring resonators coupled via 3×3 couplers," Opt. Express, vol. 15, no. 21, pp. 13 557–13 573, Oct 2007.

[143] C. Li, X. Luo, and A. W. Poon, "Dual-microring-resonator electro-optic logic switches on a silicon chip," Semiconductor Science and Technology, vol. 23, no. 6, JUN 2008.

[144] D. M. Pozar, Microwave Engineering, 4th Edition. Wiley, 2012.

[145] D. Y. K. Ko and J. R. Sambles, "Scattering matrix method for propagation of radiation in stratified media: attenuated total reflection studies of liquid crystals," J. Opt. Soc. Am. A, vol. 5, no. 11, pp. 1863–1866, Nov 1988.

[146] M. Auslender and S. Hava, "Scattering-matrix propagation algorithm in full-vectorial optics of multilayer grating structures," Opt. Lett., vol. 21, no. 21, pp. 1765–1767, Nov 1996.

[147] M. Heiblum and J. Harris, "Analysis of curved optical waveguides by conformal transformation," Quantum Electronics, IEEE Journal of, vol. 11, no. 2, pp. 75 –83, february 1975.

[148] N. Rouger, L. Chrostowski, and R. Vafaei, "Temperature effects on Silicon-on-Insulator (SOI) racetrack resonators: A coupled analytic and 2-D finite difference approach," Lightwave Technology, Journal of, vol. 28, no. 9, pp. 1380–1391, 2010.

[149] G. Cocorullo, F. Della Corte, and I. Rendina, "Temperature dependence of the thermo-optic coefficient in crystalline silicon between room temperature and 550 K at the wavelength of 1523 nm," Applied Physics Letters, vol. 74, no. 22, pp. 3338–3340, MAY 31 1999.

[150] A. Yariv and P. Yeh, Photonics: Optical Electronics in Modern Communications, 6th ed. Oxford University Press, 2007.

[151] S. Sheem and J. R. Whinnery, "Guiding by single curved boundaries in integrated optics,," Wave Electron, vol. 1, pp. 61–68, 1974.

[152] A. Hardy and W. Streifer, "Coupled mode theory of parallel waveguides," Lightwave Technology, Journal of, vol. 3, no. 5, pp. 1135 – 1146, oct 1985.

[153] G. T. Reed, Silicon Photonics: The State of the Art. New York, NY, USA: Wiley-Interscience, 2008.

[154] R. Morris and A. K. Kodi, "Exploring the design of 64-and 256-core power efficient nanophotonic interconnect," IEEE Journal Of Selected Topics In Quantum Electronics, vol. 16, no. 5, pp. 1386–1393, Sep-Oct 2010.

[155] B. Little, J. Foresi, G. Steinmeyer, E. Thoen, S. Chu, H. Haus, E. Ippen, L. Kimerling, and W. Greene, "Ultra-compact Si-SiO_2 microring resonator optical channel dropping filters," Photonics Technology Letters, IEEE, vol. 10, no. 4, pp. 549–551, 1998.

[156] T. Barwicz, M. Popović, P. Rakich, M. Watts, H. Haus, E. Ippen, and H. Smith, "Microring-resonator-based add-drop filters in SiN: fabrication and analysis," Opt. Express, vol. 12, no. 7, pp. 1437–1442, Apr 2004.

[157] T. Baehr-Jones, M. Hochberg, C. Walker, and A. Scherer, "High-Q optical resonators in silicon-on-insulator-based slot waveguides," Applied Physics Letters, vol. 86, no. 8, 2005.

[158] T. Baehr-Jones, B. Penkov, J. Huang, P. Sullivan, J. Davies, J. Takayesu, J. Luo, T.-D. Kim, L. Dalton, A. Jen, M. Hochberg, and A. Scherer, "Nonlinear polymer-clad silicon slot waveguide modulator with a half wave voltage of 0.25V," Applied Physics Letters, vol. 92, no. 16, 2008.

[159] A. Liu, L. Liao, D. Rubin, H. Nguyen, B. Ciftcioglu, Y. Chetrit, N. Izhaky, and M. Paniccia, "High-speed optical modulation based on carrier depletion in a silicon waveguide," Opt. Express, vol. 15, no. 2, pp. 660–668, Jan 2007.

[160] H. Xu, X. Xiao, X. Li, Y. Hu, Z. Li, T. Chu, Y. Yu, and J. Yu, "High speed silicon Mach-Zehnder modulator based on interleaved PN junctions," Opt. Express, vol. 20, no. 14, pp. 15 093–15 099, Jul 2012.

[161] S. Haffouz, P. J. Barrios, R. Normandin, D. Poitras, and Z. Lu, "Ultrawide-bandwidth, superluminescent light-emitting diodes using InAs quantum dots of tuned height," Opt. Lett., vol. 37, no. 6, pp. 1103–1105, Mar 2012.

[162] NKT Photonics, http://www.nktphotonics.com.

[163] P. Domachuk, N. A. Wolchover, M. Cronin-Golomb, A. Wang, A. K. George, C. M. B. Cordeiro, J. C. Knight, and F. G. Omenetto, "Over 4000 nm bandwidth of mid-IR supercontinuum generation in sub-centimeter segments of highly nonlinear tellurite PCFs," Opt. Express, vol. 16, no. 10, pp. 7161–7168, May 2008.