INCREASED-FUNCTIONALITY VLSI-COMPATIBLE DEVICES BASED ON BACKWARD-DIODE FLOATING-BASE Si/SiGe HETEROJUNCTION BIPOLAR TRANSISTORS

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1. Introduction

As modern semiconductor circuits progress towards greater complexity and ever smaller feature sizes at ever greater processing cost, increasing the functionality of logic devices is becoming a primary direction in microelectronics research and development. Several classes of semiconductor devices promising higher functionality than standard transistor logic have been intensively studied over the past decade, including multiterminal real-space transfer[1] and resonant tunneling[2] heterostructures. However, the vast majority of these devices were based on the bandgap engineering possibilities of compound semiconductor heterostructures and required low temperatures for effective operation, making them ill-suited for current digital technology. Recently, there has been a demonstration of a class of increased functionality devices based on multi-emitter heterojunction bipolar transistor (HBT's) fabricated in the InGaAs/InP material system.[3] We propose to investigate the performance of an analogous, multi-terminal backward-diode HBT structures in the Si/SiGe material system,[4] which would utilize the advantageous properties of Si/SiGe heterojunctions and, more importantly, would feature full compatibility with the silicon technology

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that will dominate microelectronics for the foreseeable future.

The increased functionality HBT's rely on the incorporation of a backward diode into the emitter-base junction of a bipolar transistor together with multiple contacts to the emitter region. The base contact is dispensed with altogether, which simplifies the fabrication process. The emitter-base backward diode characteristic allows emitter contacts to extract the base majority carriers under reverse bias, so the emitter region contacts can perform either "emitter" or "base" electrode functions. This structural symmetry leads to higher logic functionality of a single device, leading up to a ten-fold demonstrated reduction in device elements for some (but not all) logic functions.[3] Since our variant of the multi-emitter increased-functionality HBT can be implemented using a single Si/SiGe heterostructure operating at room temperature, the proposed class of devices will be fully compatible with Si VLSI technology. Furthermore, freed of the "base" contacting problem, the proposed devices will be ideally suited to BiCMOS circuits, where the simplified bipolar fabrication will simplify integration with standard multi-mask CMOS designs at no penalty to the bipolar performance.

2. Device operation

In this section we illustrate the principle of operation[3,4] of increased-functionality HBT devices built in silicon. Consider a Si/SiGe/Si *npn* bipolar transistor with a backward diode[5] emitter-base (E-B) *np* junction (created by the appropriate doping of the emitter and base regions) and a standard base-collector *pn* junction. The emitter region is contacted by two (or more) trench-isolated electrodes, while the base is left floating, as shown schematically in Fig. 1. If the E-B junction is forward-biased, minority electrons are injected into the base and extracted by the collector, resulting in ordinary bipolar transistor operation with current gain. However, because of the backward-diode characteristic shown in Fig. 2, when the E-B junction is reverse-biased it acts as an efficient Ohmic contact to the base.

If in the structure of Fig. 1 both of the emitter contacts are grounded ($V_{e1} = V_{e2} = 0$) and the collector is biased high ($V_c >> kT$), a small collector current will flow as in a standard bipolar transistor with a floating base. Conversely, if one of the emitter contacts is grounded ($V_{e1} = 0$) and the other is biased $V_{e2} < V_c$, a large hole current will flow through the reverse-biased E-B junction under the second emitter (which acts as a "base" contact), leading to a large output current. If the current densities of the forward and reverse-biased junctions are J_1 and J_2, and

corresponding ponding junction areas are A_1 and A_2 respectively, in the active transistor regime with high common-emitter current gain ($\beta >> 1$)

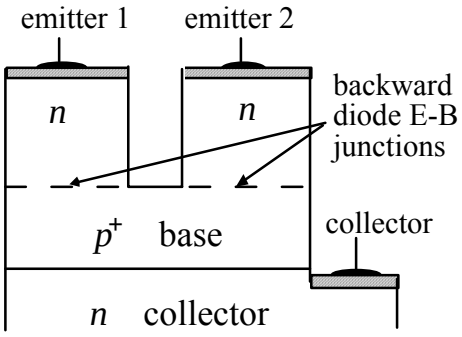

Fig. 1. Schematic of a structure with two emitter contacts (E-B junctions are backward diodes).

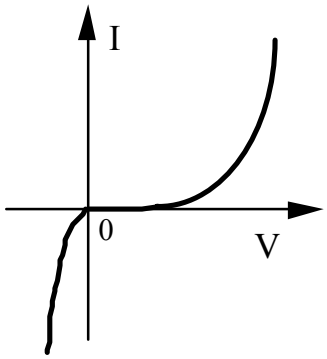

Fig. 2. I(V) characteristic of a backward diode in silicon (from Ref. 4).

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we have:

$$I_c \approx A_1 J_1 = \beta A_2 J_2 \qquad (1)$$

Given the backward-diode E-B junction characteristics shown in Fig. 2, one can determine the transconductance characteristic $I_c(V_{e2})$ using the graphical construction shown in Fig. 3. By replotting the reverse bias characteristic of the backward diode multiplied by $-\beta A_2/A_1$, one can read off the biasing difference V_{e2} between the emitter contacts for a given collector I_c as the horizontal (voltage) distance between the forward bias curve and the rescaled reverse bias curve, as shown in Fig. 3.

Since the emitter contacts are fully symmetric, the single device of Fig. 1 possesses full *xor* logic functionality. By fabricating more than two contacts to the emitter region, more complicated logic functions can be implemented. For example, an analogous three-emitter contact structure can perform the *ornand* logic function in a single device: room-temperature operation of such a three-emitter structure was demonstrated recently.[3]

The utility of the proposed class of devices hinges on two

requirements. First, the increased functionality of the device cannot come at the expense of high-speed operation typical of standard bipolar transistors. Second, since the range of high-level logic functions that can be implemented using the multiple emitter contact geometry of Fig. 1 is limited, the devices must in principle be compatible with BiCMOS logic circuits. The second requirement would appear to rule out the already demonstrated compound semiconductor versions of the device,[3] but both of these requirements can be addressed by implementing the devices using modified Si/SiGe/Si heterojunction bipolar transistor (HBT) designs.[6]

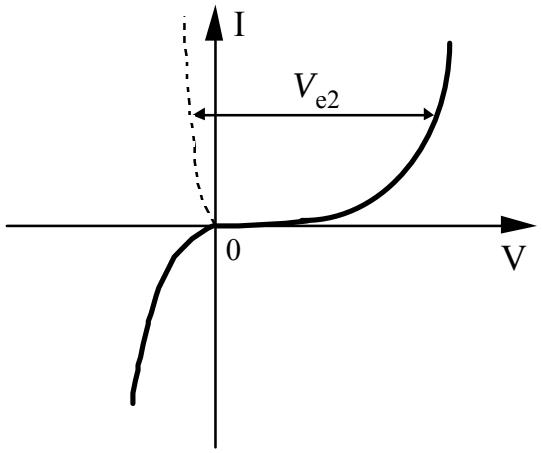

FIG. 3. Graphical determination of the transistor characteristic $I_c(V_{e2})$. The dashed line shows the reverse bias backward diode characteristic rescaled by $-\beta A_2/A_1$. For a given value of V_{e2} the output current I_c can be read off as shown.

High-speed operation of the device in Fig. 1 is governed by the standard HBT rules — high emitter efficiency (suppressed hole injection from base to emitter) in forward bias, high electron transfer coefficient through the base, and low base sheet resistance — combined with low backward diode resistance of the E-B junction in reverse bias. All of these rules can be simultaneously satisfied by making the heavily doped *p*-type base from epitaxial $Si_{1-x}Ge_x$ (with Ge content graded to $x \approx 0.25$ or $x \approx 0.3$ at the E-B junction) and then growing an n^+-Si emitter. The

band discontinuity in the $Si/Si_{1-x}Ge_x$ occurs entirely in the valence band ($\Delta E_v \approx 200$ meV for $x = 0.2$)[7] conferring the usual heterostructure advantage of permitting high base doping (and hence low base sheet resistance) without sacrificing emitter efficiency. In fact, the absence of a barrier to forward injection of minority carriers into the base confers an additional advantage to the Si/SiGe implementation of the device over its compound semi-conductor counterparts, as illustrated in Fig. 4 which shows the band diagram of the proposed *npn* Si/SiGe/Si HBT in the backward-diode (V_{e1} low; V_{e2} high) regime.

The very high base doping available in Si epitaxy reduces the tunneling resistance of the reverse-biased E-B backward diode, which is unaffected by the additional valence band barrier since the current is carried by Zener tunneling across the (narrower) bandgap. As a result, the proposed Si/SiGe/Si *npn* structures should have equivalent performance to state-of-the-art Si/SiGe heterojunction bipolar transistors and yet perform high-level logic functions in a single device.

3. Conclusion

The implementation of proposed backward-diode floating-base HBT's in Si/SiGe heterostructures is advantageous from both the processing and VLSI integration standpoints. Since contacting the base is typically the most demanding task in bipolar transistor fabrication, the proposed structures would greatly reduce the number of processing steps. The integration of these bipolar devices with standard CMOS designs will benefit from the fabrication simplicity, leading to easy implementation of such promising BiCMOS circuits as CMOS logic integrated with high current-drive bipolar Si/SiGe input-output devices.

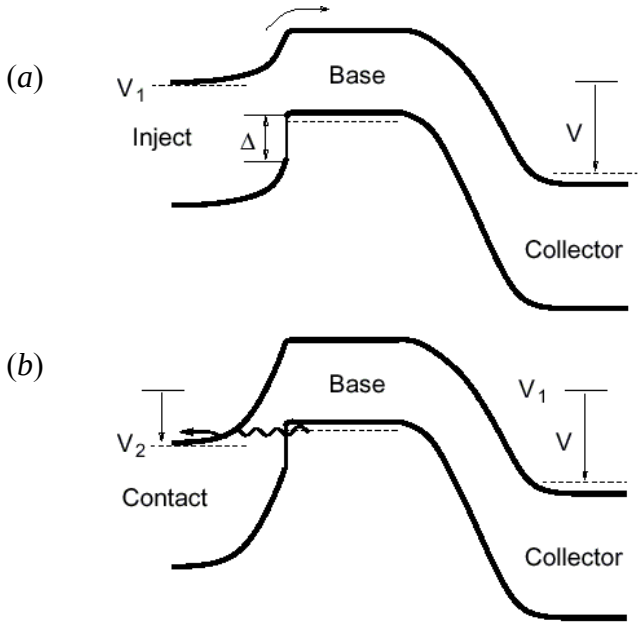

FIG. 4. Band diagrams of the device under the two emitter contacts under the V_{e1} = high (*a* — injecting emitter) and V_{e2} = low (*b* — contact emitter). The base is taken to be $Si_{1-x}Ge_x$ with the Ge fraction $x = 0.2$ (graded up from $x = 0$ in the low-doped base-collector junction).

4. References

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