# Guest Editorial System-Level Interconnect Prediction

THE community of researchers in the field of System-Level Interconnect Prediction (SLIP) is growing. This is apparent from the increasing attendance of the SLIP Workshop from 30 people in 1999 to around 50 in 2000 and 2001. Worth mentioning also is the increasing interest and appreciation from industry. The number of publications on SLIP subjects has increased dramatically over the last few years and this special issue again, as last year's special issue of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS on SLIP, provides the reader with an overview of recent advances in the field.

The growing interest in SLIP of course is linked to the increasing dominance of interconnects in today's designs. In nanometer designs, interconnects are truly the limiting factor for both performance and density, i.e., the value and the cost of a GSI system.

Finding a solution to the interconnect problems requires a coherent view on both process technology issues (e.g., reverse-scaled copper wires, low-permittivity dielectrics) and layout or system design choices and innovations (e.g., new layer assignment techniques, phase shifting and optical proximity correction). Communication between the process engineers and layout designers is a must. SLIP can provide this link because it enables the process engineer to make abstraction of the specifics of a single design while optimizing the process and vice versa.

A lot of research efforts have been focusing on Rent's rule, which is the basis of all modeling techniques used in SLIP. The first paper of this special issue, "A Differential Equation for Placement Analysis," by Christie [1], provides the reader with a new view on this rule by considering the competing processes that generate and terminate wires crossing a circuit partition. The new solution is valid for the entire range of partition sizes, including the effect of circuit boundaries and pin limitations.

The second paper, "Optimal n-tier Multilevel Interconnect Architectures for Gigascale Integration (GSI)," by Venkatesan, Davis, Bowman, and Meindl [2], uses an *a priori* wire length distribution to find a multilevel interconnect architecture design methodology that optimizes the interconnect cross-sectional dimensions of each metal layer. The paper "Toward Better Wireload Models in the Presence of Obstacles" by Cheng, Kahng, Liu, and Stroobandt, further investigates wire length distribution models in the presence of routing obstacles and thus enables their application for System-On-Chip designs where IP blocks are combined with row-based layout to facilitate timing closure. The next paper, "Buffer Block Planning for Interconnect Planning and Prediction," by Cong, Kong, and Pan [3], introduces blocks reserved for wiring buffers and plans their location in a layout.

All these papers involve entire wire length distributions or average wire lengths. In the paper "Prelayout Estimation of Individual Wire Lengths," by Bodapati and Najm [4], the authors investigate the possibility of estimating individual wire lengths. They show that there are variability limitations in doing so.

An extension of the wire length distribution models to three-dimensional architectures is provided in the paper "Impact of Three-Dimensional Architectures on Interconnects in Gigascale Integration" by Joyner, Venkatesan, Zarkesh-Ha, Davis, and Meindl [5]. The authors also show the improvements such architectures could give. The final regular paper in this special issue is on "Statistical Skew Modeling for General Clock Distribution Networks in Presence of Process Variations" by Jiang and Horiguchi [6]. It provides a new approach to estimating the mean values and variances of both clock skews and the maximal clock delay of general clock distribution networks.

A concluding brief contribution entitled "A Stochastic Model for the Interconnection Topology of Digital Circuits" by Verplaetse, Stroobandt, and Van Campenhout [7] tries to predict the variance of the terminal count distribution in order to improve on the assumption in current *a priori* interconnect prediction methods that circuits are homogeneous.

Due to an unfortunate error, six papers were published in the December 2001 issue of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. One paper has been published in the October 2001 issue and only one paper is published in this issue. On behalf of the Editor-in-Chief, I would like to apologize to the readers and especially to the authors for the inconvenience this might have caused. The reference list at the end of this Guest Editorial will guide you towards the papers that are part of this special section, but have been published earlier.

I am confident that this special issue provides a first-class view on the latest advancements in the field of a priori system-level interconnect prediction. After a thorough review process in several stages, less than half of the originally submitted papers were accepted. This issue will undoubtedly be a valued source of information for anyone involved with or interested in this field. I hope that you can appreciate and enjoy the papers presented and that they will inspire many researchers to increase their efforts in this increasingly important research domain.

DIRK STROOBANDT, *Guest Editor*
Postdoctoral Researcher at Ghent University
Electronics and Information Systems (ELIS) Department
B-9000 Gent, Belgium

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**Dirk Stroobandt** (S'92–M'98) graduated in 1994 and received the Ph.D. degree in electrotechnical engineering from Ghent University, Belgium, in May 1998.

From 1994 to 1998, he was Research Assistant and currently he is a Postdoctoral Fellow with the Fund for Scientific Research—Flanders, Belgium (F.W.O.). He is affiliated with the Department of Electronics and Information Systems (ELIS), Parallel Information Systems group (PARIS) of Ghent University. His research is oriented towards *a priori* estimations of interconnection lengths in electronic systems and its applications to CAD, computer architecture evaluation and design optimization. From July 1999 to June 2000, he visited the University of California, Los Angeles (UCLA) as a Postdoctoral Researcher affiliated with the group of Andrew B. Kahng. Together with Prof. Kahng, he was Guest Editor of the December 2000 special issue of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS on System-Level Interconnect Prediction. He has written many leading publications and the first book entirely devoted to System-Level Interconnect Prediction. He has been invited to numerous conferences, universities, and industry for presentations on this subject.

Dr. Stroobandt was the inaugural winner of the ACM/SIGDA Outstanding Doctoral Thesis Award in Design Automation and initiator and co-founder of the ACM International Workshop on System-Level Interconnect Prediction (SLIP), as well as the General Chair of SLIP-2000.