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The i860™ XP Second Generation of the i860™ Supercomputing Microprocessor Family

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Presentation Outline

- i860™ XP CPU Key Attributes
- Supercomputing/Visualization System Requirements
- The i860 XP Microprocessor
- Vector Operation Capabilities
- Multi-Processing Capabilities
- Internal Architecture
- Performance Benchmarks
- $/MFLOP Roadmap
- Summary and Conclusions

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i860™ XP CPU Key Attributes

- **Target Markets**
  - Massively Parrallel Supercomputer and Mulit-Processing Systems
  - Super Workstation & servers
  - High End Workstation Graphics/Accelerator Subsystems

- **Technology**
  - 3 Layer Metal, 0.8uM CHMOS-V Technology
  - 2.55 Million Transistors
  - Die Size: 612 X 404 mils
  - 262 pin CGA Package
  - Frequency 40 & 50 MHz
  - Power Dissipation (@50 MHz) - 5W

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Supercomputing/Visualization System Requirements

- **High Throughput Computing Performance**
  - "Number Crunching" Floating-Point Capability
  - Real Time 3D Graphics/Visualization
- **Multiprocessing/Parallel Processing**
- **Vector Processing**
- **High Bus Bandwidth**
- **Scalable Performance**
- **Cost Effectiveness**

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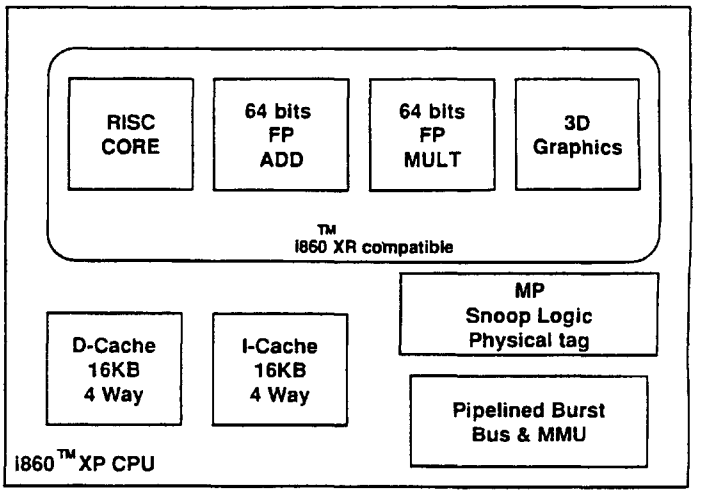
The i860™ XP Supercomputing Microprocessor

- **Very High Performance**
  - 100MFLOPS
  - 400MByte/Sec Bus Bandwidth
  - 40 & 50 MHz Operation
  - 40+ SpecMark
  - 3 operations/cycle
- **High Integration, Single Chip**
- **Multi & Parallel Processing**
  - Hardware Cache Consistency
  - Bus Snooping
  - Detached Concurrency Control Unit (DCCU)
  - Scalable - Shared Bus or Massively Parallel
- **Upward Software Compatible with i860™ XR CPU**



A SUPERCOMPUTING MICROPROCESSOR

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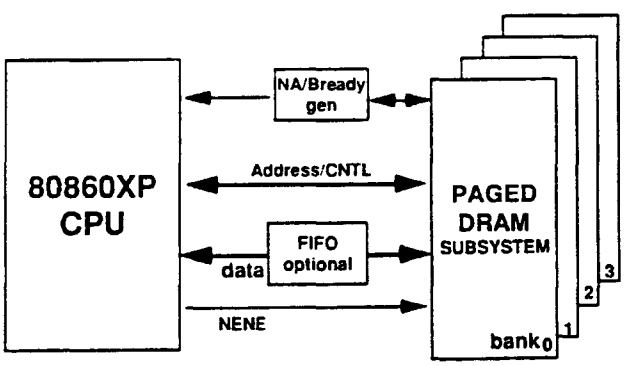
Vector Operation Capabilities



- **Pipelined Load Instructions**
  - Loads 128bits in 2 CLKs
  - Helps to Hide Memory Latency
- **Specialized Instructions to Reduce Tight Loops**
  - BLA - Add & Branch with 0 latency
  - Dual Instruction mode - FP and Integer parallelism
  - Dual Operation Instructions
- **Large D-Cache to hold large Vectors**
- **Optimized DRAM interface For Fast Bus Throughput**
  - Paged DRAM Support
  - Three levels of pipeline
  - Burst Bus
  - Wide Memory Access

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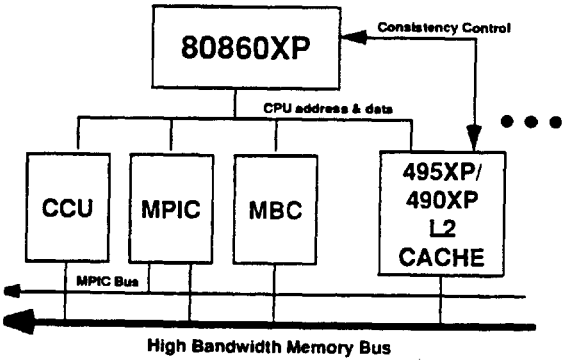
Multiprocessing Capabilities



- **Reduced Bus Utilization (Scalability)**
  - Large On-chip Write-Back Cache
  - 2nd level Write-Back Cache (82490XP/82495XP) (Consistency By Inclusion)
  - LOCK by Address
- **Data Consistency / Integrity**
  - HW Based MESI Cache Consistency Protocol
  - Bus Snooping Concurrently with Cache Look Up
  - Weak/ Strong Write Ordering Mode
  - Data Parity Check - Bus Retry Hooks
- **Parallel Processing**
  - Loop Level Parallelism (MPIC, DCCU)

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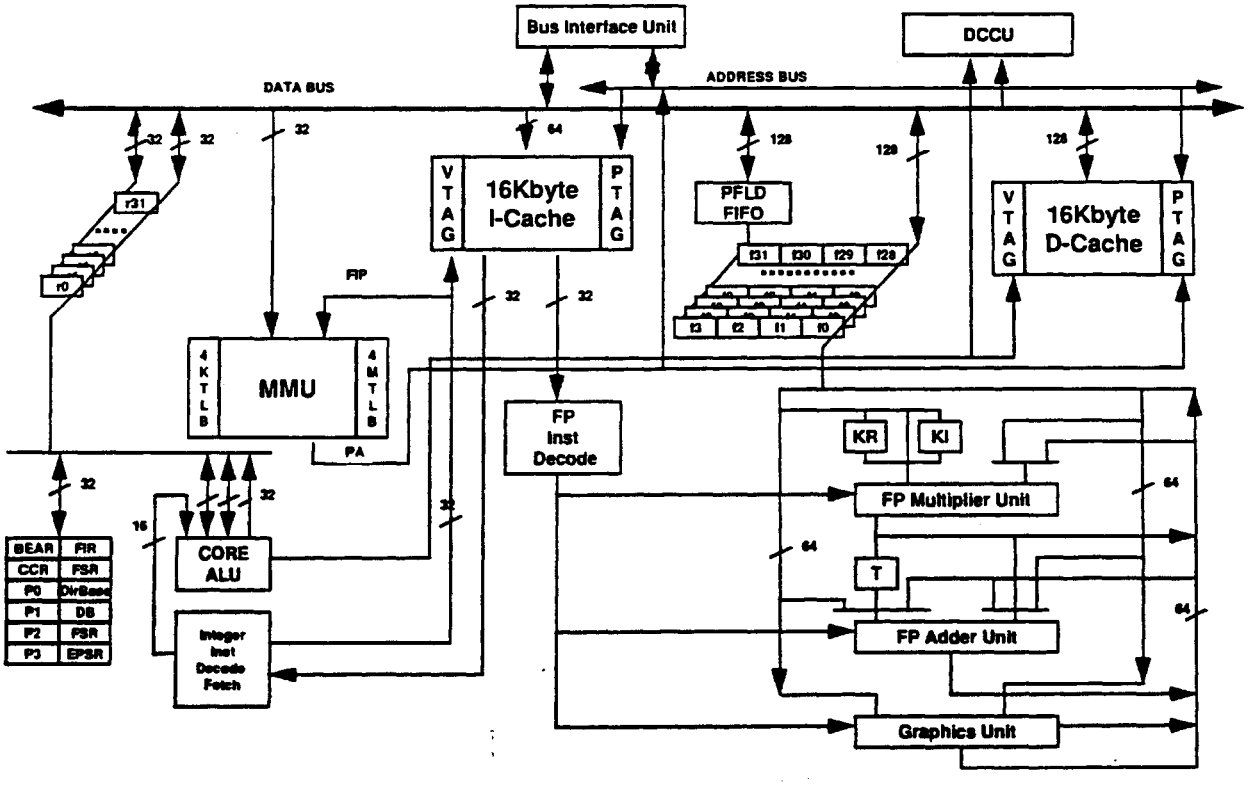
Internal Architecture



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Performance Benchmarks

Total SPEC *	41+
FP SPEC *	50
Dhrystone	103.9
Triangles/sec	80K
Linpack (Double) MFLOPS	20

* Based on preliminary results on prototype board

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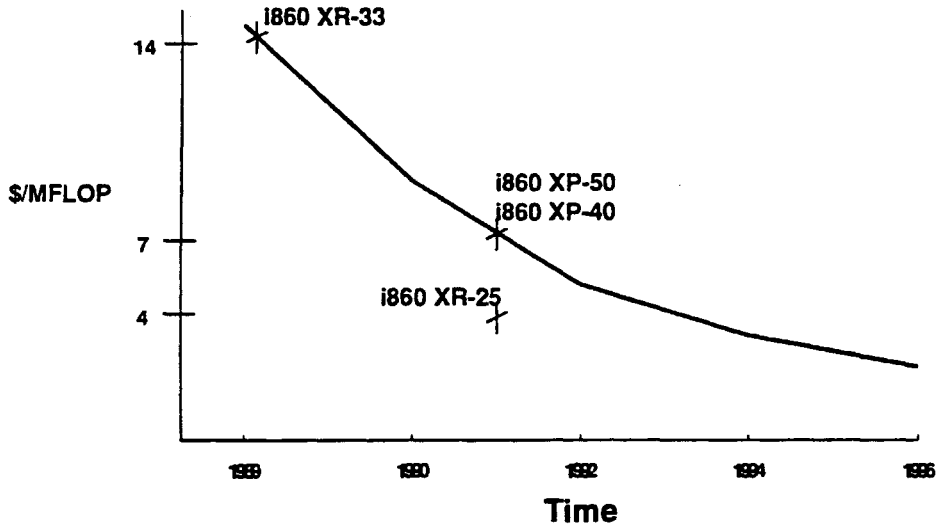
i860™ Architecture $/MFLOP Roadmap



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Summary & Conclusions

- Supports High End MP/PP Systems Via Coarse to Loop Level of Parallelism
- Supports Large Variety of Memory Sub Systems
  - From DRAM to Sophisticated Second Level Cache Based Systems
  - Scalability From Uniprocessor to Massively Parallel systems
- High Integration
  - RISC core Surrounded with FP, Caches, MMU, and CCU
- Bus Optimized for Vector Operations and Fast Throughput
- Cost Effective MFLOPS

i860™ XP CPU DELIVERS SUPERCOMPUTING PERFORMANCE TO BROAD CLASS OF AFFORDABLE SYSTEMS

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Die Photo