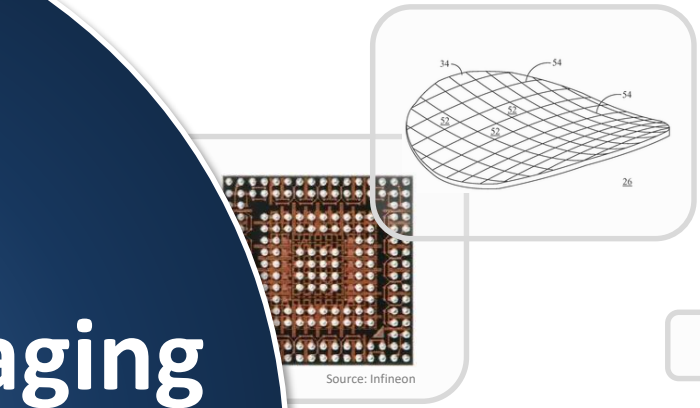
Fan-Out Wafer Level Packaging

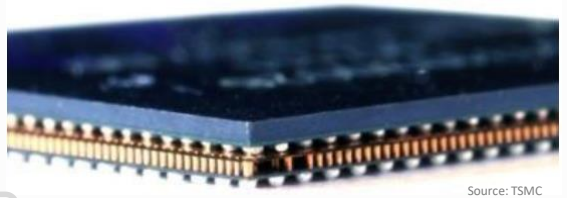
Patent Landscape Analysis

November 2016

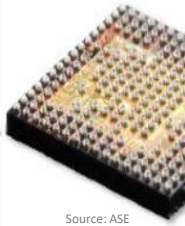
REPORT SAMPLE



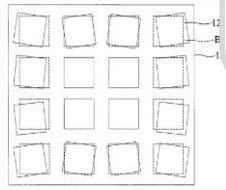
Source: Infineon

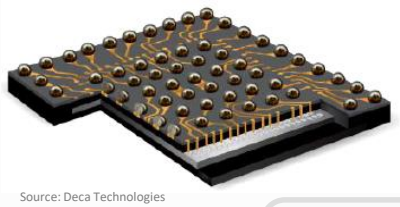


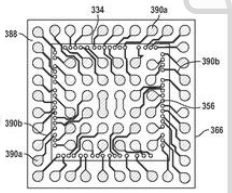
Source: TSMC



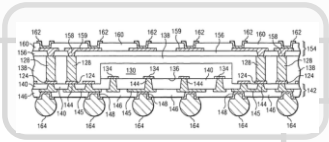
Source: ASE

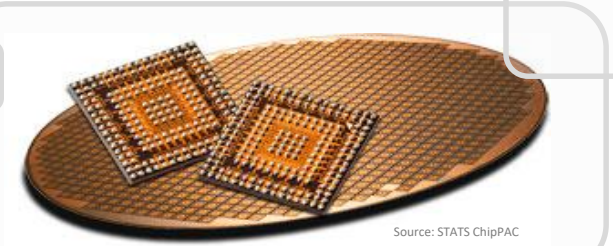






Source: Deca Technologies





Source: STATS ChipPAC

Source: Nepes

KnowMade
Patent & Technology Intelligence

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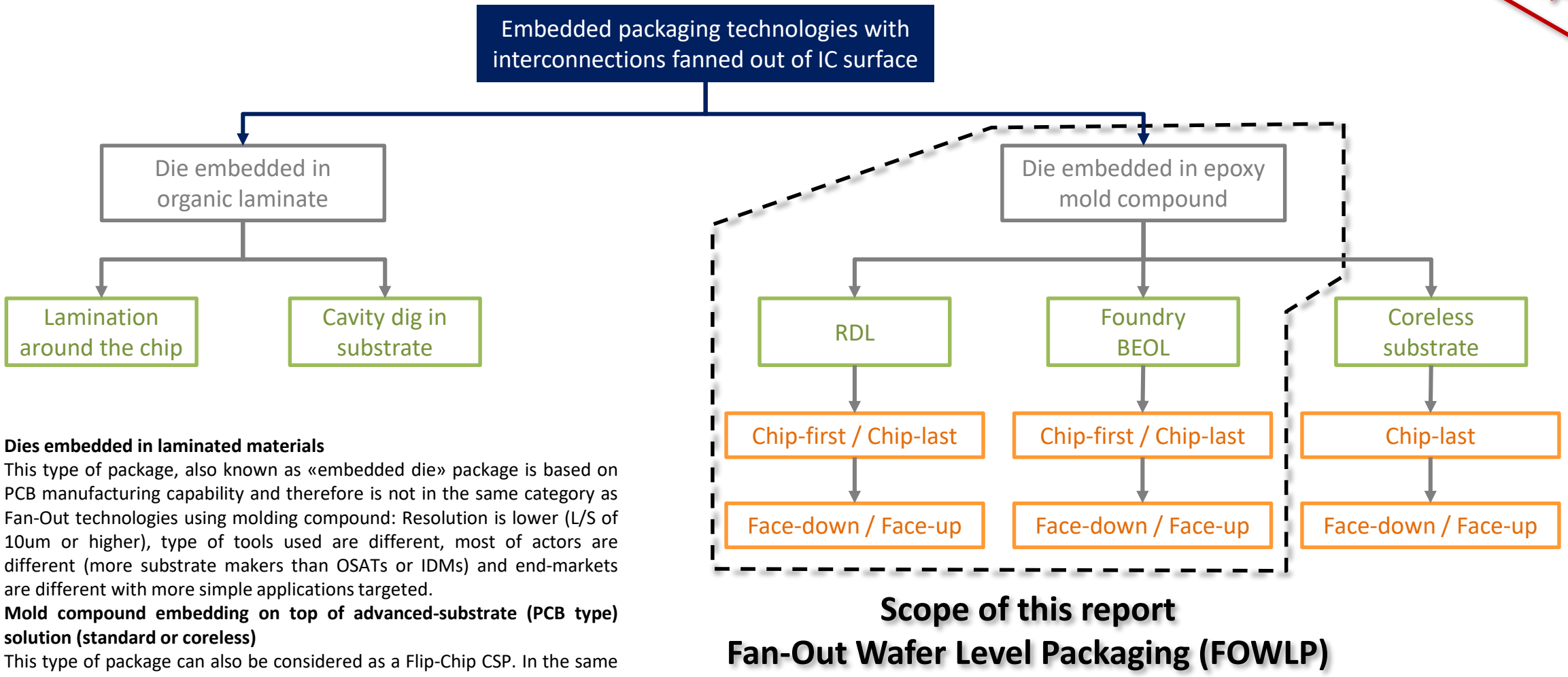
INTRODUCTION
Scope of the report (1/2)



Dies embedded in laminated materials
This type of package, also known as «embedded die» package is based on PCB manufacturing capability and therefore is not in the same category as Fan-Out technologies using molding compound: Resolution is lower (L/S of 10um or higher), type of tools used are different, most of actors are different (more substrate makers than OSATs or IDMs) and end-markets are different with more simple applications targeted.

Mold compound embedding on top of advanced-substrate (PCB type) solution (standard or coreless)
This type of package can also be considered as a Flip-Chip CSP. In the same way as dies embedded in laminated materials, Knowmade is not focusing this report on this type of technology because the resolution achieved and the end-markets targeted are different.

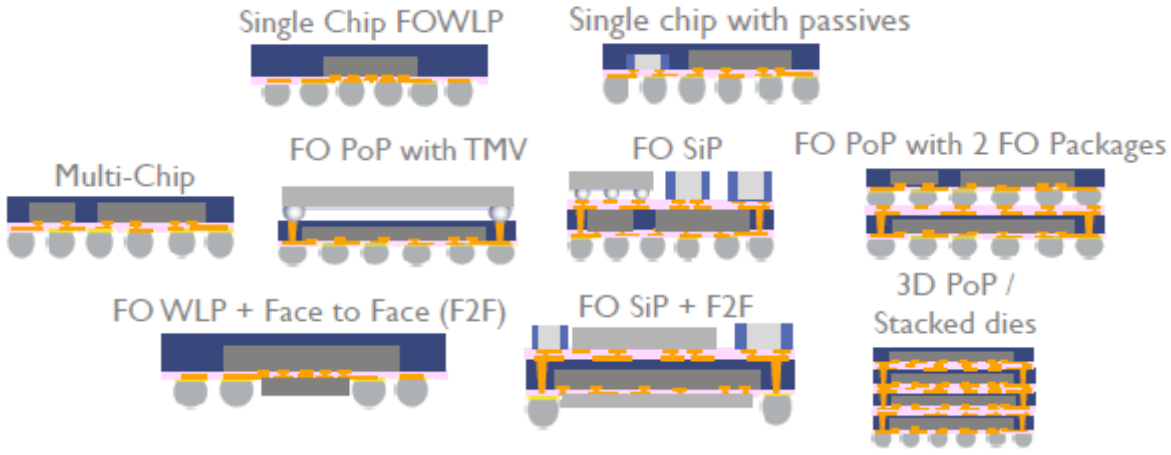
INTRODUCTION
Scope of the report (2/2)

- This report provides a detailed picture of the patent landscape for **Fan-Out wafer level packaging** (FOWLP). All patents related to Fan-Out packaging were considered: chip-first, chip-last, face-down, face-up, single chip, multi-chip module, system-in-package (SiP), package-on-package (PoP), face-to-face package (F2F), stacked dies …
- This report covers **patents published worldwide** up to **September 2016**. We have selected and analyzed more than **3,160 patents and patent applications** grouped in more than **1,260 patent families** relevant to the scope of this report.

Included in the report

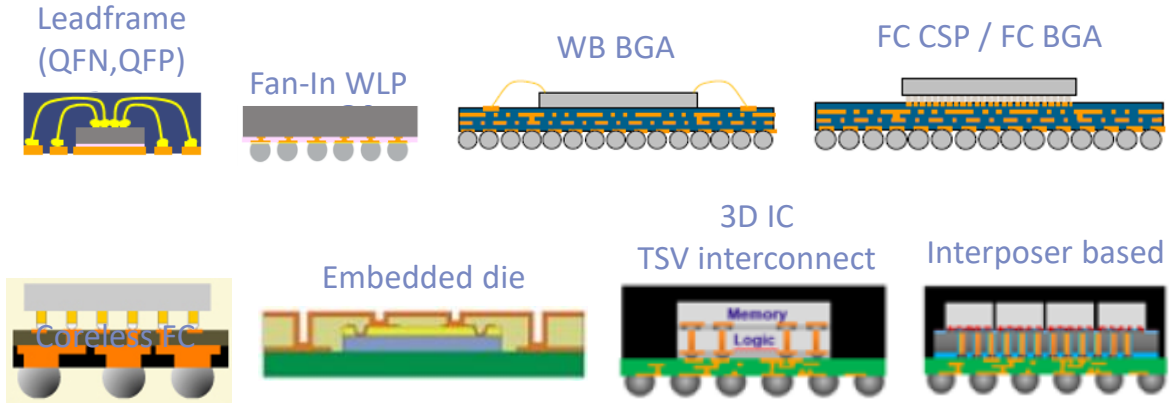
- *Patents related to "Fan-Out" solutions that are embedding dies in a mold compound and are not using laminated advanced substrate for the redistribution layers (RDL).*

eWLB (Infineon, Nanium, STATS ChipPAC, ASE …), **RCP** (Freescale/NXP, Nepes …), **InFO** (TSMC**), SWIFT** & **SLIM** (Amkore), **NTI/SLIT** (SPIL/Xilinx), **M-Series** (Deca, ASE), **CHIEFS** & **CLIP** (PTI), **WDoD** (3D PLUS), etc…



Not included in the report

- *Patents related to "Fan-Out" solutions that are embedding dies in laminated materials.*
- *Patents related to "Fan-Out" solutions where the mold compound embedding is on the top of advanced-substrate (PCB type), standard or coreless.*
- *Patent related to "Fan-Out" solutions that are using other design of package.*



INTRODUCTION

Key features of the report (1/2)

- The report provides **essential patent data** for **Fan-Out wafer level packaging** (chip-first, chip-last, face-down, face-up, single chip, multi-chip module, SiP, PoP, etc…).

- It provides **in-depth patent analyses** of **key technologies** and **key players** including:
  - **IP trends** including time evolutions and countries of patent filings.
  - Current **legal status** of patents.
  - **Ranking** of main patent applicants.
  - **IP collaborations**, joint developments and licensing agreements.
  - **IP position** of key players and **relative strength** of their patent portfolios.
  - **Segmentation** of patents by **technology solution** (chip-first/face-down, chip-first/face-up, chip-last), **process steps** (die placement, molding, planarization, RDL …), **architecture** (multi-chip module, PoP, SiP, face-to-face package …), **technical challenge** (warpage, die shift).
  - Matrix showing patent applicants and their **patented technologies**.
  - Technical solutions found in patents for **warpage** and **die-shift** issues.

- The "Fan-Out" **IP profiles of 18 key companies** is presented, including countries of filings, legal status of patents, patented technologies, prior-art strength index, IP blocking potential, partnerships and IP strategy: *Infineon, NXP/Freescale, STATS ChipPAC, TSMC, ASE, Deca Technologies, Nepes, Nanium, SPIL, Amkor, Powertech Technology, Intel, STMicroelectronics, Samsung, NCAP, WiLAN, 3D PLUS, Apple*

INTRODUCTION

Key features of the report (2/2)

- The report also provides an extensive **Excel database** with **all patents** analyzed in the report (3,100+ patents), including technology segmentation.

- This **useful patent database** allows multi-criteria searches, including:
  - Patent publication number
  - Hyperlinks to the original documents
  - Priority date
  - Title
  - Abstract
  - Patent assignees
  - Technical segmentation (chip-first/face-down, chip-first/face-up, chip-last, die placement, molding, planarization, RDL … multi-chip module, PoP, SiP, face-to-face package … warpage, die shift).
  - Legal status for each member of the patent family

- Disclaimer: This report **does not provide** any insight analyses or counsel regarding **legal aspects** or the **validity** of any individual patent. KNOWMADE is a research firm that provides technical analysis and technical opinions. KNOWMADE is not a law firm. The research, technical analysis and/or work proposed or provided by KNOWMADE and contained herein is not a legal opinion and should not be construed as such.

INTRODUCTION

Objectives of the report

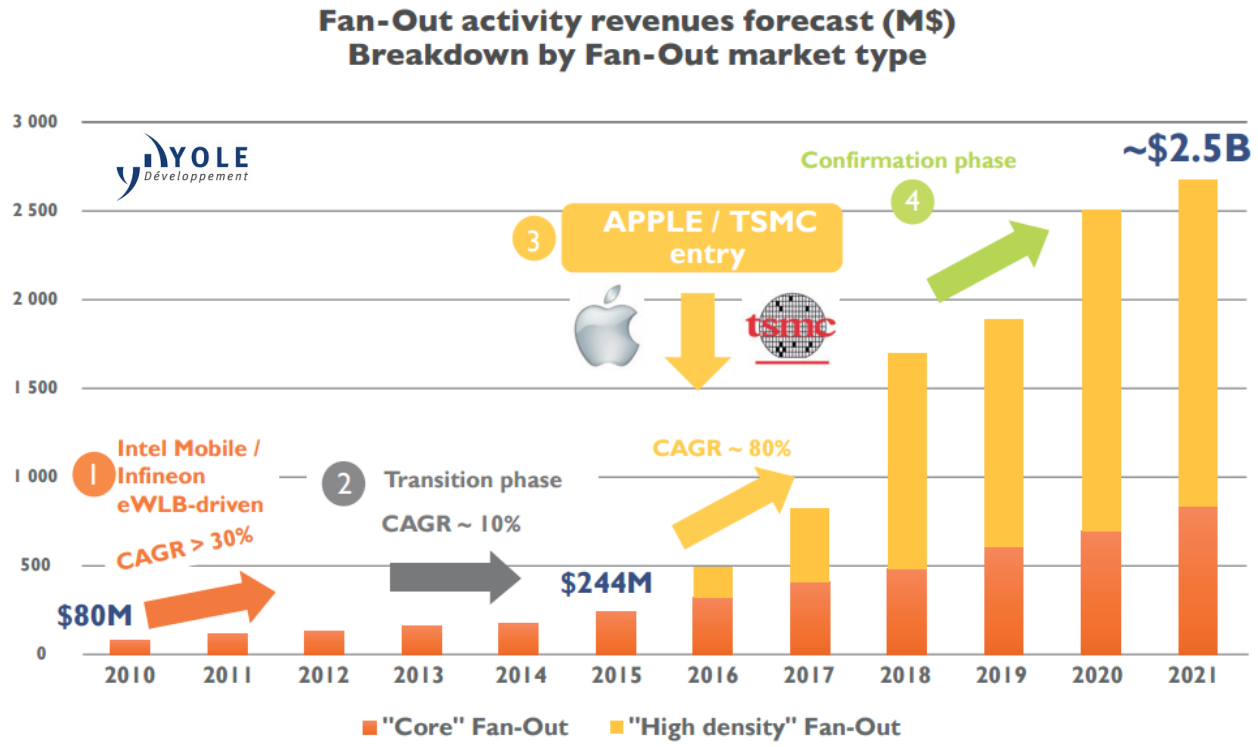
Understand the competitive environment from technology and patent perspective

- ✓ Understand technology & market from a patent perspective.
- ✓ Understand the patent landscape.
- ✓ Identify risks & opportunities.
- ✓ Comprehend key trends in IP and technology development.
- ✓ List the major players and the relative strength of their patent portfolio.
- ✓ Name new players.
- ✓ Identify IP collaboration networks between key players (industrial and academic).
- ✓ Position key players within the value chain and understand their strategic decisions.
- ✓ Understand the competitive landscape, your current and future competitors.
- ✓ Understand your competitors' strategic direction and future product offerings.
- ✓ Determine your competitors' strengths and weaknesses.
- ✓ Identify current legal status of patented technologies.
- ✓ Identify key patents by assignees and technology.
- ✓ Identify blocking and valuable patents.
- ✓ Overview of past and current litigations and licensing agreements.
- ✓ Avoid patent infringement.
- ✓ Appreciate the link between the patent landscape and market evolutions.
- ✓ Discover new markets & technology directions.
- ✓ Identify untapped areas and opportunities to direct R&D and patenting activity.

MARKET TRENDS (1/2)

Fan-Out wafer level packaging (FOWLP) began volume commercialization in 2009/2010 with initial push by Intel Mobile. Start was promising but limited to a narrow range of applications – essentially single die packages for cell phone baseband chips – and few customers. Later on, in 2012, big fab-less wireless/mobile players started slowly to require volume production after qualifying the technology for larger scope of applications including RF, Audio Codec, PMIC/PMU and more … And this growth was confirmed among time with a market size of around **US$244 million in 2015** (“Fan-out: Technology & Market Trends 2016” report, Yole Développement, August 2016).

2016 is a turning point for the Fan-Out market since **Apple** and **TSMC** changed the game and may create a trend of acceptance of Fan-Out packages. Today, with **Apple** and its A10 processor using the **InFO-PoP** technology of **TSMC**, the market explodes. According to Yole Développement, the fan-out activity revenues forecast should reach about **US$2.5billion in 2021**, with 80% growth between 2015 and 2017. The Apple getting involved will clearly bring more and more interest to the fan-out platform. Following high volume adoption of InFO and further development of eWLB technology, a wave of new players and FOWLP technologies may enter the market.



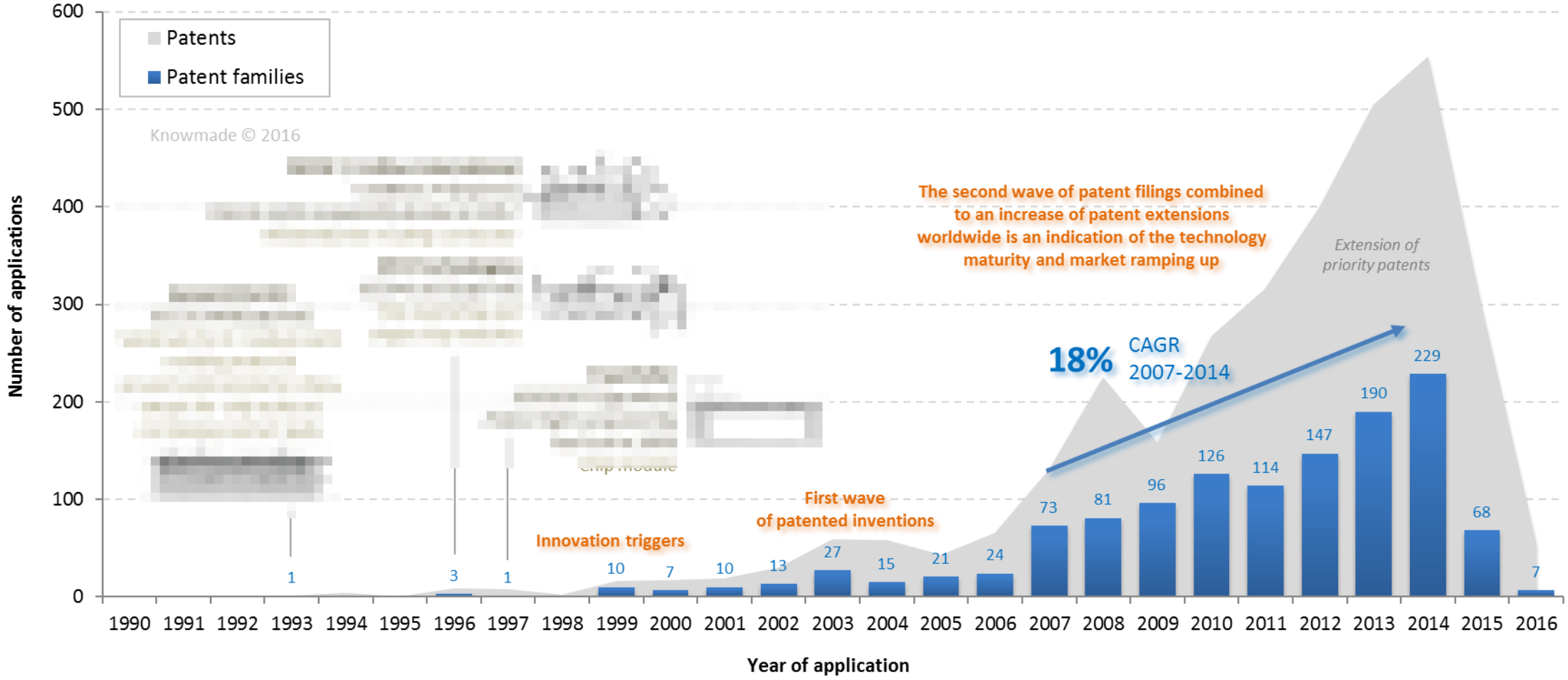
Source: Yole Développement (“Fan-out: Technology & Market Trends 2016” report, August 2016)

PATENT LANDSCAPE OVERVIEW

Time evolution of patent applications for FOWLP

Patent activity in the field of fan-out wafer level packaging

3,160+ patents (1,260+ patent families*), including 1,600+ granted patents and 1,200+ pending patent applications



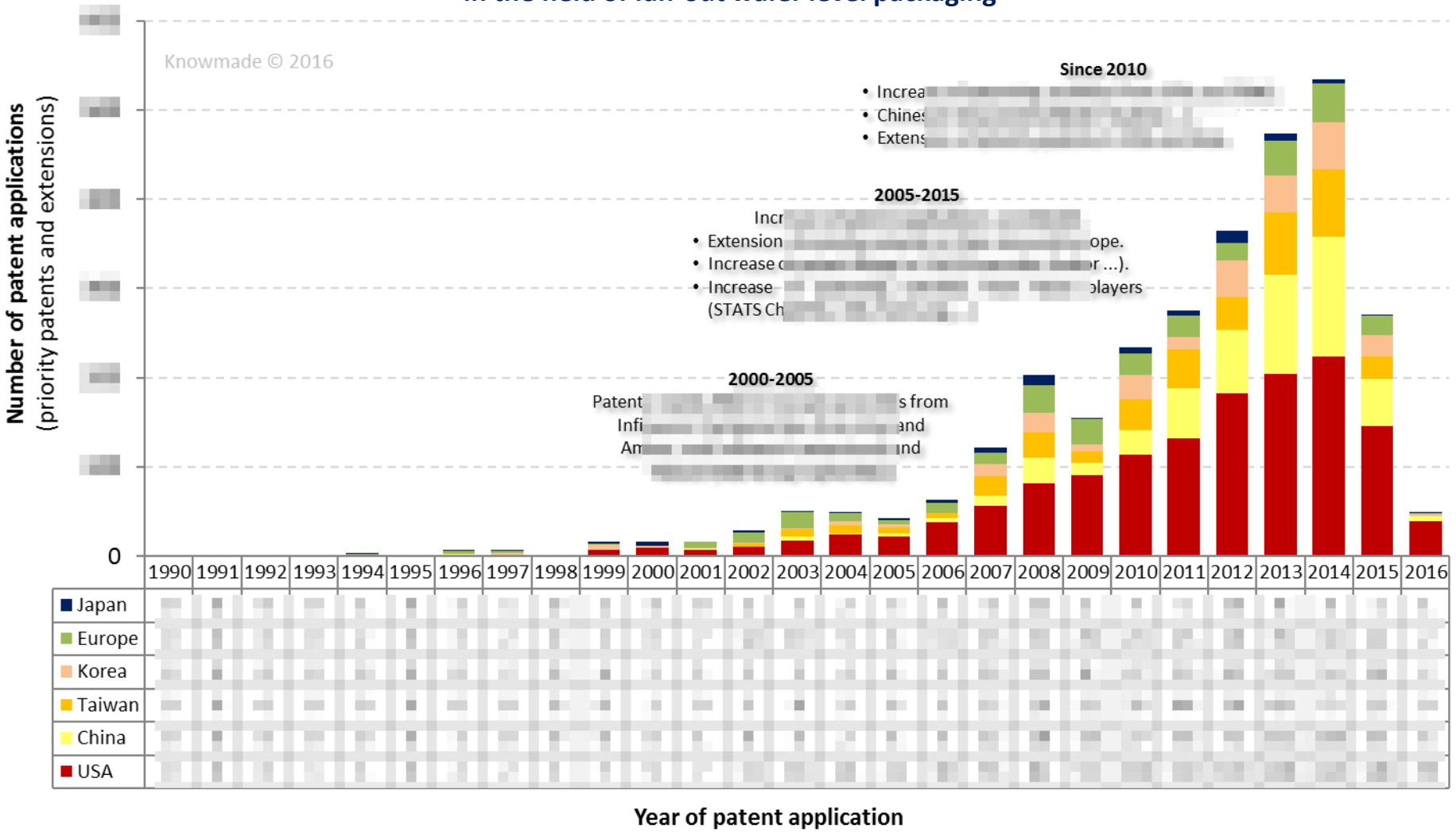
* *A patent family is a set of patents filed in multiple countries by a common inventor(s) to protect a single invention.*

Note: Due to the delay between the filing of patents and the publications by patent offices, usually 18 months, the data corresponding to the year 2015 and 2016 may not be complete since most patents filed during these years are not published yet.

PATENT LANDSCAPE OVERVIEW

Time evolution of patent applications split by countries

Time evolution of countries of patent filings in the field of fan-out wafer level packaging



- The **USA** is the **first country** of patent filings since the beginning of patenting activity in FOWLP field.
- **Decrease** of the share of **European** filings since mid-2000s.
- **Increase** of patent filings in **Asia** since 2010, especially in China.

Note: Europe includes patents filed in European countries and patents for which the European procedure was the filed document (EP patents). The European applications (EP patents) may hide countries that are not yet published.

PATENT LANDSCAPE OVERVIEW

Main patent applicants for FOWLP

Ranking of main patent applicants involved in fan-out wafer level packaging
(according to the number of their patent families*)

- **100+ play**
- The **top-3**
- The **main**
  NCAP, Nep
- **Nanium** d
- **R&D Labs**
- Note the p

** A patent family is a set of patents filed in multiple countries by a common inventor(s) to protect a single invention.*

Industrials
R&D Labs
Patent licensing companies

Other patent applicants: Ava
logies, ITRI, Medtroni
ix, Texas Instrument
, Unimicron, Camtek,
Semiconductor, Gene
oundries, Hitachi
ed Products, Micro
ng Technologies, Phil
es, Sharp, Sony, Xenc
s), Xilinx, Xintec ...

PATENT LANDSCAPE OVERVIEW

Time evolution of main patent assignees involved in FOWLP

* *A patent family is a set of patents filed in multiple countries by a common inventor(s) to protect a single invention.*

Note: Due to the delay between the filing of patents and the publications by patent offices, usually 18 months, the data corresponding to the year 2015 and 2016 may not be complete since most patents filed during these years are not published yet.

First year of application (the numbers represent the number of patent families*)

Patent Assignees	Number of Patent Families	Average Age of Patent Families	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016
Polaris Innovations (WiLAN)							1		5	2	2	1	1											
											1	3		3	1										
					1					1						1	2		1					
													1	2	2				1					
											1		1		1	1	2		2					
								2		2	6	5	3	2	5	3	16	10	10	2	5	1	1	
															6	10				2	1			
							3		1	1		2	3	1	8	8	6	5	2	4	2	3	4	
											1	1		1	1				1				2	
							1	1			2		1	3	8	2	1	1	1	5	5	4		
									4	2	9		2	4	15	22	17	16	4	22	24	7		
				1			4			1			4	1	1	6	7	12	9	16	12	14	2	
																1	7	6	4	4	1	2		
													1		7	12	23	40	28	10	21	12	4	1
														7	6	10	9	5	8	8	22	22	1	
																	3		1	2	1		1	
															2			4	4	6	8	4		
											4		2	2	4			15	1	14	30	31	1	
																			6	8		2	2	
															1					1	1		2	
										1						1				1		5	4	
										1		1			1			2	18	23	45	69	8	
																	1	1				1	2	1
											1									3		9	3	1
																		1	1	1	3	1	5	
																				1		7		
Apple	9	2																			1	5	3	
NCAP	31	2																			2	17	12	
SMIC	5	1																					4	1

Pat[redacted]aris and
Nor[redacted] in 2015
fr[redacted]on and
[redacted]vely

[redacted]

pa[redacted]ars

Newcomers in the patent landscape

PATENT LANDSCAPE OVERVIEW

Number of patents and corresponding legal status for main patent assignees in FOWLP field

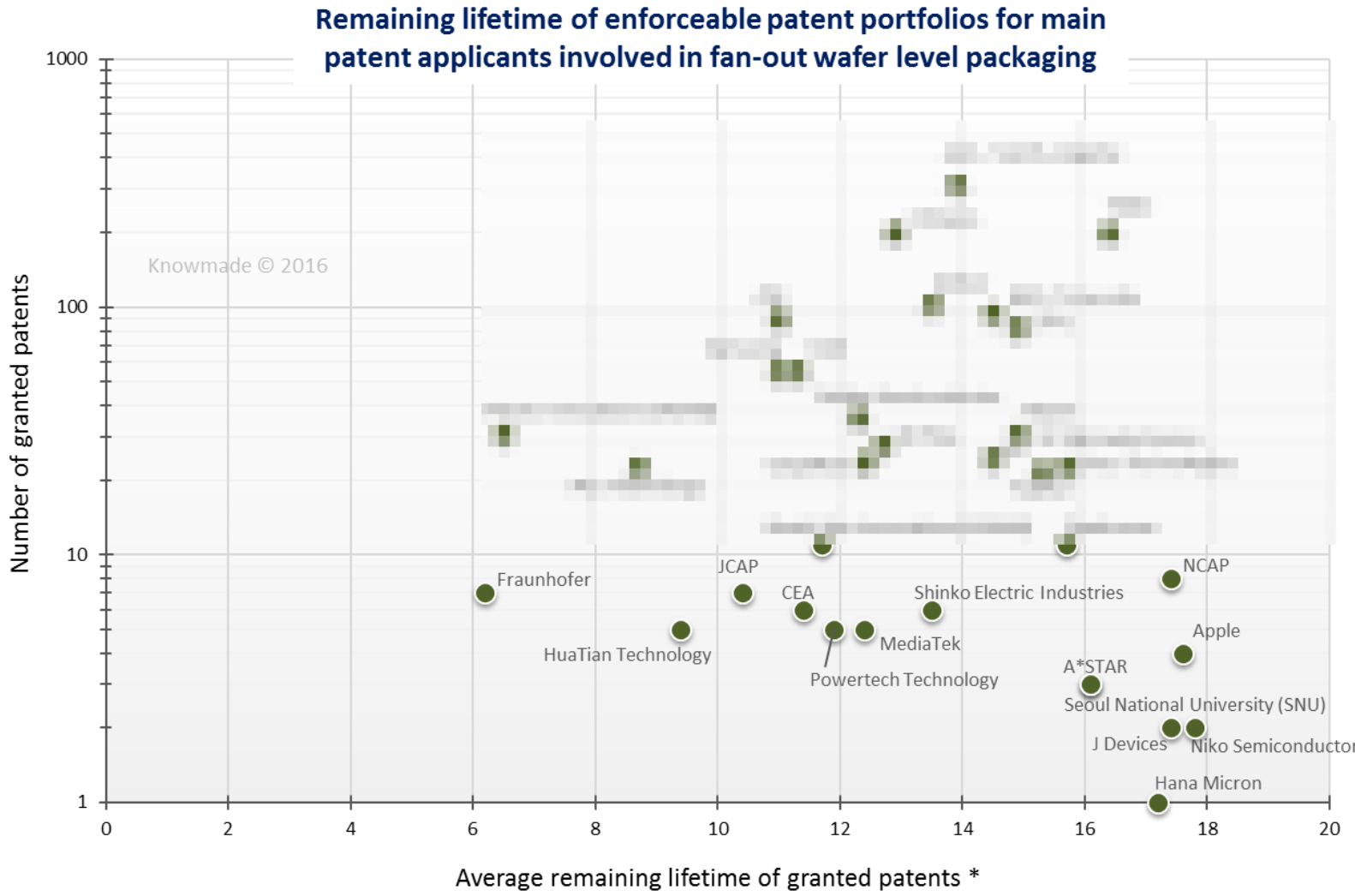
Patent Assignees	FOWLP patent porfolio					
	Number of Patent Families	Patents	Granted patents	Pending patent applications	Expired patents	Rejected or abandoned patents
[redacted]	[redacted]	499	203	288	0	8
[redacted]	[redacted]	560	316	221	0	23
[redacted]	[redacted]	408	203	167	0	38
[redacted]	[redacted]	234	84	130	0	20
[redacted]	[redacted]	152	96	34	0	22
[redacted]	[redacted]	150	104	23	5	18
[redacted]	[redacted]	126	91	10	0	25
[redacted]	[redacted]	117	56	28	0	33
[redacted]	[redacted]	130	56	57	0	17
[redacted]	[redacted]	32	8	24	0	0
[redacted]	[redacted]	55	31	16	0	8
[redacted]	[redacted]	35	25	5	0	5
[redacted]	[redacted]	38	24	7	0	7
[redacted]	[redacted]	29	22	5	0	2
[redacted]	[redacted]	22	5	17	0	0
[redacted]	[redacted]	49	23	24	0	2
[redacted]	[redacted]	37	31	3	0	3
[redacted]	[redacted]	29	11	17	0	1
[redacted]	[redacted]	17	4	13	0	0
[redacted]	[redacted]	52	23	5	0	24
[redacted]	[redacted]	43	28	14	0	1
[redacted]	[redacted]	20	2	18	0	0
[redacted]	[redacted]	8	7	1	0	0
[redacted]	[redacted]	52	36	5	0	11
[redacted]	[redacted]	19	5	14	0	0
[redacted]	[redacted]	14	11	0	0	3
[redacted]	[redacted]	13	7	2	0	4
[redacted]	[redacted]	8	5	2	0	1
[redacted]	[redacted]	5	0	5	0	0

A patent family is a set of patents filed in multiple countries to protect a single invention by a common inventor(s). A first application is made in one country – the priority country – and is then extended to other countries.

- [redacted] higher number of [redacted] and it has still a lot [redacted]eline.
- [redacted] [redacted]ivity more recently, [redacted] number of granted [redacted]
- [redacted] [redacted]d-2000s and it has [redacted] [redacted]since 2010, resulting [redacted]ge (mainly in China [redacted]
- [redacted] [redacted] have a noticeable [redacted] [redacted]cations which are [redacted]atent office.

PATENT LANDSCAPE OVERVIEW

Remaining lifetime of granted patents for main patent assignees in FOWLP field



- [illegible] have the best [illegible] ne a **large** [illegible] 00+ and 300+ [illegible] with **a long** [illegible] anted patents [illegible] respectively).
- [illegible] ceable patents [illegible] **vations** from [illegible] ars on average, [illegible] atent licensing [illegible] before their

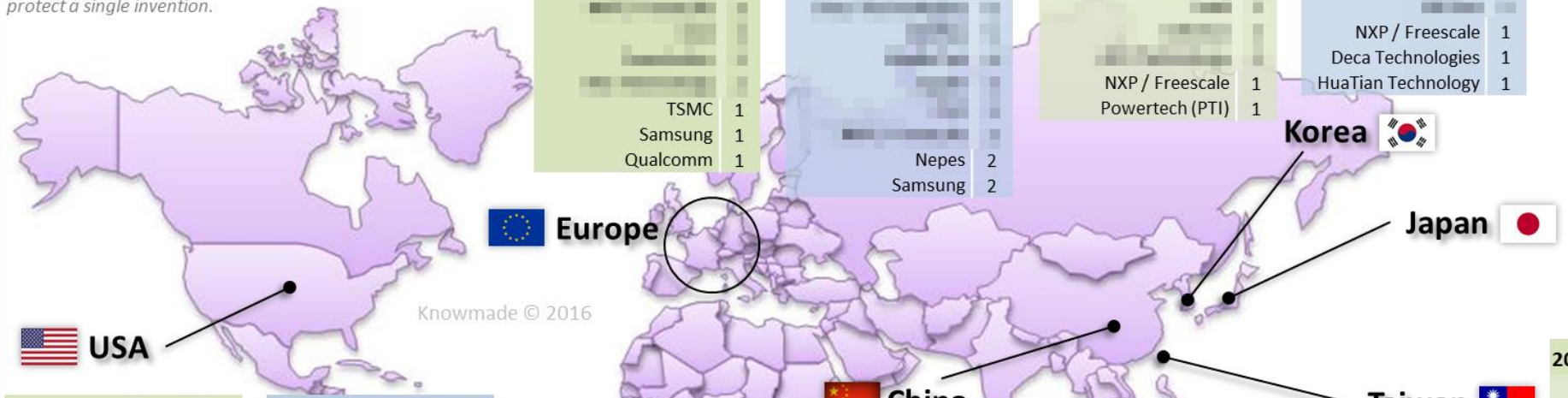
** The remaining lifetime is based on the expected expiration date. The lifetime of a patent is typically limited at 20-years, calculated from the filing date, as long as the maintenance fees are paid. The expected expiration date is dependent on the accuracy and timeliness of the information provided by the patent offices.*

PATENT LANDSCAPE OVERVIEW

Geographic map of granted patents and pending patent applications in FOWLP field

Number of patent families* containing **pending patent applications** or **granted patents** in the corresponding country.

** A patent family is a set of patents filed in multiple countries by a common inventor(s) to protect a single invention.*



80+ GRANTED PATENTS

TSMC	1
Samsung	1
Qualcomm	1

190+ PENDING PATENTS

Nepes	2
Samsung	2

140+ GRANTED PATENTS

NXP / Freescale	1
Powertech (PTI)	1

70+ PENDING PATENTS

NXP / Freescale	1
Deca Technologies	1
HuaTian Technology	1

25+ GRANTED PATENTS

Renesas / NEC	1
Toshiba	1
Oerlikon Balzers	1

20+ PENDING PATENTS

Murata Electronics	1
Hitachi Chemical	1

630+ GRANTED PATENTS

SPIL	17
Polaris (WiLAN)	12

360+ PENDING PATENTS

Nepes	6
Deca Technologies	5

165+ GRANTED PATENTS

JCAP	7
NXP/Freescale	6

300+ PENDING PATENTS

Nepes	6
SMIC	5

35+ GRANTED PATENTS

A*STAR	1

60+ PENDING PATENTS

A*STAR	1
Camtek	1

200+ GRANTED PATENTS

Nepes	4
Fujitsu	3

145+ PENDING PATENTS

Qualcomm	2
Apple	2

PATENT LANDSCAPE OVERVIEW

Countries of granted patents and pending patent applications for main patent assignees in FOWLP field

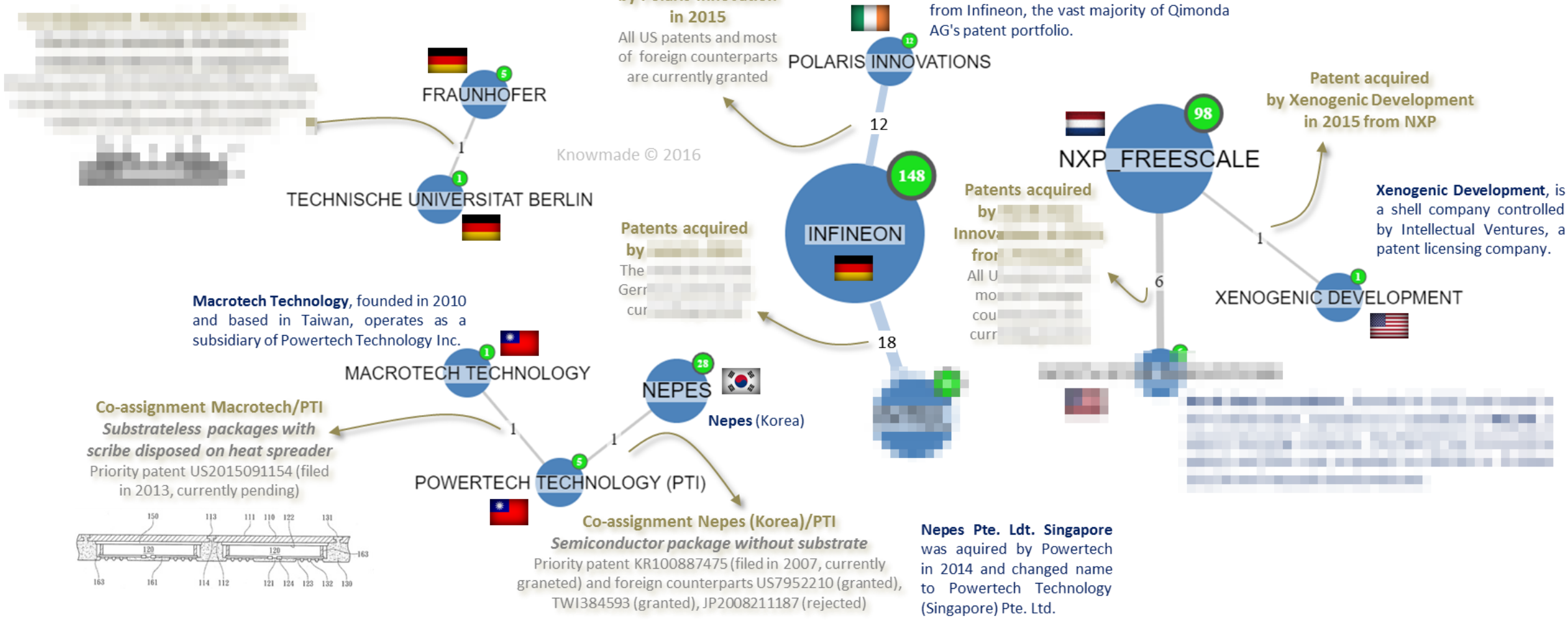
Patent Applicants	Number of patent families	Number of patent families containing granted patents in the corresponding country							Number of patent families containing pending patent applications in the corresponding country							
		USA	Europe	Japan	Korea	China	Taiwan	Singapore	USA	Europe	Japan	Korea	China	Taiwan	Singapore	PCT (WO)
			1	1	28				106	36						
					6				60							
			43		2				36	85						
									34							
			3	2	1				23	2	4					
					45				14	1	1					
									3							
			1	2	18				8	2						
			11	1	2				20	14	4					
									1							
					22				6	2						
									4							
									3							
				6					2							
										1						
									5	6						
			8	2	2	3	2			1						
			1						4	8						
							1		7	4						
			8	4			2			5	3					
			2		2	2	5									
									3	1	5					
						7										
						2	4		1							
MediaTek	6					1	1		4	4						
North Star (WiLAN)	6					2	1									
Fraunhofer	5		2							1						
Powertech Technology	5				1	1	2		1							
SMIC	5															

- [redacted] main patent [redacted] gapore with [redacted] enforceable [redacted]
- [redacted] urrently the [redacted] in terms of [redacted]
- [redacted] **enforceable** [redacted] 50 patented [redacted] the **main** [redacted] ing patent [redacted] **TS ChipPAC** [redacted]
- [redacted] of **granted** [redacted] **USA**, but the [redacted] applications [redacted] on FOWLP [redacted]
- [redacted] a significant [redacted] **Korea**, have [redacted] ent filings in [redacted]
- [redacted] **Tian** have a [redacted] **patents in** [redacted]
- [redacted] **Innovations** [redacted] quired from [redacted] **forceable in** [redacted]

PATENT LANDSCAPE OVERVIEW

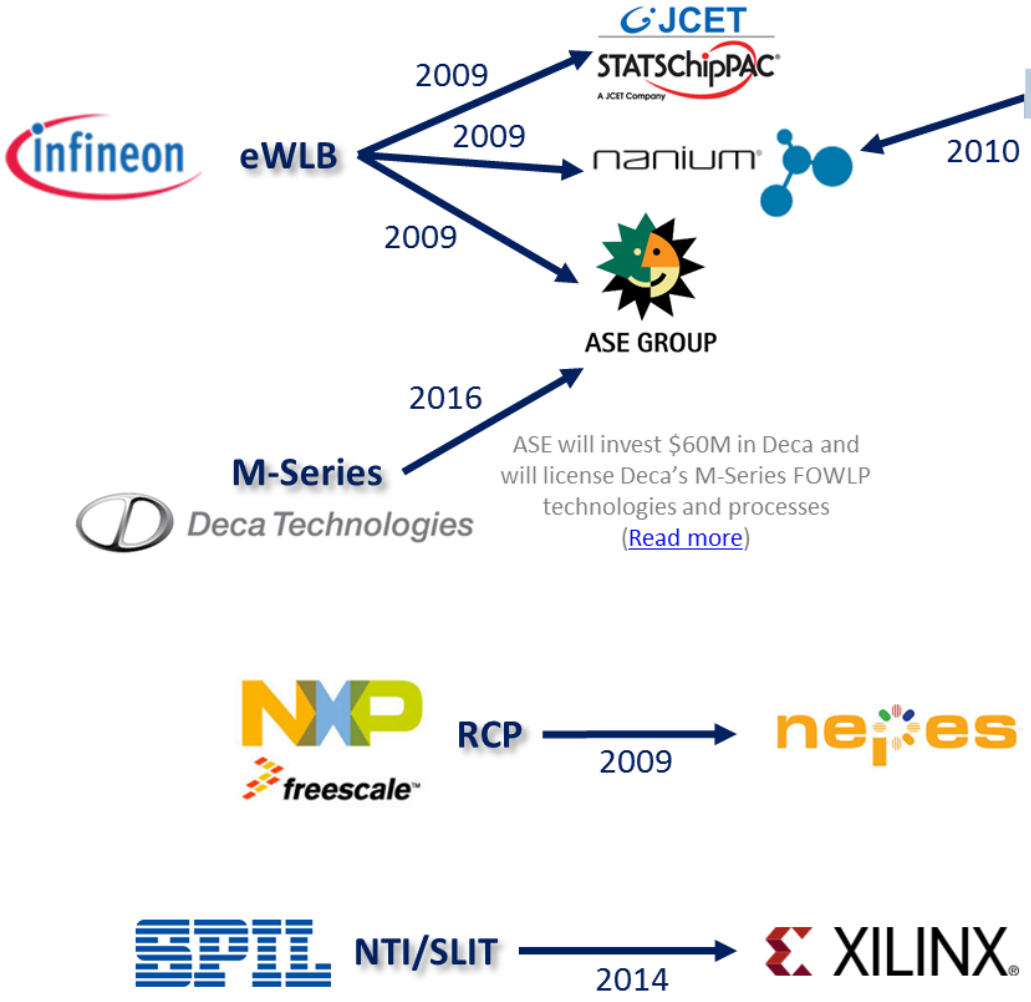
IP collaboration network in FOWLP field

- Number in black on each link between patent assignees is the **number of co-assigned patent families** in the data set of the study.
- Number up right to each bubble is the number of patent families for this applicant in the data set of the study. Bubble size is proportional to the number of patent families selected for the study.



PATENT LANDSCAPE OVERVIEW

Licensing agreements



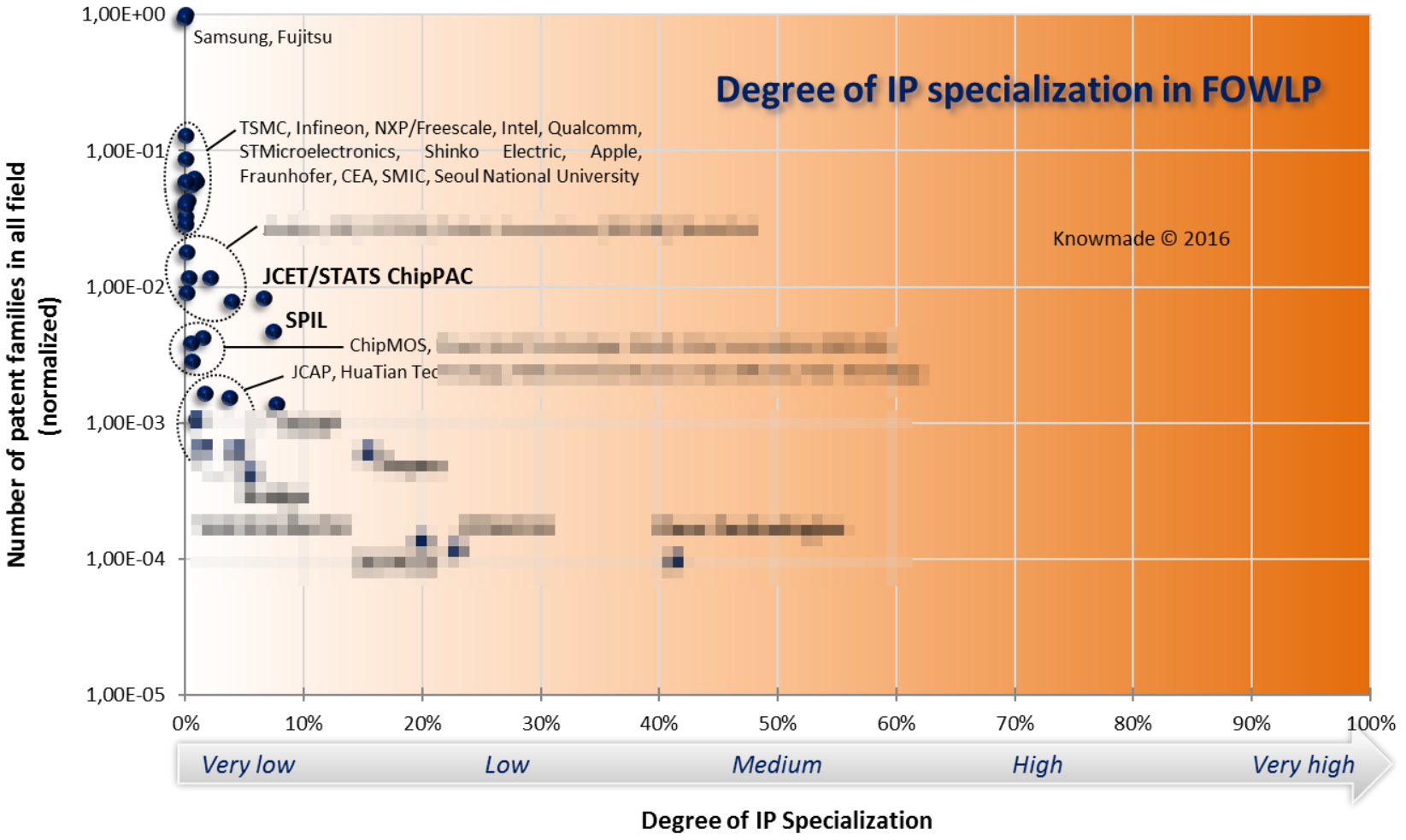
PATENT LANDSCAPE OVERVIEW

Most cited patents in FOWLP field

Patent number	Patent assignee	Title	PDF	Current legal status	Number of forward citations	Application date (YYYY-MM-DD)	Age from application date (Year)	Average number of forward citations / Year
[redacted]498	[redacted]tric (patent ri[redacted] by Lockheed [redacted]94)	Meth[redacted]	Open	Expired	724	[redacted]7-09	23.3	31.1
[redacted]193	E[redacted]ogies	Single [redacted]ion thereof	Open	Expired	457	[redacted]5-20	20.4	22.4
[redacted]469	[redacted]	Direct [redacted]	Open	Granted	345	[redacted]1-12	16.9	20.4
[redacted]033	[redacted]tric (patent ri[redacted] by Lockheed [redacted]94)	Embe[redacted]	Open	Expired	369	[redacted]5-20	22.3	16.5
[redacted]938	Sa[redacted]ronics	Wafe[redacted]	Open	Granted	235	[redacted]7-18	14.2	16.5
[redacted]303	[redacted]PAC	Meth[redacted]re	Open	Granted	103	[redacted]5-09	7.3	14.0
[redacted]389	[redacted]XP (patent ri[redacted] by North Star In[redacted]2015)	Electr[redacted]	Open	Granted	114	[redacted]2-20	8.8	12.9
[redacted]034	[redacted]PAC	Semic[redacted]re using stud bump	Open	Granted	94	[redacted]5-26	7.3	12.9
[redacted]767	E[redacted]ogies	Single [redacted]ion thereof	Open	Expired	202	[redacted]5-29	18.3	11.0
[redacted]374	[redacted]o	Semic[redacted]s for stacking and m[redacted]	Open	Granted	67	[redacted]4-02	6.5	10.3
U[redacted]54156	[redacted]PAC	Semic[redacted]	Open	Abandoned	52	[redacted]5-29	5.3	9.8
[redacted]936	[redacted]PAC	Semic[redacted]cture for 3-D FO-W[redacted]	Open	Granted	34	[redacted]3-15	3.6	9.5
[redacted]552	Sa[redacted]ronics	Chip [redacted]redistribution substr[redacted]	Open	Granted	151	[redacted]1-12	16.8	9.0
[redacted]975	[redacted]	Flip-cl[redacted]	Open	Granted	68	[redacted]2-12	7.7	8.9
[redacted]295	[redacted]PAC	Semic[redacted]rrier	Open	Granted	61	[redacted]1-10	6.9	8.8
[redacted]065	E[redacted]ogies	Stack[redacted]	Open	Granted	59	[redacted]2-22	6.8	8.7
[redacted]212	[redacted]PAC	Syste[redacted]	Open	Granted	75	[redacted]2-26	8.8	8.5
[redacted]392	[redacted]PAC	Semic[redacted]nd mounting semic[redacted]	Open	Granted	53	[redacted]5-14	6.4	8.3
[redacted]703	Sa[redacted]ronics	Semic[redacted] method of manu[redacted]	Open	Granted	68	[redacted]4-16	8.5	8.0
[redacted]466	[redacted]o	Wafe[redacted]nce shielding	Open	Granted	55	[redacted]1-19	6.9	8.0

IP POSITION OF KEY PLAYERS

Degree of IP specialization in FOWLP field



The degree of IP specialization of a company represents the percentage of patents filed in a specific field over the whole patent portfolio of the company. It is an indicator of the patenting activity on a specific field.

- [illegible] ut with the **[illegible]ialization in** [illegible]s patents are [illegible]el packaging.
- [illegible] nsung, TSMC, [illegible] over a wide [illegible] their patent [illegible] **y low degree**

IP POSITION OF KEY PLAYERS

Prior art strength index

Patent Applicants	Nunmber of patent families on FOWLP	Number of citing patent families			Relative Impact Factor of the patent portfolio (**)			Prior Art Strength Index of the patent portfolio (***)			Main citing player
		All citations	% of internal citations (*) (FOWLP)	% of external citations (*) (out of FOWLP)	R.I.F in all technology fields	R.I.F in FOWLP	R.I.F out of FOWLP	P.A.S.I in all technology fields	P.A.S.I in FOWLP	P.A.S.I out of FOWLP	
		335			0.5	1.1	0.4	81			cs, Intel
		1407			2.1	3.4	1.9	339			s, SPIL
		950			1.5	2.8	1.3	229			escale, Intel, SPIL
		161			0.4	0.8	0.3	39			
		328			0.8	1.6	0.7	79			
		432			1.2	1.9	1.0	104			oadcom
		516			1.7	2.1	1.6	124			Amkor
		714			3.2	2.6	3.4	172			, Tessera
		555			3.8	6.6	3.3	134			
		3			0.0	0.1	0.0	1			
		66			0.6	1.5	0.4	16			
		135			1.3	3.5	0.9	33			ualcomm
		114			1.4	4.2	0.9	27			
		19			0.3	1.0	0.1	5			
		69			1.0	0.8	1.0	17			ectro Mechanics
		55			1.1	4.7	0.4	13			
		226			4.5	5.8	4.3	54			
		33			0.7	0.4	0.7	8			ronics
		2			0.1	0.0	0.1	0			tor
		32			1.0	2.0	0.8	8			E Magnetics, CEA
		237			7.1	18.4	5.1	57			
		1			0.0	0.2	0.0	0			
		10			0.3	0.8	0.2	2			PIL, Mediatek
		211			7.3	5.9	7.5	51			TSMC, Tessera
		72			2.9	3.4	2.8	17			
		123			4.9	7.1	4.5	30			
		67			3.2	4.4	3.0	16			gy, STATS ChipPAC
		7			0.3	0.9	0.2	2			
		0			0.0	0.0	0.0	0			
		21			1.3	2.0	1.1	5			
		52			3.1	2.8	3.2	13			Univ. of Illinois, Fujitsu, Sumitomo Bakelite
CEA	3	9			0.7	2.6	0.4	2			Deca Technologies, Fujitsu, Infineon
Hana Micron	3	2			0.2	0.5	0.1	0			Amkor
Niko Semiconductor	3	0			0.0	0.0	0.0	0			-
Seoul National University (SNU)	3	0			0.0	0.0	0.0	0			-

The **prior art strength index** is based on the number of **different patent families citing the patent portfolio**. It indicates the **impact of the patents on the prior art** compared to other patents.

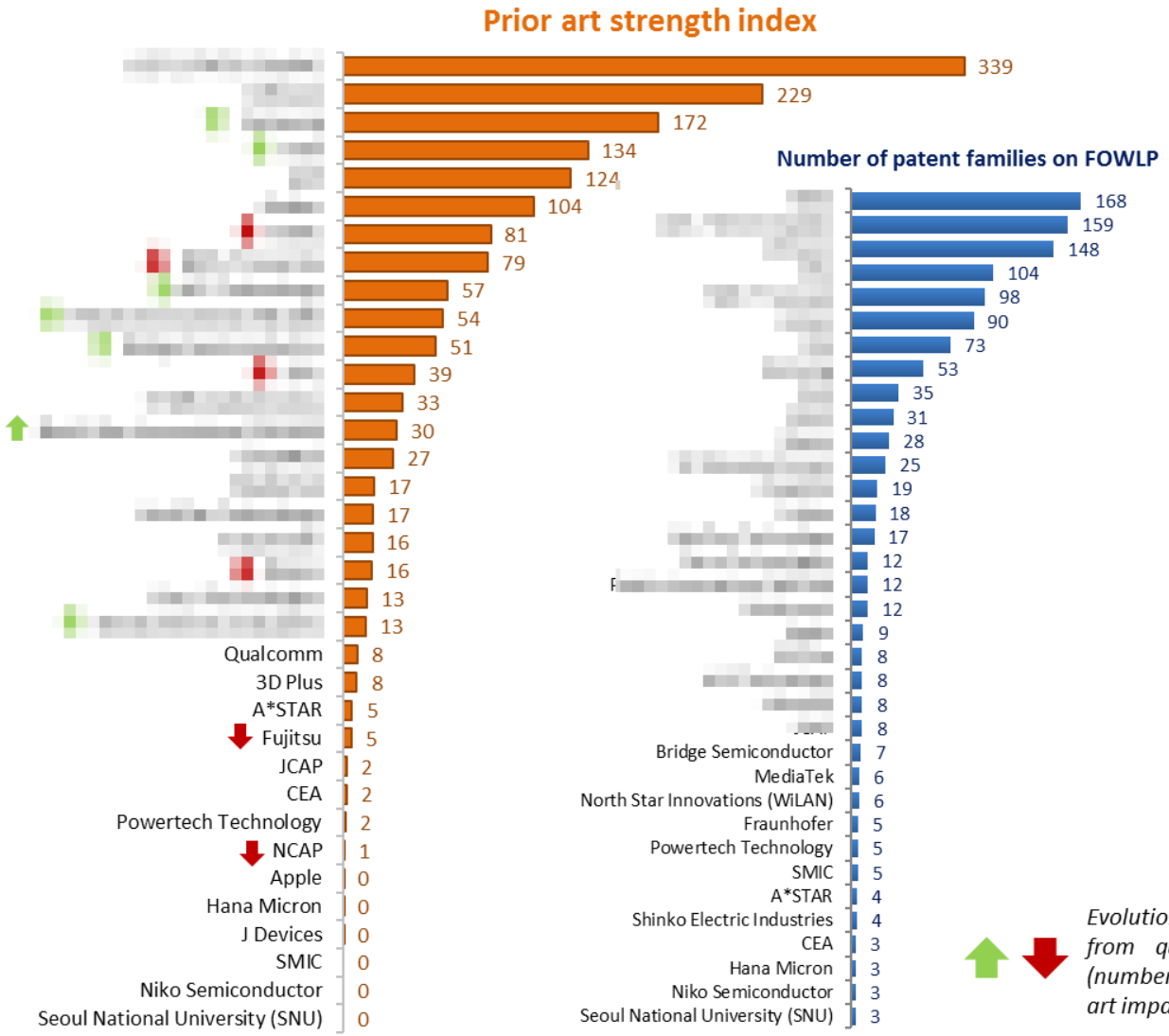
(*) **Internal citations** refer to citations coming from the corpus of patents selected for the study. **External citations** refer to citations coming from patents not selected for the study.

(**) A **relative impact factor** (R.I.F) of 2 indicates that the patent portfolio is cited by two times more different patent families than the average of the corpus selected for the study. In other terms, the patent portfolio has two times more impact than the average.

(***) **Prior Art Strength Index** = Relative Impact Factor multiplied by the number of patent families.

IP POSITION OF KEY PLAYERS

Prior art strength index (citations from all technology fields)



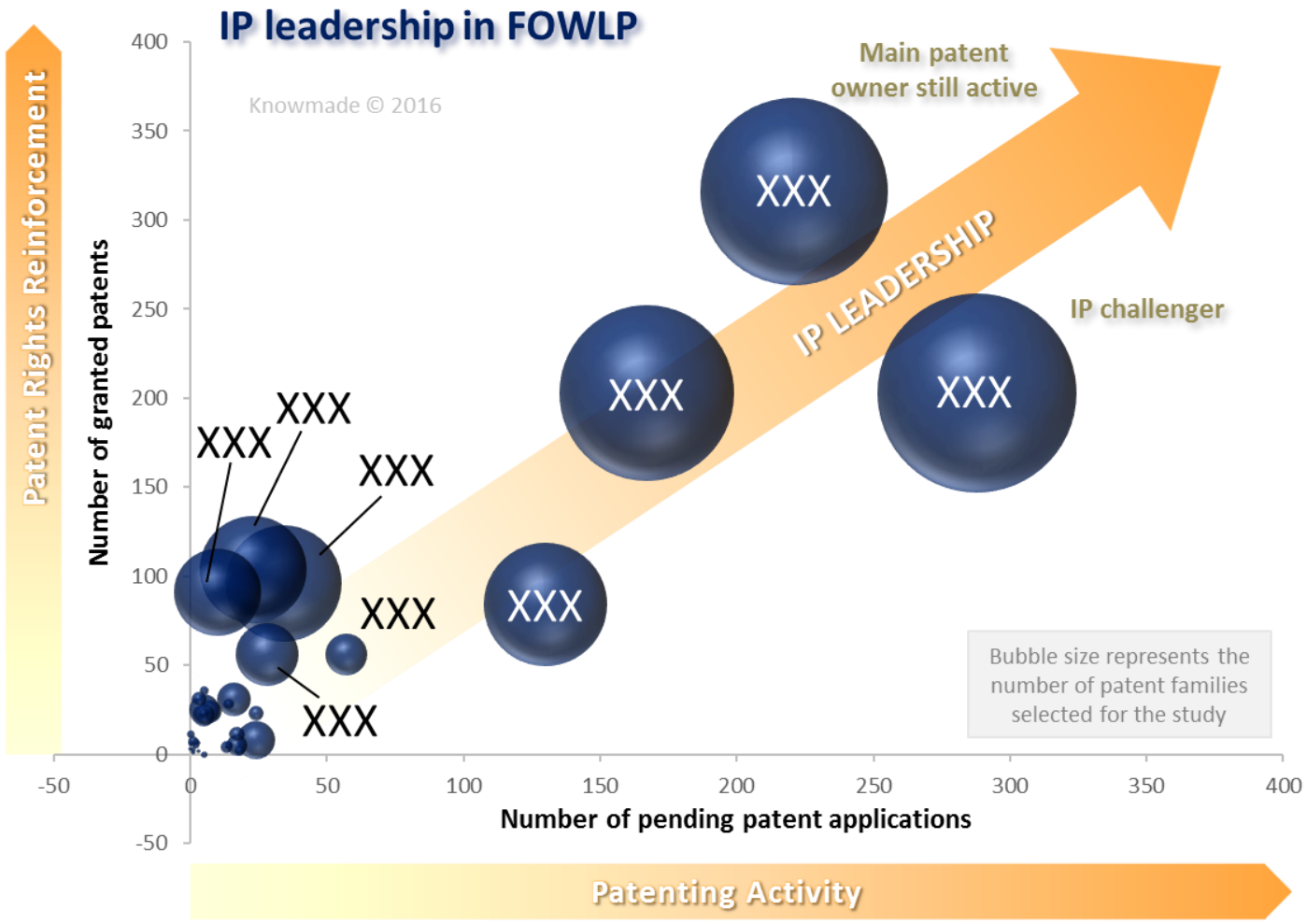
- [redacted] **ortant contribution to the prior** [redacted] **s a large patent portfolio** with [redacted] **ifferent patent families** than the [redacted].
- [redacted] rtfolio sizes (53 and 35 families [redacted] **of the prior art strength index.** [redacted] ifferent patent families than the [redacted]
- [redacted] o IP player of the FOWLP patent [redacted] ut its large patent portfolio has a [redacted] JCET/STATS ChipPAC, Infineon, [redacted]

Evolution of the ranking of IP players from quantitative point of view (number of patent families) to prior art impact (strength index)

$$\text{Prior Art Strength Index} = \left[\text{No. of patent families}\right] \times \left[\frac{\text{citation ratio of patent families}}{\text{citation ratio over all FOWLP patent families}}\right]$$

IP POSITION OF KEY PLAYERS

IP leadership in FOWLP field

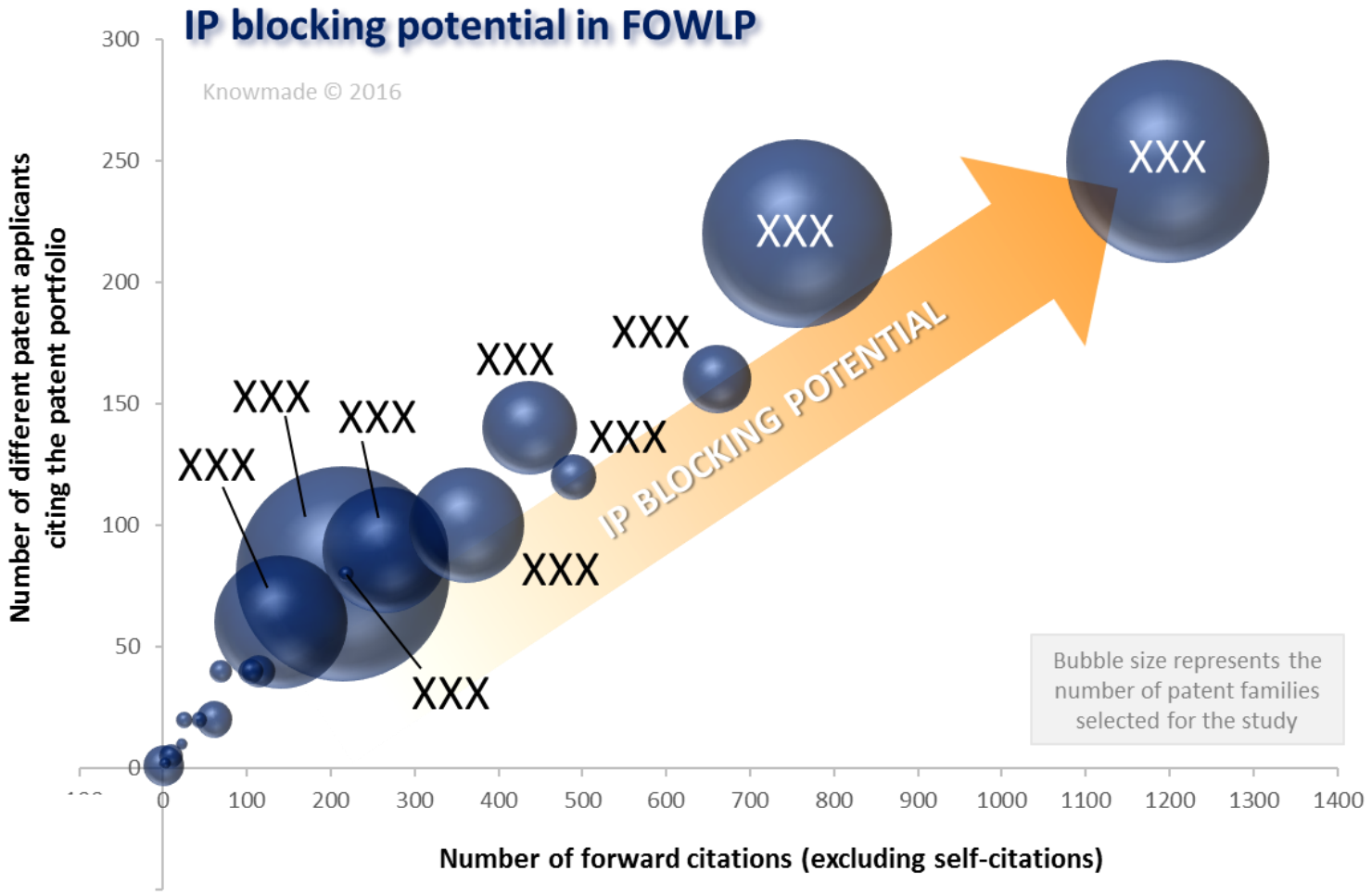


The more the patent applicant combines a high number of granted patents with a high number of pending patent applications, the more its IP leadership is high.

- [redacted] FOWLP patent **high number of** [redacted] **f pending patent**
- [redacted] **allenger** with a [redacted] io and numerous [redacted] **ould reshape the** [redacted] once its patent

IP POSITION OF KEY PLAYERS

IP blocking potential in FOWLP field

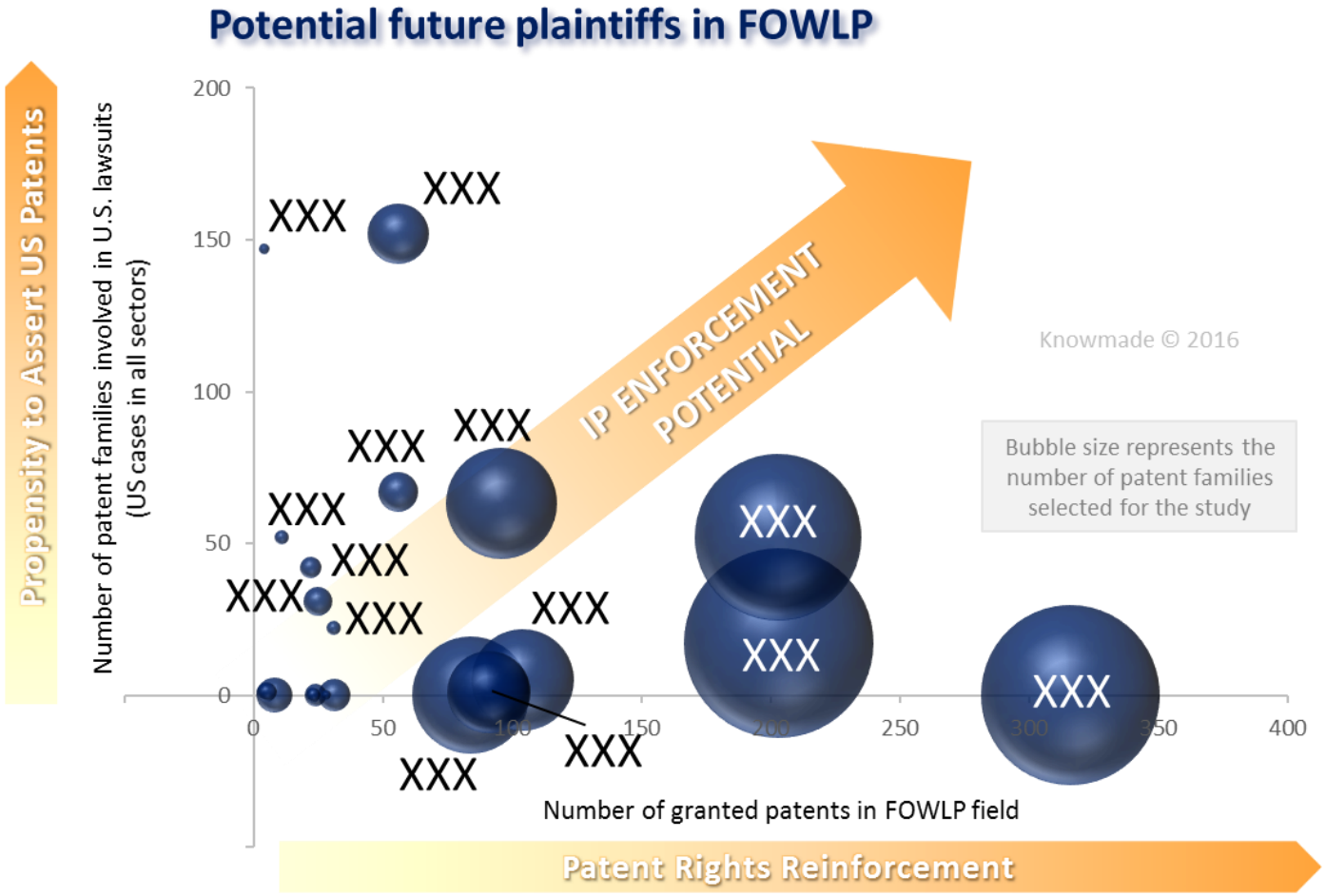


The more the number of forward citations from different patent applicants is high, the more the capacity to hamper the other firms' attempts to patent a related invention is important. Note, however, that the identification of a "blocking patent" requires an in-depth specific analysis of each patents.

higher IP
scape. Its
g received
nt patent
has the
nventions

IP POSITION OF KEY PLAYERS

Potential future plaintiffs in FOWLP field

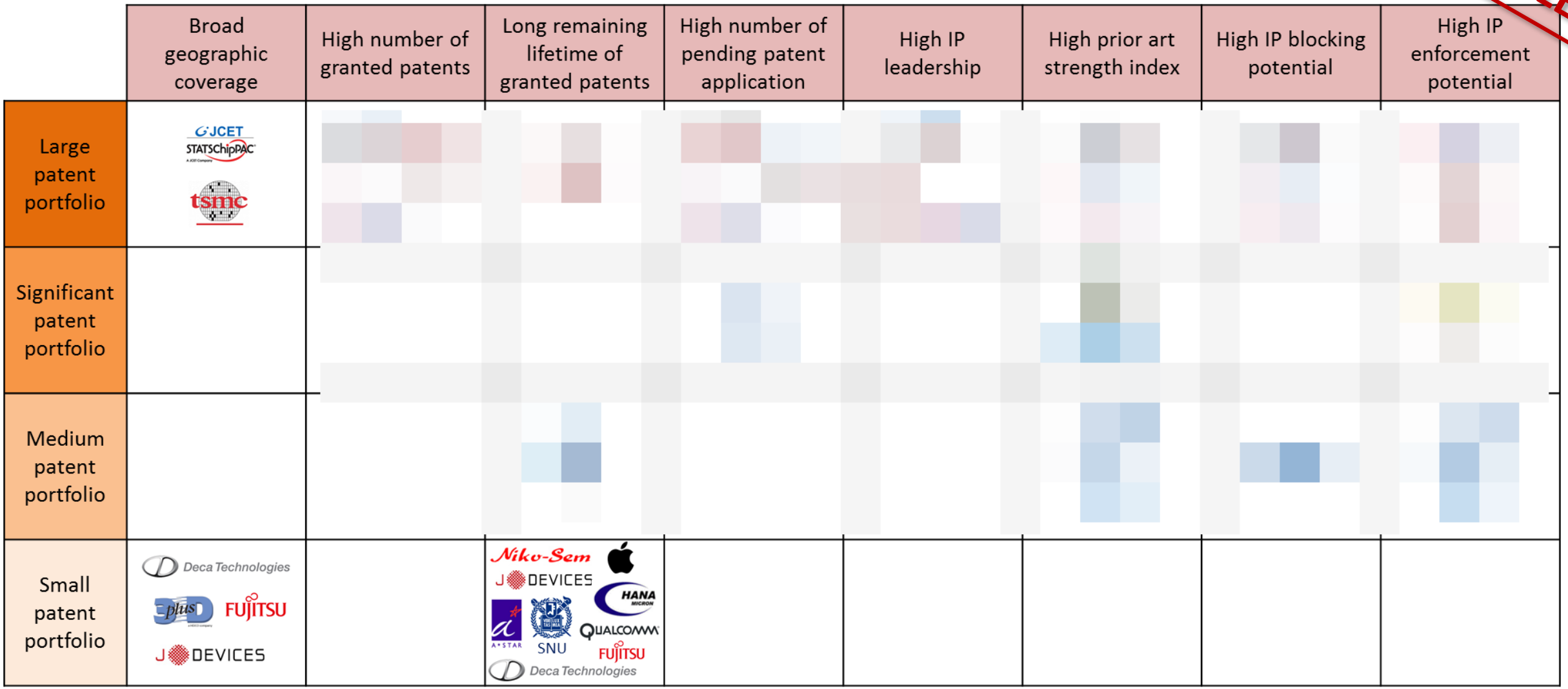


The more the patent applicant combines a high propensity to litigate its US patents (all sectors) with a high number of granted patents on fan-out wafer level packaging, the more its IP enforcement potential in the FOWLP field is high. The more the IP enforcement potential is high, the more the risk to see the patent applicant becoming a future plaintiff in the FOWLP field is important.

- **high IP enforcement** ne a propensity to tors) with a lot of afer level packaging
- ave a **noticeable IP** mbines a noticeable s (all sectors) with a n fan-out wafer level ng 100+ in USA). ate its US patents as umerous enforceable kaging (310+ grants,
- **ement potential**. The nforceable patents in grants, including 20+ sity to litigate its US
- Polaris Innovations quired in 2015 from ears.

IP POSITION OF KEY PLAYERS

The best IP positions in FOWLP patent landscape



IP POSITION OF KEY PLAYERS

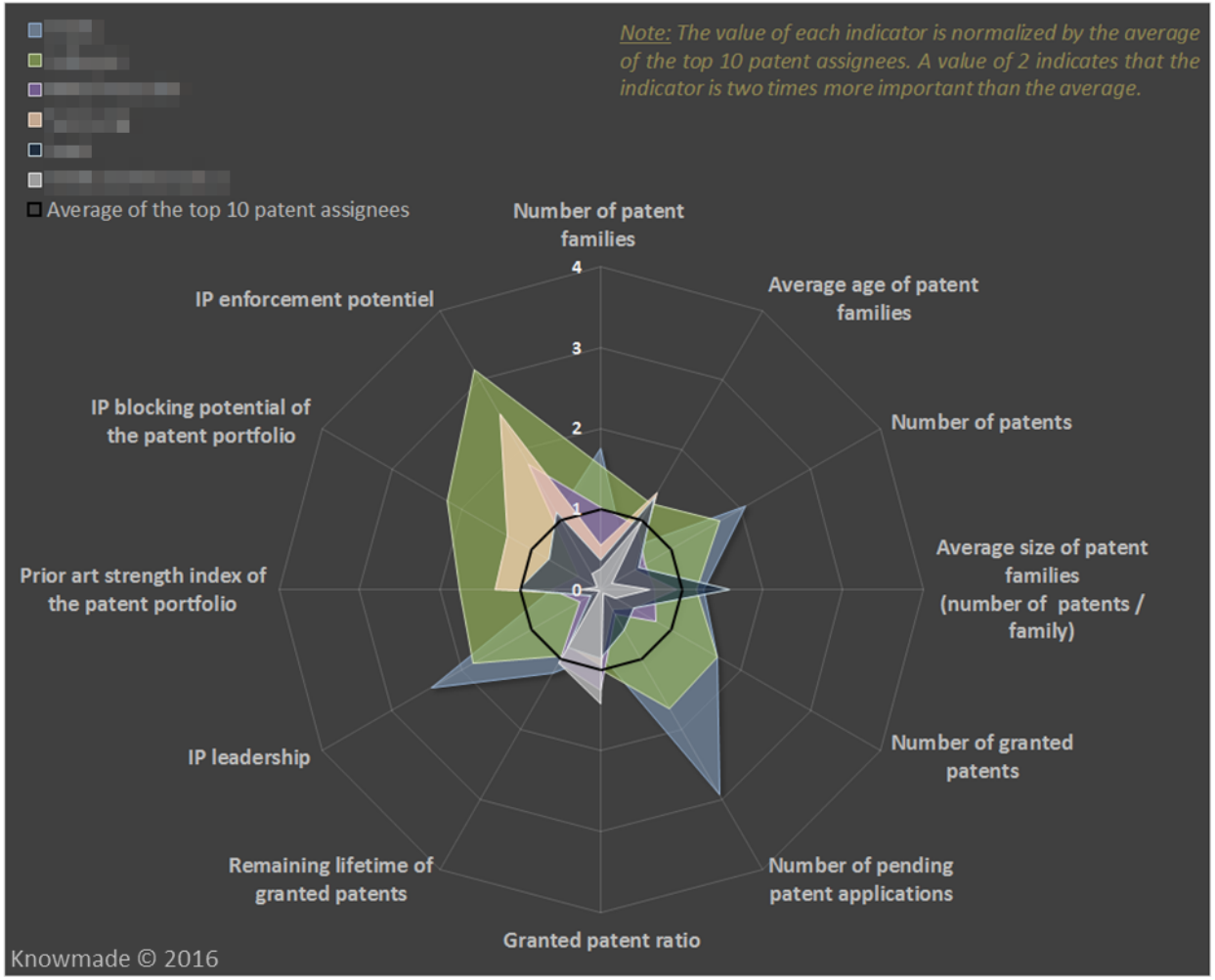
Summary of patent portfolios

Patent Applicants	Number of patent families	Earliest priority year	Average age of patent families (Year)	Average number of patent families per year	Number of patents	Average number of patents per family	Number of granted patents	Number of pending patents	Number of dead patents (abandoned, rejected or expired)	Granted patent ratio	Average remaining lifetime of granted patents (Year)	Number of patent families containing granted patents in the corresponding country							Number of patent families containing pending patent applications in the corresponding country								Number of forward citations (excluding self-citations)	Average number of forward citations per patent family	Number of different patent applicants citing the patent portfolio	Main citing patent applicants
												USA	Europe	Japan	Korea	China	Taiwan	Singapore	USA	Europe	Japan	Korea	China	Taiwan	Singapore	PCT (WO)				
			3.0	12.0		3.0			8	41%																		1.3	80	
			5.3	**14.5**		3.5			23	56%																		7.5	**250**	
			6.7	9.9		2.8			**38**	50%																		5.1	220	
			4.2	8.0		2.3			20	36%																		1.4	60	
			4.9	9.8		1.6			22	63%																		2.7	90	
			5.7	4.5		1.7			23	69%																		4.0	100	
			7.8	4.6		1.7			25	72%																		6.0	140	
			7.5	3.1		2.2			33	48%																		12.5	160	
			7.1	2.1		3.7			17	43%																		14.0	120	
			1.7	10.3		1.0			0	25%																		0.0	1	chnology)
			4.2	3.1		2.0			8	56%																		2.2	20	
			5.4	3.1		1.4			5	71%																		4.6	40	
			7.6	2.1		2.0			7	63%																		5.5	40	
			3.8	3.6		1.6			2	76%																		0.5	5	
			2.7	1.3		1.3			0	23%																		4.1	40	
		2010	2.6	2.0		4.1			2	47%																		3.6	20	
		1999	**14.1**	0.7		3.1			3	84%																		18.2	80	
		2002	3.3	0.9		2.4	11	17	1	38%																		2.1	20	
		2013	1.8	3.0		1.9	4	13	0	24%																		0.2	2	
		2003	8.1	0.6		5.4	28	14	1	65%																		2.8	10	
		2003	11.0	0.6		6.5	23	5	24	44%																		28.5	80	
		2012	2.3	2.0		2.5	2	18	0	10%	17.4																	0.0	0	
		2009	4.8	1.1	8	1.0	7	1	0	88%	10.4					7						1						1.0	3	
		2003	7.3	0.5	52	**7.4**	36	5	11	69%	12.3	5				2	4		1			2	1				**28.7**	80	
		2009	2.8	0.9	19	3.2	5	14	0	26%	12.4	2				1	1		4	4		3	3				10.8	30	
		2006	8.2	0.6	14	2.3	11	0	3	79%	11.7	6				2	1										123	20.5	40	
		1997	10.0	0.3	13	2.6	7	2	4	54%	6.2	2	2							1							66	13.2	40	
		2007	3.6	0.6	8	1.6	5	2	1	63%	11.9	1			1	1	2		1				1				7	1.4	6	
		2015	0.8	5.0	5	1.0	0	5	0	0%	0.0											5					0	0.0	0	
		2008	5.5	0.5	6	1.5	3	1	2	50%	16.1	2						1							1		21	5.3	15	Avago, Freescale
		2004	8.0	0.3	11	2.8	6	0	5	55%	13.5	3		3													48	12.0	30	University of Illinois, MC10, Fujitsu, Sumitomo Bakelite
CEA	3	2007	9.0	0.3	12	4.0	6	3	3	50%	11.4	3	3							3							8	2.7	6	Deca Technologies, Fujitsu, Infineon
Hana Micron	3	2010	4.0	0,5	4	1.3	1	1	2	25%	17.2				1				1								2	0.7	1	Amkor
Niko Semiconductor	3	2014	2.0	1,5	5	1.7	2	3	0	40%	**17.8**	1					1		1				1	1			0	0.0	0	-
Seoul National University (SNU)	3	2012	4.0	0,8	3	1.0	3	0	0	**100%**	16.1				3												0	0.0	0	-

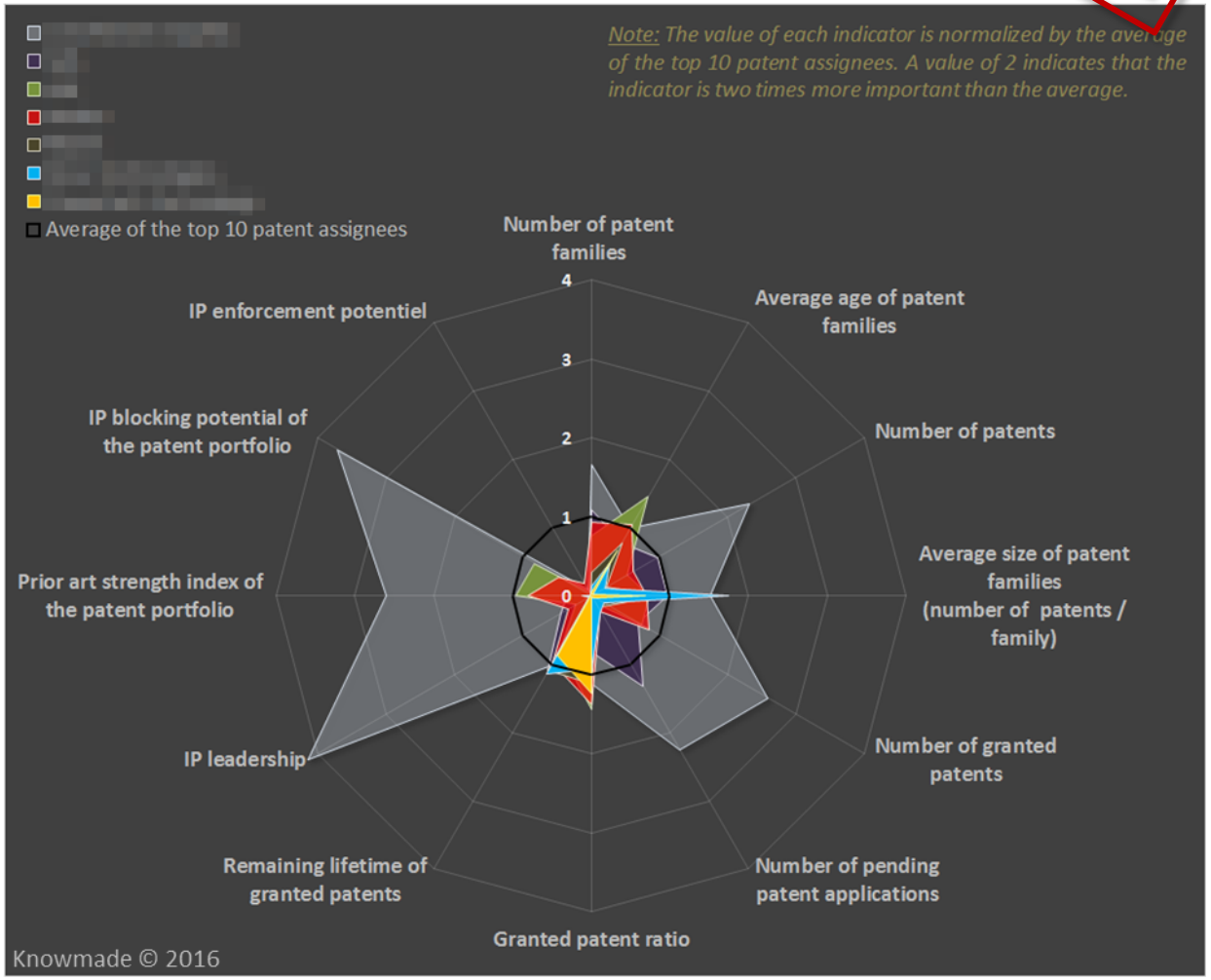
IP POSITION OF KEY PLAYERS

Comparison of FOWLP patent portfolios held by the main IDMs, Foundries and OSATs

IDMs and Foundries



OSATs



OSAT: Outsource Semiconductor Assembly and Test
IDMs: Integrated Device Manufacturers

PATENT LITIGATIONS

The situation could rapidly change due to the market adoption

Not yet litigation cases in Fan-Out wafer level packaging, but this could change in near future.

In a **patent infringement** action, the **potential sales volume plays a major role** for assessing the damage award.
The choice of **Apple** to adopt the FOWLP platform (**TSMC** InFO-PoP) for its A10 APE (iPhone 7)
and the presence of **patent licensing companies** (**WiLAN**) in the patent landscape,
are **tangible signs of the market explodes**.

Market adoption:

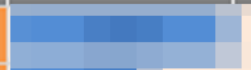
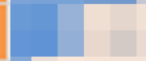
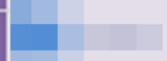
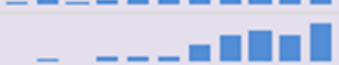
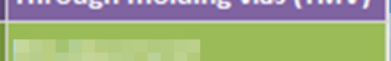
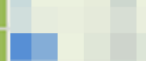
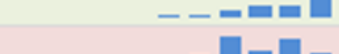
Fan-Out wafer han 240 millions
dollars, and it MC as a supplier
of Fan-Out pac ket Trends 2016"
report, Yole Dé ons with high IO
counts. Market v IO applications
will grow and by many OSATs,
IDMs, and four and **JCET/STATS**
ChipPAC. Num
As the market to a **competitive**
mode, a strict

Patent licensing companies:

WiLAN, a Round Rock Research
and Tesse . The company began
litigating i **more than 50 active**
cases incl
In June of tent assets) related to
Fan-Out w assets) from **Freescale**
Semicond

PATENT SEGMENTATION

Number of patents, time evolution of patent publications and main patent assignees

Segments		Number of patent families	Percent of patent families	Dynamics of patent publications (2005-2015)	Main patent assignees
Technology	Chip-first				nfineon, SPIL, NXP/Freescale
	Chip-first Face-down				n, NXP/Freescale, SPIL
	Chip-first Face-up				
	Chip-last				
Architecture	Multi-chip module (MCM)				
					SPIL
					
					
					g, SPIL
	Through molding vias (TMV)				TSMC
Process steps					
					C
					
	Redistribution layers (RDL)				Amkor
	Foundry BEOL				
Technical challenges	Die shift				
	Warpage				nkor, TSMC

PATENT SEGMENTATION

Matrix of patent assignees vs. technical segments

Patent Assignees	Number of patent families	TECHNOLOGY				ARCHITECTURE						PROCESS STEPS					TECHNICAL CHALLENGES	
		Chip-first	Chip-first Face-down	Chip-first Face-up	Chip-last	MCM (multi-chip module)	PoP (package-on-package)	SiP (system-in-package)	F2F (face-to-face package)	Stacked dies	TMV (through molding via)	Die placement	Molding	Planarization	RDL	Foundry BEOL	Die shift	Warpage
TOTAL	*1263*	*1059*	*654*	*309*	*118*	*131*	*274*	*26*	*33*	*70*	*139*				*183*	*24*	*58*	*136*
		159	11			17					20				28	7	5	13
		141	112			33					23				44		7	20
		140	96			13					16				19	5	2	3
		93	63			6					11				1		23	24
		92	80			16					6				14	1	5	7
		44	28			9					20				26	7		15
		45	41			3					13				18			5
		41	30			10					6				12		1	11
		32	30			3					3				5		3	3
		31	16			4												10
		20	20			2					3							5
		22	16			1					7				1			4
		17	10															
		18	14			6											1	
		16	6								3				1			2
		11	3								3				3		2	1
		10	6												4	1		1
		10	7			2									5	3		
		6	2			3												
		8	8			1											1	
		5																1
		8																
		4	3														3	
		2																2
		3	1															
		6	6			2												
		5	1															
		4																
		5	3															
		4	3			1					2							1
		4	1														1	1
CEA	3	3	3								2							
Hana Micron	3	2	2			1												
Niko Semiconductor	3	3	2															
Seoul National University (SNU)	3	2	2															3

The numbers represent the number of patent families

- [redacted]folio of [redacted]on **chip-** **FO-PoP** [redacted]echnical [redacted]e.
- [redacted]ents on **warpage**
- [redacted] market [redacted]d many [redacted]ion.

PATENT SEGMENTATION

Matrix of technology vs. process steps/technical challenges/architecture

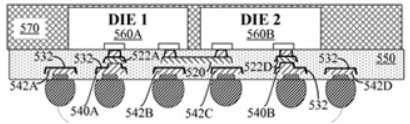
The numbers represent the number of patent families		PROCESS STEPS					TECHNICAL CHALLENGES		ARCHITECTURE					
		Die placement	Molding	Planarization	RDL	Foundry BEOL	Die shift	Warpage	MCM (multi-chip module)	PoP (package-on-package)	SiP (system-in-package)	F2F (face-to-face package)	Stacked dies	TMV (through molding via)
TECHNOLOGY	Chip-first Face-down	[illegible]	[illegible]	[illegible]	[illegible]	2	[illegible]	[illegible]	[illegible]	154	[illegible]	[illegible]	[illegible]	[illegible]
	Chip-first Face-up	15	16	6	19	5	[illegible]	[illegible]	[illegible]	87	[illegible]	[illegible]	[illegible]	[illegible]
	Chip-last	0	0	0	20	17	[illegible]	[illegible]	[illegible]	24	[illegible]	[illegible]	[illegible]	[illegible]

White space

The most of FO-POP patents are mainly chip-first solution

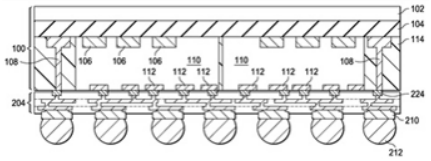
[illegible]82 (Qualcomm, 2015)

The process flow may include BEOL processes



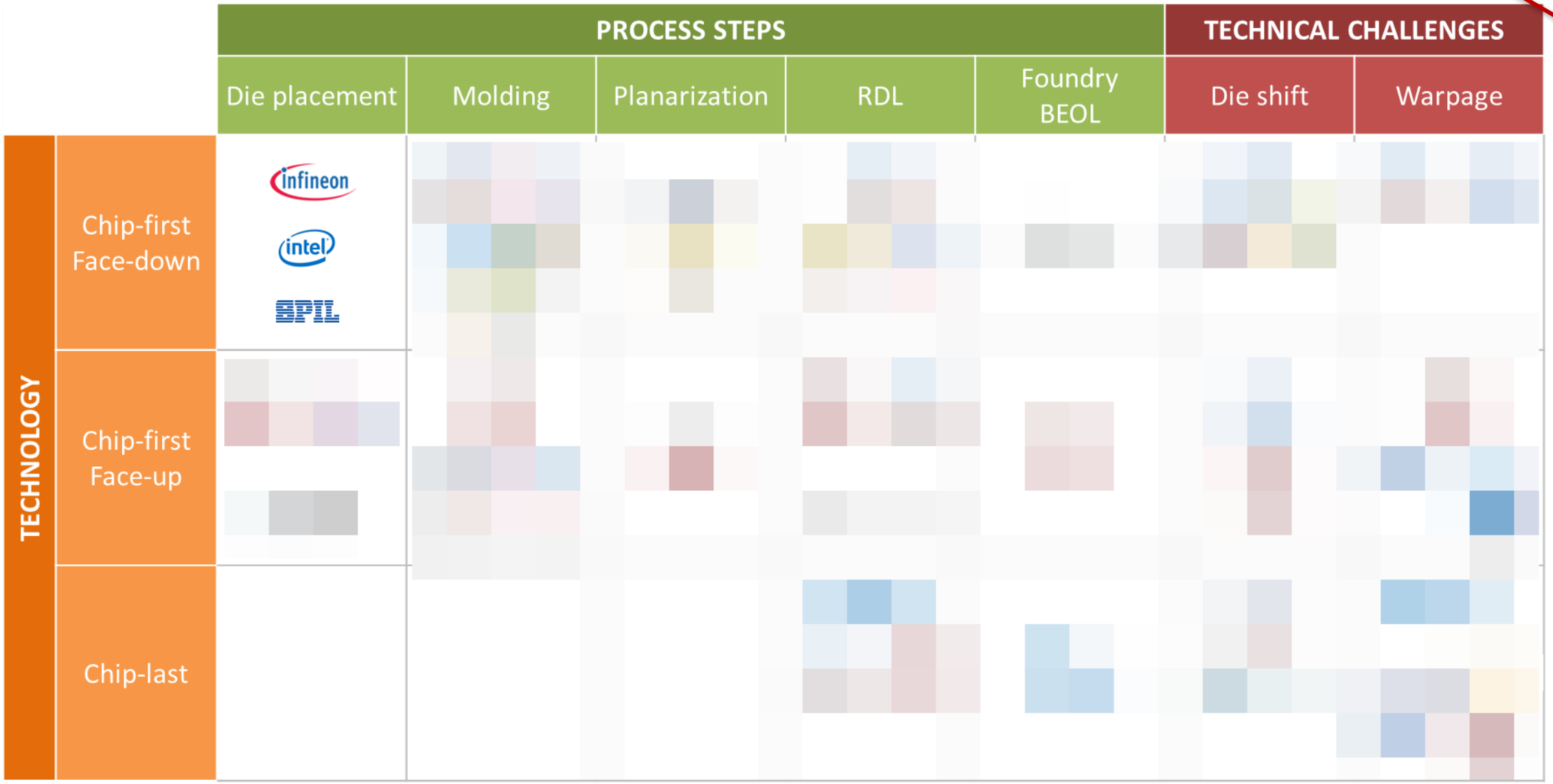
[illegible]52 (TSMC, 2014)

The metal layers may be formed using a dual-damascene process



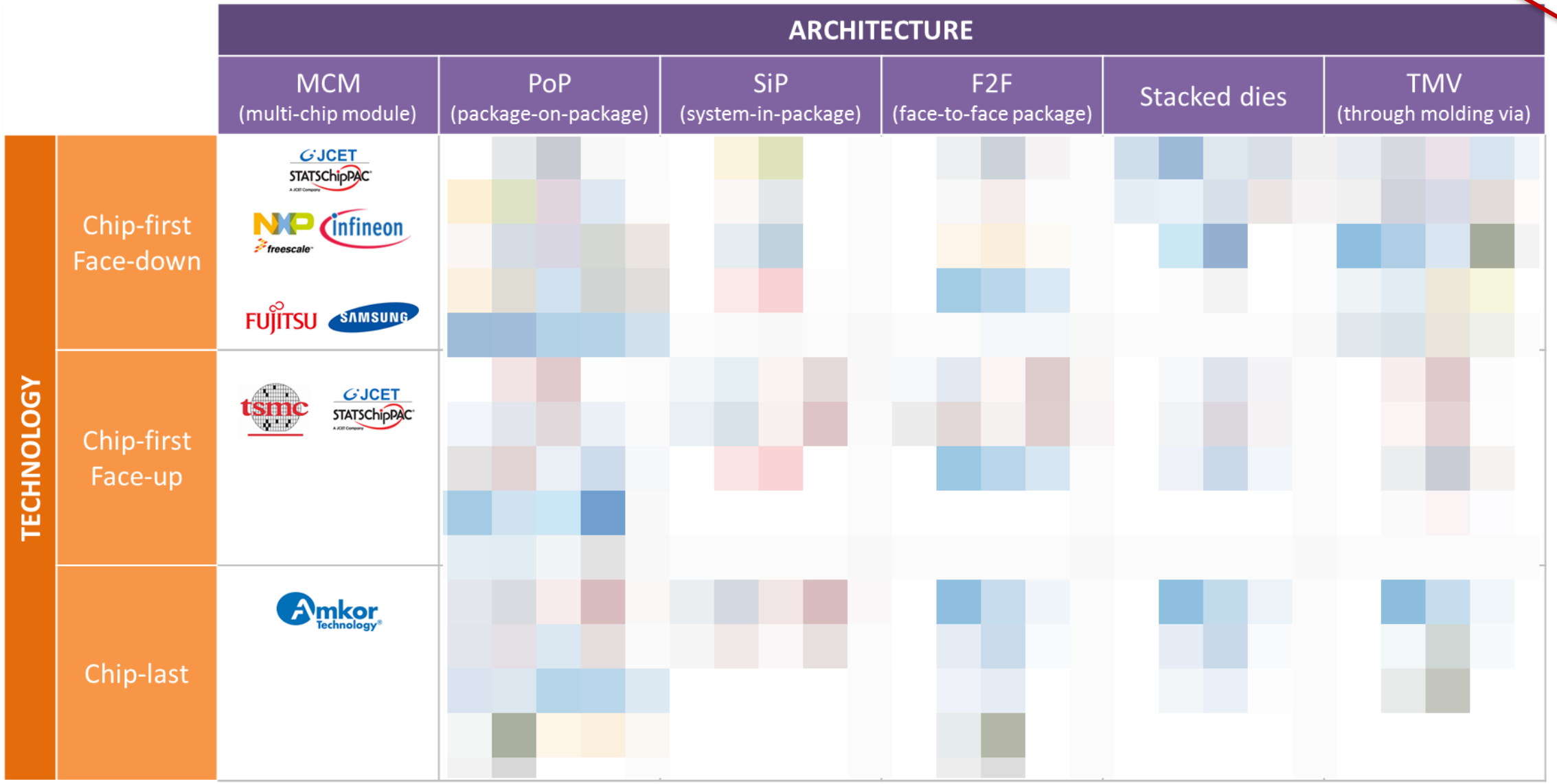
PATENT SEGMENTATION

Matrix of main patent applicants vs. technical segments



PATENT SEGMENTATION

Matrix of main patent applicants vs. technical segments

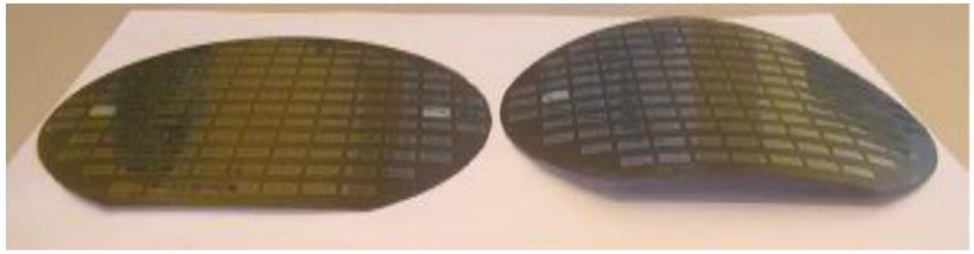


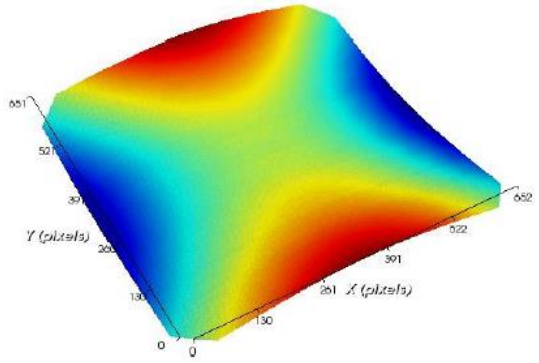
WARPAGE

Warpage issue for Fan-Out packaging

Warpage remains a major challenge for Fan-Out, and it will be even more critical with panels.

In the case of FOWLP, wafer can bend and bow due to mechanical stress during mold curing and debonding of the reconstituted wafer. Warpage leads to complications or the impossibility of following process steps once the wafer is bent due non-uniformity of the substrate (alignment issues, non-uniformity of depositions, etc…) which can result in yield loss. It creates stress on dies, which can damage them, and also can damage adhesive after RDL.





Source: Akrometrix

The encapsulation layer has a thermal expansion coefficient (CTE) higher than those of other constituents is formed on both lateral sides and upper sides of the dies, thus the die package warps, thereby deteriorating the reliability of the die package.

Warpage is a big challenge. The epoxy mold wafers can be warped after curing, and the size and shape of the warpage can change for different shapes and density of the embedded die. In an effort to reduce cost and package height, the thickness of the substrate reduces too, although this tends to make the wafer less stiff and therefore flatten under gravity.

WARPAGE

Technical solutions found in patent to solve warpage issue for Fan-Out packaging

More than [redacted] patent families are related to the warpage issue for Fan-Out wafer level packaging.

- [redacted] **inventions** claim a solution to solve the **warpage issue** in **chip-first face-down** configuration. The main patent applicants are [redacted]
- [redacted] **inventions** claim a solution to solve the **warpage issue** in **chip-first face-up** configuration. The main patent applicants are [redacted]
- **10+ inventions** claim a solution to solve the **warpage issue** in **chip-last** configuration. The main patent applicants are [redacted]

Technical solutions found in patents (more details in the next pages):

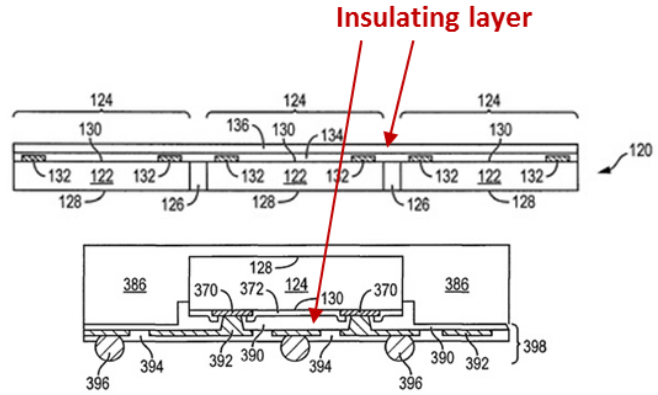
- Use of **hard wafer carrier** such as silicon, metal ([redacted]), glass (**TSMC**) or ceramics ([redacted])
- Use of a **stress relief layer** (**STATS ChipPAC**, [redacted])
- Use of a **thermally conductive sheet** ([redacted])
- Use of **embedded units** (**NXP/Freescale**, [redacted])
- Use of a **recessed portions** in the mold compound (**SPIL,** [redacted]) or in the interconnect surface (**NXP/Freescale**)
- Use of a **pressure member** on the encapsulant ([redacted])
- **Better mold compound material formulation** to reduce stress during deposition and RDL manufacturing ([redacted]).
- **Improved lithography** (better equipment) to take warpage into account while processing.
- **Improvement of monitoring** to better enhance the process.

WARPAGE

Technical solutions found in patent to solve warpage issue for Fan-Out packaging

❖ Use of a stress relief layer

JCET STATSChipPAC

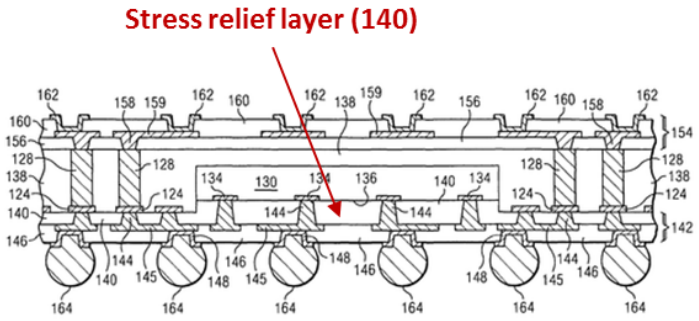


[redacted]5 (filed in 2013, granted since 2014)
[redacted]2 (filed in 2011, granted since 2013)

An insulating layer disposed over the die (and encapsulant) and into a channel formed in the die and/or encapsulant.

A firs[redacted] into the first
chan[redacted] an be formed
over [redacted] ned using spin
coati[redacted] **ting layer 136**
conta[redacted] dielectric film,
orgar[redacted] **sulating layer**
136 i[redacted] **age, or other**
dama[redacted] f the build-up
inter[redacted] nsile strength
great[redacted]

JCET STATSChipPAC



[redacted]03 (filed in 2009, granted since 2011)

Forming stress relief layer between die and interconnect structure.

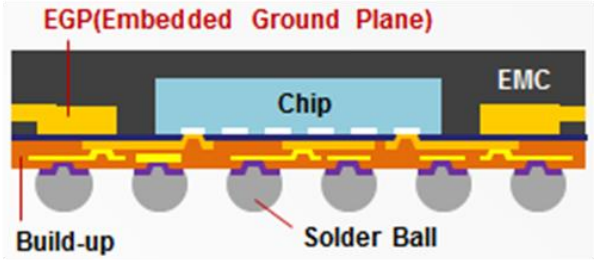
A **stre**[redacted] and active
surfac[redacted] dation**. The**
stress [redacted] con nitride
(Si3N4[redacted] er material
having[redacted] ctive region
136, c[redacted] conductive
layer 1[redacted] the portion
of **insu**[redacted] the portion
of insu[redacted]

WARPAGE

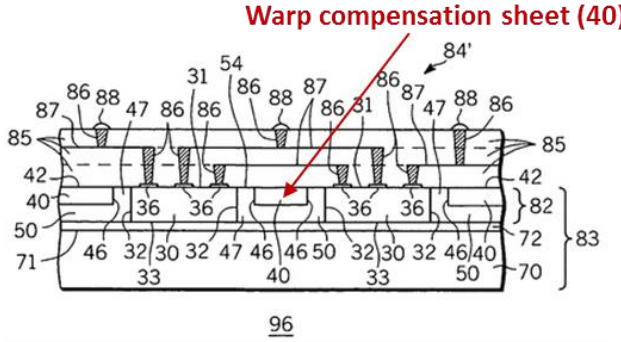
Technical solutions found in patent to solve warpage issue for Fan-Out packaging

❖ Use of embedded units

Freescale/NXP proposes a **embedded ground plane** (EGP) build into a panel assembly. More than 20 patent families refer to the embedded ground plane, and at least **4 patent families mention the EPG as a solution to solve the warpage issue** ([redacted])



The **EGP**, typically fabricated from copper, is used to control warpage of the panel assembly, but also the die shift and can also be used to provide a single routing option for ground in a finished semiconductor package.



[redacted]1 (filed in 2006, granted since 2014)
Counterparts in Taiwan, Korea and Japan

A warp compensation sheet (WCS) which laterally surrounds individual devices 30 in encapsulation.

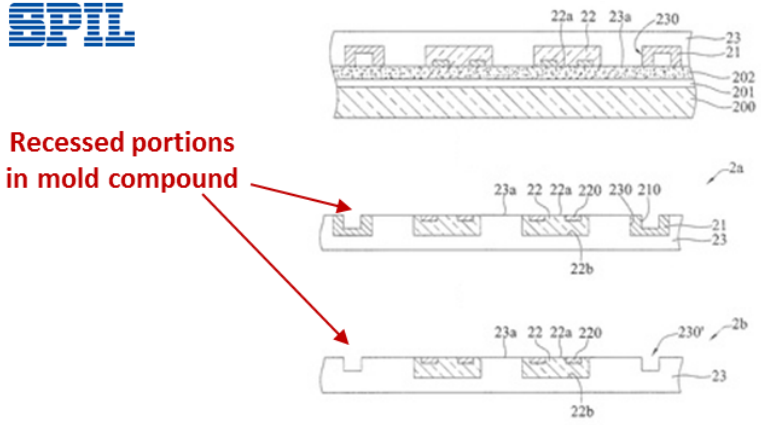
WCS [redacted] ths 45
that [redacted] lateral
edge [redacted] 46 of
winc [redacted] y also
exte [redacted]
If cc [redacted] CS 40,
then [redacted] 30 and
enca [redacted]

WARPAGE

Technical solutions found in patent to solve warpage issue for Fan-Out packaging

❖ Use of recessed portions

SPIL

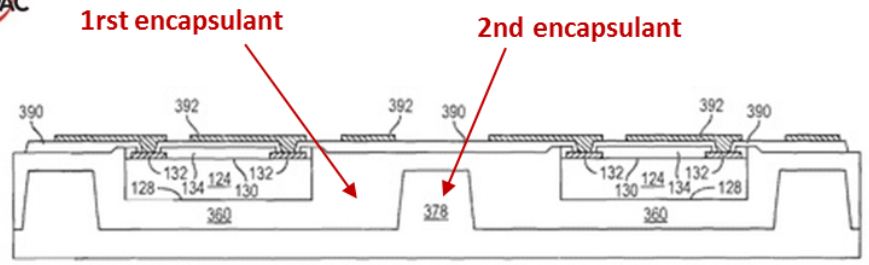


[redacted] (filed in 2014, granted since 2015)
Counterpats in Taiwan and China

The formation of the recessed portions release the stress of the insulating layer and prevent warpage of the insulating layer from taking place.

A plu[redacted] of the
insul[redacted]rrence.
There[redacted]g layer
can b[redacted]nductor
elem[redacted] is poor
are s[redacted]

JCET STATSChipPAC



[redacted] (filed in 2011, granted since 2013)

Forming thick encapsulant for stiffness with recesses.

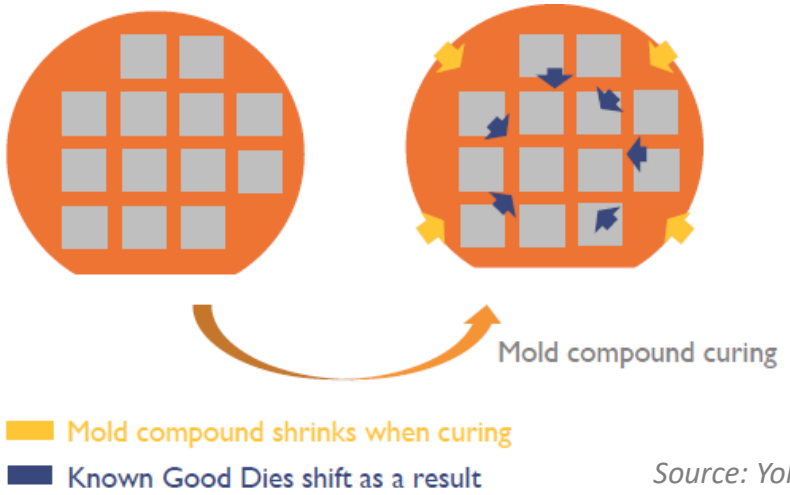
A fi[redacted]rrier. A
stiff[redacted]nductor
die. [redacted]ecesses
can [redacted]ely, the
rece[redacted] second
enca[redacted]nt. The
thic[redacted]arpage
whi[redacted]ucture.

DIE SHIFT

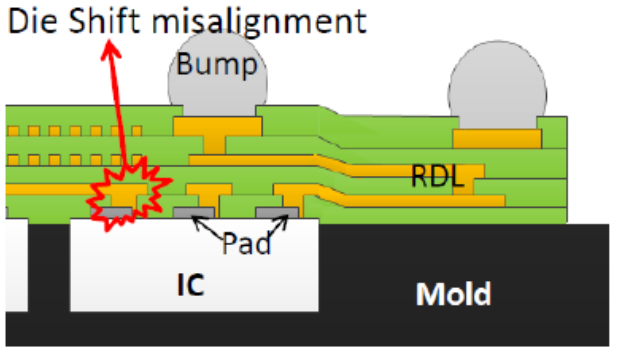
Die shift issue for **chip-first** Fan-Out packaging

Die shift during molding and mold curing is one of the major processing hurdles in chip-first FOWLP processes. It limits pitch capability and yield.

Die shift is an unwanted movement of the chip after placing it on the carrier and depositing the molding. It results from shrinkage of the mold during curing. It can go up to several tens of microns. The consequence of die shift is an inaccurate alignments of die pads of reconfigured wafers which can cause yield losses. In case of multi-components FOWLP there can be die shifts in different directions within the same package. This is a critical issue which limits integration capability.



Source: Yole Développement



*Source: A*Star*

The thermal release tape is flexible. During a molding process, the coefficient of thermal expansion (CTE) of the thermal release tape and lateral forces from the encapsulant can likely cause positional deviation of the semiconductor chips (that is, positions of the semiconductor chips are deviated from a chip areas), thereby adversely affecting the positional accuracy of the semiconductor chips. The larger the size of the carrier is, the more severe the positional deviation of the semiconductor chips becomes. As such, the electrical connection between the redistribution structure (RDL) and the semiconductor chips is adversely affected, and consequently the product yield is reduced.

DIE SHIFT

Technical solutions found in patent to solve die shift issue for **chip-first** Fan-Out packaging

More than [redacted] patent families are related to the die shift issue for chip-first FOWLP.

- **30+ inventions** claim a solution to solve the **die shift issue** in **chip-first face-down** configuration. The main patent applicants are [redacted]
- [redacted] **inventions** claim a solution to solve the **die shift issue** in **chip-first face-up** configuration. The main patent applicants are [redacted]

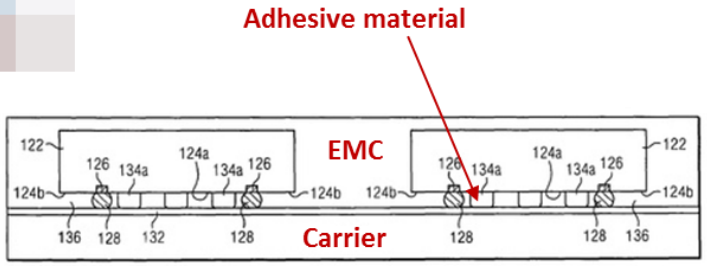
Technical solutions found in patents (more details in the next pages):

- Use of an **embedded units** (**NXP/Freescale**)
- Use of **recessed portions** ([redacted])
- Use of an **adhesive/fixing material** ([redacted])
- Use of a **positioning unit** allowing the alignment of the circuit layer to the electronic elements (**SPIL**)
- Use of a **double encapsulation** process ([redacted])
- Use of an **adaptive patterning** of RDL after die shift to take it in account (**Deca Technologies**)
- Forming the **RDL before moulding** the resin (**3D Plus**)
- **Improve alignment lithography** ([redacted])

DIE SHIFT

Technical solutions found in patent to solve die shift issue for **chip-first** Fan-Out packaging

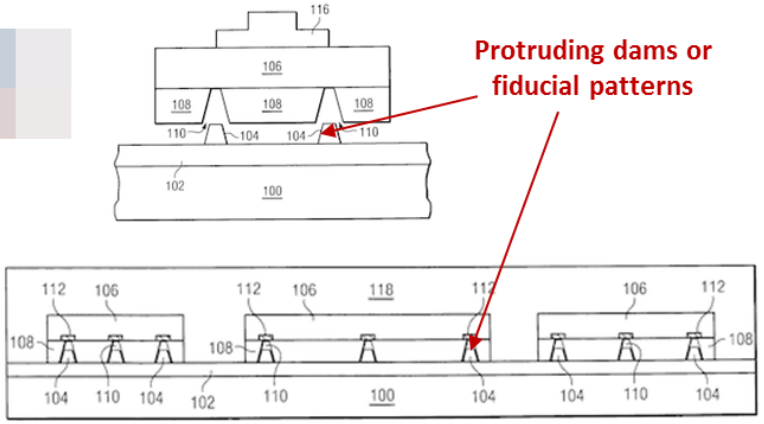
❖ Use of an adhesive/fixing material



[redacted] (filed in 2009, granted since 2014)

An adhesive material is deposited as a plurality of islands or bumps on the carrier or active surface of the semiconductor die.

The a[redacted]g during
enca[redacted] printing
or ot[redacted] polyvinyl
chlor[redacted]dhesive,
for c[redacted]l epoxy,
polyr[redacted] by light,
therr[redacted]



[redacted] (filed in 2009, granted since 2014)

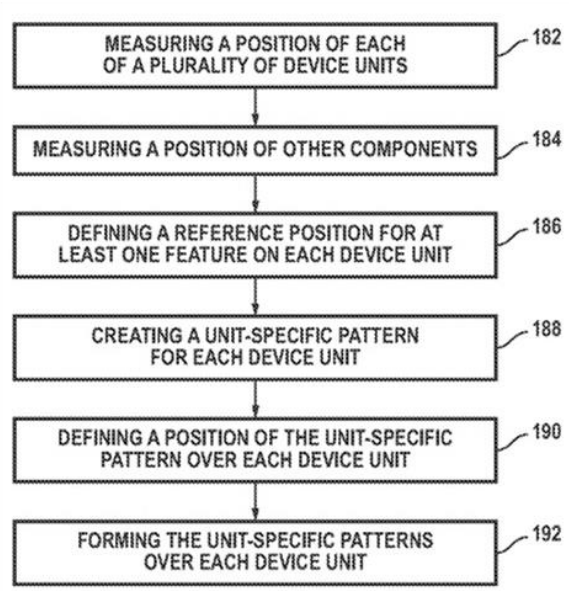
Matched patterns and alignment slots to enhance structural stability and minimize any physical shift

Duri[redacted]ctive x-y
posi[redacted]s 110 to
enha[redacted]facturing
proc[redacted] or other
suita[redacted]e metal,
poly[redacted] or spray
coat[redacted]4 can be
form[redacted]tions to
prov[redacted]

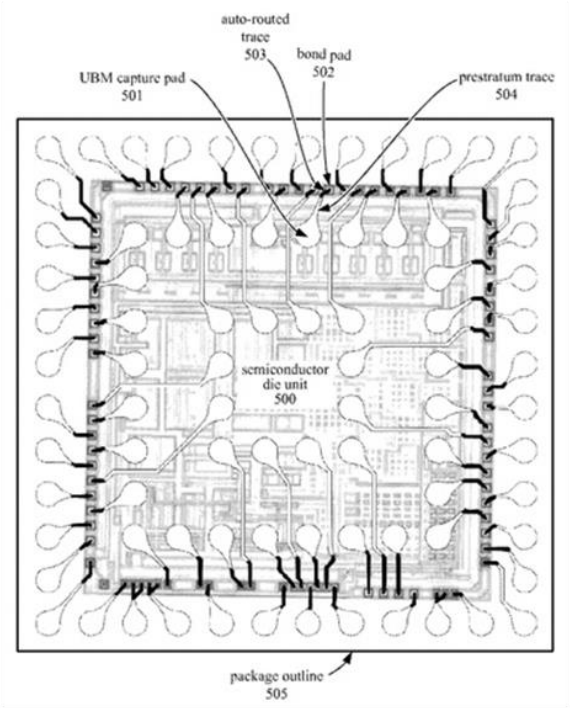
DIE SHIFT

Technical solutions found in patent to solve die shift issue for **chip-first** Fan-Out packaging

❖ Use of an adaptive patterning of RDL



(filed in 2013, granted since 2015)
Counterparts in China and Singapore



(filed in 2010, granted since 2014)
Counterparts in China and Singapore

The **adapt**
Technologi
build-up st
The **adapti**
any structu
build-up st
RDL patter

The **adap**
measurem
adaptive p
measurem
adaptive
measurem
patterning
may be sin
lot may be
relative ori

IP PROFILE OF KEY PLAYERS

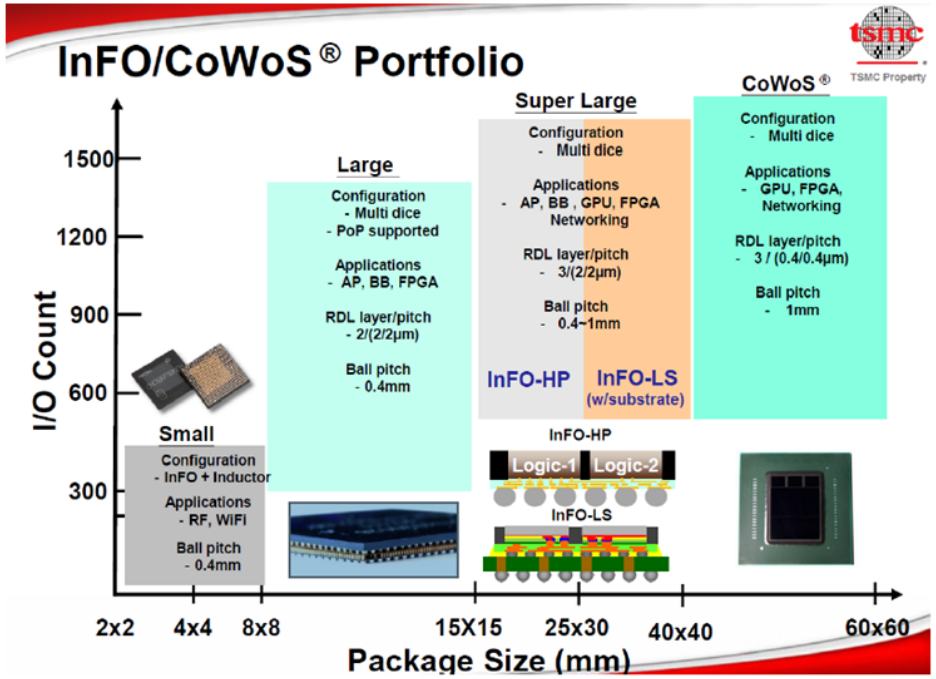
TSMC (Taiwan Semiconductor Manufacturing Company)

InFO technology

TSMC has de[illegible] strategy of becoming a st[illegible]O market of interest is PoP[illegible]t are always pushed by cus[illegible] **TSMC** as its supplier for its[illegible]ith a DRAM. **TSMC** is expec[illegible]ackaging. **TSMC** set an a[illegible] die > 10x10 mm²) with hig[illegible]market: High density applica[illegible]es (less than 1 mm for APE[illegible] packaging is part of an offe[illegible]ir yield is low but money los[illegible]keep focusing on high value [illegible]oduct to get more custome[illegible]

Packaging product	Process features	Current status	L/S Features	No. of layers	Applications
InFO	• [illegible] • [illegible] • [illegible]ated Cu via • [illegible] • [illegible]L-first approach • [illegible]L process • [illegible]e for single die • [illegible]ith 4 chips • [illegible]nductor • [illegible]e • [illegible] • [illegible]lesign	Introduced in 2016 (Apple A10 processor) In volume production on 300mm	5/5µm (2016) 2/2µm (2017)	1-4	Mobile application processor APE, baseband RFIC, PMIC

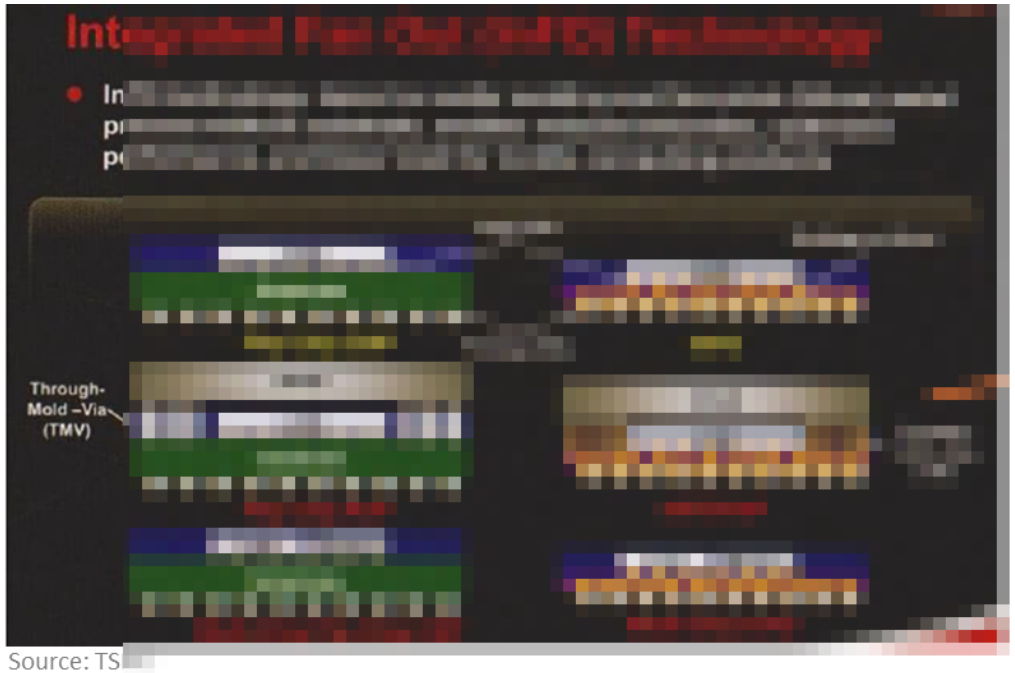
Potential of **InFO** is very high and **TSMC** is positioning its technology in a packaging portfolio that can address wide variety of applications



Source: TSMC

TSMC (Taiwan Semiconductor Manufacturing Company)

InFO technology



Source: TS

Source: TSMC

TSMC (Taiwan Semiconductor Manufacturing Company)

IP profile in Fan-Out wafer level packaging

TSMC is the

patent portfolio

granted patents

pending patent applications

, China

IP leadership

granted patents (mainly pending patent applications (mainly in

prior art strength index

t receiving a limited number of citations from

IP blocking potential

received from a limited t applicants (Amkor, ics, Intel ...)

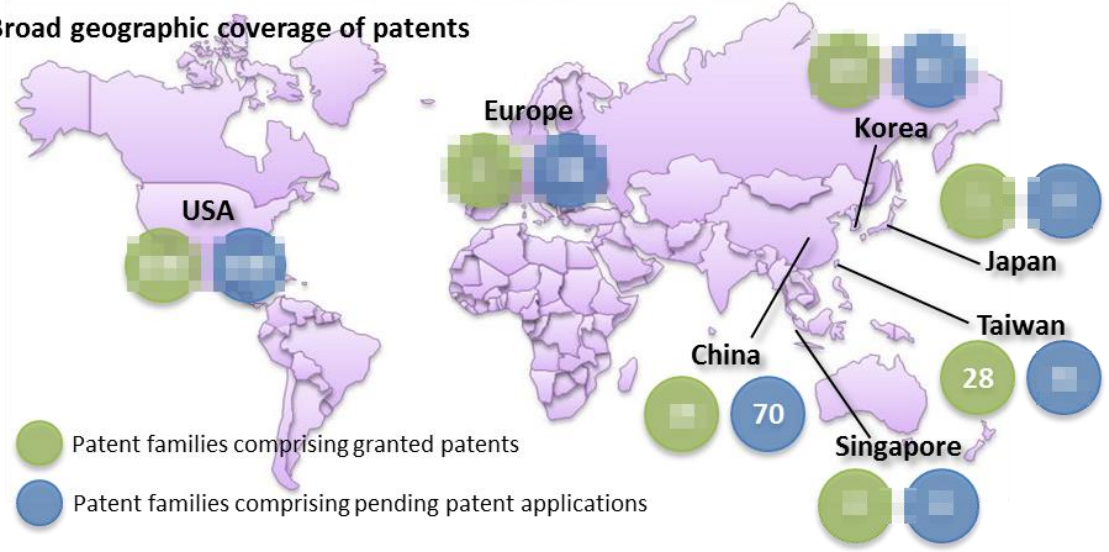
IP enforcement potential

A noticeable propen a high number of e

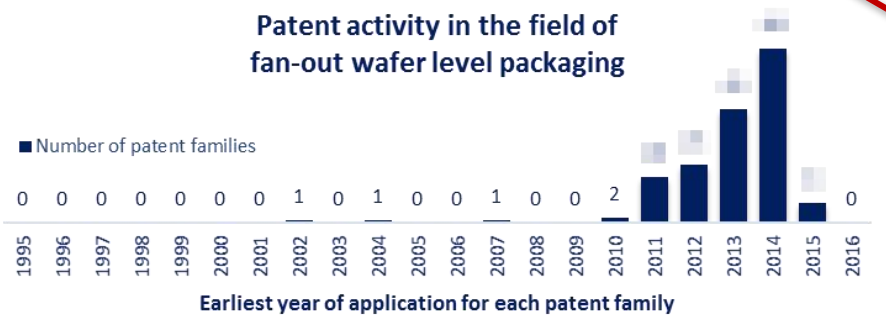
technological coverage in patents

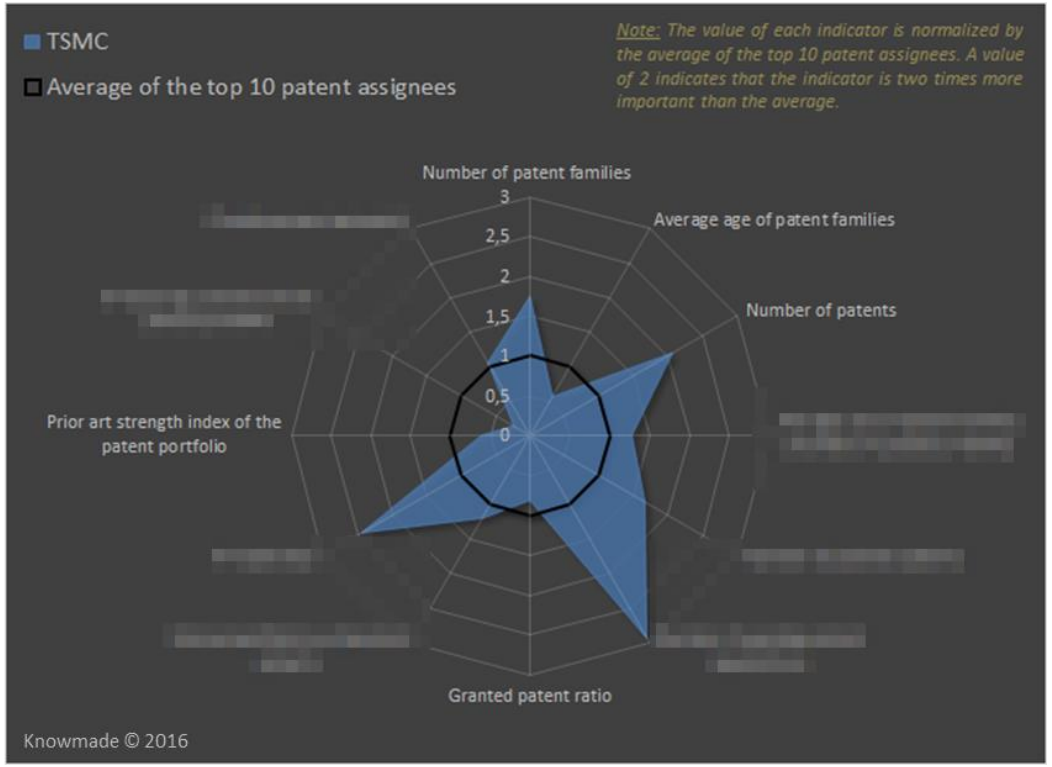
Chip-first Face-up | Die shift | Multi-chip (MCM), PoP,

Broad geographic coverage of patents



Patent activity in the field of fan-out wafer level packaging





TSMC's InFO-PoP

Teardown analysis of the Apple's A10 APE

The teardown of the **A10 application processor** has been performed by our partner **System Plus Consulting** (TSMC Integrated Fan-Out (inFO) Package in Apple's A10 Application Processor report, System Plus Consulting, October 2016). The technology analysis reveals some key features of the InFO package, such as the

A10 package cross section. Source: "TSMC Integrated Fan-Out (inFO) Package in Apple's A10 Application Processor" report, System Plus Consulting, October 2016.

under the AP

The are integ flip-chip n the last R

Related TSMC's patent
43

Polymer layer

A thick the RDL polym olymer is only , and it contai e.

Related TSMC's patents
US2 76

Copper pillars

The co tro-chemica ited on the tion process

Related TSMC's patent
US2

TSMC's InFO-PoP from Apple's A10 APE

XXXXXXXXXXXXX

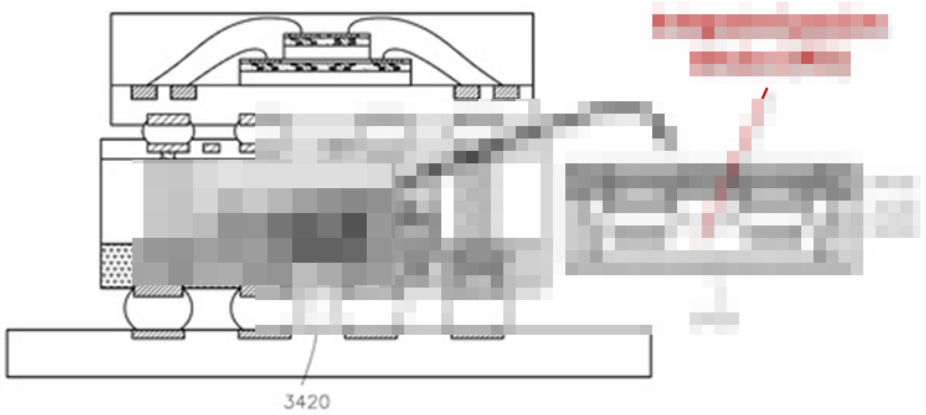
Located [illegible] **InFO-PoP**, the [illegible] configuration and supported by an [illegible]

[illegible] · *SEM view*

Related patents

Source: "TSMC Integrated Fan-Out (inFO) Package in Apple's A10 Application Processor" report, System Plus Consulting, October 2016.

One **TSMC**'s patents claims an [illegible] connected [illegible] US[illegible]



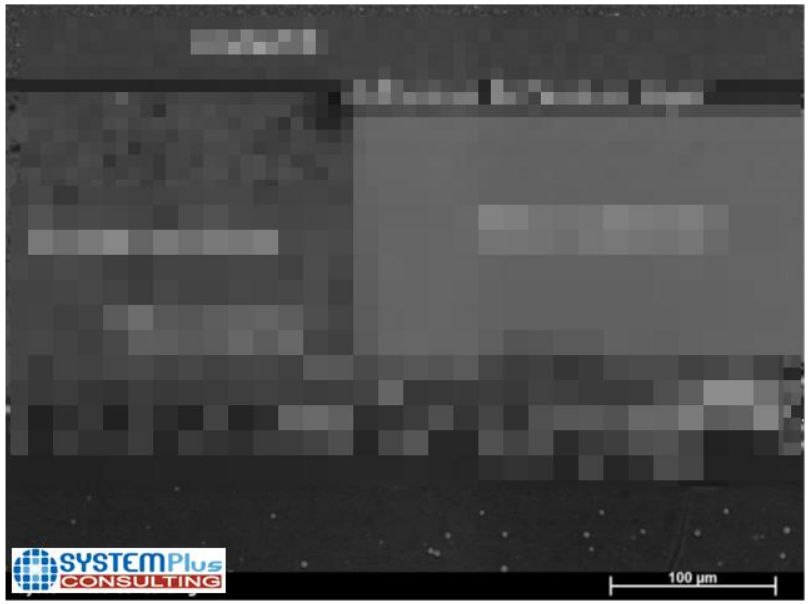
The [illegible] ive area with [illegible] ceramic cap[illegible] n, oxide dep[illegible] es **TSMC** to c[illegible] parisons with [illegible] and-side dec[illegible]

TSMC holds at least 10 patent families on [illegible]

TSMC's InFO-PoP from Apple's A10 APE

XXXXXXXXXXXXXXX

A [redacted] that could be **different** than the [redacted] contained a noticeable [redacted]



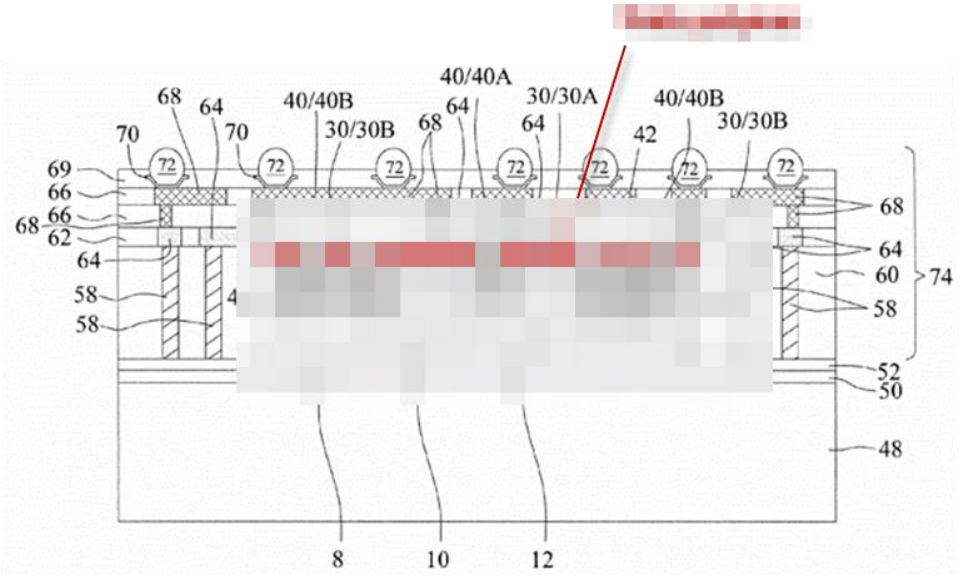
RDL cross-section – SEM view

Related patents

Source: "TSMC Integrated Fan-Out (inFO) Package in Apple's A10 Application Processor" report, System Plus Consulting, October 2016.

Some **TSMC**'s patents mention [redacted]

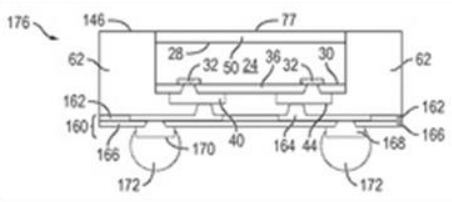
US2[redacted]76



Why did the leading company **TSMC** decide to introduce [redacted] there any technical advantages? [redacted] reduce the costs? [redacted] patents owned by [redacted] in order to **avoid patent infringement**?

[redacted] is using a molding compound to su[redacted]

US[redacted]

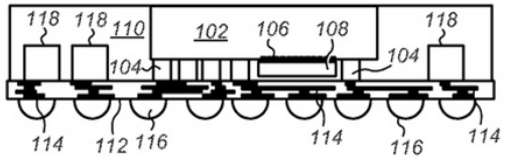


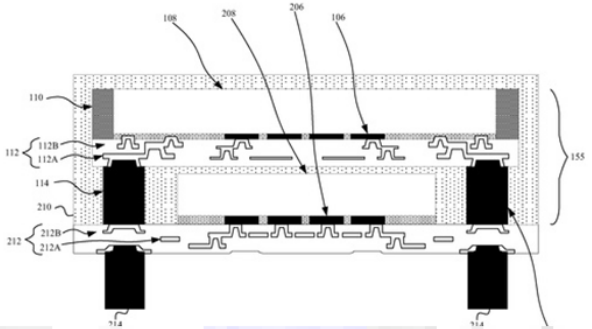
APPLE

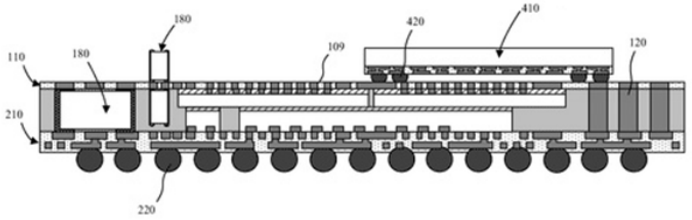
Fan-Out technology

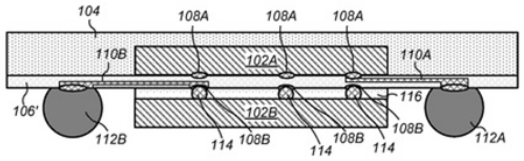
Apple chose the **TSMC**'s InFO-PoP technology for its A10 APE in 2016. According to Yole Développement, the entrance of **TSMC** as a supplier of Fan-Out packaging for **Apple**'s APE made a big change, with the market expected to jump from $244M in 2015 to $821M in 2017 ("Fan-out: Technology & Market Trends 2016" report, Yole Développement, August 2016).

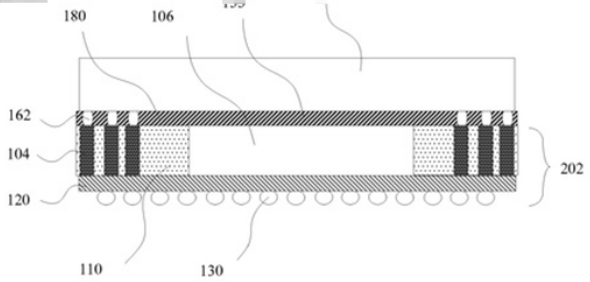
Apple has filed some patents on Fan-Out wafer level packaging in 2014-2015, including chip-last/chip-first solutions, Package-on-Package and System-in-Package. This recent patenting activity reflect a real interest for the FOWLP platform.

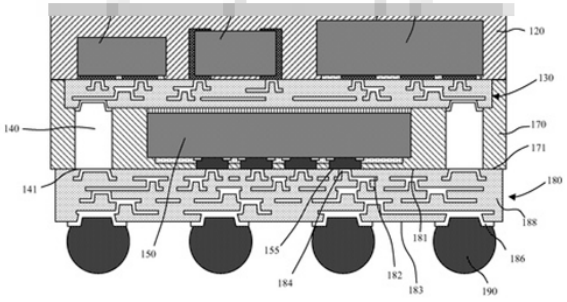








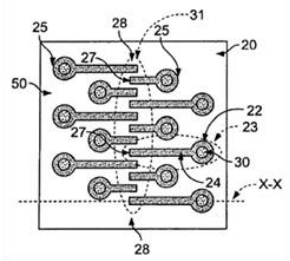


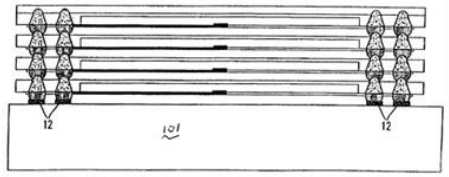


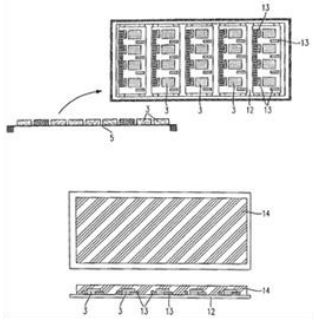
POLARIS INNOVATIONS (WILAN)

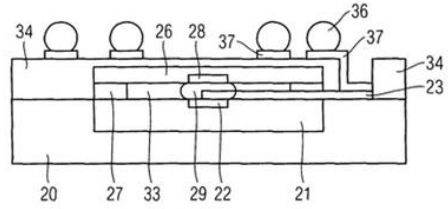
Patents on fan-out wafer level packaging

Polaris Innovations

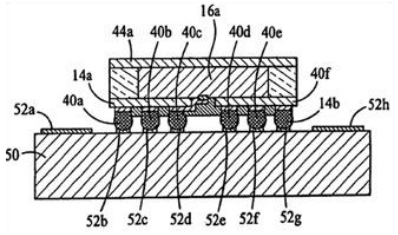


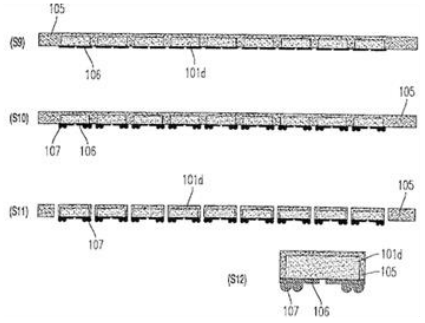


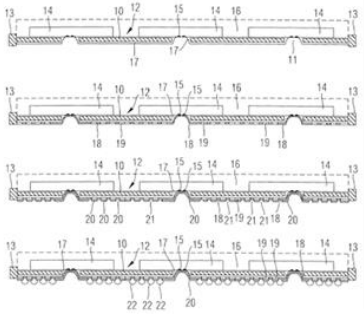




2000 2001 2002 2003 2004 2005







REPORT SAMPLE

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