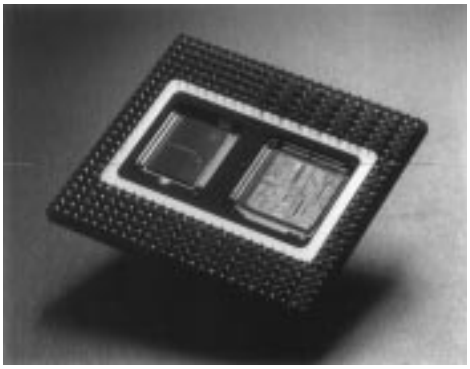
PENTIUM® PRO PROCESSOR AT 150 MHz, 166 MHz, 180 MHz and 200 MHz

- **Available at 150 MHz, 166 MHz, 180 MHz and 200MHz core speeds**
- **Binary compatible with applications running on previous members of the Intel microprocessor family**
- **Optimized for 32-bit applications running on advanced 32-bit operating systems**
- **Dynamic Execution microarchitecture**
- **Single package includes Pentium® Pro processor CPU, cache and system bus interface**
- **Scalable up to four processors and 4 GB memory**
- **Separate dedicated external system bus, and dedicated internal full-speed cache bus**
- **8 KB / 8 KB separate data and instruction, non-blocking, level one cache**
- **Available with integrated 256 KB or 512 KB, non-blocking, level two cache on package**
- **Data integrity and reliability features include ECC, Fault Analysis/Recovery, and Functional Redundancy Checking**
- **Upgradable to a Future OverDrive® processor**

The Pentium® Pro processor family is Intel's next generation of performance for high-end desktops, workstations and servers. The family consists of processors at 150 MHz and higher and is easily scalable to up to four microprocessors in a multiprocessor system. The Pentium Pro processor delivers more performance than previous generation processors through an innovation called Dynamic Execution. This is the next step beyond the superscalar architecture implemented in the Pentium processor. This makes possible the advanced 3D visualization and interactive capabilities required by today's high-end commercial and technical applications and tomorrow's emerging applications. The Pentium Pro processor also includes advanced data integrity, reliability, and serviceability features for mission critical applications.

The Pentium Pro processor may contain design defects or errors known as errata. Current characterized errata are available upon request.



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1.0. INTRODUCTION

The Pentium Pro processor is the next in the Intel386™, Intel486™, and Pentium family of processors. The Pentium Pro processor implements a **Dynamic Execution** microarchitecture—a unique combination of multiple branch prediction, data flow analysis, and speculative execution.

The Pentium Pro processor is upgradable by a future OverDrive® processor and matching voltage regulator module described in Section 8.

Increasing clock frequencies and silicon density can complicate system designs. The Pentium Pro processor integrates several system components which alleviate some of the previous system burdens. The second level cache, cache controller, and the Advanced Programmable Interrupt Controller (APIC) are some of the components that existed in previous Intel processor family systems which are integrated into this single component. This integration results in the Pentium Pro processor bus more closely resembling a symmetric multiprocessing (SMP) system bus rather than resembling a previous generation processor-to-cache bus. This added level of integration and improved performance, results in higher power consumption and a new bus technology. This means it is more important than ever to ensure adherence to this specification.

A significant new feature of the Pentium Pro processor, from a system perspective, is the built-in direct multiprocessing support. In order to achieve multi-processing for up to four processors, and maintain the memory and Input/Output (I/O) bandwidth to support them, new system designs are needed. In creating a system with multiple processors, it is important to consider the additional power burdens and signal integrity issues of supporting up to 8 loads on a high-speed bus.

1.1. Terminology

A '#' symbol after a signal name refers to an active low signal. This means that a signal is in the active state (based on the name of the signal) when driven low. For example, when FLUSH# is low a flush has been requested. When Nonmaskable Interrupt (NMI) is high, a Non-maskable interrupt has occurred. In the case of lines where the name does not imply an active state but describes part of a binary sequence (such as address or data), the '#' symbol implies that the signal is inverted. For example, D[3:0] = 'HLHL' refers to a hex 'A', and D#[3:0] = 'LHLH' also refers to a hex 'A'. (H= High logic level, L= Low logic level)

The word *Preliminary* appears occasionally. Check with your local Field Applications Engineer for recent information.

1.2. References

The following are referenced within this specification:

- *Pentium® Pro Processor I/O Buffer Models*—IBIS Format (On world wide web page http://www.intel.com)
- AP-523, *Pentium® Pro Processor Power Distribution Guidelines* Application Note (Order Number 242764)
- AP-524, *Pentium® Pro Processor GTL+ Layout Guidelines* Application Note (Order Number 242765)
- AP-525, *Pentium® Pro Processor Thermal Design Guidelines* Application Note (Order Number 242766)
- *Pentium® Pro Processor Developer's Manual, Volume 1: Specifications* (Order Number 242690)
- *Pentium® Pro Processor Developer's Manual, Volume 2: Programmer's Reference Manual* (Order Number 242691)
- *Pentium® Pro Processor Developer's Manual, Volume 3: Operating System Writer's Guide* (Order Number 242692)

2.0. PENTIUM® PRO PROCESSOR ARCHITECTURE OVERVIEW

The Pentium Pro processor has a decoupled, 12-stage, superpipelined implementation, trading less work per pipestage for more stages. The Pentium Pro processor also has a pipestage time 33 percent less than the Pentium processor, which helps achieve a higher clock rate on any given process.

The approach used by the Pentium Pro processor removes the constraint of linear instruction sequencing between the traditional "fetch" and

"execute" phases, and opens up a wide instruction window using an instruction pool. This approach allows the "execute" phase of the Pentium Pro processor to have much more visibility into the program's instruction stream so that better scheduling may take place. It requires the instruction "fetch/decode" phase of the Pentium Pro processor to be much more intelligent in terms of predicting program flow. Optimized scheduling requires the fundamental "execute" phase to be replaced by decoupled "dispatch/execute" and "retire" phases. This allows instructions to be started in any order but always be completed in the original program order. The Pentium Pro processor is implemented as three independent engines coupled with an instruction pool as shown in Figure 1.

2.1. Full Core Utilization

The three independent-engine approach was taken to more fully utilize the CPU core. Consider the code fragment in Example :

The first instruction in this example is a load of r1 that, at run time, causes a cache miss. A traditional CPU core must wait for its bus interface unit to read this data from main memory and return it before moving on to instruction 2. This CPU stalls while waiting for this data and is thus being under-utilized.

To avoid this memory latency problem, the Pentium Pro processor "looks-ahead" into its instruction pool at subsequent instructions and will do useful work rather than be stalled. In the example in Example 1, instruction 2 is not executable since it depends upon the result of instruction 1; however, both instructions 3 and 4 are executable. The Pentium Pro processor executes instructions 3 and 4 out-of-order. The results of this out-of-order execution can not be committed to permanent machine state (i.e., the programmer-visible registers) immediately since the original program order must be maintained. The results are instead stored back in the instruction pool awaiting in-order retirement. The core executes instructions depending upon their readiness to execute, and not on their original program order, and is therefore a true dataflow engine. This approach has the side effect that instructions are typically executed out-of-order.

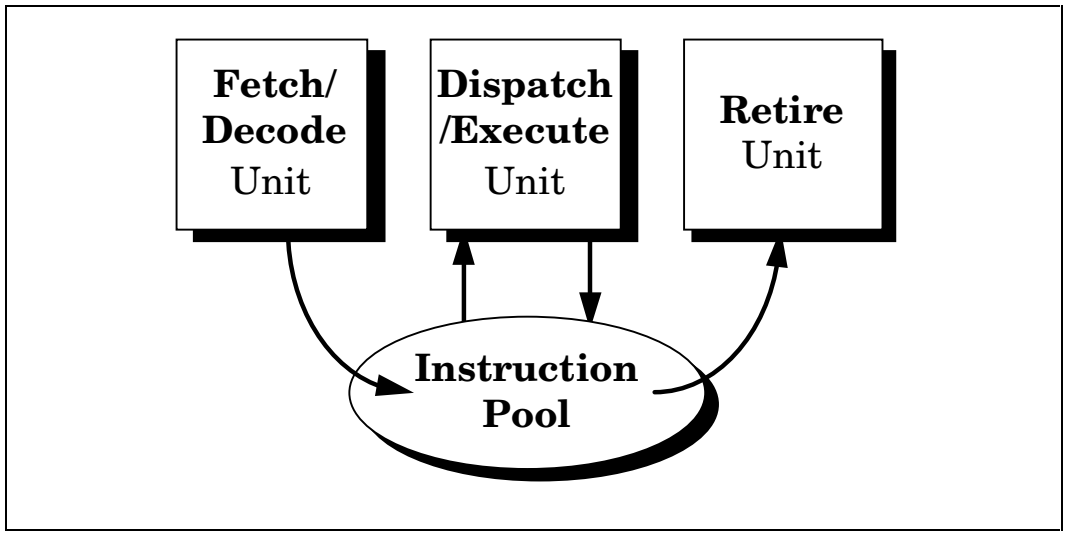

Figure 1. Three Engines Communicating Using an Instruction Pool

Example 1. A Typical Code Fragment

```
r1 <= mem [r0]    /* Instruction 1 */
r2 <= r1 + r2     /* Instruction 2 */
r5 <= r5 + r1     /* Instruction 3 */
r6 <= r6 - r3     /* Instruction 4 */
```

The cache miss on instruction 1 will take many internal clocks, so the Pentium Pro processor core continues to look ahead for other instructions that could be speculatively executed, and is typically looking 20 to 30 instructions in front of the instruction pointer. Within this 20 to 30 instruction window there will be, on average, five branches that the fetch/decode unit must correctly predict if the dispatch/execute unit is to do useful work. The sparse register set of an Intel Architecture (IA) processor will create many false dependencies on registers so the dispatch/execute unit will rename the IA registers into a larger register set to enable additional forward progress. The retire unit owns the programmer's IA register set and results are only committed to permanent machine state in these registers when it removes completed instructions from the pool in original program order.

Dynamic Execution technology can be summarized as optimally adjusting instruction execution by predicting program flow, having the ability to speculatively execute instructions in any order, and then analyzing the program's dataflow graph to choose the best order to execute the instructions.

2.2. The Pentium® Pro Processor Pipeline

In order to get a closer look at how the Pentium Pro processor implements Dynamic Execution, Figure 2 shows a block diagram including cache and memory interfaces. The "Units" shown in Figure 2 represent groups of stages of the Pentium Pro processor pipeline.

- The FETCH/DECODE unit: An in-order unit that takes as input the user program instruction stream from the instruction cache, and decodes them into a series of micro-operations (µops) that represent the dataflow of that instruction stream. The pre-fetch is speculative.
- The DISPATCH/EXECUTE unit: An out-of-order unit that accepts the dataflow stream, schedules execution of the µops subject to data dependencies and resource availability and temporarily stores the results of these speculative executions.
- The RETIRE unit: An in-order unit that knows how and when to commit ("retire") the temporary, speculative results to permanent architectural state.
- The BUS INTERFACE unit: A partially ordered unit responsible for connecting the three internal units to the real world. The bus interface unit communicates directly with the L2 (second level) cache supporting up to four concurrent cache accesses. The bus interface unit also controls a transaction bus, with Modified Exclusive Shared Invalid (MESI) snooping protocol, to system memory.

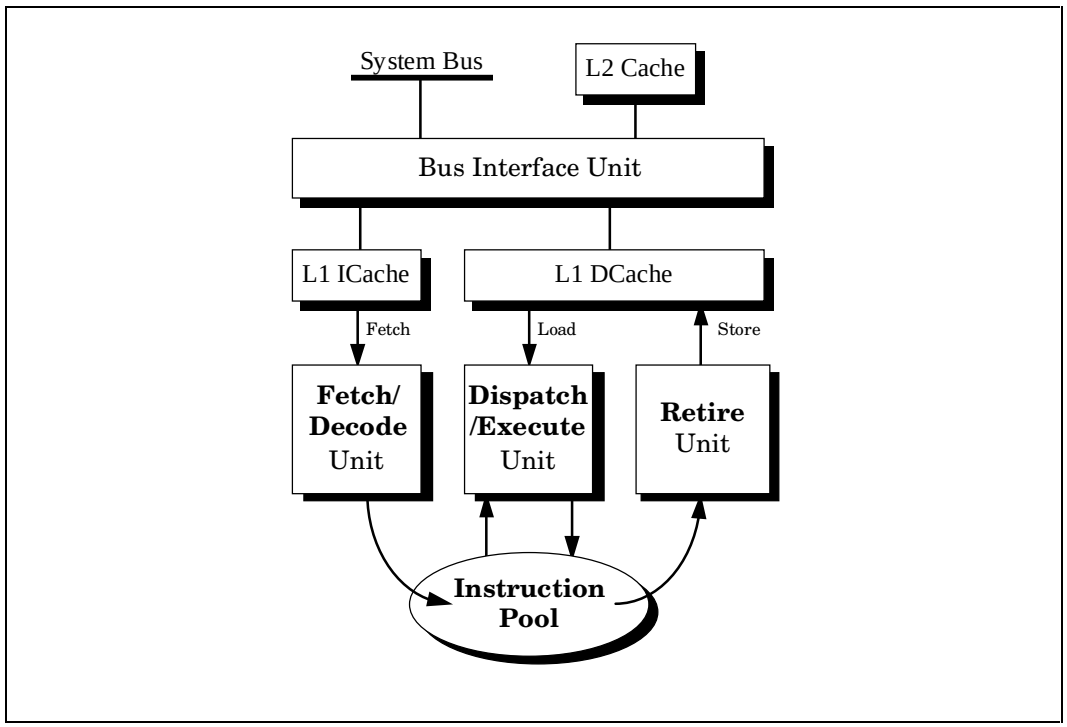

Figure 2. The Three Core Engines Interface with Memory via Unified Caches

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2.2.1. THE FETCH/DECODE UNIT

Figure 3 shows a more detailed view of the Fetch/Decode Unit.

The ICache is a local instruction cache. The Next_IP unit provides the ICache index, based on inputs from the Branch Target Buffer (BTB), trap/interrupt status, and branch-misprediction indications from the integer execution section.

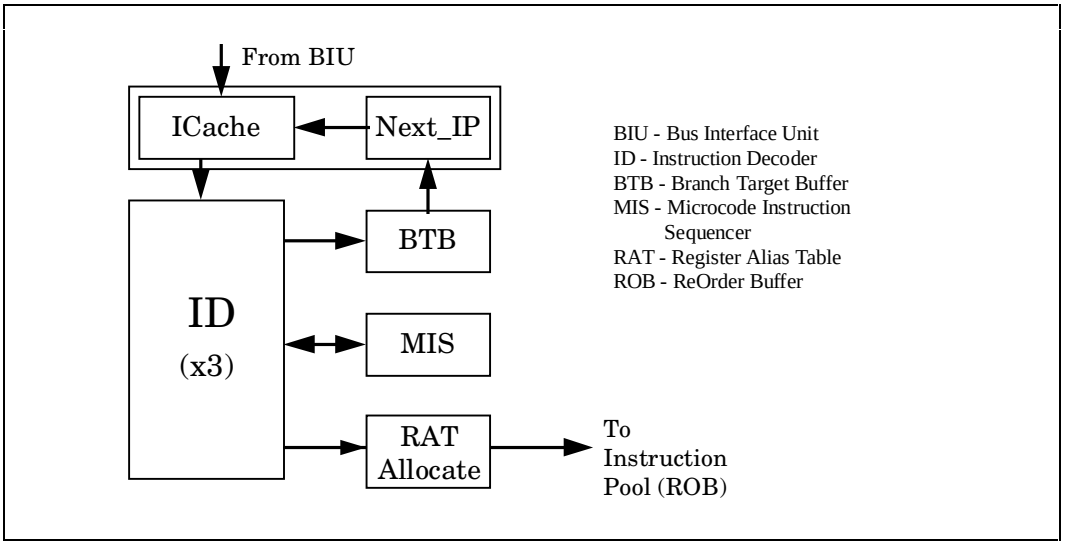


Figure 3. Inside the Fetch/Decode Unit

The ICache fetches the cache line corresponding to the index from the Next_IP, and the next line, and presents 16 aligned bytes to the decoder. The prefetched bytes are rotated so that they are justified for the Instruction Decoders (ID). The beginning and end of the IA instructions are marked.

Three parallel decoders accept this stream of marked bytes, and proceed to find and decode the IA instructions contained therein. The decoder converts the IA instructions into triadic µops (two logical sources, one logical destination per µop). Most IA instructions are converted directly into single µops, some instructions are decoded into one-to-four µops and the complex instructions require microcode (the box labeled MIS in Figure 3). This microcode is just a set of preprogrammed sequences of normal µops. The µops are queued, and sent to the Register Alias Table (RAT) unit, where the logical IA-based register references are converted into Pentium Pro processor physical register references, and to the Allocator stage, which adds status information to the µops and enters them into the instruction pool. The instruction pool is implemented as an array of Content Addressable Memory called the ReOrder Buffer (ROB).

This is the end of the in-order pipe.

2.2.2. THE DISPATCH/EXECUTE UNIT

The dispatch unit selects µops from the instruction pool depending upon their status. If the status indicates that a µop has all of its operands then the dispatch unit checks to see if the execution resource needed by that µop is also available. If both are true, the **Reservation Station** removes that µop and sends it to the resource where it is executed. The results of the µop are later returned to the pool. There are five ports on the Reservation Station, and the multiple resources are accessed as shown in Figure 4.

The Pentium Pro processor can schedule at a peak rate of 5 µops per clock, one to each resource port, but a sustained rate of 3 µops per clock is typical. The activity of this scheduling process is the out-of-order process; µops are dispatched to the execution resources strictly according to dataflow constraints and resource availability, without regard to the original ordering of the program.

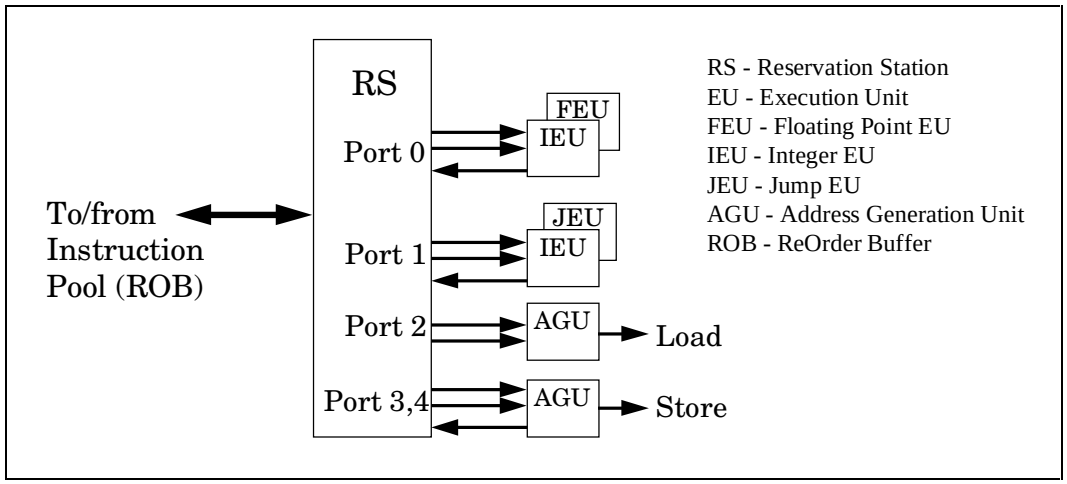


Figure 4. Inside the Dispatch/Execute Unit

Note that the actual algorithm employed by this execution-scheduling process is vitally important to performance. If only one µop per resource becomes data-ready per clock cycle, then there is no choice. But if several are available, it must choose. The Pentium Pro processor uses a pseudo First In, First Out (FIFO) scheduling algorithm favoring back-to-back µops.

Note that many of the µops are branches. The BTB will correctly predict most of these branches but it can't correctly predict them all. Consider a BTB that is correctly predicting the backward branch at the bottom of a loop; eventually that loop is going to terminate, and when it does, that branch will be mispredicted. Branch µops are tagged (in the in-order pipeline) with their fall-through address and the destination that was predicted for them. When the branch executes, what the branch actually did is compared against what the prediction hardware said it would do. If those coincide, then the branch eventually retires, and most of the speculatively executed work behind it in the instruction pool is good.

But if they do not coincide, then the Jump Execution Unit (JEU) changes the status of all of the µops behind the branch to remove them from the instruction pool. In that case the proper branch destination is provided to the BTB which restarts the whole pipeline from the new target address.

2.2.3. THE RETIRE UNIT

Figure 5 shows a more detailed view of the Retire Unit.

The retire unit is also checking the status of µops in the instruction pool. It is looking for µops that have executed and can be removed from the pool. Once removed, the original architectural target of the µops is written as per the original IA instruction. The retirement unit must not only notice which µops are complete, it must also reimpose the original program order on them. It must also do this in the face of interrupts, traps, faults, breakpoints and mispredictions.

The retirement unit must first read the instruction pool to find the potential candidates for retirement and determine which of these candidates are next in the original program order. Then it writes the results of this cycle's retirements to both the Instruction Pool and the Retirement Register File (RRF). The retirement unit is capable of retiring 3 µops per clock.

2.2.4. THE BUS INTERFACE UNIT

Figure 6 shows a detailed view of the Bus Interface Unit.

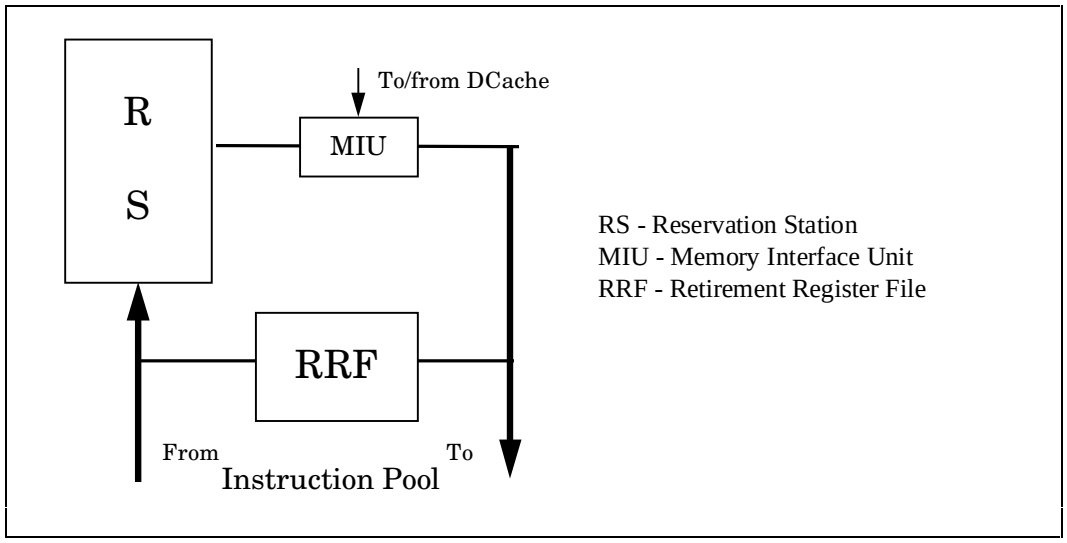


Figure 5. Inside the Retire Unit

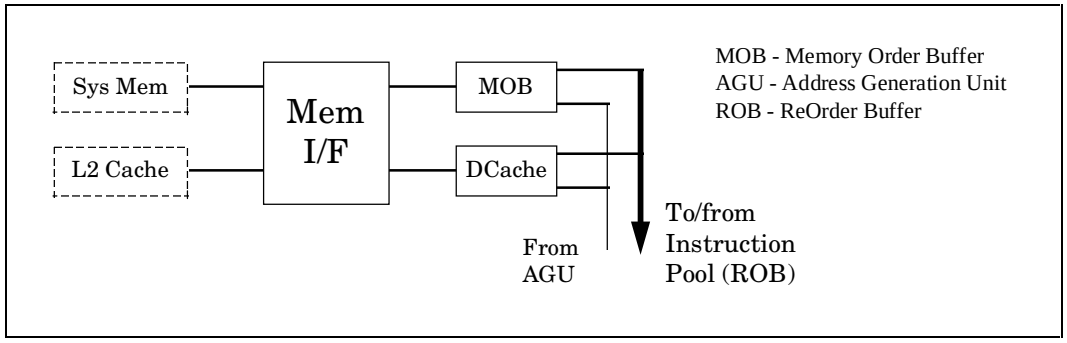


Figure 6. Inside the Bus Interface Unit

There are two types of memory access: loads and stores. Loads only need to specify the memory address to be accessed, the width of the data being retrieved, and the destination register. Loads are encoded into a single µop.

Stores need to provide a memory address, a data width, and the data to be written. Stores therefore require two µops, one to generate the address, and one to generate the data. These µops must later re-combine for the store to complete.

Stores are never performed speculatively since there is no transparent way to undo them. Stores are also never reordered among themselves. A store is dispatched only when both the address and the data are available and there are no older stores awaiting dispatch.

A study of the importance of memory access reordering concluded:

- Stores must be constrained from passing other stores, for only a small impact on performance.

- Stores can be constrained from passing loads, for an inconsequential performance loss.
- Constraining loads from passing other loads or stores has a significant impact on performance.

The Memory Order Buffer (MOB) allows loads to pass other loads and stores by acting like a reservation station and re-order buffer. It holds suspended loads and stores and re-dispatches them when a blocking condition (dependency or resource) disappears.

2.3. Architecture Summary

Dynamic Execution is this combination of improved branch prediction, speculative execution and data flow analysis that enables the Pentium Pro processor to deliver its superior performance.

3.0. ELECTRICAL SPECIFICATIONS

3.1. The Pentium® Pro Processor Bus and V_{REF}

Most of the Pentium Pro processor signals use a **variation** of the low voltage Gunning Transceiver Logic (GTL) signaling technology.

The Pentium Pro processor bus specification is similar to the GTL specification but has been enhanced to provide larger noise margins and reduced ringing. This is accomplished by increasing the termination voltage level and controlling the edge rates. Because this specification is different from the standard GTL specification, it is refered to as **GTL+** in this document.

The GTL+ signals are open-drain and require external termination to a supply that provides the high signal level. The GTL+ inputs use differential receivers which require a reference signal (V_{REF}). Termination (usually a resistor on each end of the signal trace) is used to pull the bus up to the high voltage level and to control reflections on the stub-free transmission line. V_{REF} is used by the receivers to determine if a signal is a logical 0 or a logical 1. See Table 8 for the bus termination voltage specifications for GTL+, and Section 4 for the GTL+ Interface Specification.

There are 8 V_{REF} pins on the Pentium Pro processor to ensure that internal noise will not affect the performance of the I/O buffers. Pins A1, C7, S7 and Y7 (V_{REF}[3:0]) must be tied together and pins A47, U41, AE47 and AG45 (V_{REF}[7:4]) must be tied together. The two groups may also be tied to each other if desired.

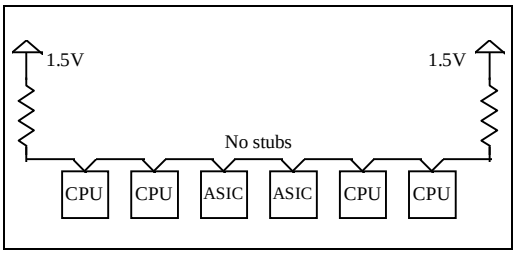


Figure 7. GTL+ Bus Topology

The GTL+ bus depends on incident wave switching. Therefore timing calculations for GTL+ signals are based on **flight time** as opposed to capacitive deratings. Analog signal simulation of the Pentium Pro processor bus including trace lengths is highly recommended when designing a system with a heavily loaded GTL+ bus. See Intel's world wide web page (http:\\www.intel.com) to download the buffer models for the Pentium Pro processor in IBIS format.

3.2. Power Management: Stop Grant and Auto HALT

The Pentium Pro processor allows the use of Stop Grant and Auto HALT modes to immediately reduce the power consumed by the device. When enabled, these cause the clock to be stopped to most of the CPU's internal units and thus significantly reduces power consumption by the CPU as a whole.

Stop Grant is entered by asserting the STPCLK# pin of the Pentium Pro processor. When STPCLK# is recognized by the Pentium Pro processor, it will stop execution and will not service interrupts. It will continue snooping the bus. Stop Grant power is specified assuming no snoop hits occur.

Auto HALT is a low-power state entered when the Pentium Pro processor executes a halt (HLT) instruction. In this state, the Pentium Pro processor behaves as if it executed a halt instruction, and it additionally powers-down most internal units. In Auto

HALT, the Pentium Pro processor will recognize all interrupts and snoops. Auto HALT power is specified assuming no snoop hits or interrupts occur.

The low-power stand-by mode of Stop Grant or Auto HALT can be defined by a **Low-Power Enable** configuration bit to be either the lowest power achievable by the Pentium Pro processor (Stop Grant power), or a power state in which the clock distribution is left running (Idle power). "Low-power stand-by" *disabled* leaves the core logic running, while "Low-power stand-by" **enabled** allows the Pentium Pro processor to enter its lowest power mode.

3.3. Power and Ground Pins

As future versions of the Pentium Pro processor are released, the operating voltage of the CPU die and of the L2 cache die may differ from each other. There are two groups of power inputs on the Pentium Pro processor package to support the possible voltage difference between the two die in the package, and one 5 V pin to support a fan for the OverDrive processor. There are also 4 pins defined on the package for voltage identification (VID). These pins specify the voltage required by the CPU die. These have been added to cleanly support voltage specification variations on the Pentium Pro processor and future processors. See Section 3.6. for an explanation of the voltage identification pins.

Future mainstream devices will fall into two groups. Either the CPU die and the L2 Cache die will both run at the same voltage ($V_{CC}P$), or the L2 Cache die will use $V_{CC}S$ (3.3V) while the CPU die runs at another voltage on $V_{CC}P$. When the L2 cache die is running on the same supply as the CPU die, the $V_{CC}S$ pins will consume no current. To properly support this, the system should distribute 3.3 V and a selectable voltage to the Pentium Pro processor socket. Selection may be provided for by socketed regulation or by using the VID pins. Note that it is possible that $V_{CC}P$ and $V_{CC}S$ are both nominally 3.3 V. It should not be assumed that these will be able to use the same power supply.

For clean on-chip power distribution, the Pentium Pro processor has 76 V_{CC} (power) and 101 V_{SS} (ground) inputs. The 76 V_{CC} pins are further divided to provide the different voltage levels to the device. $V_{CC}P$ inputs for the CPU die and some L2 die account for 47 of the V_{CC} pins, while 28 $V_{CC}S$ inputs (3.3V) are for use by the on-package L2 cache die of some processors. One $V_{CC}5$ pin is provided for use by the fan of the OverDrive processor. $V_{CC}5$, $V_{CC}S$ and $V_{CC}P$ must remain electrically separated from each other. On the circuit board, *all* $V_{CC}P$ pins must be connected to a voltage island and *all* $V_{CC}S$ pins must be connected to a separate voltage island (an island is a portion of a power plane that has been divided, or an entire plane). Similarly, *all* V_{SS} pins must be connected to a system ground plane. See Figure 44 for the locations of power and ground pins.

3.4. Decoupling Recommendations

Due to the large number of transistors and high internal clock speeds, the Pentium Pro processor can create large, short duration transient (switching) current surges that occur on internal clock edges which can cause power planes to spike above and below their nominal value if not properly controlled. The Pentium Pro processor is also capable of generating large average current swings between low and full power states, called **Load-Change Transients**, which can cause power planes to sag below their nominal value if bulk decoupling is not adequate. See Figure 8 for an example of these current fluctuations. Care must be taken in the board design to guarantee that the voltage provided to the Pentium Pro processor remains within the specifications listed in this volume. Failure to do so may result in timing violations and/or a reduced lifetime of the component.

Adequate decoupling capacitance should be placed near the power pins of the Pentium Pro processor. Low inductance capacitors such as the 1206 package surface mount capacitors are recommended for the best high frequency electrical performance. Forty (40) 1µF 1206-style capacitors with a ±22% tolerance make a good starting point for simulations as this is our recommended decoupling when using a standard Pentium Pro Voltage Regulator Module. Inductance should be reduced by connecting capacitors directly to the $V_{CC}P$ and V_{SS} planes with minimal trace length between the component pads and vias to the plane. Be sure to include the effects of board inductance within the simulation. Also, when choosing the capacitors to use, bear in mind the operating temperatures they will see and the tolerance that they are rated at. Type Y5S or better are recommended (±22% tolerance over the temperature range -30°C to +85°C).

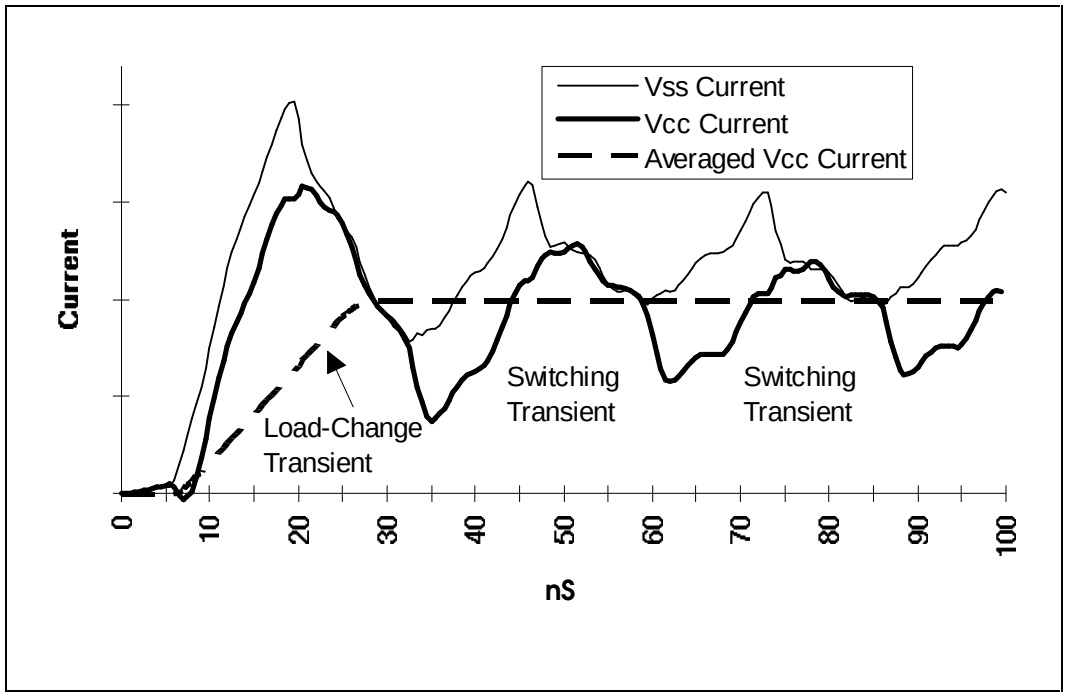


Figure 8. Transient Types

Bulk capacitance with a low Effective Series Resistance (ESR) should also be placed near the Pentium Pro processor in order to handle changes in average current between the low-power and normal operating states. About 4000uF of capacitance with an ESR of 5mΩ makes a good starting point for simulations, although more capacitance may be needed to bring the ESR down to this level due to the current technology in the industry. The standard Pentium Pro Voltage Regulator Modules already contain this bulk capacitance. Be sure to determine what is available on the market before choosing parameters for the models. Also, include power supply response time and cable inductance in a full simulation.

See *AP-523 Pentium® Pro* Processor *Power Distribution Guidelines* Application Note (Order Number 242764) for power modeling for the Pentium Pro processor.

3.4.1. $V_{CC}S$ DECOUPLING

Decoupling of ten (10) 1µF ceramic capacitors (type Y5S or better) and a minimum of five 22µF tantalum capacitors is recommended for the $V_{CC}S$ pins. This is to handle the transients that will occur in future devices.

3.4.2. GTL+ DECOUPLING

Although the Pentium Pro GTL+ processor bus receives power external to the Pentium Pro processor, it should be noted that this power supply will also require the same diligent decoupling methodologies as the processor. Notice that the existence of external power entering through the I/O buffers causes V_{SS} current to be higher than the V_{CC} current as evidenced in Figure 8.

3.4.3. PHASE LOCK LOOP (PLL) DECOUPLING

Isolated analog decoupling is required for the internal PLL. This should be equivalent to 0.1µF of ceramic capacitance. The capacitor should be type Y5R or better and should be across the PLL1 and PLL2 pins of the Pentium Pro processor. ("Y5R" implies ±15% tolerance over the temperature range -30°C to +85°C.)

3.5. BCLK Clock Input Guidelines

The BCLK input directly controls the operating speed of the GTL+ bus interface. All GTL+ external timing parameters are specified with respect to the rising edge of the BCLK input. Clock multiplying within the processor is provided by an internal Phase Lock Loop (PLL) which requires a constant frequency BCLK input. Therefore the BCLK frequency cannot be changed dynamically. It can however be changed when RESET# is active assuming that all reset specifications are met for the clock and the configuration signals.

The Pentium Pro processor core frequency must be configured during reset by using the A20M#, IGNNE#, LINT1/NMI, and LINT0/INTR pins. The value on these pins during RESET#, and until two clocks beyond the end of the RESET# pulse, determines the multiplier that the PLL will use for the internal core clock. See the Appendix A for the definition of these pins during reset. At all other times their functionality is defined as the compatibility signals that the pins are named after. These signals are 3.3 V tolerant and may be driven by existing logic devices. This is important for both functions of the pins.

Supplying a bus clock multiplier this way is required in order to increase processor performance without changing the processor design, and to maintain the bus frequency such that system boards can be designed to function properly as CPU frequencies increase.

3.5.1. SETTING THE CORE CLOCK TO BUS CLOCK RATIO

Table 44 lists the configuration pins and the values that must be driven at reset time in order to set the core clock to bus clock ratio. Figure 9 shows the timing relationship required for the clock ratio signals with respect to RESET# and BCLK. CRESET# from an 82453GX (or 82453KX) is shown since its timing is useful for controlling the multiplexing function that is required for sharing the pins.

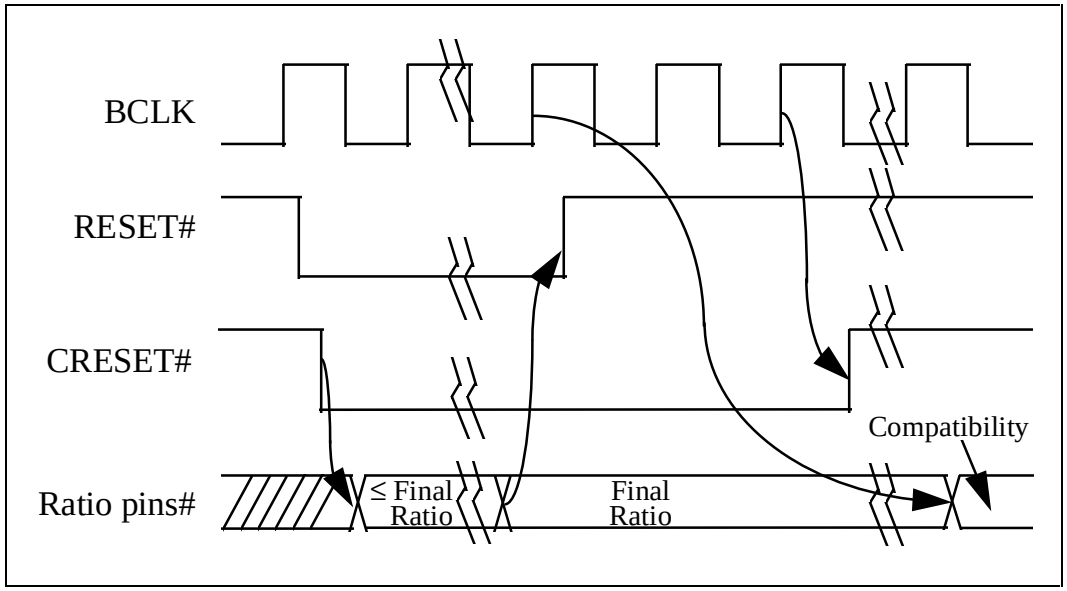


Figure 9. Timing Diagram of Clock Ratio Signals

Using CRESET# (CMOS reset), the circuit in Figure 10 can be used to share the pins. The pins of the processors are bussed together to allow any one of them to be the compatibility processor. The component used as the multiplexer must not have outputs that drive higher than 3.3 V in order to meet the Pentium Pro processor's 3.3 V tolerant buffer specifications. The multiplexer output current should be limited to 200mA maximum, in case the $V_{CC}P$ supply to the processor ever fails.

The pull-down resistors between the multiplexer and the processor (1KΩ) force a ratio of 2x into the processor in the event that the Pentium Pro processor powers up before the multiplexer and/or the chip set. This prevents the processor from ever seeing a ratio higher than the final ratio.

If the multiplexer were powered by $V_{CC}P$, CRESET# would still be unknown until the 3.3 V supply came up to power the CRESET# driver. A pull-down can be used on CRESET# instead of the four between the multiplexer and the Pentium Pro processor. In this case, the multiplexer must be designed such that the compatibility inputs are truly ignored as their state is unknown.

In any case, the compatibility inputs to the multiplexer must meet the input specifications of the multiplexer. This may require a level translation before the multiplexer inputs unless the inputs and the signals driving them are already compatible.

For FRC mode processors, one multiplexer will be needed per FRC pair, and the multiplexer will need to be clocked using BCLK to meet setup and hold times to the processors. This may require the use of high speed programmable logic.

3.5.2. MIXING PROCESSORS OF DIFFERENT FREQUENCIES

Mixing components of different internal clock frequencies is not fully supported and has not been validated by Intel. One should also note when attempting to mix processors rated at different frequencies in a multiprocessor system that a *common* bus clock frequency and a set of multipliers must be found that is acceptable to all processors in the system. Of course, a processor may be run at a core frequency as low as its minimum rating. Operating system support for multi-processing with mixed frequency components should also be considered.

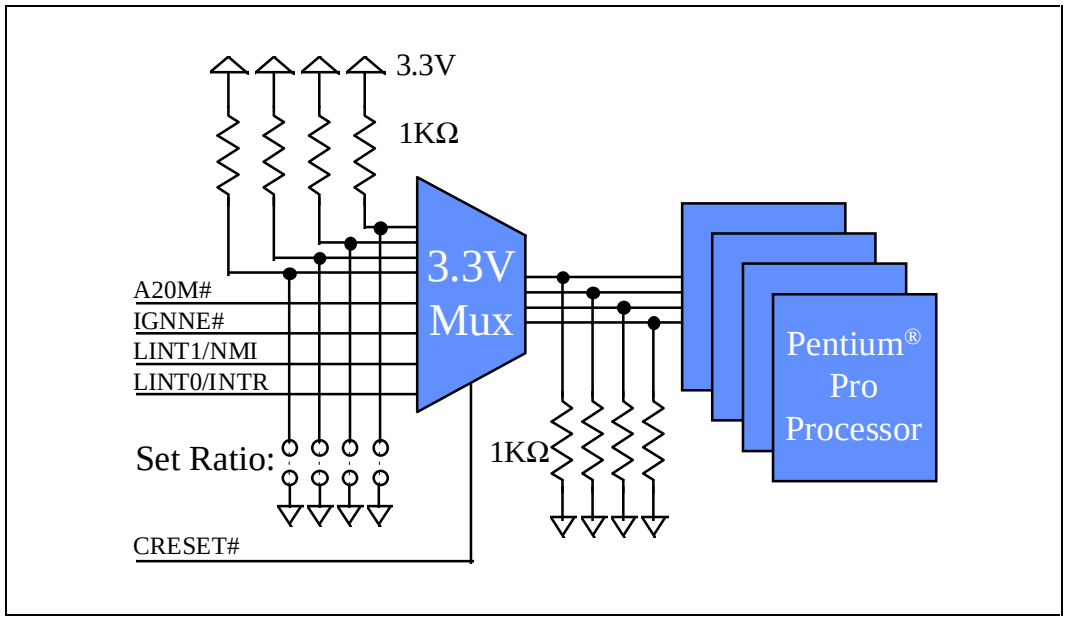


Figure 10. Example Schematic for Clock Ratio Pin Sharing

Note:

In order to support different frequency multipliers to each processor, the design shown above would require four multiplexers

3.6. Voltage Identification

There are four Voltage Identification Pins on the Pentium Pro processor package. These pins can be used to support automatic selection of power supply voltage. These pins are not *signals* but are each either an open circuit in the package or a short circuit to V_{SS}.

The opens and shorts define the voltage required by the processor. This has been added to cleanly support voltage specification variations on future Pentium Pro processors. These pins are named VID0 through VID3 and the definition of these pins is shown in Table 1. A '1' in this table refers to an open pin and '0' refers to a short to ground. **The $V_{CC}P$ power supply should supply the voltage that is requested *or* disable itself**.

Table 1. Voltage Identification Definition [1,2]

VID[3:0]	Voltage Setting	VID[3:0]	Voltage Setting
0000	3.5	1000	2.7
0001	3.4	1001	2.6
0010	3.3	1010	2.5
0011	3.2	1011	2.4
0100	3.1	1100	2.3
0101	3.0	1101	2.2
0110	2.9	1110	2.1
0111	2.8	1111	No CPU Present

NOTES:

1. Nominal setting requiring regulation to ±5% at the Pentium® Pro processor $V_{CC}P$ pins under all conditions. Support not expected for 2.1V—2.3V.
2. 1= Open circuit; 0= Short to V_{SS}

Support for a wider range of VID settings will benefit the system in meeting the power requirements of future Pentium Pro processors. Note that the '1111' (or all opens) ID can be used to detect the absence of a processor in a given socket as long as the power supply used does not affect these lines.

To use these pins, they may need to be pulled up by an external resistor to another power source. The power source chosen should be one that is guaranteed to be stable whenever the supply to the voltage regulator is stable. This will prevent the possibility of the Pentium Pro processor supply running up to 3.5 V in the event of a failure in the supply for the VID lines. Note that the specification for the standard Pentium Pro Voltage Regulator Modules allows the use of these signals either as TTL compatible levels or as opens and shorts. Using them as TTL compatible levels will require the use of pull-up resistors to 5 V if the input voltage to the regulator is 5 V and the use of a voltage divider if the input voltage to the regulator is 12 V. The resistors chosen should not cause the current through a VID pin to exceed its specification in Table 3. There must not be any other components on these signals if the VRM uses them as opens and shorts.

3.7. JTAG Connection

The debug port described in the *Pentium® Pro Processor Developer's Manual, Volume 1: Specifications* (Order Number 242690) should be at the start and end of the JTAG chain with TDI to the first component coming from the Debug Port and TDO from the last component going to the Debug Port. The recommended pull-up value for Pentium Pro processor TDO pins is 240Ω.

Due to the voltage levels supported by the Pentium Pro processor JTAG logic, it is recommended that the Pentium Pro processors and any other 3.3 V logic level components within the system be first in the JTAG chain. A translation buffer should be used to connect to the rest of the chain unless a 5 V component can be used next that is capable of accepting a 3.3 V input. Similar considerations must be made for TCK, TMS and TRST#. Components may need these signals buffered to match required logic levels.

In a multiprocessor system, be cautious when including empty Pentium Pro processor sockets in the scan chain. All sockets in the scan chain must have a processor installed to complete the chain or the system must support a method to bypass the empty sockets.

See the *Pentium® Pro Processor Developer's Manual, Volume 1: Specifications* (Order Number 242690) for full information on putting a debug port in the JTAG chain.

3.8. Signal Groups

In order to simplify the following discussion, signals have been combined into groups by buffer type. **All outputs are open drain** and require an external high-level source provided externally by the termination or a pull-up resistor.

GTL+ input signals have differential input buffers which use V_{REF} as their reference signal. GTL+ output signals require termination to 1.5 V. Later in this document, the term "GTL+ Input" refers to the GTL+ input group as well as the GTL+ I/O group when receiving. Similarly, "GTL+ Output" refers to the GTL+ output group as well as the GTL+ I/O group when driving.

The 3.3 V tolerant, Clock, APIC and JTAG inputs can each be driven from ground to 3.3V. The 3.3 V tolerant, APIC, and JTAG outputs can each be pulled high to as much as 3.3 V. See Table 7 for specifications.

The groups and the signals contained within each group are shown in Table 2. Note that the signals ASZ[1:0]#, ATTR[7:0]#, BE[7:0]#, BREQ#[3:0], DEN#, DID[7:0]#, DSZ[1:0]#, EXF[4:0]#, LEN[1:0]#, SMMEM#, and SPLCK# are all GTL+ signals that are shared onto another pin. Therefore they do not appear in this table.

3.8.1. ASYNCHRONOUS VS. SYNCHRONOUS

All GTL+ signals are synchronous. All of the 3.3 V tolerant signals can be applied asynchronously, except when running two processors in FRC mode. To run in FRC mode, synchronization logic is required on all signals, (except PWRGOOD) going to

both processors. Also note the timing requirements for PICCLK with respect to BCLK. With FRC enabled, PICCLK must be ¼X BCLK and synchronized with respect to BCLK. PICCLK must always lag BCLK by at least 1 ns and no more than 5 ns.

Table 2. Signal Groups

Group Name	Signals
GTL+ Input	BPRI#, BR[3:1]#[1], DEFER#, RESET#, RS[2:0]#, RSP#, TRDY#
GTL+ Output	PRDY#
GTL+ I/O	A[35:3]#, ADS#, AERR#, AP[1:0]#, BERR#, BINIT#, BNR#, BP[3:2]#, BPM[1:0]#, BR0#, D[63:0]#, DBSY#, DEP[7:0]#, DRDY#, FRCERR, HIT#, HITM#, LOCK#, REQ[4:0]#, RP#
3.3 V Tolerant Input	A20M#, FLUSH#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PREQ#, PWRGOOD[2], SMI#, STPCLK#
3.3 V Tolerant Output	FERR#, IERR#, THERMTRIP#[3]
Clock[4]	BCLK
APIC Clock[4]	PICCLK
APIC I/O[4]	PICD[1:0]
JTAG Input[4]	TCK, TDI, TMS, TRST#
JTAG Output[4]	TDO
Power/Other[5]	CPUPRES#, PLL1, PLL2, TESTHI, TESTLO, UP#, $V_{CC}P$, $V_{CC}S$, $V_{CC}5$, VID[3:0], V_{REF}[7:0], V_{SS}

NOTES:

1. The BR0# pin is the only BREQ# signal that is bi-directional. The internal BREQ# signals are mapped onto BR# pins after the agent ID is determined.
2. See PWRGOOD in Section 3.9.
3. See THERMTRIP# in Section 3.10.
4. These signals are tolerant to 3.3V. Use a 150Ω pull-up resistor on PICD[1:0] and 240Ω on TDO.
5. CPUPRES# is a ground pin defined to allow a designer to detect the presence of a processor in a socket. (preliminary)
   PLL1 and PLL2 are for decoupling the internal PLL (See Section 3.4.3.).
   TESTHI pins should be tied to VCCP. A 10K pull-up may be used. See Section 3.11.
   TESTLO pins should be tied to V_{SS}. A 1K pull-down may be used. See Section 3.11.
   UP# is an open in the Pentium® Pro processor and tied to V_{SS} in the OverDrive® processor (see Section 8.3.2 for usage).
   $V_{CC}P$ is the primary power supply.
   $V_{CC}S$ is the secondary power supply used by some versions of the second level cache.
   $V_{CC}5$ is unused by Pentium Pro processor and is used by the OverDrive processor for fan/heatsink power. See Section 8.
   VID[3:0] lines are described in Section 3.6.
   V_{REF} [7:0] are the reference voltage pins for the GTL+ buffers.
   V_{SS} is ground.

3.9. PWRGOOD

PWRGOOD is a 3.3 V tolerant input. It is expected that this signal will be a **clean** indication that clocks and the system 3.3 V, 5 V and $V_{CC}P$ supplies are stable and within their specifications. Clean implies that the signal will remain low, (capable of sinking leakage current) without glitches, from the time that the power supplies are turned on until they come within specification. The signal will then transition monotonically to a high (3.3 V) state. Figure 11 illustrates the relationship of PWRGOOD to other system signals. PWRGOOD can be driven inactive at any time, but power and clocks must again be stable before the rising edge of PWRGOOD. It must also meet the minimum pulse width specification in Table 13 and be followed by a 1mS RESET# pulse.

This signal must be supplied to the Pentium Pro processor as it is used to protect internal circuits against voltage sequencing issues. Use of this signal is recommended for added reliability.

This signal does not need to be synchronized for FRC operation. It should remain high throughout boundary scan testing.

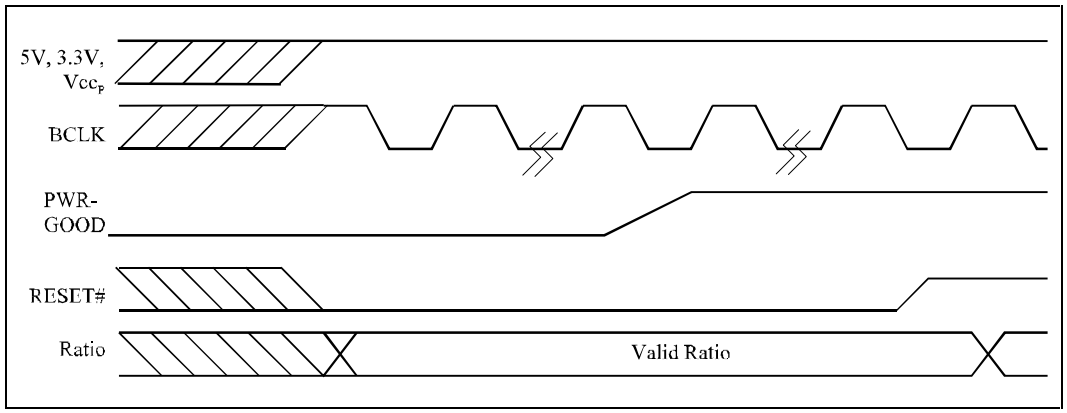


Figure 11. PWRGOOD Relationship at Power-On

3.10. THERMTRIP#

The Pentium Pro processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds ~135°C. This is signaled to the system by the THERMTRIP# pin. Once activated, the signal remains latched, and the processor stopped, until RESET# goes active. There is no hysteresis built into the thermal sensor itself, so as long as the die temperature drops below the trip level, a RESET# pulse will reset the processor and execution will continue. If the temperature has not dropped beyond the trip level, the processor will continue to drive THERMTRIP# and remain stopped.

3.11. Unused Pins

All RESERVED pins must remain unconnected. All pins named TESTHI must be pulled up, no higher than $V_{CC}P$, and may be tied directly to $V_{CC}P$. All pins named TESTLO must be pulled low and may be tied directly to V_{SS}.

PICCLK must be driven with a clock input, and the PICD[1:0] lines must each be pulled-up to 3.3 V with a separate 150Ω resistor, even when the APIC will not be used.

For reliable operation, always connect unused inputs to an appropriate signal level. Unused GTL+ inputs should be pulled-up to V_{TT}. Unused active low 3.3 V tolerant inputs should be connected to 3.3 V with a 150Ω resistor and unused active high inputs should

be connected to ground (V_{SS}). A resistor must also be used when tying bi-directional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for fully testing the processor after board assembly.

For unused pins, it is suggested that ~10KΩ resistors be used for pull-ups (except for PICD[1:0] discussed above), and ~1KΩ resistors be used as pull-downs. **Never tie a pin directly to a supply other than the processor's own V_{CC}P supply or to V_{SS}.**

3.12. Maximum Ratings

Table 3 contains Pentium Pro processor stress ratings only. Functional operation at the absolute maximum and minimum is not implied nor guaranteed. The Pentium Pro processor should not receive a clock while subjected to these conditions. Functional operating conditions are given in the AC and DC tables. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the Pentium Pro processor contains protective circuitry to resist damage from static electric discharge, one should always take precautions to avoid high static voltages or electric fields.

Table 3. Absolute Maximum Ratings[1]

Symbol	Parameter	Min	Max	Unit	Notes
$T_{Storage}$	Storage Temperature	-65	150	°C	
T_{Bias}	Case Temperature under Bias	-65	110	°C	
V_{CC}P(Abs)	Primary Supply Voltage with respect to V_{SS}	-0.5	Operating Voltage + 1.4	V	2
V_{CC}S(Abs)	3.3 V Supply Voltage with respect to V_{SS}	-0.5	4.6	V	
V_{CC}P-V_{CC}S	Primary Supply Voltage with respect to Secondary Supply	-3.7	Operating Voltage + 0.4	V	2
V_{IN}	GTL+ Buffer DC Input Voltage with respect to V_{SS}	-0.5	V_{CC}P+ 0.5 but Not to exceed 4.3	V	3
V_{IN3}	3.3 V Tolerant Buffer DC Input Voltage with respect to V_{SS}	-0.5	V_{CC}P+ 0.9 but Not to exceed 4.7	V	4
I_I	Maximum input current		200	mA	5
I_{VID}	Maximum VID pin current		5	mA	

NOTES:

1. Functional operation at the absolute maximum and minimum is not implied or guaranteed.
2. Operating voltage is the voltage that the component is designed to operate at. See Table 4.
3. Parameter applies to the GTL+ signal groups only.
4. Parameter applies to 3.3 V tolerant, APIC, and JTAG signal groups only.
5. Current may flow through the buffer ESD diodes when VIH > VCCP+1.1V, as in a power supply fault condition or while power supplies are sequencing. Thermal stress should be minimized by cycling power off if the V_{CC}P supply fails.

3.13. DC Specifications

Table 9 through Table 7 list the DC specifications associated with the Pentium Pro processor. Specifications are valid only while meeting the processor specifications for case temperature, clock frequency and input voltages. **Care should be taken to read all notes associated with each parameter.** See Section 3.3. for an explanation of voltage plans for Pentium Pro processors. See Section 8.4.1.1. for OverDrive processor information and Section 3.16 for flexible motherboard recommendations.

The DC specifications for the $V_{CC}P$, $V_{CC}S$, and $V_{CC}5$ supplies are listed in Table 4 and Table 5.

Most of the signals on the Pentium Pro processor are in the GTL+ signal group. These signals are specified to be terminated to 1.5V. The DC specifications for these signals are listed in Table 6. Care should be taken to read all notes associated with each parameter.

To allow compatibility with other devices, some of the signals are 3.3 V tolerant and can therefore be terminated or driven to 3.3V. The DC specifications for these 3.3 V tolerant inputs are listed in Table 7. Care should be taken to read all notes associated with each parameter.

Table 4. Voltage Specification

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$V_{CC}P$	Primary V_{CC}	2.945 3.135	3.1 3.3	3.255 3.465	V V	@150 MHz, 1 @ 166, 180 & 200 MHz
$V_{CC}S$	Secondary V_{CC}	3.135	3.3	3.465	V	3.3 ± 5%, 2
$V_{CC}5$	5 V Supply	4.75	5.0	5.25	V	5.0 ± 5%, 3

NOTES:

1. This is a 5% tolerance. To comply with these guidelines and the industry standard voltage regulator module specifications, the equivalent of forty (40) 1 µF±22% capacitors in 1206 packages should be placed near the power pins of the processor. More specifically, at least 40 µF of capacitance should exist on the power plane with less than 250pH of inductance and 4mΩ of resistance between it and the pins of the processor assuming a regulator set point of ±1%.
2. This voltage is currently not required by the Pentium Pro processor. The voltage is defined for future use.
3. This voltage is required for OverDrive processor support.

Table 5. Power Specifications [1]

Symbol	Parameter	Min	Typ	Max	Unit	Notes
P_{Max}	Thermal Design Power		23.0 27.5 24.8 27.3 32.6	29.2 35.0 31.7 35.0 37.9	W W W W W	@ 150 MHz, 256K L2 @ 166 MHz, 512K L2 @ 180 MHz, 256K L2 @ 200 MHz, 256K L2 @ 200 MHz, 512K L2 2, 3
I_{SGntP}	$V_{CC}P$ Stop Grant Current	0.3 0.3		1.0 1.2	A A	@ 150 MHz, 256K L2 All other components 3, 4, 5
I_{SGntS}	$V_{CC}S$ Stop Grant Current	0		0	A	All frequencies
$I_{CC}P$	$V_{CC}P$ Current			9.9 11.2 10.1 11.2 12.4	A A A A A	@ 150 MHz, 256K L2 @ 166 MHz, 512K L2 @ 180 MHz, 256K L2 @ 200 MHz, 256K L2 @ 200 MHz, 512K L2 3, 5
$I_{CC}S$	$V_{CC}S$ Current			0	A	6
$I_{CC}5$	5 V Supply Current			0	A	All frequencies
T_C	Operating Case Temp.	0		85	°C	

NOTES:

1. All power measurements taken with CMOS inputs driven to $V_{CC}P$ and to 0 V.
2. Maximum values are measured at typical $V_{CC}P$ to take into account the thermal time constant of the package. Typical values not tested, but imply the maximum power one should see when running normal high power applications on most devices. When designing a system to the typical power level, there should be a failsafe mechanism to guarantee control of the CPU T_C specification in case of statistical anomalies in the workload. This workload could cause a temporary rise in the maximum power.
3. **Power specifications for 512K L2 components are PRELIMINARY. Consult your FAE.**
4. Max values are measured at typical $V_{CC}P$ by asserting the STPCLK# pin or executing the HALT intruction (Auto Halt) with the EBL_CR_POWERON Low_Power_Enable bit set to enabled. See Model Specific Registers in Appendix C of the *Pentium® Pro Processor Developer's Manual, Volume 3: Operating System Writer's Guide* (Order Number 242692). Minimum values are guaranteed by design/characterization at minimum $V_{CC}P$.
5. Max $V_{CC}P$ current measured at max V_{CC}. All CMOS pins are driven with $V_{IH} = V_{CC}P$ and $V_{IL} = 0$ V during the execution of all Max I_{CC} and I_{CC}-stopgrant/autohalt tests.
6. The L2 of the current processors draw no current from the $V_{CC}S$ inputs. $I_{CC}S$ is 0 A when the L2 die receives its power from the $V_{CC}P$ pins. See the recommended decoupling in Section 3.4.

Table 6. GTL+ Signal Groups DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	-0.3	V_{REF} -0.2	V	1, See Table 8
V_{IH}	Input High Voltage	V_{REF} + 0.2	$V_{CC}P$	V	1
V_{OL}	Output Low Voltage	0.30	0.60	V	2
V_{OH}	Output High Voltage	—	—	V	See V_{TT} max in Table 8
I_{OL}	Output Low Current	36	48	mA	2
I_L	Leakage Current		±100	µA	3
I_{REF}	Reference Voltage Current		± 15	µA	4
C_{GTL+}	GTL+ Pin Capacitance		8.5	pF	5

NOTES:

1. V_{REF} worst case, not nominal. Noise on V_{REF} should be accounted for.
2. Parameter measured into a 25 Ω resistor to 1.5 V. Min. V_{OL} and max. I_{OL} are guaranteed by design/characterization.
3. $(0 \le V_{PIN} \le V_{CC}P)$.
4. Total current for all V_{REF} pins. Section 3.1. details the V_{REF} connections.
5. Total of I/O buffer, package parasitics and 0.5 pF for a socket. Capacitance values guaranteed by design for all GTL+ buffers.

Table 7. Non-GTL+[1] Signal Groups DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	3.6	V	
V_{OL}	Output Low Voltage		0.4 0.2	V V	2 3
V_{OH}	Output High Voltage	N/A	N/A	V	All Outputs Open-Drain
I_L	Input Leakage Current		±100	µA	4
C_{TOL}	3.3 V Tol. Pin Capacitance		10	pF	Except BCLK & TCK, 5
C_{CLK}	BCLK Input Capacitance		9	pF	5
C_{TCK}	TCK Input Capacitance		8	pF	5

NOTES:

1. Table 7 applies to the 3.3 V tolerant, APIC, and JTAG signal groups.
2. Parameter measured at 4 mA (for use with TTL inputs).
3. Parameter guaranteed by design at 100 µA (for use with CMOS inputs).
4. $(0 \le Vpin \le V_{CC}P)$.
5. Total of I/O buffer, package parasitics and 0.5 pF for a socket. Capacitance values are guaranteed by design.

3.14. GTL+ Bus Specifications

The GTL+ bus must be routed in a daisy-chain fashion with termination resistors at each end of every signal trace. These termination resistors are placed between the ends of the signal trace and the V_{TT} voltage supply and generally are chosen to approximate the board impedance. The valid high and low levels are determined by the input buffers using a reference voltage called V_{REF}. Table 8 lists the nominal specifications for the GTL+ termination voltage (V_{TT}) and the GTL+ reference voltage (V_{REF}). It is important that the printed circuit board impedance be specified and held to a ±20% tolerance, and that the intrinsic trace capacitance for the GTL+ signal group traces is known**. For more details on GTL+, see Section 4.**

Table 8. GTL+ Bus Voltage Specifications

Symbol	Parameter	Min	Typical	Max	Units	Notes
V_{TT}	Bus Termination Voltage	1.35	1.5	1.65	V	±10%
V_{REF}	Input Reference Voltage	2/3 V_{TT}-2%	2/3 V_{TT}	2/3 V_{TT} +2%	V	±2%, 1

NOTES:

- V_{REF} should be created from V_{TT} by a voltage divider of 1% resistors.

3.15. AC Specifications

Table 9 through Table 16 list the AC specifications associated with the Pentium Pro processor. Timing Diagrams begin with Figure 13. The AC specifications are broken into categories. Table 9 contains the clock specifications, Table 11 and Table 12 contain the GTL+ specifications, Table 13 is the 3.3 V tolerant Signal group specifications, Table 14 contains timings for the reset conditions, Table 15 covers APIC bus timing, and Table 16 covers Boundary Scan timing.

All AC specifications for the GTL+ signal group are relative to the rising edge of the BCLK input. All GTL+ timings are referenced to V_{REF} for both '0' and '1' logic levels unless otherwise specified.

Care should be taken to read all notes associated with a particular timing parameter.

Table 9. Bus Clock AC Specifications

T#	Parameter	Min	Max	Unit	Figure	Notes
	Core Frequency	100 150 150 150	150 166.67 180 200	MHz MHz MHz MHz		@ 150 MHz @ 166 MHz @ 180 MHz @ 200 MHz 1
	Bus Frequency	50.00	66.67	MHz		All Frequencies, 1
T1:	BCLK Period	15	20	ns	Figure 13	All Frequencies
T2:	BCLK Period Stability		300	ps		2, 3
T3:	BCLK High Time	4		ns	Figure 13	@>2.0 V, 2
T4:	BCLK Low Time	4		ns	Figure 13	@<0.8 V, 2
T5:	BCLK Rise Time	0.3	1.5	ns	Figure 13	(0.8 V - 2.0 V), 2
T6:	BCLK Fall Time	0.3	1.5	ns	Figure 13	(2.0 V- 0.8 V),2

NOTES:

1. The internal core clock frequency is derived from the bus clock. A clock ratio must be driven into the Pentium® Pro processor on the signals LINT[1:0], A20M# and IGNNE# at reset. See the descriptions for these signals in Appendix A.
2. Not 100% tested. Guaranteed by design/characterization.
3. Measured on rising edge of adjacent BCLKs at 1.5 V.
   The jitter present must be accounted for as a component of BCLK skew between devices.
   Clock jitter is measured from one rising edge of the clock signal to the next rising edge at 1.5V. To remain within the clock jitter specifications, all clock periods must be within 300 ps of the ideal clock period for a given frequency. For example, a 66.67 MHz clock with a nominal period of 15 ns, must not have any single clock period that is greater than 15.3 ns or less than 14.7 ns.

Table 10. Supported Clock Ratios [1]

Component:	2X	5/2X	3X	7/2X	4X
150 MHz	X	X	X		
166 MHz		X	X		
180 MHz		X	X		
200 MHz		X	X		X

NOTES:

1. Only those indicated by an ‘X’ are tested during the manufacturing test process.

Table 11. GTL+ Signal Groups AC Specifications

T#	Parameter	Min	Max	Unit	Figure	Notes
T7A:	GTL+ Output Valid Delay H→L	0.55 0.80	4.4 4.4	ns ns	Figure 14	@ 150 MHz, 256K L2 All other components 1, 2
T7B:	GTL+ Output Valid Delay L→H	0.55 0.80	3.9 3.9	ns ns	Figure 14	@ 150 MHz, 256K L2 All other components 1, 2
T8:	GTL+ Input Setup Time	2.2		ns	Figure 15	3, 4, 5
T9:	GTL+ Input Hold Time	0.45 0.70		ns ns	Figure 15	@ 150 MHz, 256K L2 All other components 5
T10:	RESET# Pulse Width	1		ms	Figure 18 Figure 19	6

NOTES:

1. Valid delay timings for these signals are specified into an idealized 25 Ω resistor to 1.5 V with V_{REF} at 1.0V. Minimum values guaranteed by design. See Figure 32 for the actual test configuration.
2. **GTL+ timing specifications for 166MHz and higher components are PRELIMINARY. Consult you local FAE.**
3. A minimum of 3 clocks must be guaranteed between 2 active-to-inactive transitions of TRDY#.
4. RESET# can be asserted (active) asynchronously, but must be deasserted synchronously.
5. Specification takes into account a 0.3 V/ns edge rate and the allowable V_{REF} variation. Guaranteed by design.
6. After V_{CC}, V_{TT}, V_{REF}, BCLK and the clock ratio become stable.

Table 12. GTL+ Signal Groups Ringback Tolerance

	Parameter	Min	Unit	Figure	Notes
α:	Overshoot	100	mV	Figure 17	1
τ:	Minimum Time at High	1.5	ns	Figure 17	1
ρ:	Amplitude of Ringback	-100	mV	Figure 17	1
δ:	Duration of Squarewave Ringback	N/A	ns	Figure 17	1
ϕ:	Final Settling Voltage	100	mV	Figure 17	1

NOTES:

1. Specified for an edge rate of 0.3—0.8V/ns. See Section 4.1.3.1 for the definition of these terms. See Figure 24 and Figure 25 for the generic waveforms. All values determined by design/characterization.

Table 13. 3.3 V Tolerant Signal Groups AC Specifications

T#	Parameter	Min	Max	Unit	Figure	Notes
T11:	3.3 V Tolerant Output Valid Delay	1	8	ns	Figure 14	1
T12:	3.3 V Tolerant Input Setup Time	5		ns	Figure 15	2, 3, 4, 5
T13:	3.3 V Tolerant Input Hold Time	1.5		ns	Figure 15	
T14:	3.3 V Tolerant Input Pulse Width, except PWRGOOD	2		BCLKs	Figure 14	Both levels
T15:	PWRGOOD Inactive Pulse Width	10		BCLKs	Figure 14 Figure 19	6

NOTES:

1. Valid delay timings for these signals are specified into 150 Ω to 3.3 V. See Figure 13 for a capacitive derating curve.
2. These inputs may be driven asynchronously. However, to guarantee recognition on a specific clock, the setup and hold times with respect to BCLK must be met.
3. These signals must be driven synchronously in FRC mode.
4. A20M#, IGNNE#, INIT# and FLUSH# can be asynchronous inputs, but to guarantee recognition of these signals following a synchronizing instruction such as an I/O write instruction, they must be valid with active RS[2:0]# signals of the corresponding synchronizing bus transaction.
5. INTR and NMI are only valid in APIC disable mode. LINT[1:0]# are only valid in APIC enabled mode.
6. When driven inactive, or after Power, V_{REF}, BCLK, and the ratio signals are stable.

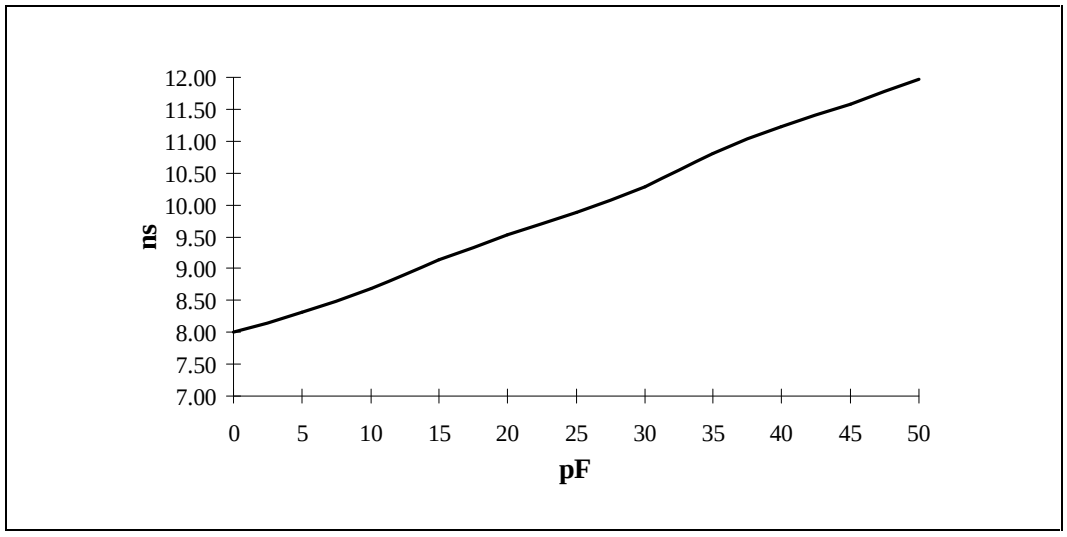


Figure 12. 3.3 V Tolerant Group Derating Curve

Table 14. Reset Conditions AC Specifications

T#	Parameter	Min	Max	Unit	Figure	Notes
T16:	Reset Configuration Signals (A[14:5]#, BR0#, FLUSH#, INIT#) Setup Time	4		BCLKs	Figure 18	Before deassertion of RESET#
T17:	Reset Configuration Signals (A[14:5]#, BR0#, FLUSH#, INIT#) Hold Time	2	20	BCLKs	Figure 18	After clock that deasserts RESET#
T18:	Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]#) Setup Time	1		ms	Figure 18	Before deassertion of RESET#
T19:	Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]#) Delay Time		5	BCLKs	Figure 18	After assertion of RESET# 1
T20:	Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]#) Hold Time	2	20	BCLKs	Figure 18 Figure 19	After clock that deasserts RESET#

NOTES:

1. For a reset, the clock ratio defined by these signals must be a safe value (their final or lower multiplier) within this delay unless PWRGOOD is being driven inactive.

Table 15. APIC Clock and APIC I/O AC Specifications

T#	Parameter	Min	Max	Unit	Figure	Notes
T21A:	PICCLK Frequency	2	33.3	MHz		
T21B:	FRC Mode BCLK to PICCLK offset	1	5	ns	Figure 16	1
T22:	PICCLK Period	30	500	ns	Figure 13	
T23:	PICCLK High Time	12		ns	Figure 13	
T24:	PICCLK Low Time	12		ns	Figure 13	
T25:	PICCLK Rise Time	1	5	ns	Figure 13	
T26:	PICCLK Fall Time	1	5	ns	Figure 13	
T27:	PICD[1:0] Setup Time	8		ns	Figure 15	2
T28:	PICD[1:0] Hold Time	2		ns	Figure 15	2
T29:	PICD[1:0] Valid Delay	2.1	10	ns	Figure 14	2, 3, 4

NOTES:

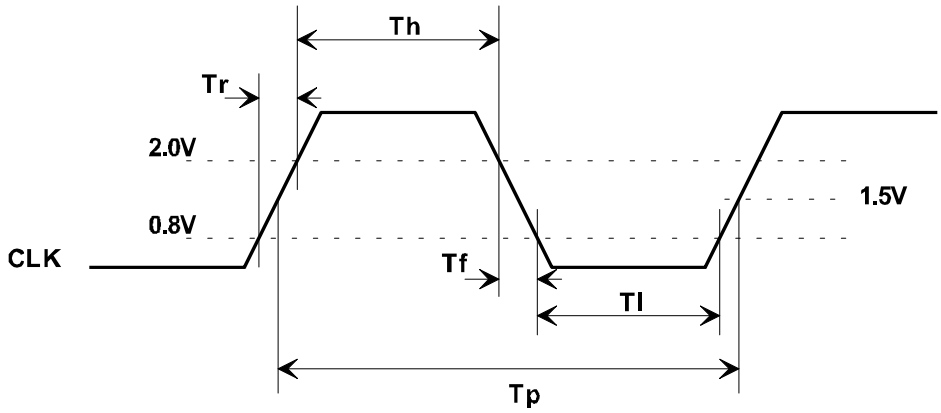
1. With FRC enabled PICCLK must be ¼X BCLK and synchronized with respect to BCLK. PICCLK must always lag BCLK by at least 1 ns and no more than 5 ns.
2. Referenced to PICCLK Rising Edge.
3. For open drain signals, Valid Delay is synonymous with Float Delay.
4. Valid delay timings for these signals are specified into 150 Ω to 3.3 V.

Table 16. Boundary Scan Interface AC Specifications

T#	Parameter	Min	Max	Unit	Figure	Notes
T30:	TCK Frequency	—	16	MHz		
T31:	TCK Period	62.5	—	ns	Figure 13	
T32:	TCK High Time	25		ns	Figure 13	@2.0 V, 1
T33:	TCK Low Time	25		ns	Figure 13	@0.8 V, 1
T34:	TCK Rise Time		5	ns	Figure 13	(0.8 V-2.0 V), 1, 2
T35:	TCK Fall Time		5	ns	Figure 13	(2.0 V-0.8 V), 1, 2
T36:	TRST# Pulse Width	40		ns	Figure 21	1, Asynchronous
T37:	TDI, TMS Setup Time	5		ns	Figure 20	3
T38:	TDI, TMS Hold Time	14		ns	Figure 20	3
T39:	TDO Valid Delay	1	10	ns	Figure 20	4, 5
T40:	TDO Float Delay		25	ns	Figure 20	1, 4, 5
T41:	All Non-Test Outputs Valid Delay	2	25	ns	Figure 20	4, 6, 7
T42:	All Non-Test Outputs Float Delay		25	ns	Figure 20	1, 4, 6, 7
T43:	All Non-Test Inputs Setup Time	5		ns	Figure 20	3, 6, 7
T44:	All Non-Test Inputs Hold Time	13		ns	Figure 20	3, 6, 7

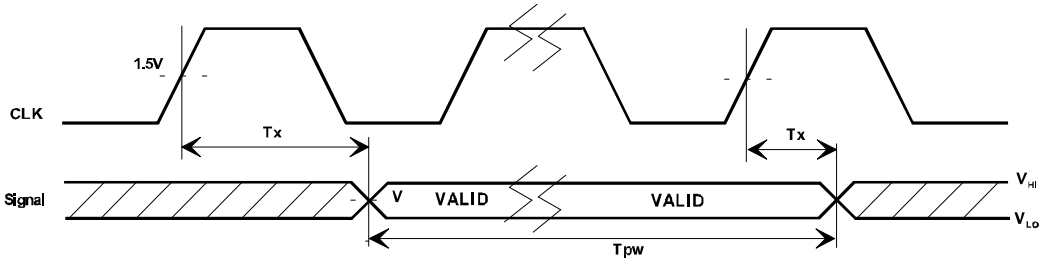
NOTES:

1. Not 100% tested. Guaranteed by design/characterization.
2. 1ns can be added to the maximum TCK rise and fall times for every 1 MHz below 16 MHz.
3. Referenced to TCK rising edge.
4. Referenced to TCK falling edge.
5. Valid delay timing for this signal is specified into 150 Ω terminated to 3.3 V.
6. Non-Test Outputs and Inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO and TMS). These timings correspond to the response of these signals due to boundary scan operations. PWRGOOD should be driven high throughout boundary scan testing.
7. During Debug Port operation, use the normal specified timings rather than the boundary scan timings.



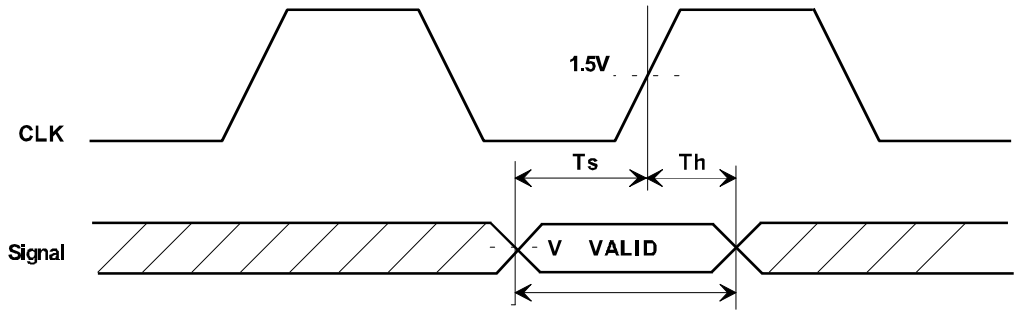
T_r = Rise Time
T_f = Fall Time
T_h = High Time
T_l = Low Time
T_p = Period

Figure 13. Generic Clock Waveform



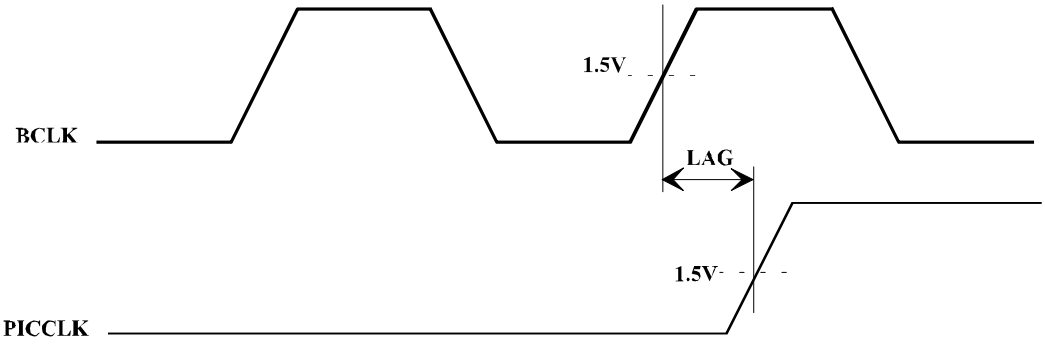
Tx = Valid Delay
Tpw = Pulse Width
V = 1.0 V for GTL+ signal group; 1.5 V for 3.3 V Tolerant, APIC, and JTAG signal groups
V_{HI} = GTL+ signals must achieve a DC high level of at least 1.2V
V_{LO} = GTL+ signals must achieve a DC low level of at most 0.8V

Figure 14. Valid Delay Timings



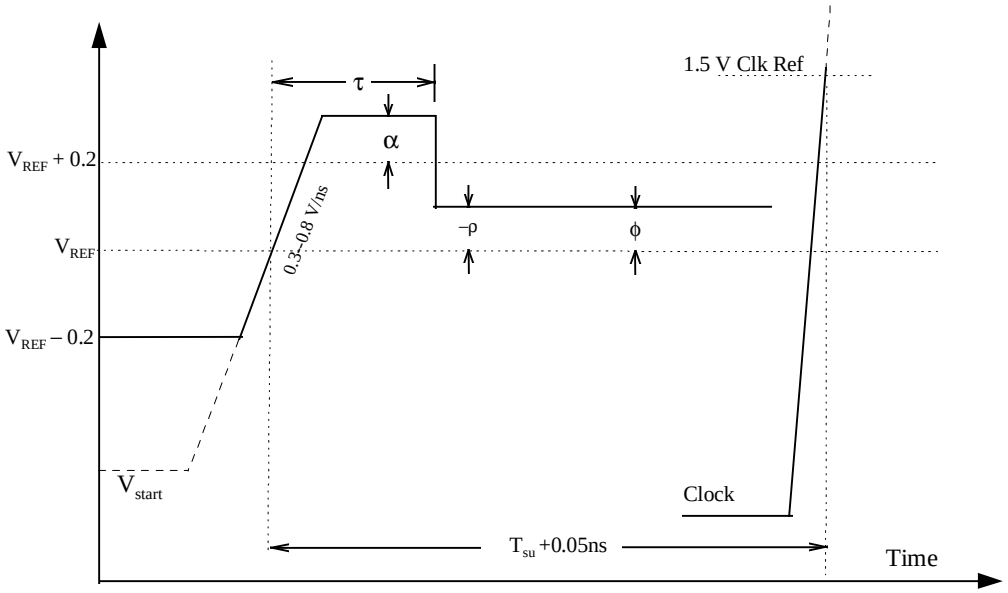
T_s = Setup Time
T_h = Hold Time
V = 1.0 V for GTL+ signal group; 1.5 V for 3.3 V Tolerant, APIC and JTAG signal groups

Figure 15. Setup and Hold Timings



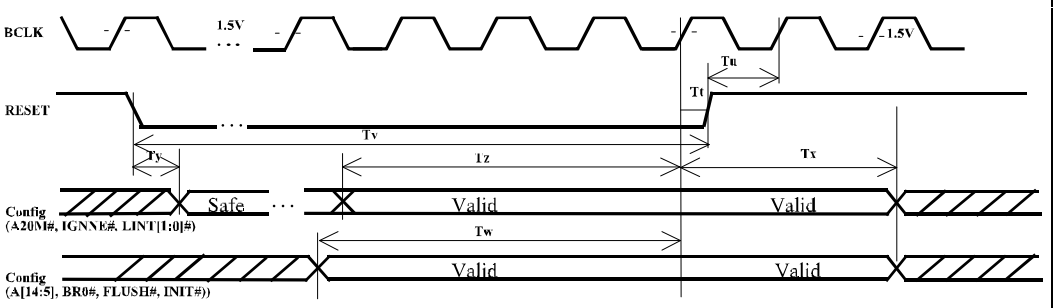
LAG = T21B (FRC Mode BCLK to PICCLK offset)

Figure 16. FRC Mode BCLK to PICCLK Timing



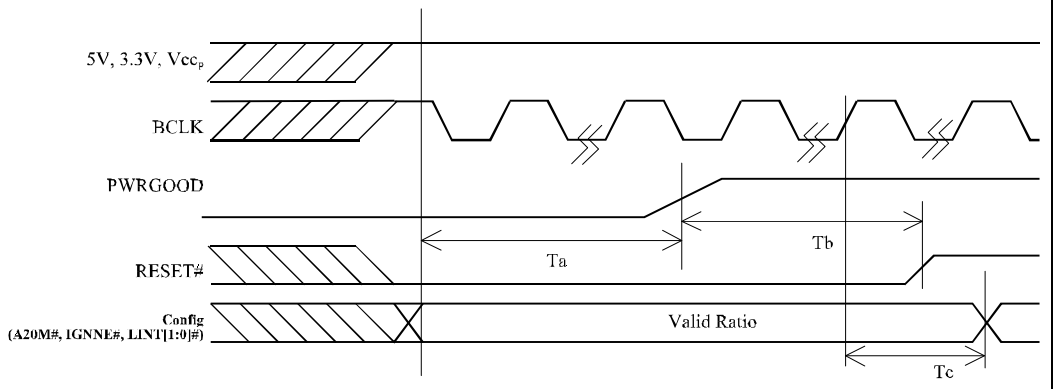
The Hi to Low Case is analogous.
α = Overshoot
τ = Minimum Time at High
ρ = Amplitude of Ringback
ϕ = Final Settling Voltage

Figure 17. Low to High GTL+ Receiver Ringback Tolerance



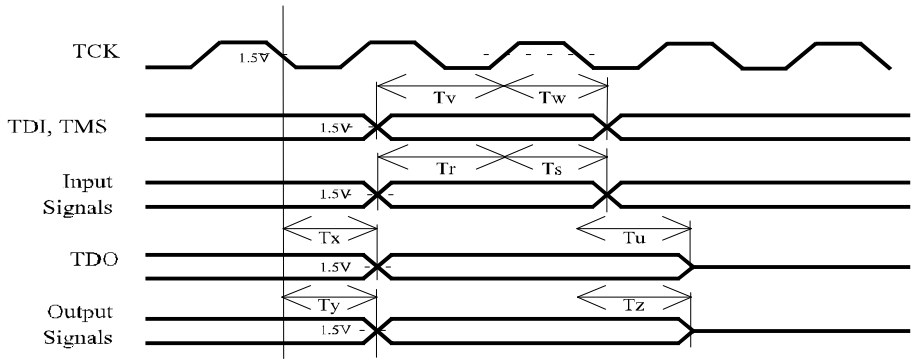
Tt = T9 (GTL+ Input Hold Time)
Tu = T8 (GTL+ Input Setup Time)
Tv = T10 (RESET# Pulse Width)
Tw = T16 (Reset Configuration Signals (A[14:5]#, BR0#, FLUSH#, INIT#) Setup Time)
Tx = T17 (Reset Configuration Signals (A[14:5]#, BR0#, FLUSH#, INIT#) Hold Time).
T20 (Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]#) Hold Time)
Ty = T19 (Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]#) Delay Time)
Tz = T18 (Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]#) Setup Time)

Figure 18. Reset and Configuration Timings



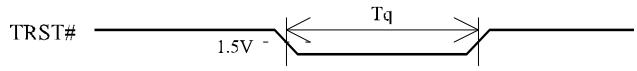
Ta = T15 (PWRGOOD Inactive Pulse Width)
Tb = T10 (RESET# Pulse Width)
Tc = T20 (Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]#) Hold Time)

Figure 19. Power-On Reset and Configuration Timings



Tr = T43 (All Non-Test Inputs Setup Time)
Ts = T44 (All Non-Test Inputs Hold Time)
Tu = T40 (TDO Float Delay)
Tv = T37 (TDI, TMS Setup Time)
Tw = T38 (TDI, TMS Hold Time)
Tx = T39 (TDO Valid Delay)
Ty = T41 (All Non-Test Outputs Valid Delay)
Tz = T42 (All Non-Test Outputs Float Delay)

Figure 20. Test Timings (Boundary Scan)



Tq = T36 (TRST# Pulse Width)

Figure 21. Test Reset Timings

3.16. Flexible Motherboard Recommendations

Table 17 provides recommendations for designing a “flexible” motherboard for supporting future Pentium Pro processors. By meeting these recommendations, the same system design should be able to support future standard Pentium Pro processors. If the voltage regulator module is socketed using Header 8, a smaller range of support is required by the voltage regulator module. See Section 8. for information on Header 8. **These values are preliminary.**

The use of a zero-insertion force socket for the processor and the voltage regulator module is recommended. One should also make every attempt to leave margin in the system where possible.

Table 17. Flexible Motherboard (FMB) Power Recommendations[1]

Symbol	Parameter	Low End	High End	Unit	Notes
$V_{CC}P$	Full FMB Primary V_{CC} Socketed VRM Primary V_{CC}	2.4 3.1	3.5 3.5	V V	5% tolerance over range
$V_{CC}S$	FMB Secondary V_{CC}	3.3	3.3	V	5% tolerance
$V_{CC}5$	FMB 5 V V_{CC}	5.0	5.0	V	5% tolerance
P_{Max}	FMB Thermal Design power		45	W	
I_{CCP}	Full FMB $V_{CC}P$ Current	0.3	14.5	A	
I_{CCS}	FMB $V_{CC}S$ Current	0	3.0	A	
I_{CC5}	FMB $V_{CC}5$ Current		340	mA	
C_P	High Frequency $V_{CC}P$ Decoupling		40	µF	40 1 µF 1206 packages
C_S	High Frequency $V_{CC}S$ Decoupling		10	µF	10 1 µF 1206 packages
T_C	FMB Operating Case Temperature		85	°C	

NOTE:

1. Values are preliminary, per processor, and are not tested parameters. They are solely recommendations.

4.0 GTL+ Interface Specification

This section defines the new open-drain bus called GTL+. The primary target audience is designers developing systems using GTL+ devices such as the Pentium Pro processor and the 82450 PCIset. This specification will also be useful for I/O buffer designers developing an I/O cell and package to be used on a GTL+ bus.

This specification is an enhancement to the GTL specification. The enhancements were made to allow the interconnect of up to eight devices operating at 66.6 MHz and higher using manufacturing techniques that are standard in the microprocessor industry. The specification enhancements over standard GTL provide better noise margins and reduced ringing. Since this specification is different from the GTL specification, it is referred to as GTL+.

The GTL+ specification defines an open-drain bus with external pull-up resistors providing termination to a termination voltage (V_{TT}). The specification includes a maximum driver output low voltage (V_{OL}) value, output driver edge rate requirements, example AC timings, maximum bus agent loading (capacitance and package stub length), and a receiver threshold (V_{REF}) that is proportional to the termination voltage.

The specification is given in two parts. The first, is the system specification which describes the system environment. The second, is the actual I/O specification, which describes the AC and DC characteristics for an I/O transceiver.

Note that some of the critical distances, such as routing length, are given in electrical length (time) instead of physical length (distance). This is because the system design is dependent on the propagation time of the signal on a printed circuit board trace rather than just the length of the trace. Different PCB materials, package materials and system construction result in different signal propagation velocities. Therefore, a given physical length does not correspond to a fixed electrical length. The distance (time) calculation up to the designer.

4.1. System Specification

Figure 22 shows a typical system that a GTL+ device would be placed into. The typical system is shown with two terminations and multiple transceiver agents connected to the bus. The receivers have differential inputs connected to a reference voltage, V_{REF}, which is generated externally by a voltage divider. Typically, one voltage divider exists at each component. Here one is shown for the entire network.

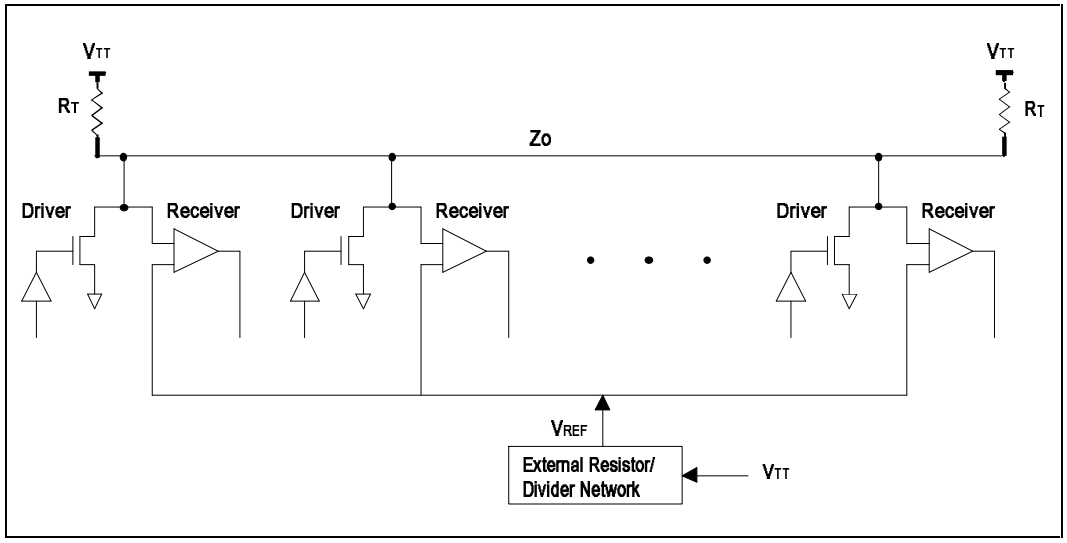


Figure 22. Example of Terminated Bus with GTL+ Transceivers

4.1.1. System DC Parameters

The following system DC parameters apply to Figure 22.

Table 18. System DC Parameters

Symbol	Parameter	Value	Tolerance	Notes
V_{TT}	Termination Voltage	1.5 V	±10%	
V_{REF}	Input Reference Voltage	2/3 V_{TT}	±2%	1
R_T	Termination Resistance	Z_{EFF} (nominal)	See Note	2, 4
Z_{EFF}	Effective (Loaded) Network Impedance	45–65 Ω		2, 3

NOTES:

1. This ±2% tolerance is in addition to the ±10% tolerance of V_{TT}, and could be caused by such factors as voltage divider inaccuracy.
2. $$Z_{EFF} = \frac{Zo\ (nominal)}{(1+Cd/Co)^{1/2}}$$
3. Zo = Nominal board impedance; recommended to be 65Ω ±10%. Zo is a function of the trace cross-section, the distance to the reference plane(s), the dielectric constant, ε_r, of the PCB material and the dielectric constant of the solder-mask/air for micro-strip traces.

   Co = Total intrinsic nominal trace capacitance between the first and last bus agents, excluding the termination resistor tails. Co is a function of Zo and εr. For Zo= 65 Ω and ε_r = 4.3, Co is approximately 2.66 pF/in times the network length (first agent to last agent).

   Cd = Sum of the Capacitance of all devices and PCB stubs (if any) attached to the net,
   = PCB Stub Capacitance +Socket Capacitance +Package Stub Capacitance + Die Capacitance.
4. Z_{EFF} of all 8-load nets must remain between 45-65 Ω under all conditions, including variations in Zo, Cd, temperature, V_{CC}, etc.
5. To reduce cost, a system would usually employ one value of R_T for all its GTL+ nets, irrespective of the Z_{EFF} of individual nets. The designer may start with the average value of Z_{EFF} in the system. The value of R_T may be adjusted to balance the Hi-to-Lo and Lo-to-Hi noise margins. Increasing the value of R_T tends to slow the rising edge, increasing rising flight time, decreasing the Lo-to-Hi noise margin, and increasing the Hi-to-Lo noise margin by lowering V_{OL}. R_T can be decreased for the opposite effects.

   R_T affects GTL+ rising edge rates and the “apparent clock-to-out” time of a driver in a net as follows: A large R_T causes the standing current in the net to be low when the (open drain) driver is low (on). As the driver switches off, the small current is turned off, launching a relatively small positive-going wave down the net. After a few trips back and forth between the driver and the terminations (undergoing reflections at intervening agents in the meantime) the net voltage finally climbs to V_{TT}. Because the wave launched initially is relatively small in amplitude (than it would have been had R_T been smaller and the standing current larger), the overall rising edge climbs toward V_{TT} at a slower rate. Notice that this effect causes an increase in flight time, and has no influence on the true clock-to-out timing of the driver into the standard 25 Ω test load.

4.1.2. Topological Guidelines

The board routing should use layout design rules consistent with high-speed digital design (i.e., minimize trace length and number of vias, minimize trace-to-trace coupling, maintain consistent impedance over the length of a net, maintain consistent impedance from one net to another, ensure sufficient power to ground plane bypassing, etc.). In addition, the signal routing should be done in a **Daisy Chain** topology (such as shown in Figure 7) without any significant stubs. Table 19 describes, more completely, some of these guidelines. Note that the critical distances are measured in electrical length (propagation time) instead of physical length.

Table 19. System Topological Guidelines

Parameter	Description
Maximum Trace Length	To meet a specific clock cycle time, the maximum trace length between any two agents must be restricted. The flight time (defined later) must be less than or equal to the maximum amount of time which leaves enough time within one clock cycle for the remaining system parameters such as driver clock-out delay (T_{CO}), receiver setup time (T_{SU}), clock jitter and clock skew.
Maximum Stub Length	All signals should use a Daisy Chain routing (i.e. no stubs). It is acknowledged that the package of each device on the net imposes a stub, and that a practical layout using PQFP parts may require SHORT stubs, so a truly stubless network is impossible to achieve, but any stub on the network (including the device package) should be no greater than 250 ps in electrical length.
Distributed Loads	Minimum spacing lengths are determined by hold time requirements and clock skew. Maintaining 3" ±30% inter-agent spacing minimizes the variation in noise margins between the various networks, and can provide a significant improvement for the networks. This is only a guideline.

4.1.3. System AC Parameters: Signal Quality

The system AC parameters fall into two categories, Signal Quality and Flight Time. Acceptable signal quality must be maintained over all operating conditions to ensure reliable operation. Signal Quality is defined by three parameters: Overshoot/Undershoot, Settling Limit, and Ringback. These parameters are illustrated in Figure 23 and are described in Table 20.

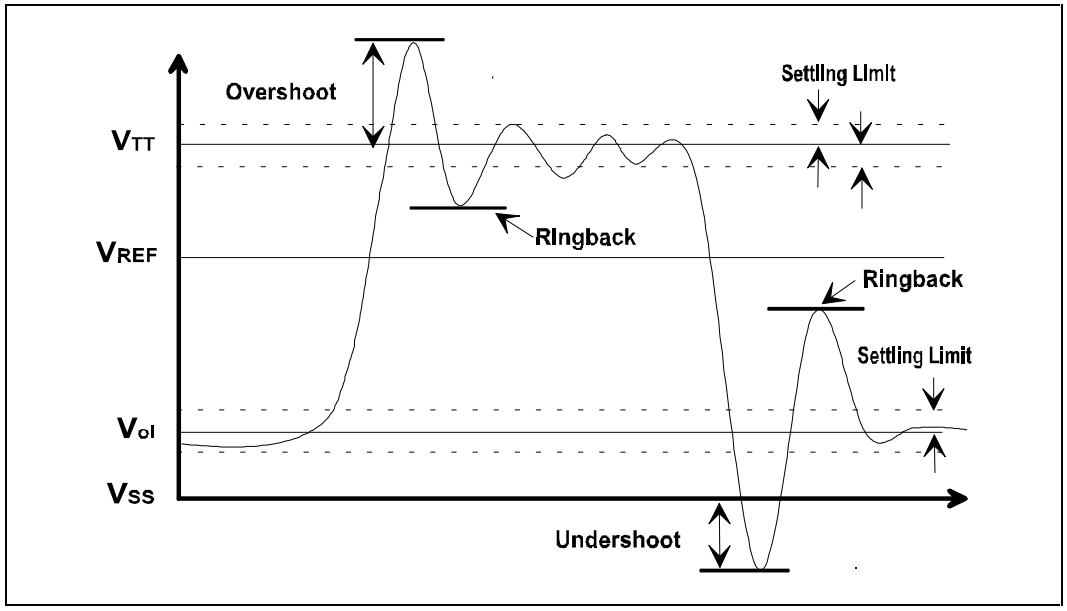


Figure 23. Receiver Waveform Showing Signal Quality Parameters

Table 20. Specifications for Signal Quality

Parameter	Description	Specification
Maximum Signal Overshoot/Undershoot	Maximum Absolute voltage a signal extends above V_{TT} or below V_{SS} (simulated w/o protection diodes).	0.3 V (guideline)
Settling Limit	The maximum amount of ringing, at the receiving chip pad, a signal must be limited to before its next transition. This signal should be within 10% of the signal swing to its final value, when either in its high state or low state.	±10% of (V_{OH}-V_{OL}) (guideline)
Maximum Signal Ringback (Nominal)	The maximum amount of ringing allowed for a signal at a receiving chip pad within the receiving chips setup and hold time window before the next clock. This value is dependent upon the specific receiver design. (Normally ringing within the setup and hold windows must not come within 200 mV of V_{REF} although specific devices may allow more ringing and loosen this specification. See Section 4.1.3.1 for more details.)	V_{REF} ±200 mV

The overshoot/undershoot guideline is provided to limit signals transitioning beyond V_{CC} or V_{SS} due to fast signal edge rates. Violating the overshoot/undershoot guideline is acceptable, but since excessive ringback is the harmful effect associated with overshoot/undershoot it will make satisfying the ringback specification very difficult.

Violations of the Settling Limit guideline are acceptable if simulations of 5 to 10 successive transitions do not show the amplitude of the ringing increasing in the subsequent transitions. If a signal has not settled close to its final value before the next logic transition, then the timing delay to V_{REF} of the succeeding transition may vary slightly due to the stored reactive energy in the net inherited from the previous transition. This is akin to "eye" patterns in communication systems caused by inter-symbol interference. The resulting effect is a slight variation in flight time.

4.1.3.1. Ringback Tolerance

The nominal maximum ringback tolerated by GTL+ receivers is stated in Table 20, namely: no closer to V_{REF} than a ±200 mV overdrive zone. This requirement is usually necessary to guarantee that a receiver meets its specified minimum setup time (T_{SU}), since set-up time usually degrades as the magnitude of overdrive beyond the switching threshold (V_{REF}) is reduced.

Exceptions to the nominal overdrive requirement can be made when it is known that a particular receiver's setup time (as specified by its manufacturer) is *relatively* insensitive (less than 0.05 ns impact) to well-controlled ringing into the overdrive zone or even to brief re-crossing of the switching threshold, V_{REF}. Such "ringback-tolerant" receivers give the system designer more design freedom, and, if not exploited, at least help maintain high system reliability.

To characterize ringback tolerance, employ the idealized Lo-to-Hi input signal shown in Figure 34. The corresponding waveform for a Hi-to-Lo transition is shown in Figure 35. The object of ringback characterization is to determine the range of values for the different parameters shown on the diagram, which would maintain receiver setup time and correct logic functionality.

These parameters are defined as follows:

τ is the minimum time that the input must spend, after crossing V_{REF} at the high level, before it can ring back, having overshot $V_{IN\_HIGH\_MIN}$ by at least α, while ρ, δ, and ϕ (defined below) are at some preset values, all without increasing T_{SU} by more than 0.05 ns. Analogously for Hi-to-Lo transitions.

It is expected that the larger the overshoot α, the smaller the amount of time, τ, needed to maintain setup time to within +0.05 ns of the nominal value. For a given value of α, it is likely that τ will be the longest for the slowest input edge rate of 0.3 V/ns. Furthermore, there may be some dependence between τ and lower starting voltages than V_{REF} – 0.2 V (for Lo-to-Hi transitions) for the reason described later in Section 4.2.3.2. Minimum Set-up and Hold Times.

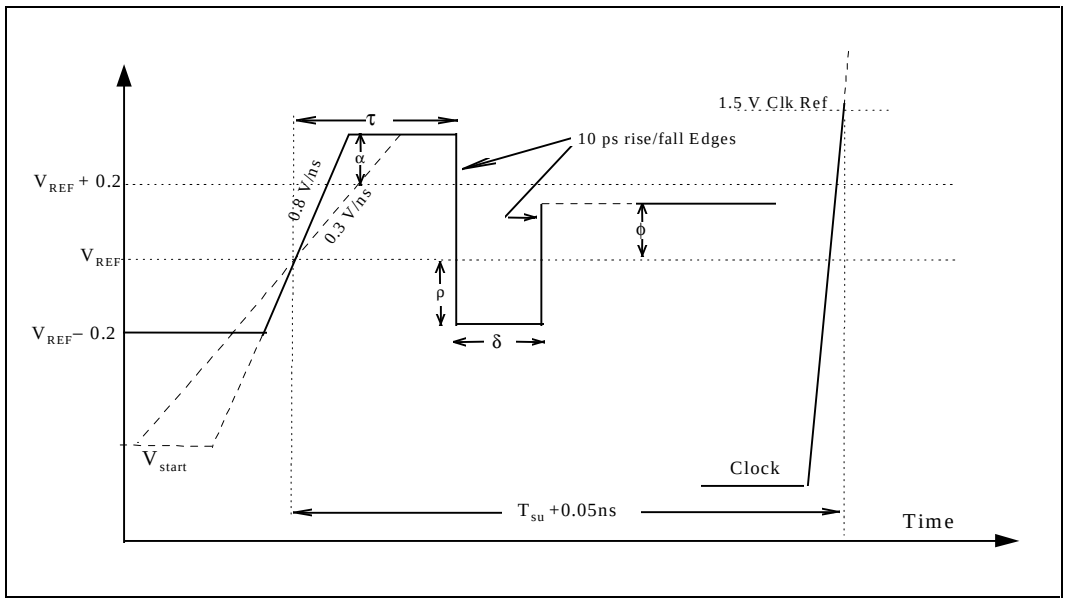


Figure 24. Standard Input Lo-to-Hi Waveform for Characterizing Receiver Ringback Tolerance

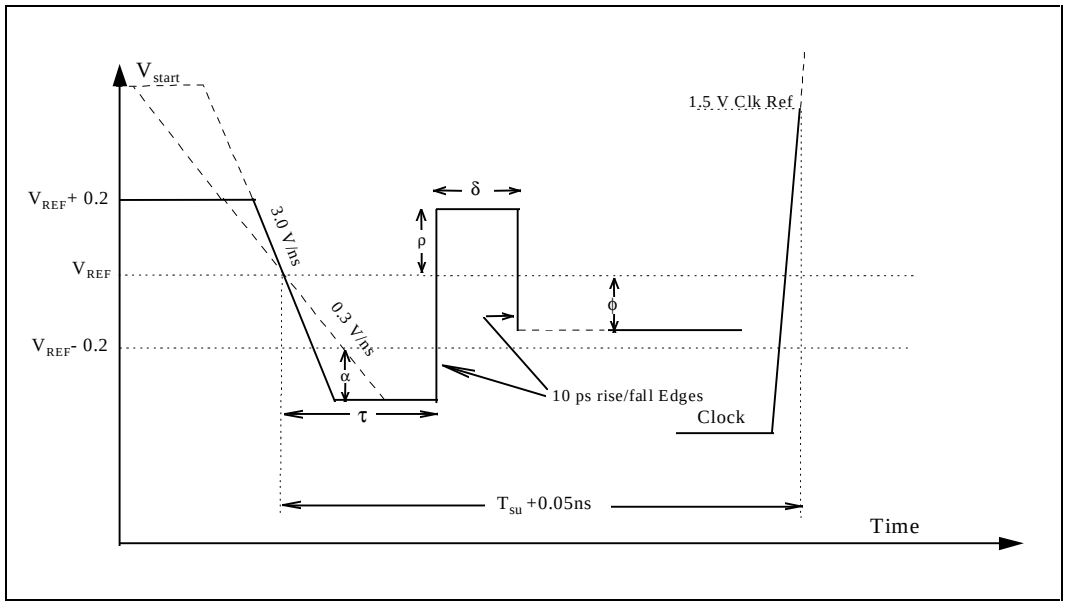


Figure 25. Standard Input Hi-to-Lo Waveform for Characterizing Receiver Ringback Tolerance

ρ and δ are respectively, the amplitude and duration of square-wave ringback, below the threshold voltage (V_{REF}), that the receiver can tolerate without increasing T_{SU} by more than 0.05 ns for a given pair of (α, τ) values.

If, for any reason, the receiver cannot tolerate any ringback across the reference threshold (V_{REF}), then ρ would be a negative number, and δ may be infinite. Otherwise, expect an inverse (or near-inverse) relationship between ρ and δ, where the more the ringback, the shorter is the time that the ringback is allowed to last without causing the receiver to detect it.

ϕ is the final minimum settling voltage, relative to the reference threshold (V_{REF}), that the input should return to after ringback to guarantee a valid logic state at the internal flip-flop input.

ϕ is a function of the input amplifier gain, its differential mode offset, and its intrinsic maximum level of differential noise.

Specifying the values of α, τ, ρ, δ, and ϕ is the responsibility of the receiver vendor. The system designer should guarantee that all signals arriving at such a receiver remain in the permissible region specified by the vendor parameters as they correspond to those of the idealized square waves of Figure 24 and Figure 25. For instance, a signal with ringback inside the box delineated by ρ and δ can have a τ equal to or longer than the minimum, and an α equal to or larger than the minimum also.

A receiver that does not tolerate any ringback would show the following values for the above parameters:

$\alpha \geq 0V$, $\tau \geq T_{su}$, $\rho = -200$ mV, δ = undefined, ϕ = 200 mV.

A receiver which tolerates 50 mV of ringback would show the following values for the above parameters:

$\alpha \geq 0V$, τ = data sheet, $\rho = -150$ mV, δ = data sheet, $\phi \geq$ tens of mV (data sheet).

Finally, a receiver which tolerates ringback across the switching threshold would show the following values for the above parameters:

$\alpha \geq 0$ V, τ = data sheet, $\rho \geq 0$ mV (data sheet), δ = data sheet, $\phi \geq$ tens of mV.

where δ would usually be a brief amount of time, yielding a pulse (or “blip”) beyond V_{REF}.

4.1.4. AC Parameters: Flight Time

Signal Propagation Delay is the time between when a signal appears at a driver pin and the time it arrives at a receiver pin. Flight Time is often used interchangeably with Signal Propagation Delay but it is actually quite different. Flight time is a term in the timing equation that includes the signal propagation delay, any effects the system has on the T_{CO} of the driver, plus any adjustments to the signal at the receiver needed to guarantee the T_{SU} of the receiver. More precisely, Flight Time is defined to be:

> The time difference between when a signal at the **input pin** of a receiving agent (adjusted to meet the receiver manufacturer's conditions required for AC specifications) crosses V_{REF}, and the time that the **output pin** of the driving agent crosses V_{REF} **were it driving the test load** used by the manufacturer to specify that driver's AC timings.

An example of the simplest Flight Time measurement is shown in Figure 26. The receiver specification assumes that the signal maintains an edge rate greater than or equal to 0.3 V/ns at the **receiver chip pad** in the OverDrive processor region from V_{REF} to V_{REF} +200 mV for a rising edge and that there are no signal quality violations after the input crosses V_{REF} at the *pad*. The Flight Time measurement is similar for a simple Hi-to-Lo transition. Notice that timing is measured at the driver and receiver *pins* while signal integrity is observed at the receiver chip *pad*. When signal integrity at the pad violates the guidelines of this specification, and adjustments need to be made to flight time, the adjusted flight time obtained at the chip pad can be assumed to have been obtained at the package pin, usually with a small timing error penalty.

The 0.3V/ns edge rate will be addressed later in this document, since it is related to the conditions used to specify a GTL+ receiver's minimum set-up time. What is meant by edge rate is neither instantaneous, nor strictly average. Rather, it can best be described for a rising edge—by imagining an 0.3 V/ns line crossing V_{REF} at the same moment that the signal crosses it, and extending to V_{REF} +200 mV, with the signal staying ahead (earlier in time) of that line at all times, until it reaches V_{REF} +200 mV. Such a requirement would always yield signals with an average edge rate >0.3 V/ns, but which could have instantaneous slopes that are lower or higher than 0.3V/ns, as long as they do not cause a crossing of the inclined line.

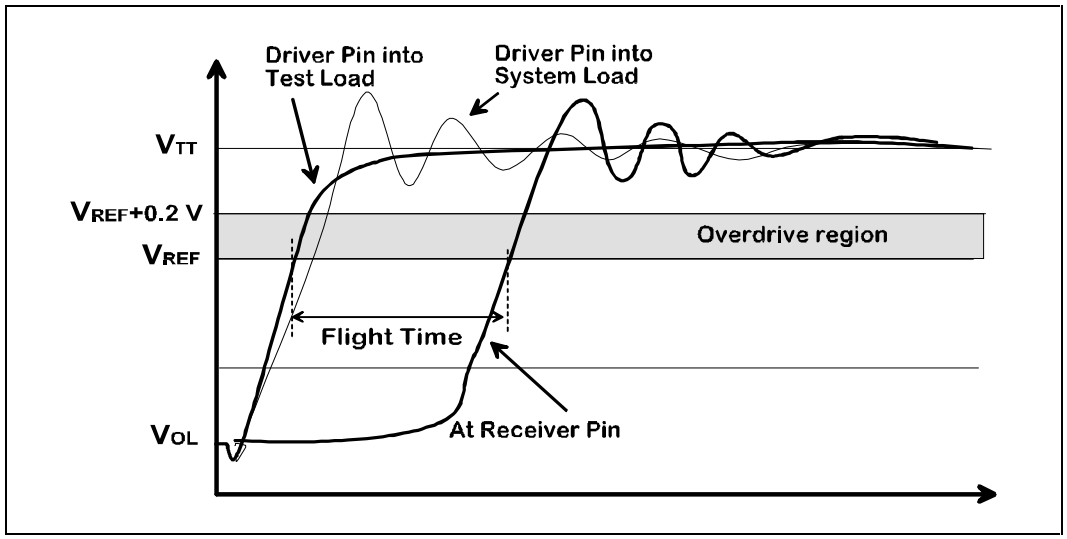


Figure 26. Measuring Nominal Flight Time

If either the rising or falling edge is slower than 0.3V/ns through the overdrive region beyond V_{REF}, (i.e., does not always stay ahead of an 0.3 V/ns line), then the flight time for a rising edge is determined by extrapolating back from the signal crossing of V_{REF} +200 mV to V_{REF} using an 0.3 V/ns slope as indicated in Figure 27.

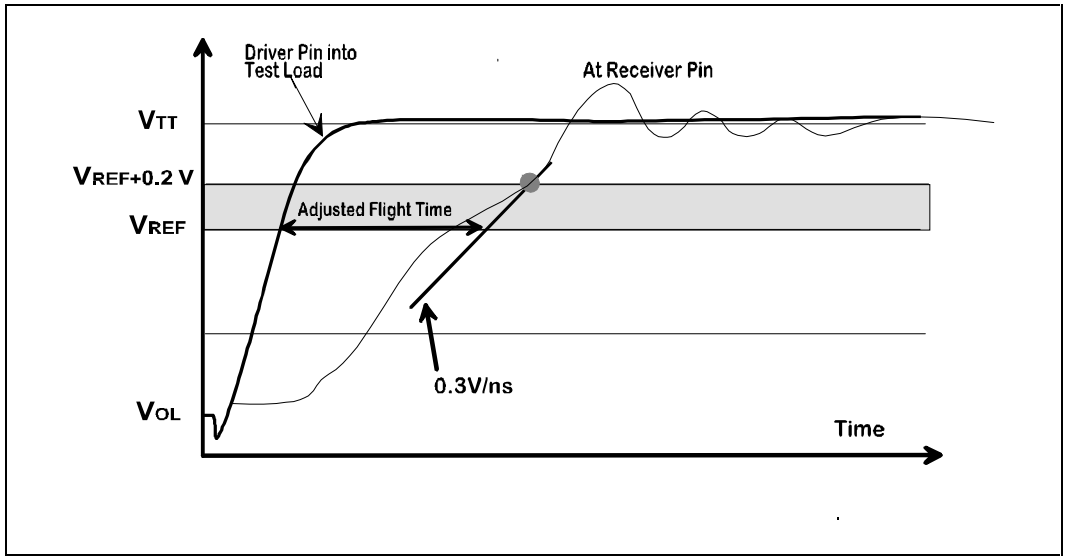


Figure 27. Flight Time of a Rising Edge Slower Than 0.3V/ns

If the signal is not monotonic while traversing the overdrive region (V_{REF} to V_{REF} +200 mV rising, or V_{REF} to V_{REF}-200 mV falling), or rings back into the overdrive region after crossing V_{REF}, then flight time is determined by extrapolating back from the last crossing of V_{REF} ± 200 mV using a line with a slope of 0.8 V/ns (the maximum allowed rising edge rate). This yields a new V_{REF} crossing point to be used for the flight time calculation. Figure 28 represents the situation where the signal is non-monotonic after crossing V_{REF} on the rising edge.

Figure 29 shows a falling edge that rings back into the overdrive region after crossing V_{REF}, and the 0.8V/ns line used to extrapolate flight time. Since strict adherence to the edge rate specification is not required for Hi-to-Lo transitions, and some drivers' falling edges are substantially faster than 0.8V/ns—at both the fast and slow corners—care should be taken when using the 0.8 V/ns extrapolation. The extrapolation is invalid whenever it yields a V_{REF} crossing that occurs earlier than when the signal's actual edge crosses V_{REF}. In that case, flight time is defined to be the longer of: the time when the input at the receiver crosses V_{REF} initially, or when the line extrapolated (at 0.8 V/ns) crosses V_{REF}. Figure 29 illustrates the situation where the extrapolated value would be used.

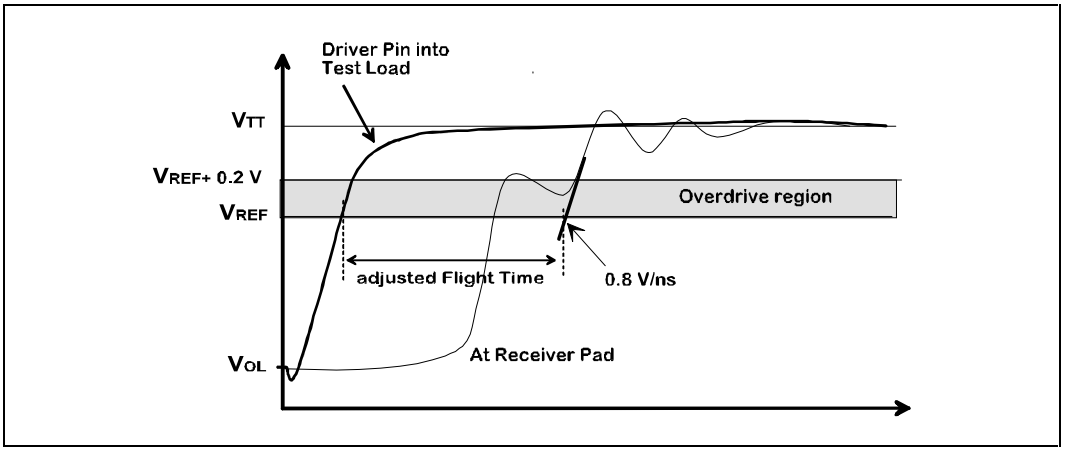


Figure 28. Extrapolated Flight Time of a Non-Monotonic Rising Edge

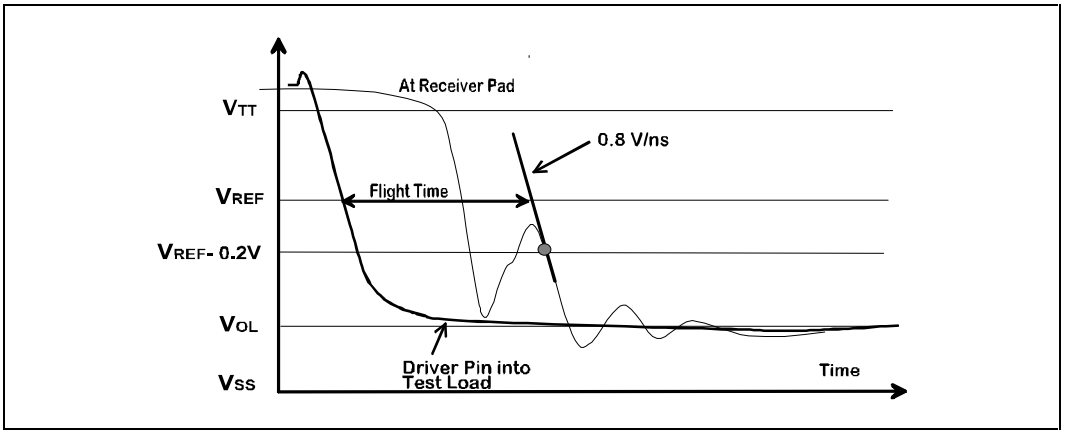


Figure 29. Extrapolated Flight Time of a Non-Monotonic Falling Edge

The maximum acceptable Flight Time is determined on a net-by-net basis, and is usually different for each unique driver-receiver pair. The maximum acceptable Flight Time can be calculated using the following equation (known as the setup time equation):

$$T_{FLIGHT\text{-}MAX} \leq T_{PERIOD\text{-}MIN} - (T_{CO\text{-}MAX} + T_{SU\text{-}MIN} + T_{CLK\_SKEW\text{-}MAX} + T_{CLK\_JITTER\text{-}MAX})$$

Where, $T_{CO\text{-}MAX}$ is the maximum clock-to-out delay of a driving agent, $T_{SU\text{-}MIN}$ is the minimum setup time required by a receiver on the same net, $T_{CLK\_SKEW\text{-}MAX}$ is the maximum anticipated time difference between the driver's and the receiver's clock inputs, and $T_{CLK\_JITTER\text{-}MAX}$ is maximum anticipated edge-to-edge phase jitter. The above equation should be checked for all pairs of devices on all nets of a bus.

The minimum acceptable Flight Time is determined by the following equation (known as the hold time equation):

$$T_{HOLD\text{-}MIN} \leq T_{FLIGHT\text{-}MIN} + T_{CO\text{-}MIN} - T_{CLK\_SKEW\text{-}MAX}$$

Where, T_{CO-MIN} is the minimum clock-to-out delay of the driving agent, $T_{HOLD-MIN}$ is the minimum hold time required by the receiver, and $T_{CLK\_SKEW-MAX}$ is defined above. The Hold time equation is independent of clock jitter, since data is released by the driver and is required to be held at the receiver on the same clock edge.

4.2. General GTL+ I/O Buffer Specification

This specification identifies the key parameters for the driver, receiver, and package that must be met to operate in the system environment described in the previous section. All specifications must be met over all possible operating conditions including temperature, voltage, and semiconductor process. **This information is included for designers of components for a GTL+ bus.**

4.2.1. I/O Buffer DC Specification

Table 21 contains the I/O Buffer DC parameters.

Table 21. I/O Buffer DC Parameters

Symbol	Parameter	Min	Max	Units	Notes
V_{OL}	Driver Output Low Voltage		0.600	V	1
V_{IH}	Receiver Input High Voltage	V_{REF} + 0.2		V	2
V_{IL}	Receiver Input Low Voltage		V_{REF} – 0.2	V	2
V_{ILC}	Input Leakage Current		10	µA	3
C_{IN}, C_o	Total Input/Output Capacitance		10	pF	4

NOTES:

1. Measured into a 25Ω test load tied to V_{TT} = 1.5 V, as shown in Figure 32.
2. V_{REF} = 2/3 V_{TT}. (V_{TT} = 1.5 V ±10%), V_{REF} has an additional tolerance of ± 2%.
3. This parameter is for inputs without internal pull-ups or pull downs and $0 \le V_{IN} \le V_{TT}$.
4. Total capacitance, as seen from the attachment node on the network, which includes traces on the PCB, IC socket, component package, driver/receiver capacitance, and ESD structure capacitance.

4.2.2. I/O Buffer AC Specification

Table 22 contains the I/O Buffer DC parameters.

Table 22. I/O Buffer AC Parameters

Symbol	Parameter	Min	Max	Unit	Figure	Notes
dV/dt_{EDGE}	Output Signal Edge Rate, rise	0.3	0.8	V/ns		1, 2, 3
dV/dt_{EDGE}	Output Signal Edge Rate, fall	0.3	–0.8	V/ns		1, 2, 3
T_{CO}	Output Clock to Data Time		no spec	ns	Figure 33	4, 5
T_{SU}	Input Setup Time		no spec	ns	Figure 24 Figure 25	4, 6
T_{HOLD}	Input Hold Time		no spec	ns		4, 6

NOTES:

1. This is the maximum instantaneous dV/dt over the entire transition range (Hi-to-Lo or Lo-to-Hi) as measured at the driver's output *pin* while driving the Ref8N network, with the driver and its package model located near the center of the network (see Section 4.4).
2. These are design targets. The acceptance of the buffer is also based on the resultant signal quality. In addition to edge rate, the shape of the rising edge can also have a significant effect on the buffer's performance, therefore the driver must also meet the signal quality criteria in the next section. For example, a rising linear ramp of at 0.8V/ns will generally produce worse signal quality (more ringback) than an edge that rolls off as it approaches V_{TT} even though it might have exceeded that rate earlier. Hi-to-Lo edge rates may exceed this specification and produce acceptable results with a corresponding reduction in V_{OL}. For instance, a buffer with a falling edge rate larger than 1.5V/ns can been deemed acceptable because it produced a V_{OL} less than 500 mV. Lo-to-Hi edges must meet both signal quality and maximum edge rate specifications.
3. The minimum edge rate is a design target, and slower edge rates can be acceptable, although there is a timing impact associated with them in the form of an increase in flight time, since the signal at the receiver will no longer meet the required conditions for T_{SU}. Refer to Section 4.1.4 on computing flight time for more details on the effects of edge rates slower than 0.3 V/ns.
4. These values are not specific to this specification, they are dependent on the location of the driver along a network and the system requirements such as the number of agents, the distances between agents, the construction of the PCB (Z_0, ε_r, trace width, trace type, connectors), the sockets being used, if any, and the value of the termination resistors. Good targets for components to be used in an 8-load 66.6 MHz system would be: T_{CO_MAX} = 4.5 ns, T_{CO_MIN} = 1 ns, T_{SU} = 2.5 ns, and T_{HD} = 0.
5. This value is specified at the output pin of the device. T_{CO} should be measured at the test probe point shown in the Figure 32, but the delay caused by the 50Ω transmission line must be subtracted from the measurement to achieve an accurate value for T_{co} at the output pin of the device. For simulation purposes, the tester load can be represented as a single 25Ω termination resistor connected directly to the pin of the device.
6. See Section 4.2.3 for a description of the procedure for determining the receiver's minimum required setup and hold times.

4.2.2.1. Output Driver Acceptance Criteria

Although Section 4.1.4 describes ways of amending flight time to a receiver when the edge rate is lower than the requirements shown in Table 22, or when there is excessive ringing, it is still preferable to avoid slow edge rates or excessive ringing through good driver and system design, hence the criteria presented in this section.

As mentioned in note 2 of the previous section, the criteria for acceptance of an output driver relate to the edge rate and the signal quality for the Lo-to-Hi transition, and primarily to the signal quality for the Hi-to-Lo transition when the device, with its targeted package, is simulated into the Ref8n network (Figure 36). The edge rate portion of the AC specification is a good initial target, but is insufficient for guaranteeing acceptable performance.

Since Ref8N is not the worst case network, and is expected to be modeled without many real system effects (e.g., inter-trace crosstalk, DC & AC losses), the required signal quality is slightly different than that specified in Section 4.1.3 of this document.

The signal quality criterion for an acceptable driver design is that the signals produced by the driver (at its fastest corner) at all Ref8N receiver *pads* must remain outside of the shaded areas shown in Figure 30. Simulations must be performed at both device and operating extremes: fast process corner at high VCC and low temperature, and slow process corner at low VCC and high temperature, for both the rising and falling edges. The clock frequency should be at the desired maximum (e.g. 66.6 MHz, or higher), and the simulation results should be analyzed both from a quiescent start (i.e., first cycle in a simulation), and when preceded by at least one previous transition (i.e. subsequent simulation cycles).

The boundaries of the keep-out area for the Lo-to-Hi transition are formed by a vertical line at the start of the receiver setup window (a distance T_{SU}' from the next clock edge), an 0.3V/ns ramp line passing through the intersection between the V_{REF} +100 mV level (the 100 mV is assumed extra noise) and the beginning of the setup window, a horizontal line at V_{REF} +300 mV (which covers 200 mV of specified overdrive, and the 100 mV margin for extra noise coupled to the waveform), and finally a vertical line behind the Clock at T_{HD}'. The keep-out zone for the Hi-to-Lo transition uses analogous boundaries in the other direction. Raising V_{REF} by 100 mV is assumed to be equivalent to having 100 mV of extra noise coupled to the waveform giving it more downward ringback, such coupled noise could come from a variety of sources such as trace-to-trace PCB coupling.

T_{SU}' is the receiver's setup time plus board clock driver and clock distribution skew and jitter, plus an additional number that is inherited from the driver's internal timings (to be described next). Since the I/O buffer designer will most likely be simulating the driver circuit alone, certain delays that add to T_{CO}, such as: on-chip clock phase shift, clock distribution skew, and jitter, plus other data latch or JTAG delays would be missing. It is easier if these numbers are added to T_{SU}, yielding T_{SU}' making the driver simulation simpler. For example, assume T_{SU} to be 2.8 ns, PCB clock generation and distribution skew plus jitter to be 1 ns, and unmodeled delays in the driver to be typically about 0.8 ns, this yields a total T_{SU}' = 4.6 ns.

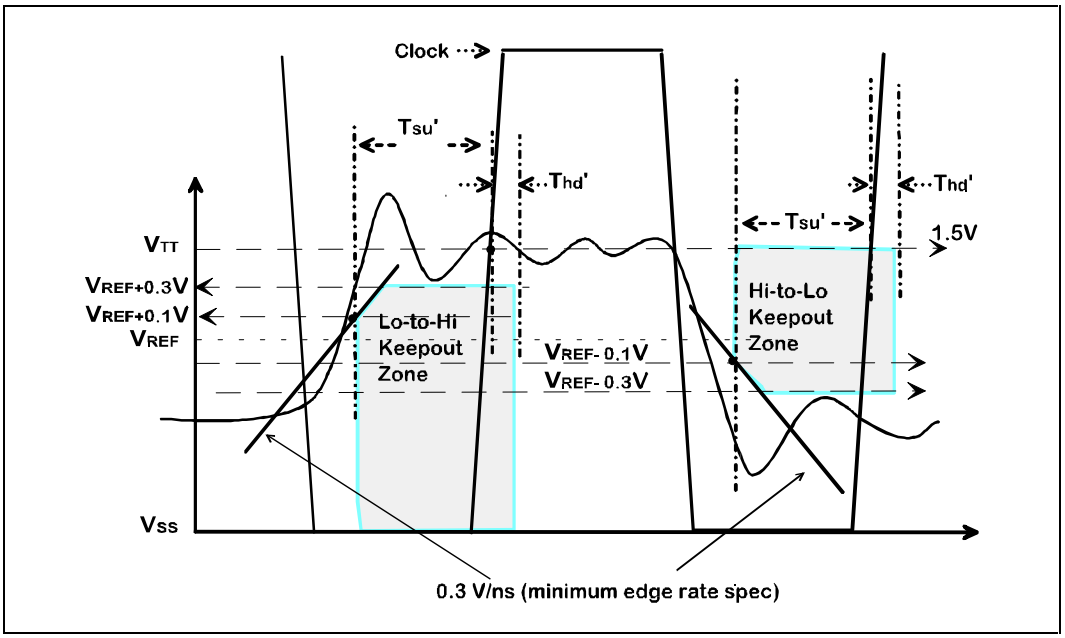


Figure 30. Acceptable Driver Signal Quality

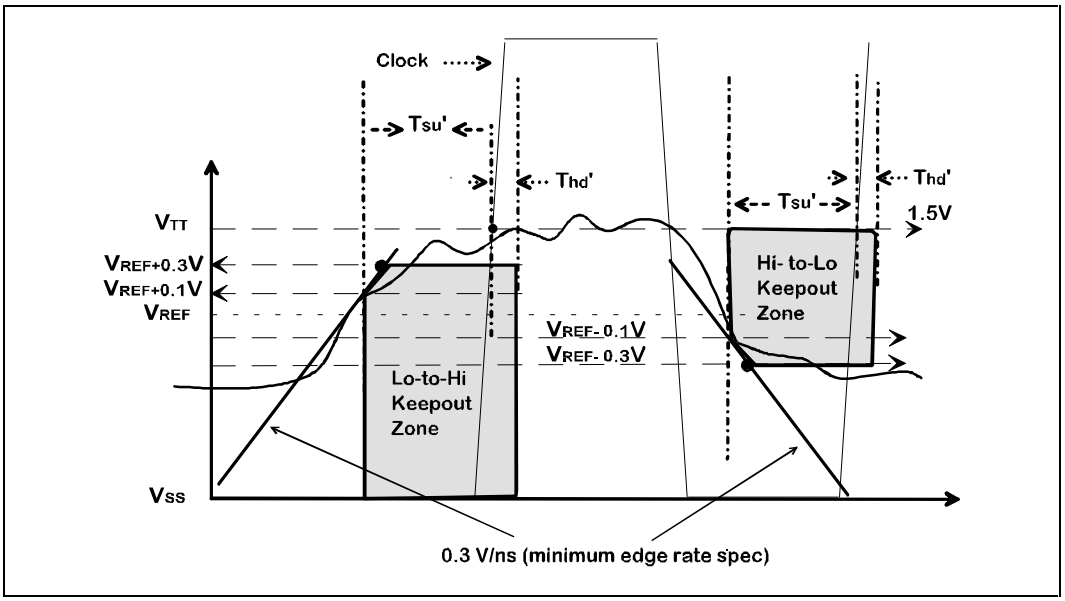


Figure 31. Unacceptable signal, Due to Excessively Slow Edge After Crossing V_{REF}

T_{HD}' is the receiver's hold time plus board clock driver and clock distribution skew **minus** the driver's on-chip clock phase shift, clock distribution skew, and jitter, plus other data latch or JTAG delays (assuming these driver numbers are not included in the driver circuit simulation, as was done for setup in the above paragraph). Note that T_{HD}' may end up being a negative number, i.e. ahead of the clock, rather than after it. That would be acceptable, since that is equivalent to shifting the driver output later in time had these extra delays been added to the driver as opposed to setup and hold.

When using Ref8N to validate a driver design, it is recommended that all relevant combinations of driver and receiver locations be checked.

As with other buffer technologies, such as TTL or CMOS, any given buffer design is not guaranteed to always meet the requirements of all possible system and network topologies. Meeting the acceptance criteria listed in this document helps ensure the I/O buffer can be used in a variety of GTL+ applications, but it is the system designer's responsibility to examine the performance of the buffer in the specific application to ensure that all GTL+ networks meet the signal quality requirements.

4.2.3. Determining Clock-To-Out, Setup and Hold

This section describes how to determine setup, hold and clock to out timings.

4.2.3.1. Clock-to-Output Time, T_{CO}

T_{CO} is measured using the test load in Figure 32, and is the delay from the 1.5 V crossing point of the clock signal at the clock input *pin* of the device, to the V_{REF} crossing point of the output signal at the output *pin* of the device. For simulation purposes, the test load can be replaced by its electrical equivalent, which is a single 25 Ω resistor connected directly to the package pin and terminated to 1.5 V.

In a production test environment, it is nearly impossible to measure T_{CO} directly at the output pin of the device, instead, the test is performed a finite distance away from the pin and compensated for the finite distance. The test load circuit shown in Figure 32 takes this into account by making this finite distance a 50-Ω transmission line. To get the exact timings at the output pin, the propagation delay along the transmission line must be subtracted from the measured value at the probe point.

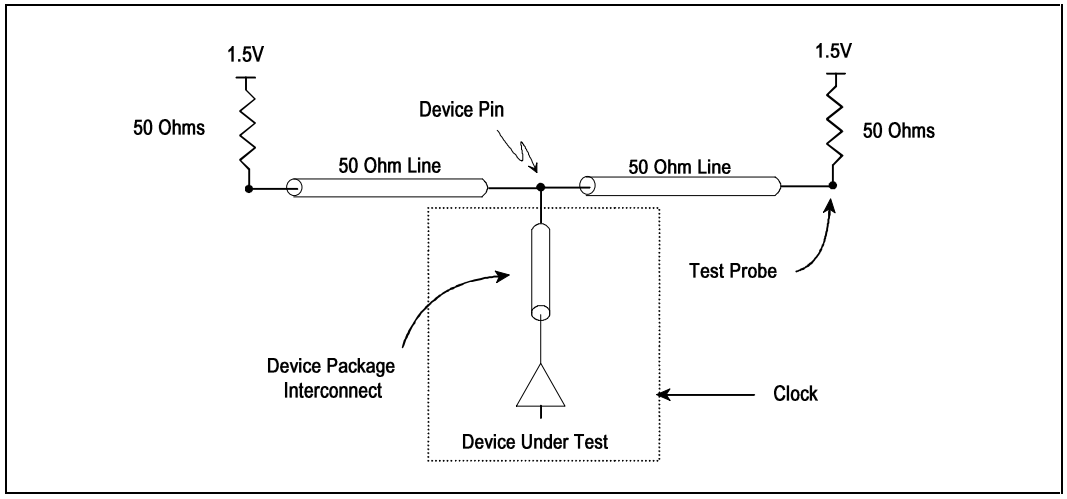


Figure 32. Test Load for Measuring Output AC Timings

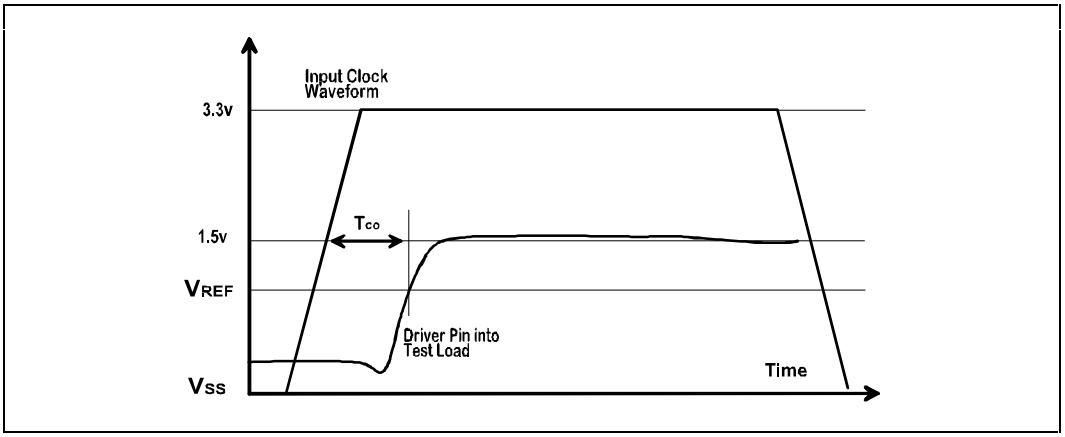


Figure 33. Clock to Output Data Timing (T_{CO})

T_{CO} measurement for a Lo-to-Hi signal transition is shown in Figure 35. The T_{CO} measurement for Hi-to-Lo transitions is similar.

4.2.3.2. Minimum Setup and Hold Times

Setup time for GTL+ (T_{SU}) is defined as:

> The minimum time from the input signal pin crossing of V_{REF} to the clock pin of the receiver crossing the 1.5 V level, which guarantees that the input buffer has captured **new** data at the input pin, given an infinite hold time.

Strictly speaking, setup time must be determined when the input barely meets minimum hold time (see definition of hold time below). However, for current GTL+ systems, hold time should be met well beyond the minimum required in cases where setup is critical. This is because setup is critical when the receiver is far removed from the driver. In such cases, the signal will be held at the receiver for a long time after the clock, since the change needs a long time to propagate from the driver to the receiver.

The recommended procedure for the I/O buffer designer to extract T_{SU} is outlined below. If one employs additional steps, it would be beneficial that any such extra steps be documented with the results of this receiver characterization:

1. The full receiver circuit must be used, comprising the input differential amplifier, any shaping logic gates, and the edge-triggered (or pulse-triggered) flip-flop. The output of the flip-flop must be monitored.
2. The receiver's Lo-to-Hi setup time should be determined using a nominal input waveform like the one shown in Figure 34 (solid line). The Lo-to-Hi input starts at $V_{IN\_LOW\_MAX}$ (V_{REF} - 200 mV) and goes to $V_{IN\_HIGH\_MIN}$ = V_{REF} +200 mV, at a slow edge rate of 0.3 V/ns, with the process, temperature, voltage, and $V_{REF\_INTERNAL}$ of the receiver set to the worst (longest T_{SU}) corner values. Here, V_{REF} is the external (system) reference voltage at the device pin. Due to tolerance in V_{TT} (1.5V, ±10%) and the voltage divider generating system V_{REF} from V_{TT} (±2%), V_{REF} can shift around 1 V by a maximum of ±122 mV. When determining setup time, the internal reference voltage $V_{REF\_INTERNAL}$ (at the reference gate of the diff. amp.) must be set to the value which yields the longest setup time. Here, $V_{REF\_INTERNAL}$ = V_{REF} ±(122 mV +V_{NOISE}). Where, V_{NOISE} is the net maximum differential noise amplitude on the component's internal V_{REF} distribution bus (at the amplifier's reference input gate) comprising noise picked up by the connection from the V_{REF} package pin to the input of the amp.
3. Analogously, for the setup time of Hi-to-Lo transitions (Figure 35), the input starts at $V_{IN\_HIGH\_MIN}$ = V_{REF} +200 mV and drops to

$V_{IN\_LOW\_MAX}$ = V_{REF} - 200 mV at the rate of 0.3V/ns.

4. For both the 0.3 V/ns edge rate and faster edge rates (up to 0.8 V/ns for Lo-to-Hi, and 3 V/ns for Hi-to-Lo —dashed lines in Figure 34 and Figure 35), one must ensure that lower starting voltages of the input swing (V_{START} in the range 'V_{REF}–200 mV' to 0.5 V for Lo-to-Hi transitions, and 1.5 V to 'V_{REF}+200 mV' for Hi-to-Lo transitions —dashed lines in Figure 34 and Figure 35) do not require T_{SU} to be made longer. This step is needed since a lower starting voltage may cause the input differential amplifier to require more time to switch, due to having been in deeper saturation in the initial state.

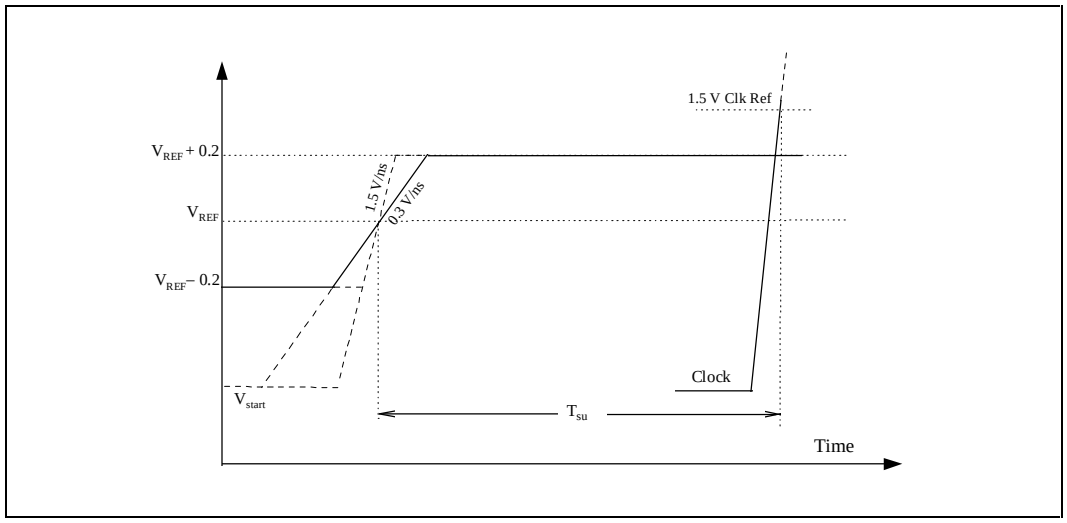


Figure 34. Standard Input Lo-to-Hi Waveform for Characterizing Receiver Setup Time

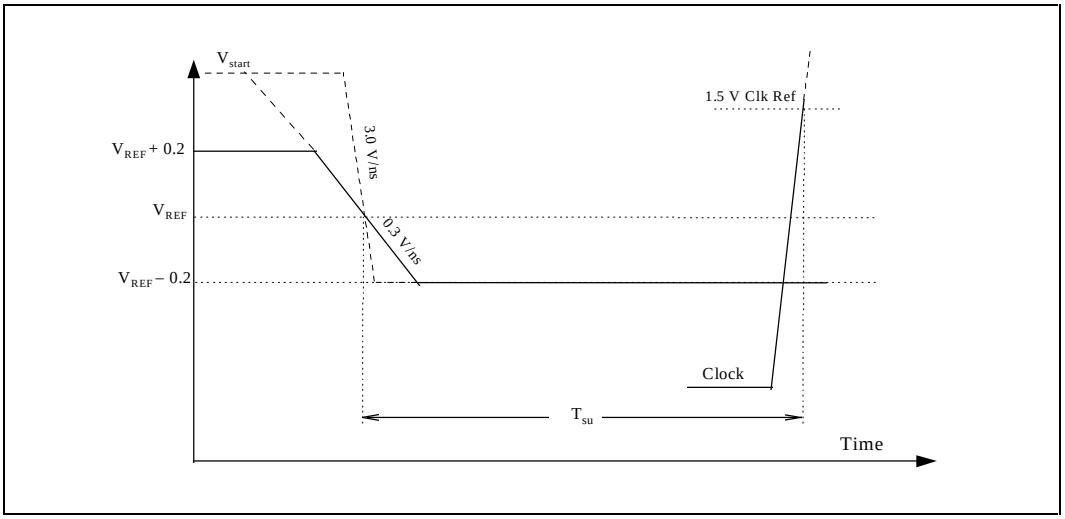


Figure 35. Standard Input Hi-to-Lo Waveform for Characterizing Receiver Setup Time

Hold time for GTL+ , T_{HOLD}, is defined as:

> The minimum time from the clock pin of the receivers crossing of the 1.5 V level to the receiver input signal pin crossing of V_{REF}, which guarantees that the input buffer has captured **new** data at the receiver input signal pin, given an infinite setup time.

Strictly speaking, hold time must be determined when the input barely meets minimum setup time (see definition of setup time above). However, for current GTL+ systems, setup time is expected to be met, well beyond the minimum required in cases where hold is critical. This is because hold is critical when the receiver is very close to the driver. In such cases, the signal will arrive at the receiver shortly after the clock, hence meeting setup time with comfortable margin.

The recommended procedure for extracting T_{HOLD} is outlined below. If one employs additional steps, it would be beneficial that any such extra steps be documented with the results of this receiver characterization:

1. The full receiver circuit must be used, comprising the input differential amplifier, any shaping logic gates, and the edge-triggered (or pulse-triggered) flip-flop. The output of the flip-flop must be monitored.
2. The receiver's Lo-to-Hi hold time should be determined using a nominal input waveform that starts at $V_{IN\_LOW\_MAX}$ (V_{REF} - 200 mV) and goes to V_{TT}, at a fast edge rate of 0.8V/ns, with the process, temperature, voltage, and $V_{REF\_INTERNAL}$ of the receiver set to the fastest (or best) corner values (yielding the longest T_{HOLD}). Here, V_{REF} is the external (system) reference voltage at the device pin. Due to tolerance in V_{TT} (1.5 V, ±10%) and the voltage divider generating system V_{REF} from V_{TT} (±2%), V_{REF} can shift around 1 V by a maximum of ±122 mV. When determining hold time, the internal reference voltage $V_{REF\_INTERNAL}$ (at the reference gate of the diff. amp.) must be set to the value which yields the worst case hold time. Here, $V_{REF\_INTERNAL}$ = V_{REF} ± (122 mV +V_{NOISE}). Where, V_{NOISE} is the net maximum differential noise amplitude on the component's internal V_{REF} distribution bus (at the amplifier's reference input gate) comprising noise picked up by the connection from the V_{REF} package pin to the input of the amp.
3. Analogously, for the hold time of Hi-to-Lo transitions, the input starts at $V_{IN\_HIGH\_MIN}$ = V_{REF} +200 mV and drops to < 0.5 V at the rate of 3V/ns.

4.2.3.3. Receiver Ringback Tolerance

Refer to Section 4.1.3.1 for a complete description of the definitions and methodology for determining receiver ringback tolerance.

4.2.4. System-Based Calculation of Required Input and Output Timings

Below are two sample calculations. The first determines T_{CO-MAX} and T_{SU-MIN}, while the second determines $T_{HOLD-MIN}$. These equations can be used for any system by replacing the assumptions listed below, with the actual system constraints.

4.2.4.1. Calculating Target T_{CO-MAX}, and T_{SU-MIN}

T_{CO-MAX} and T_{SU-MIN} can be calculated from the Setup Time equation given earlier in Section 4.1.4:

$$T_{FLIGHT-MAX} \leq T_{PERIOD-MIN} - (T_{CO-MAX} + T_{SU-MIN} + T_{CLK\_SKEW-MAX} + T_{CLK\_JITTER-MAX})$$

As an example, for two identical agents located on opposite ends of a network with a flight time of 7.3 ns, and the other assumptions listed below, the following calculations for T_{CO-MAX} and T_{SU-MIN} can be done:

Assumptions:

- $T_{PERIOD-MIN}$ 15 ns (66.6 MHz)
- $T_{FLIGHT-MAX}$ 7.3 ns (given flight time)
- $T_{CLK\_SKEW-MAX}$ 0.7 ns (0.5ns for clk driver) (0.2 ns for board skew)
- $T_{CLK\_JITTER-MAX}$ 0.2 ns (Clock phase error)
- T_{CO-MAX} ?? (Clock to output data time)
- T_{SU-MIN} ?? (Required input setup time)

Calculation:

- $7.3 \leq 15 - (T_{CO-MAX} + T_{SU-MIN} + 0.7 + 0.2)$
- $T_{CO-MAX} + T_{SU-MIN} \leq 6.8$ ns

The time remaining for T_{CO-MAX} and T_{SU-MIN} can be split ~60/40% (recommendation). Therefore, in this example, T_{CO-MAX} would be 4.0 ns, and T_{SU-MIN} 2.8 ns.

NOTE

This a numerical example, and does not necessarily apply to any particular device.

Off-end agents will have less distance to the farthest receiver, and therefore will have shorter flight times. T_{CO} values longer than the example above do not necessarily preclude high-frequency (e.g. 66.6 MHz) operation, but will result in placement constraints for the device, such as being required to be placed in the middle of the daisy-chain bus.

4.2.5. Calculating Target $T_{HOLD-MIN}$

To calculate the longest possible minimum required hold time target value, assume that T_{CO-MIN} is one fourth of T_{CO-MAX}, and use the hold time equation given earlier. Note that Clock Jitter is not a part of the equation, since data is released by the driver and must be held at the receiver relative to the same clock edge:

$$T_{HOLD-MIn} \leq T_{FLIGHT-MIN} + T_{CO-MIN} - T_{CLK\_SKEW-MAX}$$

Assumptions:

- T_{CO-MAX} 4.0 ns (Max clock to data time)
- T_{CO-MIN} 1.0 ns (Assumed ¼ of max)
- $T_{CLK\_SKEW-MAX}$ 0.7 ns (Driver to receiver skew)
- $T_{FLIGHT-MIN}$ 0.1 ns (Min of 0.5” at 0.2 ns/inch)
- $T_{HOLD-MIN}$?? (Minimum signal hold time)

Calculation:

- $T_{HOLD-MIN} \leq 0.1 + 1.0 - 0.7$
- $T_{HOLD-MIN} \leq 0.4$ ns.

NOTE

This a numerical example, and does not necessarily apply to any particular device.

4.3. Package Specification

This information is also included for designers of components for a GTL+ bus. The package that the I/O transceiver will be placed into must adhere to two critical parameters. They are package trace length, (the electrical distance from the pin to the die), and package capacitance. The specifications for package trace length and package capacitance are not explicit, but are implied by the system and I/O buffer specifications.

4.3.1. Package Trace Length

The System specification requires that all signals be routed in a daisy chain fashion, and that no stub in the network exceed 250 ps in electrical length. The stub includes any printed circuit board (PCB) routing to the pin of the package from the "Daisy Chain" net, as well as a socket if necessary, and the trace length of the package interconnect (i.e. the electrical length from the pin, through the package, across a bond wire if necessary, and to the die). For example, for a PGA package, which allows PCB routing both to and from a pin and is soldered to the PCB, the maximum package trace length cannot exceed 250 ps. If the PGA package is socketed, the maximum package trace length would be ~225 ps since a typical PGA socket is around 25 ps in electrical length. For a QFP package, which typically requires a short stub on the PCB from the pad landing to a via (~50 ps), the package lead frame length should be less than ~200 ps.

4.3.2. Package Capacitance

The maximum package pin capacitance is a function of the Input/Output capacitance of the I/O transceiver. The I/O Buffer specification requires the total of the package capacitance, output driver, input receiver and ESD structures, as seen from the pin, to be less than 10 pF. Thus, the larger the I/O transceiver capacitance, the smaller the allowable package capacitance.

4.4. Ref8N Network

The Ref8N network shown in Figure 36, which represents an eight-node reference network (hence the name Ref8N), is used to characterize I/O drivers' behavior into a known environment. This network is not a worst case, but a representative sample of a typical system environment. A SPICE deck of the network is also given.

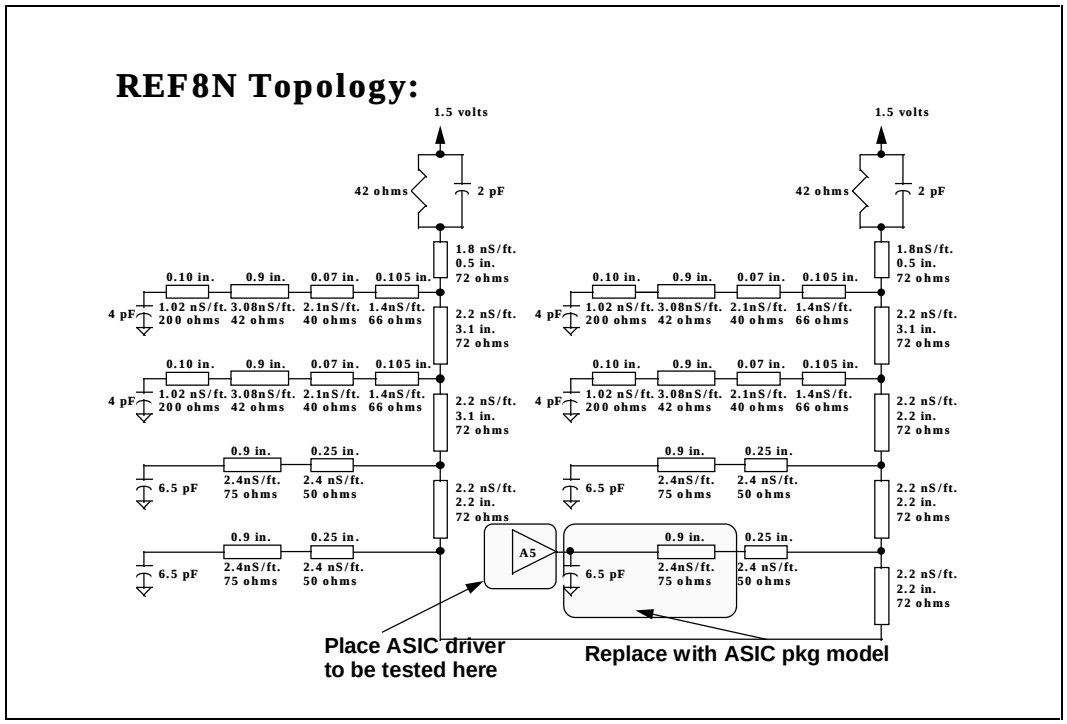


Figure 36. Ref8N Topology

4.4.1. Ref8N HSPICE Netlist

```
$REF8N, Rev 1.1

Vpu vpu GND DC(vtt)

rterm PU1 vpu (R=42)                $ Pull-up termination resistance
crterm PU1 vpu 2PF                  $ Pull-up termination capacitance
TPU PU1 0 line1 0 Z0=72 TD=.075NS   $ PCB link from terminator to load 1

X1 line1 load1 socket               $ Socket model
T1 load1 0 load1a 0 Z0=42 TD=230PS  $ CPU package model
T2 load1a 0 CPU_1 0 Z0=200 TD=8.5PS $ Bondwire
CCPU_1 CPU_1 0 4PF                  $ CPU input capacitance

T3 line1 0 line2 0 Z0=72 TD=568PS   $ PCB trace between packages

x2 line2 load2 socket               $ Socket model
T4 load2 0 load2a 0 Z0=42 TD= 230ps $ CPU worst case package
```

```
T5 load2a 0 p6_2 0 Z0=200 TD=8.5ps   $ Bondwire
CCPU_2 p6_2 0 4pf                    $ CPU input capacitance

T6 line2 0 line3 0 Z0=72 TD=568ps    $ PCB trace between packages
T7 line3 0 load3 0 Z0=50 TD=50ps     $ PCB trace from via to landing pad
T8 load3 0 asic_1 0 Z0=75 TD=180PS   $ ASIC package
CASIC_1 asic_1 0 6.5PF               $ ASIC input capacitance (die capacitance)

T9 line3 0 line4 0 Z0=72 TD=403PS    $ PCB trace between packages
T10 line4 0 load4 0 Z0=50 TD=50PS    $ PCB trace from via to landing pad
T11 load4 0 asic_2 0 Z0=75 TD=180PS  $ ASIC package
CASIC_2 asic_2 0 6.5PF               $ ASIC input capacitance (die capacitance)

T12 line4 0 line5 0 Z0=72 TD=403PS   $ PCB trace between packages
T13 line5 0 load5 0 Z0=50 TD=50PS    $ PCB trace from via to landing pad
T14 load5 0 asic_3 0 Z0=75 TD=180PS  $ Replace these two lines with
CASIC_3 asic_3 0 6.5PF               $ the equivalent model for your package.
                                     $ (This model should include the package
                                     $ pin, package trace, bond wire and any die
                                     $ capacitance that is not already included
                                     $ in your driver model.)

T15 line5 0 line6 0 Z0=72 TD=403PS   $ PCB trace between packages
T16 line6 0 load6 0 Z0=50 TD=50PS    $ PCB trace from via to landing pad
T17 load6 0 asic_4 0 Z0=75 TD=180PS  $ ASIC package
CASIC_4 asic_4 0 6.5PF               $ ASIC input capacitance

T18 line6 0 line7 0 Z0=72 TD=403PS   $ PCB trace between packages
X3 line7 load7 socket                $ Socket model
T19 load7 0 load7a 0 Z0=42 TD=230PS  $ CPU worst case package
T20 load7a 0 p6_3 0 Z0=200 TD=8.5PS  $ Bondwire
CCPU_3 p6_3 0 4PF                    $ CPU input capacitance

T21 line7 0 line8 0 Z0=72 TD=568PS   $ PCB trace between packages
X4 line8 load8 socket                $ Socket model
T22 load8 0 load8a 0 Z0=42 TD=230PS  $ CPU worst case package
T23 load8a 0 p6_4 0 Z0=200 TD=8.5PS  $ Bondwire
CCPU_4 p6_4 0 4PF                    $ CPU input capacitance

T24 line8 0 R_TERM 0 Z0=72 TD=75PS   $ PCB trace to termination resistor
Rterm1 R_TERM vpu (R=42)              $ Pull-up termination resistance
CRTERM1 R_TERM vpu (C=2PF)           $ Pull-up termination capacitance

Rout bond asic_3.001

.subckt socket in out                $ Socket model
```

```
TX out 0 jim 0 Z0=40 TD=12.25PS
ty jim 0 in 0 Z0=66 TD=12.25ps
.ENDS
```

5.0 3.3 V Tolerant Signal Quality Specifications

The signals that are 3.3 V tolerant should also meet signal quality specifications to guarantee that the components read data properly and to ensure that incoming signals do not affect the long term reliability of the component. There are three signal quality parameters defined for the 3.3 V tolerant signals. They are Overshoot/Undershoot, Ringback and Settling Limit. All three signal quality parameters are shown in Figure 37. The *Pentium® Pro Processor I/O Buffer Models—IBIS Format (On world wide web page http://www.intel.com)* contain models for simulating 3.3 V tolerant signal distribution.

5.1. OVERSHOOT/UNDERSHOOT GUIDELINES

Overshoot (or undershoot) is the absolute value of the maximum voltage allowed above the nominal high voltage or below VSS. The overshoot/undershoot guideline limits transitions beyond $V_{CC}P$ or V_{SS} due to the fast signal edge rates. See Figure 37. The processor can be damaged by repeated overshoot events on 3.3 V tolerant buffers if the charge is large enough (i.e. if the overshoot is great enough). However, excessive ringback is the dominant harmful effect resulting from overshoot or undershoot (i.e. violating the overshoot/undershoot guideline will make satisfying the ringback specification difficult). The **overshoot/undershoot guideline is 0.8 V** and assumes the absence of diodes on the input. These guidelines should be verified in simulations **without the on-chip ESD protection diodes present** because the diodes will begin clamping the 3.3 V tolerant signals beginning at approximately 1.5 V above $V_{CC}P$ and 0.5 V below VSS. If signals are not reaching the clamping voltage, then this is not an issue. A system should not rely on the diodes for overshoot/undershoot protection as this will negatively affect the life of the components and make meeting the ringback specification very difficult.

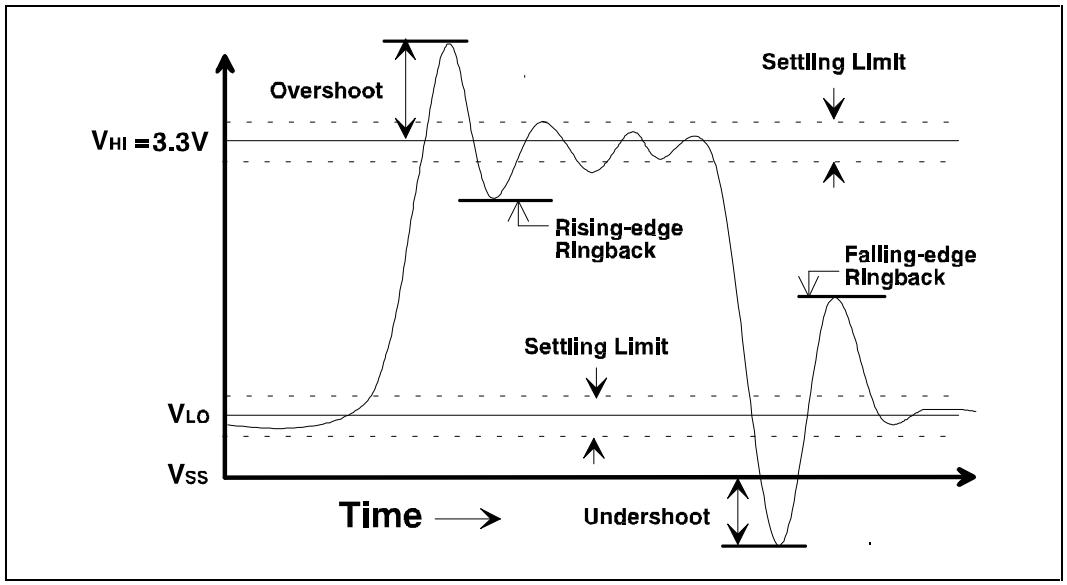


Figure 37. 3.3 V Tolerant Signal Overshoot/Undershoot and Ringback

5.2. RINGBACK SPECIFICATION

Ringback refers to the amount of reflection seen after a signal has undergone a transition. **The ringback specification is the voltage that the signal rings back to after achieving its farthest excursion.** See Figure 37 for an illustration of ringback. Excessive ringback can cause false signal detection or extend the propagation delay. The ringback specification applies to the input pin of each receiving agent. Violations of the signal Ringback specification are not allowed under any circumstances.

Ringback can be simulated with or without the input protection diodes that can be added to the input buffer model. However, signals that reach the clamping voltage should be evaluated further. See Table 23 for the signal ringback specifications for Non-GTL+ signals

Table 23. Signal Ringback Specifications

Transition	Maximum Ringback (with input diodes present)
0→1	2.5 V
1→0	0.8 V

5.3. SETTLING LIMIT GUIDELINE

A Settling Limit defines the maximum amount of ringing at the receiving pin that a signal must be limited to before its next transition. The amount allowed is 10% of the total signal swing (V_{HI}-V_{LO}) above and below its final value. A signal should be within the settling limits of its final value, when either in its high state of low state, before it transitions again.

Signals that are not within their settling limit before transitioning are at risk of unwanted oscillations which could jeopardize signal integrity. Simulations to verify Settling Limit may be done either with or without the input protection diodes present. Violation of the Settling Limit guideline is acceptable if simulations of 5-10 successive transitions do not show the amplitude of the ringing increasing in the subsequent transitions.

6.0. THERMAL SPECIFICATIONS

Table 5 specifies the Pentium Pro processor power dissipation. It is highly recommended that systems be designed to dissipate at least ***35-40W*** per processor to allow the same design to accommodate

higher frequency or otherwise enhanced members of the Pentium Pro processor family.

6.1. Thermal Parameters

This section defines the terms used for Pentium Pro processor thermal analysis.

6.1.1. AMBIENT TEMPERATURE

Ambient temperature, T_A, is the temperature of the ambient air surrounding the package. In a system environment, ambient temperature is the temperature of the air upstream from the package and in its close vicinity; or in an active cooling system, it is the inlet air to the active cooling device.

6.1.2. CASE TEMPERATURE

To ensure functionality and reliability, the Pentium Pro processor is specified for proper operation when T_C (case temperature) is within the specified range in Table 5. Special care is required when measuring the case temperature to ensure an accurate temperature measurement. Thermocouples are often used to measure T_C. Before any temperature measurements, the thermocouples must be calibrated. When measuring the temperature of a surface which is at a different temperature from the surrounding ambient air, errors could be introduced in the measurements if not handled properly. The measurement errors could be due to having a poor thermal contact between the thermocouple junction and the surface, heat loss by radiation, or by conduction through thermocouple leads. To minimize the measurement errors, the following approach is recommended:

- Use a 35 gauge K-type thermocouple or equivalent.
- Attach the thermocouple bead or junction to the package top surface at a location corresponding to the center of the Pentium Pro processor die. (Location A in Figure 38) Using the center of the Pentium Pro processor die gives a more accurate measurement and less variation as the boundary condition changes
- Attach the thermocouple bead or junction at a 90° angle by an adhesive bond (such as thermal grease or heat-tolerant tape) to the package top surface as shown in Figure 39. When a heat sink is attached, a hole should be drilled through the heat sink to allow probing the Pentium Pro processor package above the center of the Pentium Pro processor die. The hole diameter should be no larger than 0.150.”

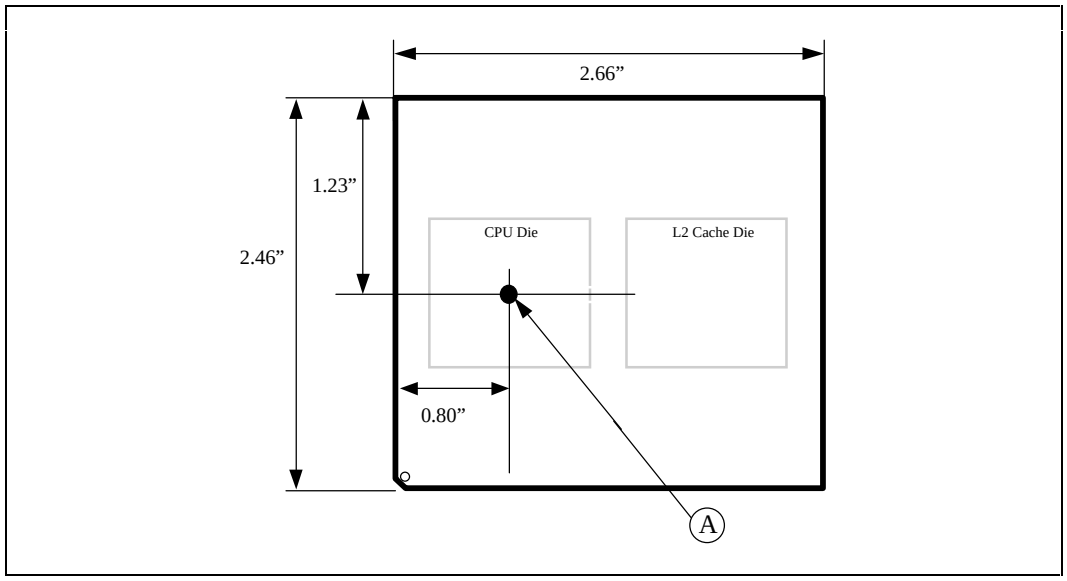


Figure 38. Location of Case Temperature Measurement (Top-side View)

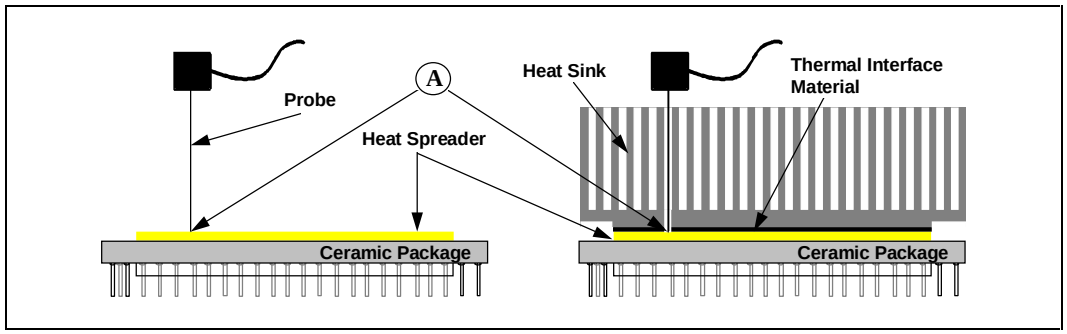


Figure 39. Thermocouple Placement

6.1.3. THERMAL RESISTANCE

The thermal resistance value for the case-to-ambient, Θ_{CA}, is used as a measure of the cooling solution's thermal performance. Θ_{CA} is comprised of the case-to-sink thermal resistance, Θ_{CS}, and the sink-to-ambient thermal resistance, Θ_{SA}. Θ_{CS} is a measure of the thermal resistance along the heat flow path from the top of the IC package to the bottom of the thermal cooling solution. This value is strongly dependent on the material, conductivity, and thickness of the thermal interface used. Θ_{SA} is a measure of the thermal resistance from the top of the cooling solution to the local ambient air. Θ_{SA} values depend on the material, thermal conductivity, and geometry of the thermal cooling solution as well as on the airflow rates.

The parameters are defined by the following relationships where Θ is measured in °C/W (See also Figure 40.):

- $\Theta_{CA} = (T_C - T_A) / P_D$
- $\Theta_{CA} = \Theta_{CS} + \Theta_{SA}$

Where:

- Θ_{CA} = Case-to-Ambient thermal resistance
- Θ_{CS} = Case-to-Sink thermal resistance
- Θ_{SA} = Sink-to-Ambient thermal resistance
- T_C = Case temperature at defined location (°C)
- T_A = Ambient temperature (°C)
- P_D = Device power dissipation (W)

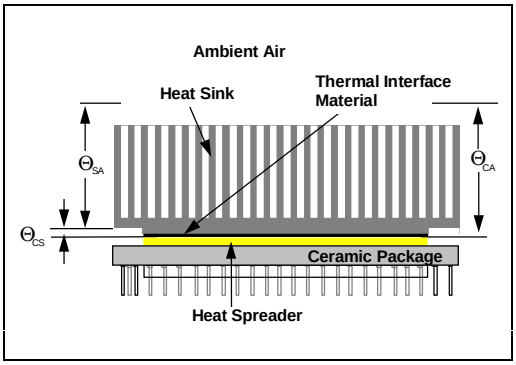


Figure 40. Thermal Resistance Relationships

6.2. Thermal Analysis

Table 24 below lists the case-to-ambient thermal resistances of the Pentium Pro processor for different air flow rates and heat sink heights.

Table 24. Case-To-Ambient Thermal Resistance

	Θ_{CA} [°C/W] vs. Airflow [Linear Feet per Minute] and Heat Sink Height[1]					
Airflow (LFM):	**100**	**200**	**400**	**600**	**800**	**1000**
With 0.5” Heat Sink [2]	—	3.16	2.04	1.66	1.41	1.29
With 1.0” Heat Sink [2]	2.55	1.66	1.08	0.94	0.80	0.76
With 1.5” Heat Sink [2]	1.66	1.31	0.90	0.78	0.71	0.67
With 2.0” Heat Sink [2]	1.47	1.23	0.87	0.75	0.69	0.65

NOTES:

1. All data taken at sea level. For altitudes above sea level, it is recommended that a derating factor of 1°C/1000 feet be used.
2. Heat Sink: 2.235” square omni-directional pin, aluminum heat sink with a pin thickness of 0.085”, a pin spacing of 0.13” and a base thickness of 0.15”. See Figure 41. A thin layer of thermal grease (Thermoset TC208 with thermal conductivity of 1.2W/m-°K) was used as the interface material between the heat sink and the package.

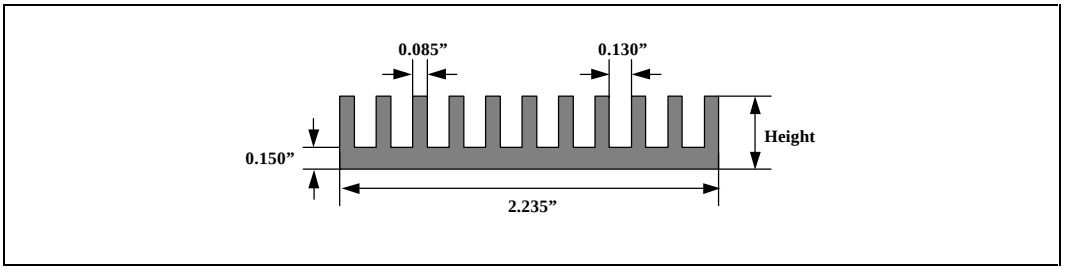


Figure 41. Analysis Heat Sink Dimensions

Table 25 shows the T_A required given a 29.2 W processor (150 MHz, 256K cache), and a T_C of 85°C.. Table 26 shows the T_A required assuming a 40W processor. Table 25 and Table 26 were produced by using the relationships of Section 6.1.3. and the data of Table 24.

Table 25. Ambient Temperature Required per Heat Sink Height for 29.2 W and 85° Case

	T_A vs. Airflow [Linear Feet per Minute] and Heat Sink Height[1]					
Airflow (LFM):	**100**	**200**	**400**	**600**	**800**	**1000**
With 0.5” Heat Sink [2]	—	-8	25	36	43	47
With 1.0” Heat Sink [2]	10	36	53	57	61	62
With 1.5” Heat Sink [2]	36	46	58	62	64	65
With 2.0” Heat Sink [2]	42	49	59	63	64	66

NOTES:

1. At sea level. See Table 24.
2. Heat Sink design as in Table 24.

Table 26. Ambient Temperature Required per Heat Sink Height for 40 W and 85° Case

	T_A vs. Airflow [Linear Feet per Minute] and Heat Sink Height[1]					
Airflow (LFM):	**100**	**200**	**400**	**600**	**800**	**1000**
With 0.5" Heat Sink [2]	—	—	3	18	28	33
With 1.0" Heat Sink [2]	—	18	41	47	53	54
With 1.5" Heat Sink [2]	18	32	49	53	56	58
With 2.0" Heat Sink [2]	26	35	50	55	57	59

NOTES:

1. At sea level. See Table 24.
2. Heat Sink design as in Table 24.

7.0. MECHANICAL SPECIFICATIONS

The Pentium Pro processor is packaged in a modified staggered 387 pin ceramic pin grid array (SPGA) with a gold plated Copper-Tungsten (CuW) heat spreader on top. Mechanical specifications and the pin assignments follow.

7.1. Dimensions

The mechanical specifications are provided in Table 27. Figure 42 shows the bottom and side views with package dimensions for the Pentium Pro processor and Figure 43 shows the top view with dimensions. Figure 44 is the top view of the Pentium Pro processor with V_{CCP}, V_{CCS}, V_{CC5}, and V_{SS} locations shown. **Be sure to read Section 8 for the mechanical constraints for the OverDrive processor. Also, investigate the tools that will be used to debug the system before laying out the system.**

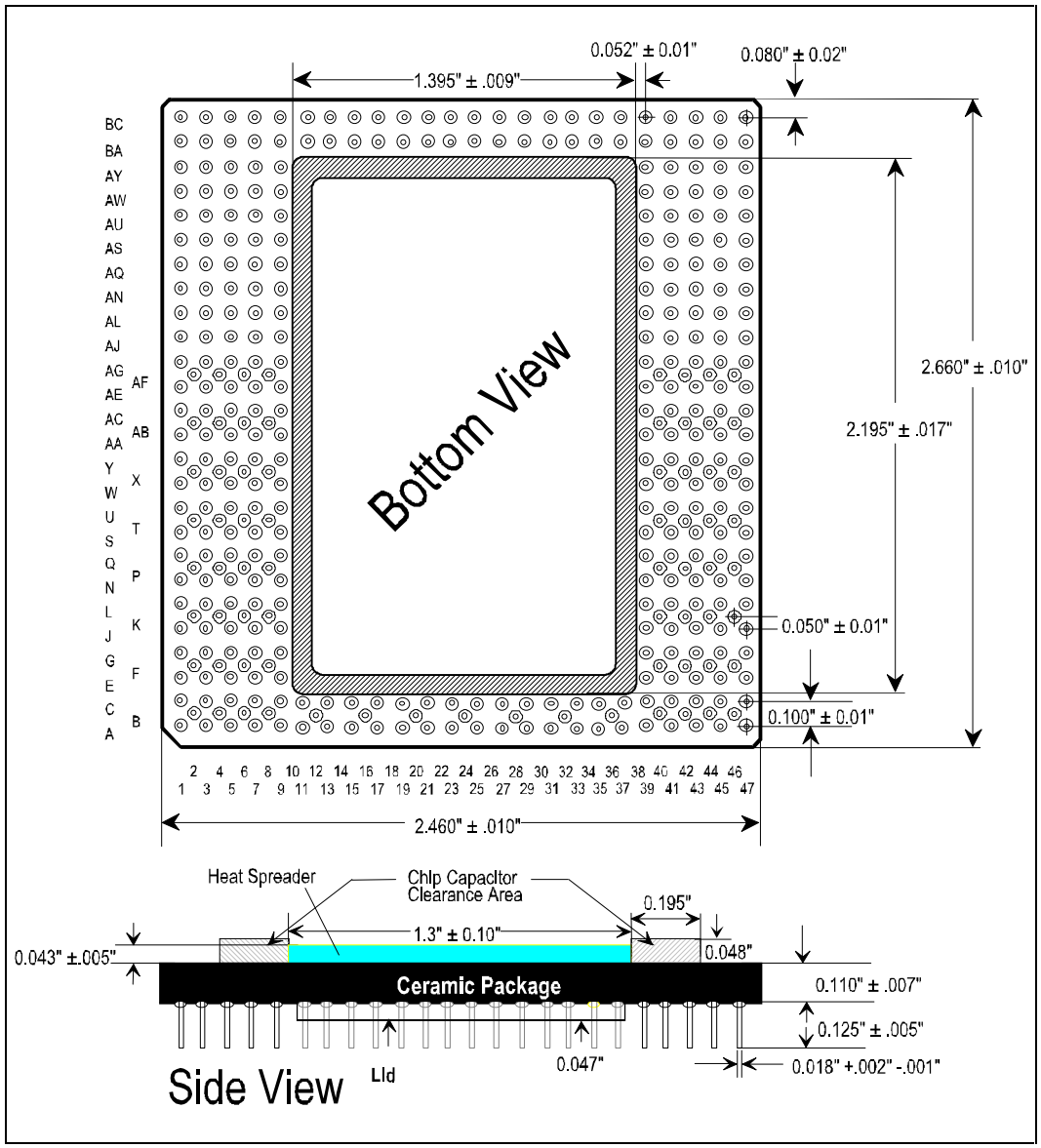


Figure 42. Package Dimensions (Bottom View)

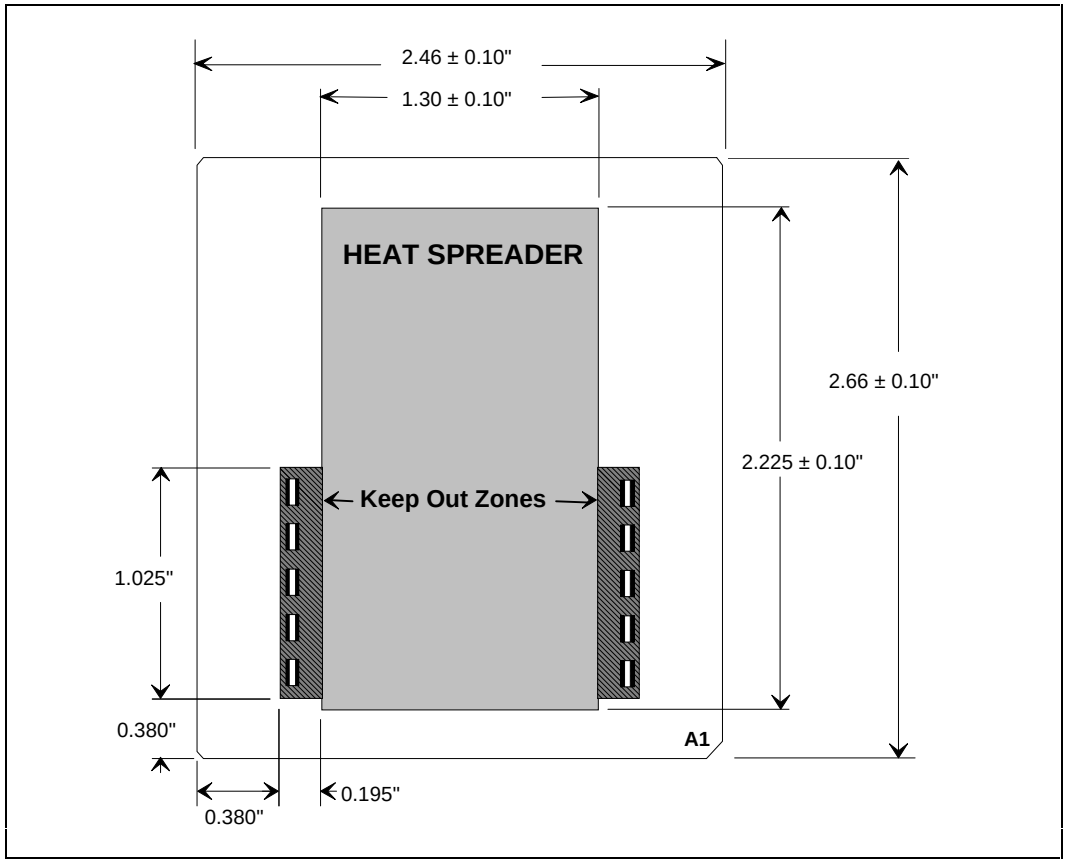


Figure 43. Top View of Keep Out Zones and Heat Spreader

Table 27. Pentium® Pro Processor Package

Parameter	Value
Package Type	PGA
Total Pins	387
Pin Array	Modified Staggered
Package Size	2.66” x 2.46” (7.76cm x 6.25cm)
Heat Spreader Size	2.225” x 1.3” x 0.04” (5.65cm x 3.3cm x 0.1cm)
Approximate Weight	90 grams

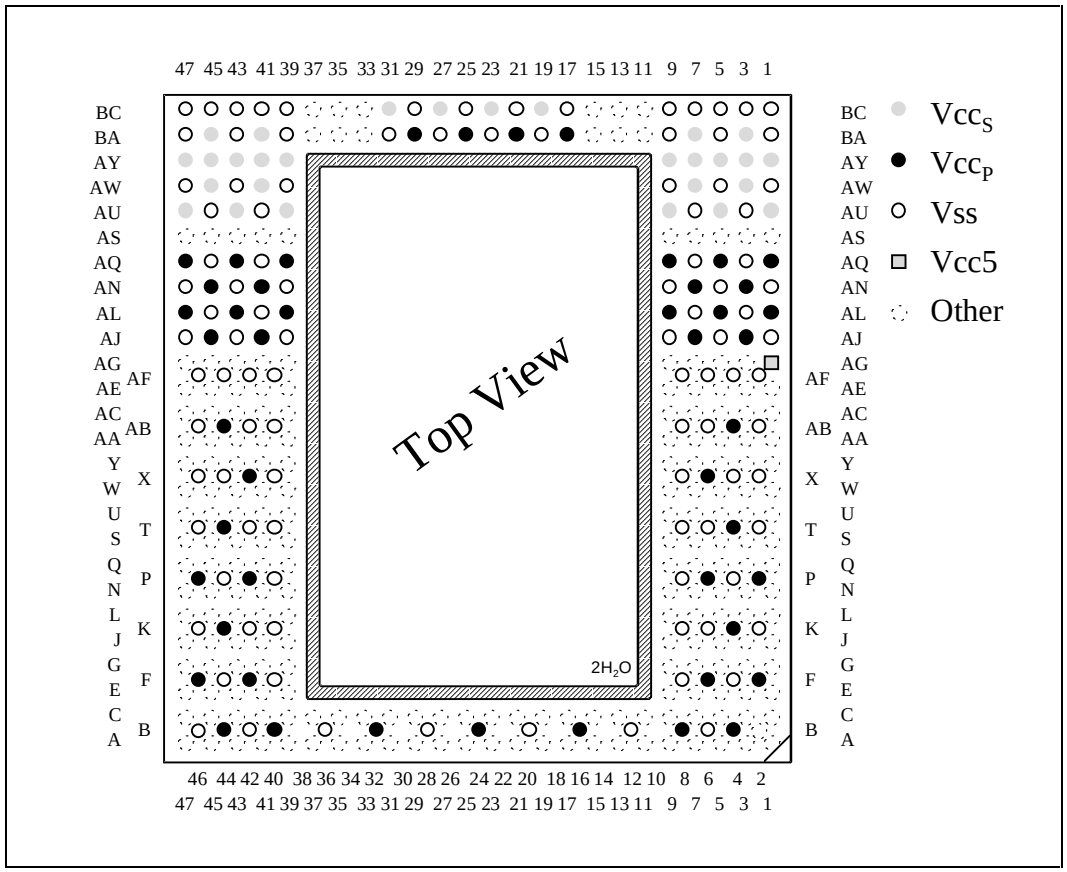


Figure 44. Pentium® Pro Processor Top View with Power Pin Locations

7.2. Pinout

Table 28 is the pin listing in pin number order. Table 29 is the pin listing in pin name order. Please see Section 3.8. to determine a signal's I/O type. Bus signals are described in Appendix A and the other pins are described in Section 3 and in Table 2.

Table 28. Pin Listing in Pin # Order

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
A1	$V_{REF}0$	B24	$V_{CC}P$	C47	D21#
A3	STPCLK#	B28	V_{SS}	E1	A29#
A5	TCK	B32	$V_{CC}P$	E3	A30#
A7	TRST#	B36	V_{SS}	E5	A32#
A9	IGNNE#	B40	$V_{CC}P$	E7	A33#
A11	A20M#	B42	V_{SS}	E9	A34#
A13	TDI	B44	$V_{CC}P$	E39	D22#
A15	FLUSH#	B46	V_{SS}	E41	D23#
A17	THERMTRIP#	C1	A35#	E43	D25#
A19	BCLK	C3	IERR#	E45	D24#
A21	RESERVED	C5	BERR#	E47	D26#
A23	TESTHI	C7	$V_{REF}1$	F2	$V_{CC}P$
A25	TESTHI	C9	FRCERR	F4	V_{SS}
A27	D1#	C11	INIT#	F6	$V_{CC}P$
A29	D3#	C13	TDO	F8	V_{SS}
A31	D5#	C15	TMS	F40	V_{SS}
A33	D8#	C17	FERR#	F42	$V_{CC}P$
A35	D9#	C19	PLL1	F44	V_{SS}
A37	D14#	C21	TESTLO	F46	$V_{CC}P$
A39	D10#	C23	PLL2	G1	A22#
A41	D11#	C25	D0#	G3	A24#
A43	D13#	C27	D2#	G5	A27#
A45	D16#	C29	D4#	G7	A26#
A47	$V_{REF}4$	C31	D6#	G9	A31#
B2	CPUPRES#	C33	D7#	G39	D27#
B4	$V_{CC}P$	C35	D12#	G41	D29#
B6	V_{SS}	C37	D15#	G43	D30#
B8	$V_{CC}P$	C39	D17#	G45	D28#
B12	V_{SS}	C41	D20#	G47	D31#
B16	$V_{CC}P$	C43	D18#	J1	A19#
B20	V_{SS}	C45	D19#	J3	A21#

Table 28. Pin Listing in Pin # Order (Continued)

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
J5	A20#	N39	D44#	S45	D53#
J7	A23#	N41	D45#	S47	D50#
J9	A28#	N43	D47#	T2	V_{SS}
J39	D32#	N45	D42#	T4	$V_{CC}P$
J41	D35#	N47	D41#	T6	V_{SS}
J43	D38#	P2	$V_{CC}P$	T8	V_{SS}
J45	D33#	P4	V_{SS}	T40	V_{SS}
J47	D34#	P6	$V_{CC}P$	T42	V_{SS}
K2	V_{SS}	P8	V_{SS}	T44	$V_{CC}P$
K4	$V_{CC}P$	P40	V_{SS}	T46	V_{SS}
K6	V_{SS}	P42	$V_{CC}P$	U1	AP0#
K8	V_{SS}	P44	V_{SS}	U3	RSP#
K40	V_{SS}	P46	$V_{CC}P$	U5	BPRI#
K42	V_{SS}	Q1	A9#	U7	BNR#
K44	$V_{CC}P$	Q3	A7#	U9	BR3#
K46	V_{SS}	Q5	A5#	U39	DEP7#
L1	RESERVED	Q7	A8#	U41	$V_{REF}6$
L3	A16#	Q9	A10#	U43	D60#
L5	A15#	Q39	D51#	U45	D56#
L7	A18#	Q41	D52#	U47	D55#
L9	A25#	Q43	D49#	W1	SMI#
L39	D37#	Q45	D48#	W3	BR1#
L41	D40#	Q47	D46#	W5	REQ4#
L43	D43#	S1	A6#	W7	REQ1#
L45	D36#	S3	A4#	W9	REQ0#
L47	D39#	S5	A3#	W39	DEP2#
N1	A12#	S7	$V_{REF}2$	W41	DEP4#
N3	A14#	S9	AP1#	W43	D63#
N5	A11#	S39	D59#	W45	D61#
N7	A13#	S41	D57#	W47	D58#
N9	A17#	S43	D54#	X2	V_{SS}

Table 28. Pin Listing in Pin # Order (Continued)

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
X4	V_{SS}	AB40	V_{SS}	AF46	V_{SS}
X6	$V_{CC}P$	AB42	V_{SS}	AG1	$V_{CC}5$
X8	V_{SS}	AB44	$V_{CC}P$	AG3	UP#
X40	V_{SS}	AB46	V_{SS}	AG5	RESERVED
X42	$V_{CC}P$	AC1	RESERVED	AG7	PWRGOOD
X44	V_{SS}	AC3	HIT#	AG9	RESERVED
X46	V_{SS}	AC5	BR0#	AG39	RESERVED
Y1	REQ3#	AC7	RP#	AG41	LINT1/NMI
Y3	REQ2#	AC9	RS0#	AG43	LINT0/INTR
Y5	DEFER#	AC39	BP3#	AG45	$V_{REF}7$
Y7	$V_{REF}3$	AC41	BPM0#	AG47	RESERVED
Y9	TRDY#	AC43	BINIT#	AJ1	V_{SS}
Y39	PRDY#	AC45	DEP0#	AJ3	$V_{CC}P$
Y41	RESET#	AC47	DEP3#	AJ5	V_{SS}
Y43	DEP1#	AE1	RESERVED	AJ7	$V_{CC}P$
Y45	DEP6#	AE3	ADS#	AJ9	V_{SS}
Y47	D62#	AE5	RS1#	AJ39	V_{SS}
AA1	BR2#	AE7	RS2#	AJ41	$V_{CC}P$
AA3	DRDY#	AE9	AERR#	AJ43	V_{SS}
AA5	DBSY#	AE39	TESTHI	AJ45	$V_{CC}P$
AA7	HITM#	AE41	PICD1	AJ47	V_{SS}
AA9	LOCK#	AE43	BP2#	AL1	$V_{CC}P$
AA39	BPM1#	AE45	RESERVED	AL3	V_{SS}
AA41	PICD0	AE47	$V_{REF}5$	AL5	$V_{CC}P$
AA43	PICCLK	AF2	V_{SS}	AL7	V_{SS}
AA45	PREQ#	AF4	V_{SS}	AL9	$V_{CC}P$
AA47	DEP5#	AF6	V_{SS}	AL39	$V_{CC}P$
AB2	V_{SS}	AF8	V_{SS}	AL41	V_{SS}
AB4	$V_{CC}P$	AF40	V_{SS}	AL43	$V_{CC}P$
AB6	V_{SS}	AF42	V_{SS}	AL45	V_{SS}
AB8	V_{SS}	AF44	V_{SS}	AL47	$V_{CC}P$

Table 28. Pin Listing in Pin # Order (Continued)

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
AN1	V_{SS}	AU3	V_{SS}	BA5	V_{SS}
AN3	$V_{CC}P$	AU5	$V_{CC}S$	BA7	$V_{CC}S$
AN5	V_{SS}	AU7	V_{SS}	BA9	V_{SS}
AN7	$V_{CC}P$	AU9	$V_{CC}S$	BA11	RESERVED
AN9	V_{SS}	AU39	$V_{CC}S$	BA13	TESTLO
AN39	V_{SS}	AU41	V_{SS}	BA15	TESTLO
AN41	$V_{CC}P$	AU43	$V_{CC}S$	BA17	$V_{CC}P$
AN43	V_{SS}	AU45	V_{SS}	BA19	V_{SS}
AN45	$V_{CC}P$	AU47	$V_{CC}S$	BA21	$V_{CC}P$
AN47	V_{SS}	AW1	V_{SS}	BA23	V_{SS}
AQ1	$V_{CC}P$	AW3	$V_{CC}S$	BA25	$V_{CC}P$
AQ3	V_{SS}	AW5	V_{SS}	BA27	V_{SS}
AQ5	$V_{CC}P$	AW7	$V_{CC}S$	BA29	$V_{CC}P$
AQ7	V_{SS}	AW9	V_{SS}	BA31	V_{SS}
AQ9	$V_{CC}P$	AW39	V_{SS}	BA33	TESTLO
AQ39	$V_{CC}P$	AW41	$V_{CC}S$	BA35	RESERVED
AQ41	V_{SS}	AW43	V_{SS}	BA37	TESTLO
AQ43	$V_{CC}P$	AW45	$V_{CC}S$	BA39	V_{SS}
AQ45	V_{SS}	AW47	V_{SS}	BA41	$V_{CC}S$
AQ47	$V_{CC}P$	AY1	$V_{CC}S$	BA43	V_{SS}
AS1	VID0	AY3	$V_{CC}S$	BA45	$V_{CC}S$
AS3	VID1	AY5	$V_{CC}S$	BA47	V_{SS}
AS5	VID2	AY7	$V_{CC}S$	BC1	V_{SS}
AS7	VID3	AY9	$V_{CC}S$	BC3	V_{SS}
AS9	RESERVED	AY39	$V_{CC}S$	BC5	V_{SS}
AS39	TESTLO	AY41	$V_{CC}S$	BC7	V_{SS}
AS41	TESTLO	AY43	$V_{CC}S$	BC9	V_{SS}
AS43	TESTLO	AY45	$V_{CC}S$	BC11	RESERVED
AS45	TESTLO	AY47	$V_{CC}S$	BC13	TESTLO
AS47	RESERVED	BA1	V_{SS}	BC15	TESTLO
AU1	$V_{CC}S$	BA3	$V_{CC}S$	BC17	V_{SS}

Table 28. Pin Listing in Pin # Order (Continued)

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
BC19	$V_{CC}S$	BC29	V_{SS}	BC39	V_{SS}
BC21	V_{SS}	BC31	$V_{CC}S$	BC41	V_{SS}
BC23	$V_{CC}S$	BC33	TESTLO	BC43	V_{SS}
BC25	V_{SS}	BC35	RESERVED	BC45	V_{SS}
BC27	$V_{CC}S$	BC37	TESTLO	BC47	V_{SS}

Table 29. Pin Listing in Alphabetic Order

Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #
A3#	S5	A33#	E7	D10#	A39
A4#	S3	A34#	E9	D11#	A41
A5#	Q5	A35#	C1	D12#	C35
A6#	S1	ADS#	AE3	D13#	A43
A7#	Q3	AERR#	AE9	D14#	A37
A8#	Q7	AP0#	U1	D15#	C37
A9#	Q1	AP1#	S9	D16#	A45
A10#	Q9	BCLK	A19	D17#	C39
A11#	N5	BERR#	C5	D18#	C43
A12#	N1	BINIT#	AC43	D19#	C45
A13#	N7	BNR#	U7	D20#	C41
A14#	N3	BP2#	AE43	D21#	C47
A15#	L5	BP3#	AC39	D22#	E39
A16#	L3	BPM0#	AC41	D23#	E41
A17#	N9	BPM1#	AA39	D24#	E45
A18#	L7	BPRI#	U5	D25#	E43
A19#	J1	BR0#	AC5	D26#	E47
A20#	J5	BR1#	W3	D27#	G39
A20M#	A11	BR2#	AA1	D28#	G45
A21#	J3	BR3#	U9	D29#	G41
A22#	G1	CPUPRES#	B2	D30#	G43
A23#	J7	D0#	C25	D31#	G47
A24#	G3	D1#	A27	D32#	J39
A25#	L9	D2#	C27	D33#	J45
A26#	G7	D3#	A29	D34#	J47
A27#	G5	D4#	C29	D35#	J41
A28#	J9	D5#	A31	D36#	L45
A29#	E1	D6#	C31	D37#	L39
A30#	E3	D7#	C33	D38#	J43
A31#	G9	D8#	A33	D39#	L47
A32#	E5	D9#	A35	D40#	L41

Table 29. Pin Listing in Alphabetic Order (Continued)

Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #
D41#	N47	DEP6#	Y45	RESERVED	AE45
D42#	N45	DEP7#	U39	RESERVED	AG5
D43#	L43	DRDY#	AA3	RESERVED	AG9
D44#	N39	FERR#	C17	RESERVED	AG39
D45#	N41	FLUSH#	A15	RESERVED	AG47
D46#	Q47	FRCERR	C9	RESERVED	AS9
D47#	N43	HIT#	AC3	RESERVED	AS47
D48#	Q45	HITM#	AA7	RESERVED	BA11
D49#	Q43	IERR#	C3	RESERVED	BA35
D50#	S47	IGNNE#	A9	RESERVED	BC11
D51#	Q39	INIT#	C11	RESERVED	BC35
D52#	Q41	LINT0/INTR	AG43	RESET#	Y41
D53#	S45	LINT1/NMI	AG41	RP#	AC7
D54#	S43	LOCK#	AA9	RS0#	AC9
D55#	U47	PICCLK	AA43	RS1#	AE5
D56#	U45	PICD0	AA41	RS2#	AE7
D57#	S41	PICD1	AE41	RSP#	U3
D58#	W47	PLL1	C19	SMI#	W1
D59#	S39	PLL2	C23	STPCLK#	A3
D60#	U43	PRDY#	Y39	TCK	A5
D61#	W45	PREQ#	AA45	TDI	A13
D62#	Y47	PWRGOOD	AG7	TDO	C13
D63#	W43	REQ0#	W9	TESTHI	A23
DBSY#	AA5	REQ1#	W7	TESTHI	A25
DEFER#	Y5	REQ2#	Y3	TESTHI	AE39
DEP0#	AC45	REQ3#	Y1	TESTLO	C21
DEP1#	Y43	REQ4#	W5	TESTLO	AS39
DEP2#	W39	RESERVED	A21	TESTLO	AS41
DEP3#	AC47	RESERVED	L1	TESTLO	AS43
DEP4#	W41	RESERVED	AC1	TESTLO	AS45
DEP5#	AA47	RESERVED	AE1	TESTLO	BA13

Table 29. Pin Listing in Alphabetic Order (Continued)

Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #
TESTLO	BA15	$V_{CC}P$	T44	$V_{CC}S$	AU9
TESTLO	BA33	$V_{CC}P$	X6	$V_{CC}S$	AU39
TESTLO	BA37	$V_{CC}P$	X42	$V_{CC}S$	AU43
TESTLO	BC13	$V_{CC}P$	AB4	$V_{CC}S$	AU47
TESTLO	BC15	$V_{CC}P$	AB44	$V_{CC}S$	AW3
TESTLO	BC33	$V_{CC}P$	AJ3	$V_{CC}S$	AW7
TESTLO	BC37	$V_{CC}P$	AJ7	$V_{CC}S$	AW41
THERMTRIP#	A17	$V_{CC}P$	AJ41	$V_{CC}S$	AW45
TMS	C15	$V_{CC}P$	AJ45	$V_{CC}S$	AY1
TRDY#	Y9	$V_{CC}P$	AL1	$V_{CC}S$	AY3
TRST#	A7	$V_{CC}P$	AL5	$V_{CC}S$	AY5
UP#	AG3	$V_{CC}P$	AL9	$V_{CC}S$	AY7
$V_{CC}5$	AG1	$V_{CC}P$	AL39	$V_{CC}S$	AY9
$V_{CC}P$	B4	$V_{CC}P$	AL43	$V_{CC}S$	AY39
$V_{CC}P$	B8	$V_{CC}P$	AL47	$V_{CC}S$	AY41
$V_{CC}P$	B16	$V_{CC}P$	AN3	$V_{CC}S$	AY43
$V_{CC}P$	B24	$V_{CC}P$	AN7	$V_{CC}S$	AY45
$V_{CC}P$	B32	$V_{CC}P$	AN41	$V_{CC}S$	AY47
$V_{CC}P$	B40	$V_{CC}P$	AN45	$V_{CC}S$	BA3
$V_{CC}P$	B44	$V_{CC}P$	AQ1	$V_{CC}S$	BA7
$V_{CC}P$	F2	$V_{CC}P$	AQ5	$V_{CC}S$	BA41
$V_{CC}P$	F6	$V_{CC}P$	AQ9	$V_{CC}S$	BA45
$V_{CC}P$	F42	$V_{CC}P$	AQ39	$V_{CC}S$	BC19
$V_{CC}P$	F46	$V_{CC}P$	AQ43	$V_{CC}S$	BC23
$V_{CC}P$	K4	$V_{CC}P$	AQ47	$V_{CC}S$	BC27
$V_{CC}P$	K44	$V_{CC}P$	BA17	$V_{CC}S$	BC31
$V_{CC}P$	P2	$V_{CC}P$	BA21	VID0	AS1
$V_{CC}P$	P6	$V_{CC}P$	BA25	VID1	AS3
$V_{CC}P$	P42	$V_{CC}P$	BA29	VID2	AS5
$V_{CC}P$	P46	$V_{CC}S$	AU1	VID3	AS7
$V_{CC}P$	T4	$V_{CC}S$	AU5	$V_{REF}0$	A1

Table 29. Pin Listing in Alphabetic Order (Continued)

Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #
$V_{REF}1$	C7	V_{SS}	T40	V_{SS}	AL41
$V_{REF}2$	S7	V_{SS}	T42	V_{SS}	AL45
$V_{REF}3$	Y7	V_{SS}	T46	V_{SS}	AN1
$V_{REF}4$	A47	V_{SS}	X2	V_{SS}	AN5
$V_{REF}5$	AE47	V_{SS}	X4	V_{SS}	AN9
$V_{REF}6$	U41	V_{SS}	X8	V_{SS}	AN39
$V_{REF}7$	AG45	V_{SS}	X40	V_{SS}	AN43
V_{SS}	B6	V_{SS}	X44	V_{SS}	AN47
V_{SS}	B12	V_{SS}	X46	V_{SS}	AQ3
V_{SS}	B20	V_{SS}	AB2	V_{SS}	AQ7
V_{SS}	B28	V_{SS}	AB6	V_{SS}	AQ41
V_{SS}	B36	V_{SS}	AB8	V_{SS}	AQ45
V_{SS}	B42	V_{SS}	AB40	V_{SS}	AU3
V_{SS}	B46	V_{SS}	AB42	V_{SS}	AU7
V_{SS}	F4	V_{SS}	AB46	V_{SS}	AU41
V_{SS}	F8	V_{SS}	AF2	V_{SS}	AU45
V_{SS}	F40	V_{SS}	AF4	V_{SS}	AW1
V_{SS}	F44	V_{SS}	AF6	V_{SS}	AW5
V_{SS}	K2	V_{SS}	AF8	V_{SS}	AW9
V_{SS}	K6	V_{SS}	AF40	V_{SS}	AW39
V_{SS}	K8	V_{SS}	AF42	V_{SS}	AW43
V_{SS}	K40	V_{SS}	AF44	V_{SS}	AW47
V_{SS}	K42	V_{SS}	AF46	V_{SS}	BA1
V_{SS}	K46	V_{SS}	AJ1	V_{SS}	BA5
V_{SS}	P4	V_{SS}	AJ5	V_{SS}	BA9
V_{SS}	P8	V_{SS}	AJ9	V_{SS}	BA19
V_{SS}	P40	V_{SS}	AJ39	V_{SS}	BA23
V_{SS}	P44	V_{SS}	AJ43	V_{SS}	BA27
V_{SS}	T2	V_{SS}	AJ47	V_{SS}	BA31
V_{SS}	T6	V_{SS}	AL3	V_{SS}	BA39
V_{SS}	T8	V_{SS}	AL7	V_{SS}	BA43

Table 29. Pin Listing in Alphabetic Order (Continued)

Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #
V_{SS}	BA47	V_{SS}	BC9	V_{SS}	BC39
V_{SS}	BC1	V_{SS}	BC17	V_{SS}	BC41
V_{SS}	BC3	V_{SS}	BC21	V_{SS}	BC43
V_{SS}	BC5	V_{SS}	BC25	V_{SS}	BC45
V_{SS}	BC7	V_{SS}	BC29	V_{SS}	BC47

8.0. OVERDRIVE® PROCESSOR SOCKET SPECIFICATION

8.1. Introduction

Intel will offer future OverDrive processors for the Pentium Pro processor. This OverDrive processor will be based on a faster, future Intel processor core.

The future OverDrive processor for Pentium Pro processor-based systems is a processor upgrade that will make all software run faster on an existing Pentium Pro processor system. The OverDrive processor is binary compatible with the Pentium Pro processor. The OverDrive processor is intended for use as a replacement upgrade for single and dual processor Pentium Pro processor designs. The OverDrive processor will be equipped with an integral fan/heatsink and retention clips. Intel plans to ship OverDrive processors with a matched Voltage Regulator Module (OverDrive VRM).

To support processor upgrades, a Zero Insertion Force (ZIF) socket (Socket 8) and a Voltage Regulator Module connector (Header 8) have been defined along with the Pentium Pro processor. Header 8 can be populated with an OEM Pentium Pro processor VRM or with the OverDrive VRM which Intel plans to ship with the OverDrive processor as part of the retail package.

The OverDrive processor will also support Voltage Identification as described in Section 3.6. The four Voltage ID outputs (VID0-VID3) can be used to design a programmable power supply that will meet the power requirements of both the Pentium Pro and OverDrive processors via the Header 8 described in this section, or on the motherboard. If you plan to use VID to design a programmable supply for the OverDrive processor, please contact Intel for additional information.

A single socket system should include Socket 8 and Header 8. When this system configuration is upgraded, the Pentium Pro processor and its VRM are replaced with a future OverDrive processor for Pentium Pro processor-based systems and its matching OverDrive VRM. The OverDrive VRM is capable of delivering the lower voltage and higher current required by the upgrade. Other voltage regulation configurations are described in Section 8.3.2.

8.1.1. TERMINOLOGY

Header 8: 40-pin Voltage Regulator Module (VRM) connector defined to contain the OEM VRM and OverDrive VRM.

OverDrive® Processor: A future OverDrive processor for Pentium Pro processor-based systems.

OverDrive® VRM: A VRM designed to provide the specific voltage required by the future OverDrive processor for Pentium Pro processor-based systems.

Socket 8: 387-pin SPGA Zero Insertion Force (ZIF) socket defined to contain either a Pentium Pro or OverDrive processor.

8.2. Mechanical Specifications

This section specifies the mechanical features of Socket 8 and Header 8. This section includes the pinout, surrounding space requirements, and standardized clip attachment features.

Figure 45 shows a mechanical representation of the OverDrive processor in Socket 8 and the OverDrive VRM in Header 8.

8.2.1. VENDOR CONTACTS FOR SOCKET 8 AND HEADER 8

Contact your local Intel representative for a list of participating Socket 8 and Header 8 suppliers.

8.2.2. SOCKET 8 DEFINITION

Socket 8 is a 387-pin, modified staggered pin grid array (SPGA), Zero Insertion Force (ZIF) socket. The pinout is identical to the Pentium Pro processor. Two pins are used to support the on-package fan/heatsink included on the OverDrive processor and indicate the presence of the OverDrive processor. The OverDrive processor package is oriented in Socket 8 by the asymmetric use of interstitial pins. Standardized heat sink clip attachment tabs are also defined as part of Socket 8 (Section 8.2.2.3.).

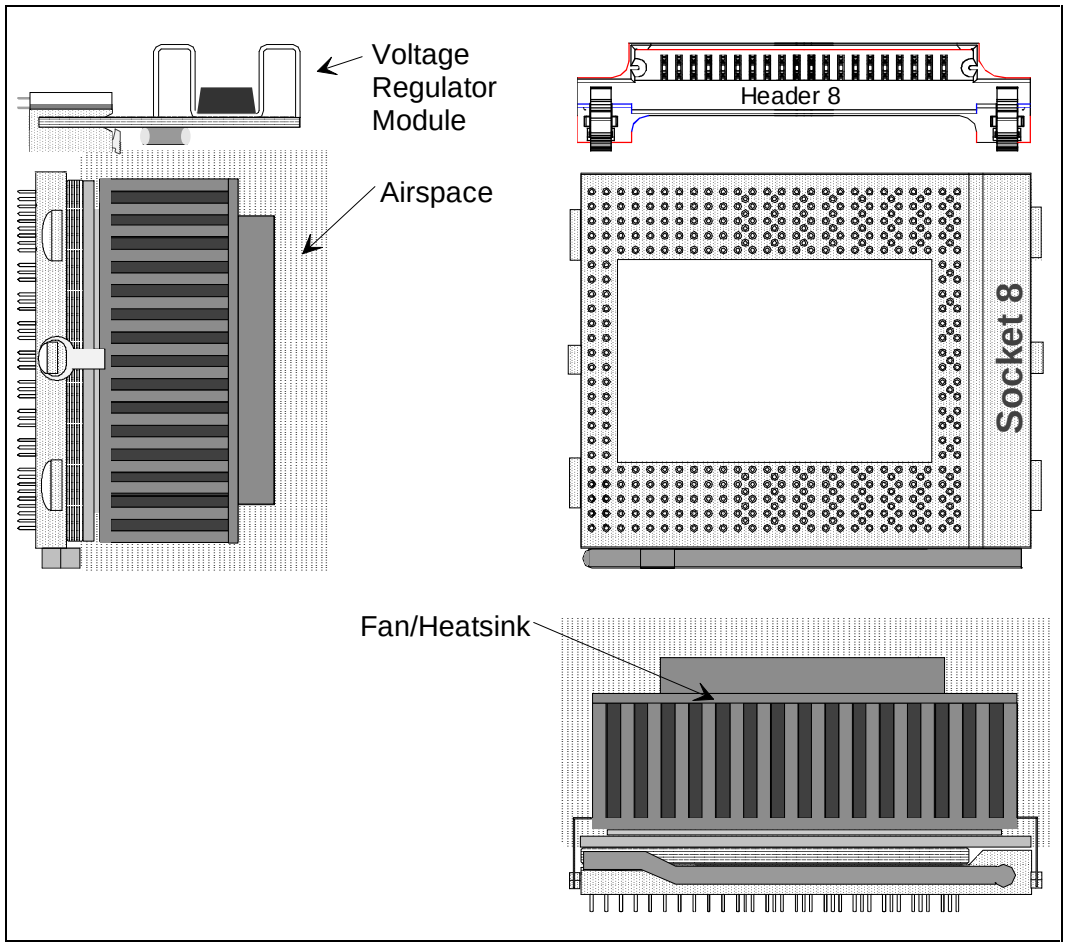


Figure 45. Socket 8 Shown with the Fan/heatsink Cooling Solution, Clip Attachment Features and Adjacent Voltage Regulator Module

8.2.2.1. Socket 8 Pinout

Socket 8 is shown in Figure 46 along with the VRM (Header 8) connector. Refer to Section 7.2, for pin listings of the Pentium Pro processor. The OverDrive processor pinout is identical to the Pentium Pro processor pinout.

Descriptions of the upgrade specific pins are presented in Table 30. Note the location of pin A1 in relation to the cam shelf position. If the socket has the cam shelf located in a different position, then correct insertion of the OverDrive processor may not be possible. See Section 8.2.2.2. for space requirements.

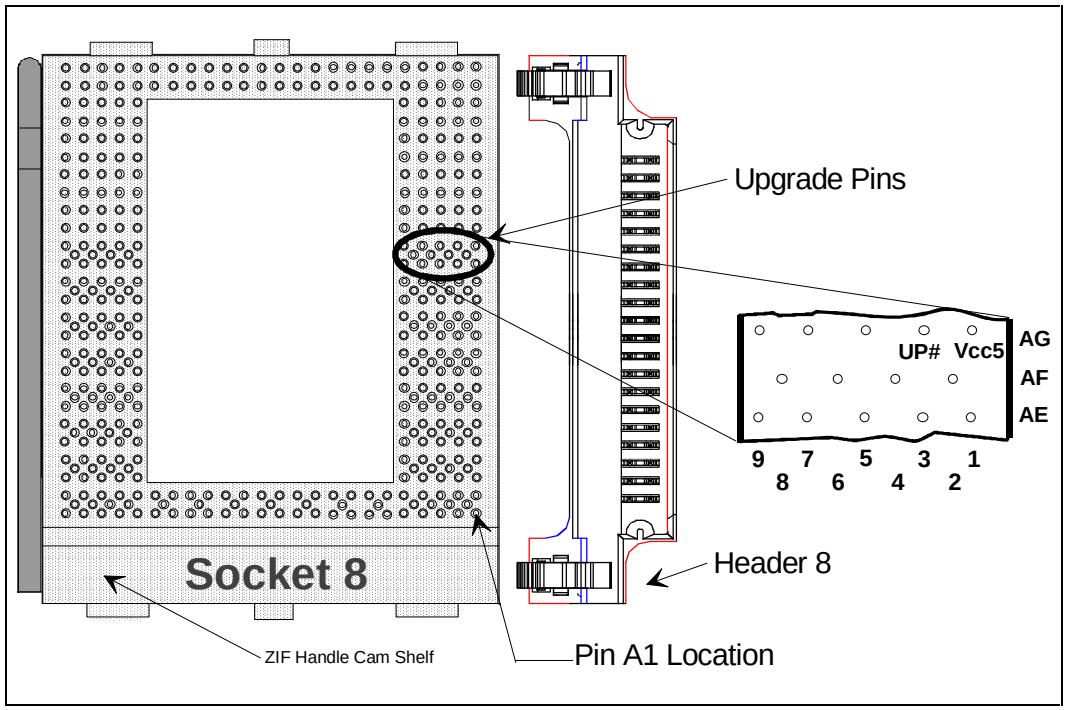


Figure 46. OverDrive® Processor Pinout

Table 30. OverDrive® Processor Signal Descriptions

Pin Name	Pin #	I/O	Function
$V_{CC}5$	AG1	Input	+5 **V** Supply required for OverDrive processor fan/heatsink.
UP#	AG3	Output	This output is tied to V_{SS} in the OverDrive processor to indicate the presence of an upgrade processor. This output is an open in the Pentium® Pro processor.

NOTE:

- Refer to Section 8.3. for a functional description of the above signals.

8.2.2.2. Socket 8 Space Requirements

The OverDrive processor will be equipped with a fan/heatsink thermal management device. The package envelope dimensions for the OverDrive processor with attached fan/heatsink are shown in Figure 47. Clearance is required around the fan/heatsink to ensure unimpeded air flow for proper cooling (refer to Section 8.5.1.1. for details). Figure 48 shows the Socket 8 space requirements for the OverDrive processor. All dimensions are in inches.

"Keep out zones," also shown in Figure 48, have been established around the heat sink clip attachment tabs to prevent damage to surface mounted components during clip installation and removal. The keep out zones extend upwards from the surface of the motherboard to the top of the heat sink. The lateral limits of the keep out zones extend 0.1 inch from the perimeter of each tab.

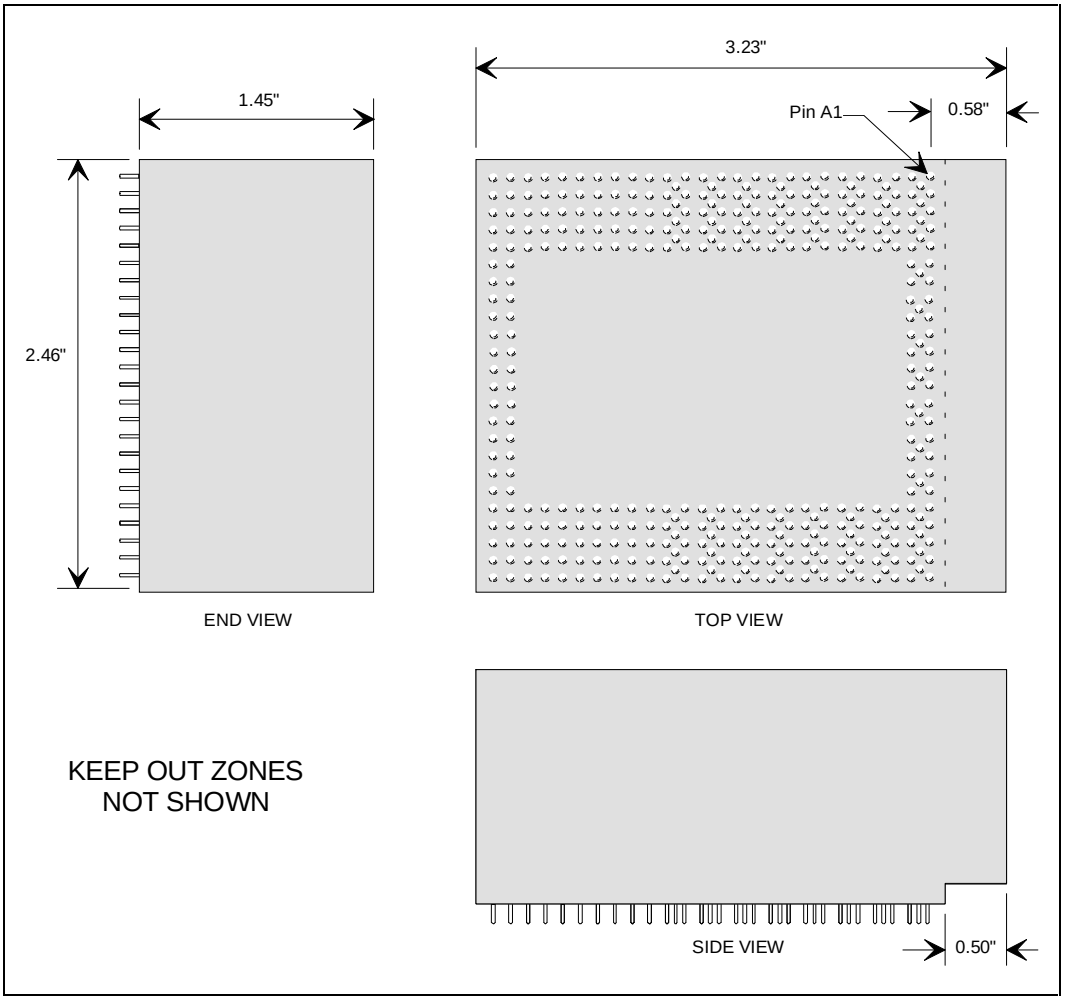


Figure 47. OverDrive® Processor Envelope Dimensions

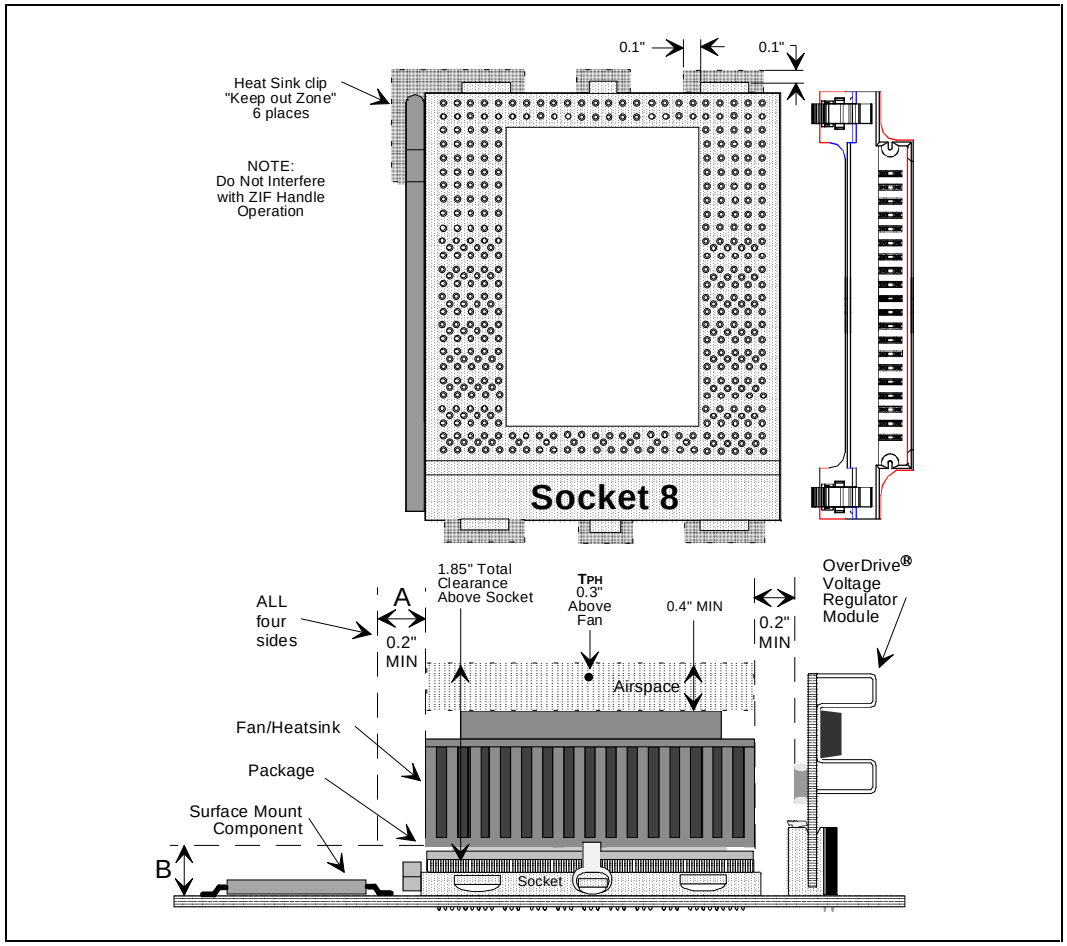


Figure 48. Space Requirements for the OverDrive® Processor

Immovable objects must not be located less than 1.85 inches above the seating plane of the ZIF socket. Removable objects must also not be located less than the 1.85 inches above the seating plane of the ZIF socket required for the processor and fan/heatsink. These requirements also apply to the area above the cam shelf.

As shown in Figure 48 it is acceptable to allow any device (i.e. add-in cards, surface mount device, chassis etc.) to enter within the free space distance of 0.2" from the chip package if it is not taller than the level of the heat sink base. In other words, if a component is taller than height 'B', it cannot be closer to the chip package than distance 'A'. This applies to all four sides of the chip package (the handle side of the ZIF socket will generally meet this specification since its width is typically larger than distance 'A' (0.2").

For designs which use Header 8, the header itself can violate the 0.2” airspace around the OverDrive processor package. A VRM (either Pentium Pro processor VRM or OverDrive VRM), once installed in Header 8, and any components on the module, MUST NOT violate the 0.2” airspace. Also, the

header must not interfere with the installation of the Pentium Pro or OverDrive processors, and must not interfere with the operation of the ZIF socket lever. Alternately, Socket 8, and the installed processor must not interfere with the installation and removal of a VRM in Header 8.

NOTE

Components placed close to Socket 8 must not impede access to and operation of the handle of the ZIF socket lever. Adequate clearance must be provided within the proximity of the ZIF socket lever to provide fingertip access to the lever for normal operation, and to allow raising the lever to the full open position.

8.2.2.3. Socket 8 Clip Attachment Tabs

Standardized clip attachment tabs will be provided on Socket 8. These will allow clips to secure the OverDrive processor to the socket to enhance shock and vibration protection. OEMs may utilize the attachment tabs for their own thermal solutions. As an option, OEMs may use customized attachment features providing that the additional features do not interfere with the standard tabs used by the upgrade.

Details of the clip attachment tabs and overall dimensions of Intel qualified sockets may be obtained from participating socket suppliers.

8.2.3. OVERDRIVE® VOLTAGE REGULATOR MODULE DEFINITION

Header 8 is a 2-row, 40-pin shrouded header designed to accommodate a Pentium Pro processor VRM, OverDrive VRM, or a programmable VRM. The OverDrive VRM is used to convert the standard 5.0 V supply to the OverDrive processor core operating voltage. Integral OverDrive VRM hold down tabs are included as part of the header definition for enhanced shock and vibration protection.

OEMs who plan to design a custom VRM PC Board to fit into Header 8 should refer to the AP-523, *Pentium® Pro Processor Power Distribution Guidelines* Application Note (Order Number 242764).

8.2.3.1. OVERDRIVE® VRM Requirement

When upgrading with an OverDrive processor, Intel suggests the use of its matched Voltage Regulator Module, which Intel plans to ship with the OverDrive processor retail package.

If the OEM includes on-board voltage regulation and the Header 8 for the OverDrive VRM, the on-board voltage regulator must be shut off via the UP# output of the CPU. When the OverDrive processor is installed, and the UP# signal is driven LOW, the on-board VR must never power on. This will ensure that there is no contention between the OverDrive VRM and the on-board regulator.

8.2.3.2. OverDrive® VRM Location

It is recommended that Header 8 be located within approximately 1 inch of Socket 8 to facilitate end user installation. For optimum electrical performance, the Header 8 should be as close as possible to Socket 8. The location must not interfere with the operation of the ZIF socket handle or heatsink attachment clips. To allow system design flexibility, Header 8 placement is optional, but it is recommended that Header 8 NOT be placed on the same side of the ZIF socket as the handle.

8.2.3.3. OverDrive ® VRM Pinout

The OverDrive VRM pinout and pin description is presented in Figure 49 and Table 31, respectively.

8.2.3.4. OverDrive ® VRM Space Requirements

Figure 50 describes the maximum OverDrive VRM envelope. No part of the OverDrive VRM will extend beyond the defined space.

Pin #	Signal Name	Pin #	Signal Name
A1	5Vin	B1	5Vin
A2	5Vin	B2	5Vin
A3	5Vin	B3	5Vin
A4	12Vin	B4	12Vin
A5	Reserved	B5	Reserved
A6	Reserved	B6	OUTEN
A7	VID0	B7	VID1
A8	VID2	B8	VID3
A9	UP#	B9	PwrGood
A10	Vcc_P	B10	Vss
A11	Vss	B11	Vcc_P
A12	Vcc_P	B12	Vss
A13	Vss	B13	Vcc_P
A14	Vcc_P	B14	Vss
A15	Vss	B15	Vcc_P
A16	Vcc_P	B16	Vss
A17	Vss	B17	Vcc_P
A18	Vcc_P	B18	Vss
A19	Vss	B19	Vcc_P
A20	Vcc_P	B20	Vss

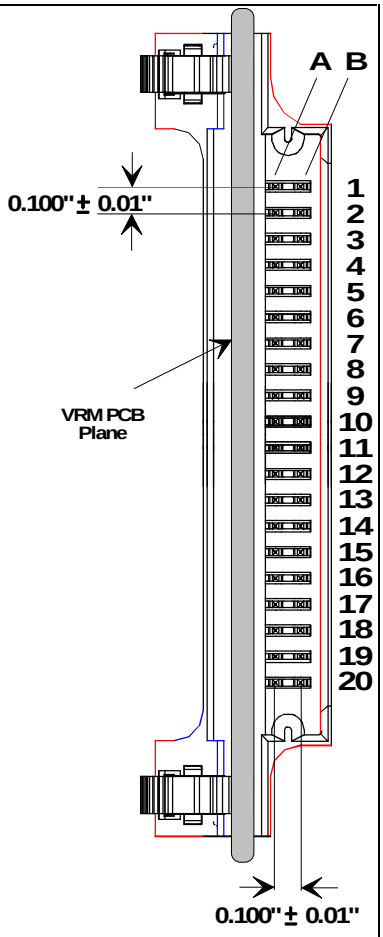


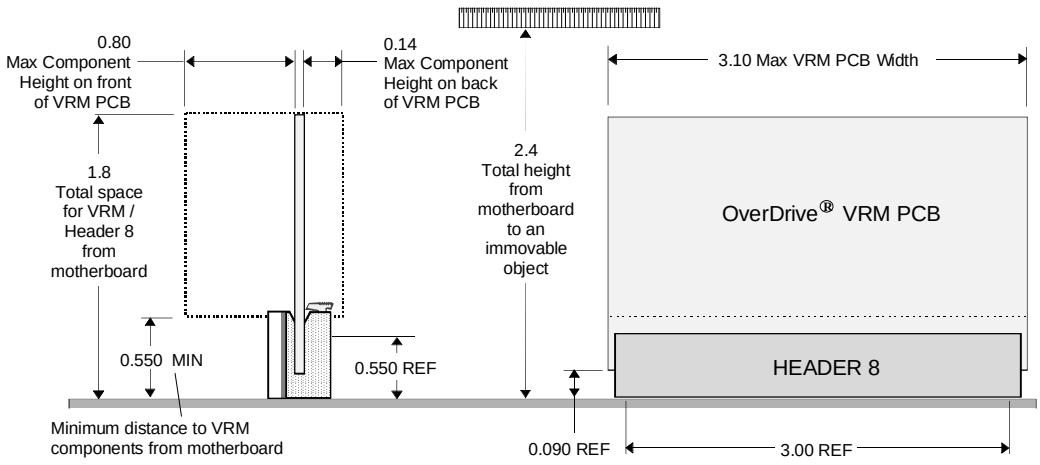
Figure 49. Header 8 Pinout

Table 31. Header 8 Pin Reference

Pin Name	I/O	Usage	Function
12 V_{IN}	Input	Required	+12V±5% Supply
5 V_{IN}	Input	Required	+5V±5% Supply [1]
V_{SS}	Input	Required	Ground Reference
OUTEN	Input	Optional	When driven high this input will enable the OEM VRM output and float the OverDrive® VRM output. When this input is driven low, the output of the OEM module will float and the OverDrive VRM output will be enabled.
PWRGOOD	Output	Optional	Power Good is driven high upon the VRM output reaching valid levels. This output requires an external pull-up resistor (~10KΩ).
RES		No connect	Reserved for future use.
UP#	Input	Required	This signal is held high via an external pull-up resistor on the open collector output of the Pentium® Pro processor, and is driven low by the grounded output of the OverDrive processor.
$V_{CC}P$	Output	Required	Voltage Regulator Module core voltage output. Voltage level for the OverDrive processor will be lower than for the Pentium Pro processor.
VID3-VID0	Inputs	Optional	Used by the Pentium Pro processor VRM to determine what output voltage to provide to the CPU. The OverDrive VRM does not require these pins to be connected as it will be voltage matched in advance to the OverDrive processor. Refer to Table 1 for Voltage ID pin decoding.

NOTE:

- The OverDrive® Voltage Regulator Module requires both 5 **V** and 12 V. Routing for the 5 V VRM supply must support the full requirements of the OverDrive VRM given in Table 34 even if the 12 V supply is utilized for the OEM VRM.



NOTE: The connector comprises a header mounted on the motherboard and a receptacle on the edge of the VRM PCB.

Figure 50. OverDrive® Voltage Regulator Module Envelope

8.3. Functional Operation of OverDrive® Processor Signals

8.3.1. FAN/HEATSINK POWER ($V_{CC}5$)

This 5 V supply provides power to the fan of the fan/heatsink assembly. See Table 33 for $V_{CC}5$ specifications.

8.3.2. UPGRADE PRESENT SIGNAL (UP#)

The Upgrade Present signal is used to prevent operation of voltage regulators providing a potentially harmful voltage to the OverDrive processor, and to prevent contention between on-board regulation and the OverDrive VRM. UP# is an open collector output, held high using a pull-up resistor on the motherboard tied to +5 Volts.

There are several system voltage regulation design options to support both the Pentium Pro processor and its OverDrive processor. The use of the UP# signal for each case is described below:

- Case 1: Header 8 only
  If the system is designed with voltage regulation from the Header 8 only, then the UP# signal must be connected between the CPU socket (Socket 8) and the VRM connector (Header 8). The Pentium Pro processor VRM should internally connect the UP# input directly to the VRM OUTEN input. If the Pentium Pro processor is replaced with an OverDrive processor and the OEM VRM is NOT replaced with the OverDrive VRM, the original voltage regulator will never enable its outputs because the lower voltage OverDrive processor could be damaged. Refer to Figure 51.

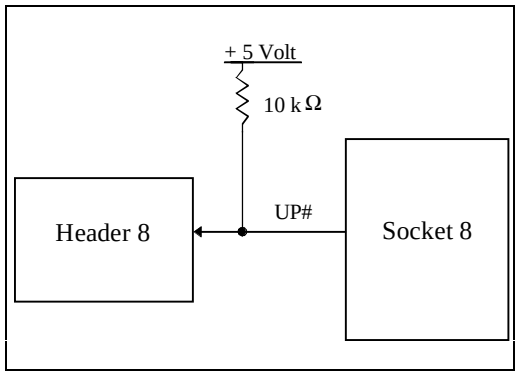


Figure 51. Upgrade Presence Detect Schematic—Case 1

- Case 2: *Header 8 AND alternate voltage source* If the system is designed with alternate voltage source and a Header 8 for future upgrade support, then the UP# signal must be connected between Socket 8, Header 8, and the alternate voltage source. The Pentium Pro Voltage Regulator should use the UP# signal to disable the voltage output when detected low (indicating that an OverDrive processor has been installed). The OverDrive VRM, when installed into the Header 8 will use the UP# signal to enable its outputs (when detected low). When the Pentium Pro processor is replaced with an OverDrive processor and the OverDrive VRM is installed, the original voltage regulator must never enable its outputs because the lower voltage OverDrive processor could be damaged. Refer to Figure 52.

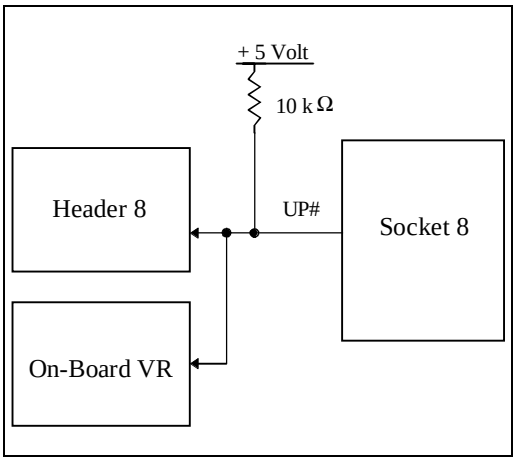


Figure 52. Upgrade Presence Detect Schematic—Case 2

- Case 3: Alternate voltage source only If the system is designed with only a programmable voltage source using the VID3-VID0 pins, then the UP# signal need not be used.

NOTE

The programmable voltage source needs to be able to provide the OverDrive processor with its required power. Refer to Figure 53.

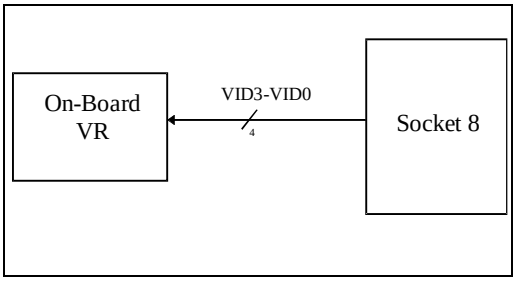


Figure 53. Upgrade Presence Detect Schematic—Case 3

8.3.3. BIOS CONSIDERATIONS

Please refer to the *Pentium® Pro Processor Developers Manual: Volume 3, Programmer's Reference Manual* (Order Number 242691) for BIOS requirements.

It is the responsibility of the BIOS to detect the type of CPU in the system and program the support hardware accordingly. In most cases, the BIOS does this by reading the CPU signature, comparing it to known signatures, and, upon finding a match, executing the corresponding hardware initialization code.

The CPUID instruction is used to determine several processor parameters. Following execution of the CPUID instruction, bits 12 and 13 of the EAX register can be used to determine if the processor is an OEM or an OverDrive processor. An OverDrive processor is present if bit 13=0 and bit 12=1.

NOTE

Contact your BIOS vendor to ensure that the above requirements have been included.

8.3.3.1. OverDrive® Processor CPUID

Following power-on RESET or the CPUID instruction, the EAX register contains the values shown in Table 32.

Table 32. OverDrive® Processor CPUID

Type [13:12]	Family [11:8]	Model [7:4]	Stepping [3:0]
1	6	3	X

8.3.3.2. Common Causes of Upgradability Problems Due to BIOS

CPU signature detection has been a common cause of current upgradability problems due to BIOS. A few precautions within the BIOS can help to eliminate future upgradability problems with Pentium Pro processor-based systems. When programming or modifying a BIOS, be aware of the impact of future OverDrive processors. The following recommendations should prevent problems in the future:

- Always use the CPU signature and feature flags to identify the processor, including future processors.
- Never use timing loops for delays.
- If an OverDrive processor is detected, report the presence of an "OverDrive processor" to the end-user.
- If an OverDrive processor is detected, don't test on-chip cache sizes or organization. The OverDrive processor cache parameters differ from those of the Pentium Pro processor.
- If an OverDrive processor is detected, don't use the Pentium Pro processor model specific registers and test registers. OverDrive processor MSRs differ from those of the Pentium Pro processor.
- MTRRs must be programmed as a Pentium Pro processor.

8.4. OverDrive® Processor Electrical Specifications

This section describes the electrical requirements for the OverDrive processor.

NOTE

ZIF socket electrical parameters may differ from LIF socket parameters; therefore, be sure to use the appropriate ZIF socket parameters for electrical design simulations.

8.4.1. DC SPECIFICATIONS

8.4.1.1. OverDrive® Processor DC Specifications

Table 33 lists the DC specifications for the OverDrive processor that are either different from or in addition to the Pentium Pro processor specifications.

8.4.1.2. OverDrive® VRM DC Specifications

The DC specifications for the OverDrive VRM are presented in Table 34.

Table 33. OverDrive® Processor DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$I_{CC}P$	Primary I_{CC} Current	0.100		11.2 12.5 13.9	A A A	1 2 3
$V_{CC}P$	Primary V_{CC} Voltage	2.375	2.5	2.625		$V_{CC}P$ = 2.5V±5% 4
$I_{CC}S$	Secondary I_{CC} Current			0	A	
VCCS	Secondary V_{CC} Voltage	3.145	3.3	3.465		$V_{CC}S$ = 3.3 V ±5%
$I_{CC}5_{FAN}$	Fan/heatsink Current			340	mA	
$V_{CC}5$	Fan/heatsink Voltage	4.75	5	5.25		$V_{CC}5$ = 5 V ± 5%
P_{MAX}	Maximum Thermal Design Power		21.4 23.8 26.3	26.7 29.7 32.9	W W W	1 2 3

NOTES:

1. This specification applies to the future OverDrive® processor for 150 MHz Pentium® Pro processor-based systems.
2. This specification applies to the future OverDrive processor for 166 and 180 MHz Pentium Pro processor-based systems.
3. This specification applies to the future OverDrive processor for 200 MHz Pentium Pro processor-based systems.
4. This is the TARGET OverDrive processor Voltage. It is recommended that the Voltage Identification be used to determine processor voltage for programmable voltage sources and implement a voltage range which adequately covers the OverDrive processor Target Voltage (~2.4-2.7V).

Table 34. OverDrive® VRM Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Control Signal Input Low Voltage	-0.3	0.8	V	
V_{IH}	Control Signal Input High Voltage	2.0	$V_{CC}5$+0.3	V	
V_{OL}	Control Signal Output Low Voltage		0.4V	V	
$V_{OH}5$	Control Signal Output High Voltage	2.4	$V_{CC}5$+0.3	V	PWRGOOD
$I_{CC}5$	5.0 V Power Supply Current (VRM input current)	0.100	7.0 7.8 8.7	A A A	1 2 3
$I_{CC}12$	12.0 V Power Supply Current (VRM input current)		150	mA	
I_{OUT}	VRM Output Current		11.2 12.5 13.9	A A A	1 2 3
L_{MB}	Total inductance between VRM output and processor pins		2.5	nH	
R_{MB}	Total resistance between VRM output and processor pins		2.1	mΩ	4
di_{CC}/dt	Worst Case Input ($I_{CC}5$) Load Change		100	mA/ µS	
T_{VOUT}	Valid Input Supply to Output Delay		10	ms	

NOTES:

1. This specification applies to the future OverDrive® VRM for 150 MHz Pentium® Pro processor-based systems.
2. This specification applies to the future OverDrive VRM for 166 and 180 MHz Pentium Pro processor-based systems.
3. This specification applies to the future OverDrive VRM for 200 MHz Pentium Pro processor-based systems.
4. Maximum total resistance from VRM output to CPU pins cannot exceed 2.1 mΩ. For example, a breakdown of the resistive path might be 0.45 mΩ for VRM header, 1.0 mΩ for motherboard power plane resistance, and 0.65 mΩ for ZIF socket.

8.4.2. OverDrive® PROCESSOR DECOUPLING REQUIREMENTS

No additional decoupling capacitance is required to support the OverDrive processor beyond what is necessary for the Pentium Pro processor. Any incremental decoupling, both bulk and high speed, required by the OverDrive processor will be provided on the processor package. It is strongly recommended that liberal, low inductance decoupling capacitance be placed near Socket 8 following the guidelines in Note 1 of Table 4 and the AP-523, *Pentium® Pro Processor Power Distribution Guidelines* Application Note (Order Number 242764). Capacitor values should be chosen to ensure they eliminate both low and high frequency noise components.

8.4.3. AC SPECIFICATIONS

Except for internal CPU core Clock frequency, the OverDrive processor will operate within the same AC specifications as the Pentium Pro processor.

8.5. Thermal Specifications

This section describes the cooling solution utilized by the OverDrive processor and the cooling requirements for both the processor and VRM. Heat dissipation by the OverDrive processor will be no greater than the Pentium Pro processor, as described in Section 6 and Table 5.

8.5.1. OverDrive ® PROCESSOR COOLING REQUIREMENTS

The OverDrive processor will be cooled with a fan/heatsink cooling solution. The OverDrive processor will operate properly when the preheat temperature, T_{PH}, is a maximum of 50°C (T_{PH} is the temperature of the air entering the fan/heatsink, measured 0.3" above the center of the fan — See Figure 48). When the preheat temperature requirement is met, the fan/heatsink will keep the case temperature, T_C, within the specified range, provided airflow through the fan/heatsink is unimpeded (see Space Requirements, Section 8.2.2.2.).

It is strongly recommended that testing be conducted to determine if the fan inlet temperature requirement is met at the system maximum ambient operating temperature.

NOTE

The OverDrive processor will operate properly when the preheat temperature, T_{PH}, is a maximum of 50°C (T_{PH} is the temperature of the air entering the fan/heatsink, measured 0.3" above the center of the fan — See Figure 48.)

8.5.1.1. Fan/Heatsink Cooling Solution

A height of 0.4" airspace above the fan/heatsink unit and a distance of 0.2" around all four sides of the OverDrive processor is REQUIRED to ensure that the airflow through the fan/heatsink is not blocked. The fan/heatsink will reside within the boundaries of the surface of the chip. Blocking the airflow to the fan/heatsink reduces the cooling efficiency and decreases fan life. Figure 48 illustrates an acceptable airspace clearance above the fan/heatsink and around the OverDrive processor package.

8.5.2. OEM PROCESSOR COOLING REQUIREMENTS

The OEM processor cooling solution must not impede the upgradability of the system. For example:

- If an OEM fan/heatsink is used, then electrical connections between the OEM fan/heatsink and system must be through an end user separable connector.
- If an OEM fan/heatsink is used, removal of the assembly must not interfere with the operation of the OverDrive processor, for example, by activating cooling failure protection mechanisms employed by the OEM.
- Custom attachment features in addition to the features covered in Section 8.2.2.3. must not interfere with attachment of the upgrade retention clips.

8.5.3. OverDrive ® VRM COOLING REQUIREMENTS

The OverDrive Voltage Regulator Module will be shipped with a passive heat sink. Voltage regulator case temperature must not exceed 105°C. The ambient temperature, T_A, required to properly cool the VRM can be estimated from the following section.

8.5.4. THERMAL EQUATIONS AND DATA

The OverDrive Voltage Regulator Module requires that T_C does not exceed 105°C. T_C is measured on the surface of the hottest component of the VRM. To calculate T_A values for the VRMs at different flow rates, the following equations and data may be used:

$$T_A = T_C - (P \times \Theta_{CA})$$

Where,

T_A and T_C =	Ambient and Case temperature, respectively. (°C)
Θ_{CA} =	Case-to-Ambient Thermal Resistance (°C/Watt)
P =	Maximum Power Consumption (Watt)

Table 35. OverDrive® VRM Power Dissipation for Thermal Design

Parameter	Typ [1]	Max [1]	Unit	Notes
OverDrive VRM Power Dissipation	6.0 6.5 7.0	7.0 7.8 8.7	W W W	2 3 4
T_C, Max		105	°C	Voltage Regulator Maximum Case Temperature

NOTES:

1. Specification for the OverDrive® Voltage Regulator Module. A Pentium® Pro processor OEM Module is specific to the design and may differ.
2. This specification applies to the future OverDrive® VRM for 150 MHz Pentium® Pro processor-based systems.
3. This specification applies to the future OverDrive VRM for 166 and 180 MHz Pentium Pro processor-based systems.
4. This specification applies to the future OverDrive VRM for 200 MHz Pentium Pro processor-based systems.

Table 36. Thermal Resistance and Maximum Ambient Temperature

	Airflow - Ft./Min (M/Sec) [1]				
	100 (0.50)	150 (0.75)	200 (1.01)	250 (1.26)	300 (1.52)
OverDrive® processor T_A, Max (°C)	Fan/Heatsink requires Ambient of 50°C or less regardless of external airflow.				
OverDrive VRM Θ_{CA} (°C/W)	9.8	8.3	6.8	6.4	6.0
OverDrive VRM T_A, Max (°C) [2,3]	46	55	64	67	69
OverDrive VRM T_A, Max (°C) [2,4]	41	51	61	63	66
OverDrive VRM T_A, Max (°C) [2,5]	36	47	57	60	63

NOTES:

1. Airflow direction parallel to long axis of VRM PCB.
2. T_{CASE} = 105°C, Power as per Table 35.
3. This specification applies to the future OverDrive® VRM for 150 MHz Pentium® Pro processor-based systems.
4. This specification applies to the future OverDrive VRM for 166 and 180 MHz Pentium Pro processor-based systems.
5. This specification applies to the future OverDrive VRM for 200 MHz Pentium Pro processor-based systems.

8.6. Criteria for OverDrive® Processor

This section provides PC system designers with information on the engineering criteria required to ensure that a system is upgradable. The diagrams and checklists will aid the OEM to check specific criteria. Several design tools are available through Intel field representatives which will help the OEM meet the criteria. Refer to Section 8.6.1 for a list of documents.

The criteria are divided into 5 different categories:

- Electrical Criteria
- Thermal Criteria
- Mechanical Criteria
- Functional Criteria
- End User Criteria

8.6.1. RELATED DOCUMENTS

All references to related documents within this section imply the latest published revision of the related document, unless specifically stated otherwise. Contact your local Intel Sales representative for latest revisions of the related documents.

Processor and Motherboard Documentation:

- *Pentium® Pro Processor Developer's Manual: Programmer's Reference Manual* (Order Number 242691)

8.6.2. ELECTRICAL CRITERIA

The criteria in this section concentrates on the CPU and VRM, and covers pin to plane continuity, signal connections, signal timing and quality, and voltage transients.

8.6.2.1. OverDrive® Processor Electrical Criteria

The electrical criteria for the OverDrive processor is split into three tables. Most of the criteria refer directly to previous sections of this document.

The criteria for the OverDrive processor that only apply to motherboards and systems which employ a Header 8 are presented in Table 37. See Table 39 for criteria that apply regardless of a Header 8.

The criteria for the OverDrive processor that apply to all motherboards and systems are presented in Table 39.

Table 37. Electrical Test Criteria for Systems Employing Header 8

Criteria	Refer To:	Comment
5 Vin Tolerance Header 8 Input	Table 30	Measured Under the following Loading Conditions: Max I_{CC5} at Steady-State Min I_{CC5} at Steady-State Fast Switch between Max and Min I_{CC5} Refer to Table 32 for OverDrive VRM $I_{CC}5$ specification.
Pentium® Pro Processor V_{CCP} Specification	Table 4	Measured Under the following Loading Conditions: Max $I_{CC}P$ at Steady-State Min $I_{CC}P$ at Steady-State Fast Switch between Max and Min $I_{CC}P$ Refer to Table 5 for Pentium Pro processor $I_{CC}P$ specification.
VRM RES pins	Table 31	Must not be connected.
VRM control signals (5Vin, VSS, PWRGOOD, UP#, V_{CCP}, and VID3-VID0)	Table 31	Must be connected as specified. OUTEN is optional.
VRM control input signal quality	Table 31	VRM control input signals must meet the DC specifications of the VRM.
Maximum Total LMB	Table 31	Inductance between VRM output and CPU socket pins.
Maximum Total RMB	Table 31	Resistance between VRM output and CPU socket pins.

Table 38. Electrical Test Criteria for Systems Not Employing Header 8

Criteria	Refer To:	Comment
$V_{CC}P$ Primary CPU V_{CC} Voltage	Table 33 including note 4	Measured Under the following Loading Conditions: Max $I_{CC}P$ at Steady-State Min $I_{CC}P$ at Steady-State Fast Switch between Max and Min $I_{CC}P$ Refer to Table 33 for OverDrive® processor $I_{CC}P$ specification.

Table 39. Electrical Test Criteria for all Systems

Criteria	Refer To:	Comment
V_{CCS} Secondary CPU V_{CC} Voltage	Table 33	Loading Conditions: • Max $I_{CC}S$ at Steady-State • Min $I_{CC}S$ at Steady-State • Fast Switch between Max and Min $I_{CC}S$ Refer to Table 33 for OverDrive® processor $I_{CC}S$ specification.
V_{CC5}	Table 33	Fan/Heatsink Voltage
V_{CC} continuity to Socket 8	Table 28	0.5W or less for any single pin from Socket 8 V_{CC} pins to V_{CC} supply. Applies to both primary and secondary pins and their respective supplies.
VSS continuity to Socket 8	Table 28	0.5W or less for any single pin From Socket 8 VSS pins to VSS supply.
RESERVED Pins	Table 28	Must not be connected.
Input signal quality	Section 5.2	Must meet specification of the Pentium® Pro processor.
AC timing specifications	Section 3.15	Must meet all AC specifications of the Pentium Pro processor.

8.6.2.2. Pentium® Pro Processor Electrical Criteria

Motherboards and systems will be tested to the specifications of the Pentium Pro processor in Section 3.

8.6.3. THERMAL CRITERIA

8.6.3.1. OverDrive® Processor Cooling Requirements (Systems Testing Only)

The maximum preheat temperature, T_{PH}, for the OverDrive processor must not be greater than specified in Section 8.5.1. T_{PH} is the temperature of the air entering the fan heatsink and is measured 0.3 inches (0.76 cm) above the center of the fan. Thermal testing should be performed at the OEM specified maximum system operating temperature (not less than 32°C), and under worst case thermal loading. Worst case thermal loading requires every I/O bus expansion slot to be filled with the longest typical add-in card that will not violate the required clearance for airflow around the OverDrive processor (refer to Section 8.2.2.2. for these requirements). These add-in cards represent typical power dissipation per type and form factor (Full length PCI, VL, ISA, and ½ length PCI dissipate 10W; ¾ length ISA dissipates 7.5W, ½ length ISA dissipates 5W, and ¼ length ISA dissipates 3.3W).

8.6.3.2. Pentium® Pro Processor Cooling Requirements (Systems Testing Only)

The Pentium Pro processor case temperature must meet the specifications of the Pentium Pro processor. Thermal testing should be performed under worst case thermal loading (Refer to 8.6.3.1. for loading description), and with a cooling solution representative of the OEM's cooling solution.

Refer to Table 5 for the Pentium Pro processor case temperature specification.

8.6.3.3. Voltage Regulator Modules (Systems Employing a Header 8 Only)

The case temperature of the voltage regulator on the OverDrive VRM must not exceed the specification of Table 40.

Table 40. Thermal Test Criteria

Criteria	Refer To:	Comment
T_{PH}	Section 8.5.1.	Air temperature entering the fan/heatsink of the OverDrive® processor. Measured 0.3 inches (0.76 cm) above the center of the fan/heatsink.
Pentium® Pro processor Case Temperature	Table 5	T_C must meet the specifications of the Pentium Pro Processor. Measured with a cooling solution representative of the OEM's.
Voltage Regulator Case Temperature	Table 35	

8.6.4. MECHANICAL CRITERIA

8.6.4.1. OverDrive® Processor Clearance and Airspace Requirements

Refer to Figure 48 for a drawing of the various clearance and airspace requirements

Table 41. Mechanical Test Criteria for the OverDrive® Processor

Criteria	Refer To:	Comment
Minimum airspace from top surface of socket to any object.	Figure 48	See "Total Clearance Above Socket" in Figure 40.
Minimum airspace around all 4 sides of the OverDrive® processor fan/heatsink.	Figure 48	Required from the CPU package side to the top of the vertical clearance area. See "A" in Figure 40.
Minimum airspace around heatsink clip tabs.	Figure 48	Extend from the motherboard surface to the top of the fan/heatsink. See "Keep Out Zones" in Figure 40.
ZIF socket lever operation.	Figure 48	Must operate from fully closed to fully open position with no interference.

8.6.4.2. OverDrive® VRM Clearance and Airspace Requirements

Refer to Figure 50 for a drawing of the various clearance and airspace requirements of the OverDrive VRM. Nothing must intrude into the space envelope, including airspace region, defined in Figure 50 with the exception of Header 8 itself.

8.6.5. FUNCTIONAL CRITERIA

The OverDrive processor is intended to replace the original Pentium Pro processor. The system must boot properly without error messages when the OverDrive processor is installed.

8.6.5.1. Software Compatibility

System hardware and software that operates properly with the original Pentium Pro processor must operate properly with the OverDrive processor.

Table 42. Functional Test Criteria

Criteria	Refer To:	Comment
Software Compatibility		No incompatibilities resulting from upgrade installation.
BIOS Functionality	Section 8.3.3.	• CPU Type Reported on Screen must be reported correctly or not at all. Intel recommends reporting "OverDrive Processor". • Never Use Timing Loops. • Do not test the cache, or use model specific registers when the upgrade is detected.

8.6.5.2. BIOS Functionality

The BIOS must continue to operate correctly with the OverDrive processor installed in the system. Always use the CPU Signature and Feature flags to identify if an OverDrive processor is installed. Please refer to the *Pentium® Pro Processor Developer's Manual: Volume 3, Programmer's Reference Manual:* (Order Number 242691) for the BIOS recommendations.

8.6.6. END USER CRITERIA

8.6.6.1. Qualified OverDrive® Processor Components

To ensure processor upgradability, a system should employ the following Intel-qualified OverDrive processor components. For a list of qualified components contact your Intel sales representative, or if in the US, contact Intel FaxBACK Information Service at (800) 525-3019.

- Genuine Intel OEM CPU
- Socket 8, 387-hole ZIF
- Header 8, 40-pin shrouded (Systems and Motherboards employing Header 8 solution only.) OR programmable voltage regulator capable of providing the voltage and current required by the OverDrive processor.

8.6.6.2. Visibility and Installation

Socket 8 and Header 8 must be visible upon removal of the system cover. Otherwise, the OEM must include diagrams or other indicators visible upon removal of the system cover or clear instructions in the user's manual to guide the end user to the CPU socket and the VRM header. Special tools, other than a screw driver, must not be required for an upgrade installation.

8.6.6.3. Jumper Configuration

End user configured jumpers are not recommended. If design requires jumpers or switches to upgrade the system, a detailed jumper description in the manual is required. The jumpers must be easy to locate and set. Jumper identification should be silk-screened on the motherboard if possible. Jumper tables on the inside of the system case are recommended.

8.6.6.4. BIOS Changes

BIOS changes or additional software must not be required to upgrade the system with the OverDrive processor.

8.6.6.5. Documentation

The system documentation must include installation instructions, with illustrations of the system, Socket 8 and Header 8 location, and any heatsink clip's operation and orientation instructions. Furthermore, there must be no documentation anywhere stating that the warranty is void if the OEM processor is removed.

8.6.6.6. Upgrade Removal

The upgrade process must be reversible such that upon re-installation of the original CPU, the system must retain original functionality and the cooling solution must return to its original effectiveness.

APPENDIX A

This appendix provides an alphabetical listing of all Pentium Pro processor signals. **Pins that do not appear here are not considered bus signals and are described in Table 2.**

A.1 A[35:3]# (I/O)

The A[35:3]# signals are the address signals. They are driven during the two-clock Request Phase by the request initiator. The signals in the two clocks are referenced Aa[35:3]# and Ab[35:3]#. During both clocks, A[35:24]# signals are protected with the AP1# parity signal, and A[23:3]# signals are protected with the AP0# parity signal.

The Aa[35:3]# signals are interpreted based on information carried during the first Request Phase clock on the REQa[4:0]# signals.

For memory transactions as defined by REQa[4:0]# = {XX01X,XX10X,XX11X}, the Aa[35:3]# signals define a 2^{36}-byte physical memory address space. The cacheable agents in the system observe the Aa[35:3]# signals and begin an internal snoop. The memory agents in the system observe the Aa[35:3]# signals and begin address decode to determine if they are responsible for the transaction completion. Aa[4:3]# signals define the critical word, the first data chunk to be transferred on the data bus. Cache line transactions use the standard burst order described in *Pentium® Pro Processor Developer's Manual, Volume 1: Specifications (Order* Number 242690) to transfer the remaining three data chunks.

For Pentium Pro processor IO transactions as defined by REQa[4:0]# = 1000X, the signals Aa[16:3]# define a 64K+3 byte physical IO space. The IO agents in the system observe the signals and begin address decode to determine if they are responsible for the transaction completion. Aa[35:17]# are always zero. Aa16# is zero unless the IO space being accessed is the first three bytes of a 64KByte address range.

For deferred reply transactions as defined by REQa[4:0]# = 00000, Aa[23:16]# carry the deferred ID. This signal is the same deferred ID supplied by the request initiator of the original transaction on Ab[23:16]#/DID[7:0]# signals. Pentium Pro processor bus agents that support deferred replies sample the deferred ID and perform an internal match against any outstanding transactions waiting for deferred replies. During a deferred reply, Aa[35:24]# and Aa[15:3]# are reserved.

For the branch-trace message transaction as defined by REQa[4:0]# = 01001 and for special and interrupt acknowledge transactions, as defined by REQa[4:0]# = 01000, the Aa[35:3]# signals are reserved and undefined.

During the second clock of the Request Phase, Ab[35:3]# signals perform identical signal functions for all transactions. For ease of description, these functions are described using new signal names. Ab[31:24]# are renamed the attribute signals ATTR[7:0]#. Ab[23:16]# are renamed the Deferred ID signals DID[7:0]#. Ab[15:8]# are renamed the eight-byte enable signals BE[7:0]#. Ab[7:3]# are renamed the extended function signals EXF[4:0]#.

Table 43. Request Phase Decode

Ab[31:24]#	Ab[23:16]#	Ab[15:8]#	Ab[7:3]#
ATTR[7:0]#	DID[7:0]#	BE[7:0]#	EXF[4:0]#

On the active-to-inactive transition of RESET#, each Pentium Pro processor bus agent samples A[35:3]# signals to determine its power-on configuration.

A.2 A20M# (I)

The A20M# signal is the address-20 mask signal in the PC Compatibility group. If the A20M# input signal is asserted, the Pentium Pro processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap around at the one Mbyte boundary. Only assert A20M# when the processor is in real mode. The effect of asserting A20M# in protected mode is undefined and may be implemented differently in future processors.

Snoop requests and cache-line writeback transactions are unaffected by A20M# input. Address 20 is not masked when the processor samples external addresses to perform internal snooping.

A20M# is an asynchronous input. However, to guarantee recognition of this signal following an I/O write instruction, A20M# must be valid with active RS[2:0]# signals of the corresponding I/O Write bus transaction. In FRC mode, A20M# must be synchronous to BCLK.

During active RESET#, the Pentium Pro processor begins sampling the A20M#, IGNNE#, and LINT[1:0] values to determine the ratio of core-clock frequency to bus-clock frequency. After the PLL-lock time, the core clock becomes stable and is locked to the external bus clock. On the active-to-inactive transition of RESET#, the Pentium Pro processor latches A20M#, IGNNE#, and LINT[1:0] and freezes the frequency ratio internally. 29See Table 44.

A.3 ADS# (I/O)

The ADS# signal is the address Strobe signal. It is asserted by the current bus owner for one clock to indicate a new Request Phase. A new Request Phase can only begin if the In-order Queue has less than the maximum number of entries defined by the power-on configuration (1 or 8), the Request Phase is not being stalled by an active BNR# sequence and the ADS# associated with the previous Request Phase is sampled inactive. Along with the ADS#, the request initiator drives A[35:3]#, REQ[4:0]#, AP[1:0]#, and RP# signals for two clocks. During the second Request Phase clock, ADS# must be inactive. RP# provides parity protection for REQ[4:0]# and ADS# signals during both clocks. If the transaction is part of a bus locked operation, LOCK# must be active with ADS#.

If the request initiator continues to own the bus after the first Request Phase, it can issue a new request every three clocks. If the request initiator needs to release the bus ownership after the Request Phase, it can deactivate its BREQn#/ BPRI# arbitration signal as early as with the activation of ADS#.

All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction. On sampling the asserted ADS#, all agents load the new transaction in the In-order Queue and update internal counters. The Error, Snoop, Response, and Data Phase of the transaction are defined with respect to ADS# assertion.

Table 44. Bus Clock Ratios Versus Pin Logic Levels

Ratio of Core Clock to Bus Clock	LINT[1]/NMI	LINT[0]/INTR	IGNNE#	A20M#
2	L	L	L	L
2	H	H	H	H
3	L	L	H	L
4	L	L	L	H
RESERVED	L	L	H	H
5/2	L	H	L	L
7/2	L	H	H	L
RESERVED	L	H	L	H
RESERVED	L	H	H	H
RESERVED	ALL OTHER COMBINATIONS			

A.4 AERR# (I/O)

The AERR# signal is the address parity error signal. Assuming the AERR# driver is enabled during the power-on configuration, a bus agent can drive AERR# active for exactly one clock during the Error Phase of a transaction. AERR# must be inactive for a minimum of two clocks. The Error Phase is always three clocks from the beginning of the Request Phase.

On observing active ADS#, all agents begin parity and protocol checks for the signals valid in the two Request Phase clocks. Parity is checked on AP[1:0]# and RP# signals. AP1# protects A[35:24]#, AP0# protects A[23:3]# and RP# protects REQ[4:0]#. A parity error without a protocol violation is signaled by AERR# assertion.

If AERR# observation is enabled during power-on configuration, AERR# assertion in a valid Error Phase aborts the transaction. All bus agents remove the transaction from the In-order Queue and update internal counters. The Snoop Phase, Response Phase, and Data Phase of the transaction are aborted. All signals in these phases must be deasserted two clocks after AERR# is asserted, even if the signals have been asserted before AERR# has been observed. Specifically if the Snoop Phase associated with the aborted transaction is driven in the next clock, the snoop results, including a STALL condition (HIT# and HITM# asserted for one clock), are ignored. All bus agents must also begin an arbitration reset sequence and deassert BREQn#/BPRI# arbitration signals on sampling AERR# active. A current bus owner in the middle of a bus lock operation must keep LOCK# asserted and assert its arbitration request BPRI#/BREQn# after keeping it inactive for two clocks to retain its bus ownership and guarantee lock atomicity. All other agents, including the current bus owner not in the middle of a bus lock operation, must wait at least 4 clocks before asserting BPRI#/BREQn# and beginning a new arbitration.

If AERR# observation is enabled, the request initiator can retry the transaction up to n times until it reaches the retry limit defined by its implementation. (The Pentium Pro processor retries once.) After n retries, the request initiator treats the error as a hard error. The request initiator asserts BERR# or enters the Machine Check Exception handler, as defined by the system configuration.

If AERR# observation is disabled during power-on configuration, AERR# assertion is ignored by all bus agents except a central agent. Based on the Machine Check Architecture of the system, the central agent can ignore AERR#, assert NMI to execute NMI handler, or assert BINIT# to reset the bus units of all agents and execute an MCE handler.

A.5 AP[1:0]# (I/O)

The AP[1:0]# signals are the address parity signals. They are driven by the request initiator during the two Request Phase clocks along with ADS#, A[35:3]#, REQ[4:0]#, and RP#. AP1# covers A[35:24]#. AP0# covers A[23:3]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This rule allows parity to be high when all the covered signals are high.

Provided “AERR# drive” is enabled during the power-on configuration, all bus agents begin parity checking on observing active ADS# and determine if there is a parity error. On observing a parity error on any one of the two Request Phase clocks, the bus agent asserts AERR# during the Error Phase of the transaction.

A.6 ASZ[1:0]# (I/O)

The ASZ[1:0]# signals are the memory address-space size signals. They are driven by the request initiator during the first Request Phase clock on the REQa[4:3]# pins. The ASZ[1:0]# signals are valid only when REQa[1:0]# signals equal 01B, 10B, or 11B, indicating a memory access transaction. The ASZ[1:0]# decode is defined in Table 45.

Table 45. ASZ[1:0]# Signal Decode

ASZ[1:0]#		Description
0	0	0 <= A[35:3]# < 4 GB
0	1	4 GB <= A[35:3]# < 64 GB
1	X	Reserved

If the memory access is within the 0-to-(4GByte -1) address space, ASZ[1:0]# must be 00B. If the memory access is within the 4Gbyte-to-(64GByte -1) address space, ASZ[1:0]# must be 01B. All observing bus agents that support the 4Gbyte (32 bit) address space must respond to the transaction only

when ASZ[1:0]# equals 00. All observing bus agents that support the 64GByte (36- bit) address space must respond to the transaction when ASZ[1:0]# equals 00B or 01B.

A.7 ATTR[7:0]# (I/O)

The ATTR[7:0]# signals are the attribute signals. They are driven by the request initiator during the second Request Phase clock on the Ab[31:24]# pins. The ATTR[7:0]# signals are valid for all transactions. The ATTR[7:3]# are reserved and undefined. The ATTR[2:0]# are driven based on the Memory Range Register attributes and the Page Table attributes. Table 47. defines ATTR[3:0]# signals.

A.8 BCLK (I)

The BCLK (clock) signal is the Execution Control group input signal. It determines the bus frequency. All agents drive their outputs and latch their inputs on the BCLK rising edge.

The BCLK signal indirectly determines the Pentium Pro processor's internal clock frequency. Each Pentium Pro processor derives its internal clock from BCLK by multiplying the BCLK frequency by a ratio as defined and allowed by the power-on configuration. See Table 42.

All external timing parameters are specified with respect to the BCLK signal.

A.9 BE[7:0]# (I/O)

The BE[7:0]# signals are the byte-enable signals. They are driven by the request initiator during the second Request Phase clock on the Ab[15:8]# pins. These signals carry various information depending on the REQ[4:0]# value.

For memory or I/O transactions (REQa[4:0]# = {10000B, 10001B, XX01XB, XX10XB, XX11XB}) the byte-enable signals indicate that valid data is requested or being transferred on the corresponding byte on the 64 bit data bus. BE0# indicates D[7:0]# is valid, BE1# indicates D[15:8]# is valid,..., BE7# indicates D[63:56]# is valid.

For Special transactions ((REQa[4:0]# = 01000B) and (REQb[1:0]# = 01B)), the BE[7:0]# signals carry special cycle encodings as defined in Table 46. All other encodings are reserved.

Table 46. Special Transaction Encoding on BE[7:0]#

BE[7:0]#	Special Cycle
0000 0000	Reserved
0000 0001	Shutdown
0000 0010	Flush
0000 0011	Halt
0000 0100	Sync
0000 0101	Flush Acknowledge
00000 0110	Stop Clock Acknowledge
00000 0111	SMI Acknowledge
Other	Reserved

For Deferred Reply, Interrupt Acknowledge, and Branch Trace Message transactions, the BE[7:0]# signals are undefined.

Table 47. ATTR[7:0]# Field Descriptions

ATTR[7:3]#	ATTR[2]#	ATTR[1:0]#			
XXXXX	X	11	10	01	00
Reserved	Potentially Speculatable	Write-Back	Write-Protect	Write-Through	UnCacheable

A.10 BERR# (I/O)

The BERR# signal is the Error group Bus Error signal. It is asserted to indicate an unrecoverable error without a bus protocol violation.

The BERR# protocol is as follows: If an agent detects an unrecoverable error for which BERR# is a valid error response and BERR# is sampled inactive, it asserts BERR# for three clocks. An agent can assert BERR# only after observing that the signal is inactive. An agent asserting BERR# must deassert the signal in two clocks if it observes that another agent began asserting BERR# in the previous clock.

BERR# assertion conditions are defined by the system configuration. Configuration options enable the BERR# driver as follows:

- Enabled or disabled
- Asserted optionally for internal errors along with IERR#
- Optionally asserted by the request initiator of a bus transaction after it observes an error
- Asserted by any bus agent when it observes an error in a bus transaction

BERR# sampling conditions are also defined by the system configuration. Configuration options enable the BERR# receiver to be enabled or disabled. When the bus agent samples an active BERR# signal and if MCE is enabled, the Pentium Pro processor enters the Machine Check Handler. If MCE is disabled, typically the central agent forwards BERR# as an NMI to one of the processors. The Pentium Pro processor does not support BERR# sampling (always disabled).

A.11 BINIT# (I/O)

The BINIT# signal is the bus initialization signal. If the BINIT# driver is enabled during the power on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future information.

The BINIT# protocol is as follows: If an agent detects an error for which BINIT# is a valid error response, and BINIT# is sampled inactive, it asserts BINIT# for three clocks. An agent can assert BINIT# only after observing that the signal is inactive. An agent asserting BINIT# must deassert the signal in two clocks if it observes that another agent began asserting BINIT# in the previous clock.

If BINIT# observation is enabled during power-on configuration, and BINIT# is sampled asserted, all bus state machines are reset. All agents reset their rotating ID for bus arbitration to the state after reset, and internal count information is lost. The L1 and L2 caches are not affected.

If BINIT# observation is disabled during power-on configuration, BINIT# is ignored by all bus agents except a central agent that must handle the error in a manner appropriate to the system architecture.

A.12 BNR# (I/O)

The BNR# signal is the Block Next Request signal in the Arbitration group. The BNR# signal is used to assert a bus stall by any bus agent who is unable to accept new bus transactions to avoid an internal transaction queue overflow. During a bus stall, the current bus owner cannot issue any new transactions.

Since multiple agents might need to request a bus stall at the same time, BNR# is a wire-OR signal. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges. A valid bus stall involves assertion of BNR# for one clock on a well-defined clock edge (T1), followed by de-assertion of BNR# for one clock on the next clock edge (T1+1). BNR# can first be sampled on the second clock edge (T1+1) and must always be ignored on the third clock edge (T1+2). An extension of a bus stall requires one clock active (T1+2), one clock inactive (T1+3) BNR# sequence with BNR# sampling points every two clocks (T1+1, T1+3,...).

After the RESET# active-to-inactive transition, bus agents might need to perform hardware initialization of their bus unit logic. Bus agents intending to create a request stall must assert BNR# in the clock after RESET# is sampled inactive.

After BINIT# assertion, all bus agents go through a similar hardware initialization and can create a request stall by asserting BNR# four clocks after BINIT# assertion is sampled.

On the first BNR# sampling clock that BNR# is sampled inactive, the current bus owner is allowed to issue one new request. Any bus agent can immediately reassert BNR# (four clocks from the previous assertion or two clocks from the previous de-assertion) to create a new bus stall. This throttling

mechanism enables independent control on every new request generation.

If BNR# is deasserted on two consecutive sampling points, new requests can be freely generated on the bus. After receiving a new transaction, a bus agent can require an address stall due to an anticipated transaction-queue overflow condition. In response, the bus agent can assert BNR#, three clocks from active ADS# assertion and create a bus stall. Once a bus stall is created, the bus remains stalled until BNR# is sampled asserted on subsequent sampling points.

A.13 BP[3:2]# (I/O)

The BP[3:2]# signals are the System Support group Breakpoint signals. They are outputs from the Pentium Pro processor that indicate the status of breakpoints.

A.14 BPM[1:0]# (I/O)

The BPM[1:0]# signals are more System Support group breakpoint and performance monitor signals. They are outputs from the Pentium Pro processor that indicate the status of breakpoints and programmable counters used for monitoring Pentium Pro processor performance.

A.15 BPRI# (I)

The BPRI# signal is the Priority-agent Bus Request signal. The priority agent arbitrates for the bus by asserting BPRI#. The priority agent is always be the next bus owner. Observing BPRI# active causes the current symmetric owner to stop issuing new requests, unless such requests are part of an ongoing locked operation.

If LOCK# is sampled inactive two clocks from BPRI# driven asserted, the priority agent can issue a new request within four clocks of asserting BPRI#. The priority agent can further reduce its arbitration latency to two clocks if it samples active ADS# and inactive LOCK# on the clock in which BPRI# was driven active and to three clocks if it samples active ADS# and inactive LOCK# on the clock in which BPRI# was sampled active. If LOCK# is sampled active, the priority agent must wait for LOCK# deasserted and gains bus ownership in two clocks after LOCK# is sampled deasserted. The priority agent can keep BPRI# asserted until all of its requests are completed and can release the bus by de-asserting BPRI# as early as the same clock edge on which it issues the last request.

On observation of active AERR#, RESET#, or BINIT#, BPRI# must be deasserted in the next clock. BPRI# can be reasserted in the clock after sampling the RESET# active-to-inactive transition or three clocks after sampling BINIT# active and RESET# inactive. On AERR# assertion, if the priority agent is in the middle of a bus-locked operation, BPRI# must be re-asserted after two clocks, otherwise BPRI# must stay inactive for at least 4 clocks.

After the RESET# inactive transition, Pentium Pro processor bus agents begin BPRI# and BNR# sampling on BNR# sample points. When both BNR# and BPRI# are observed inactive on a BNR# sampling point, the APIC units in Pentium Pro processors on a common APIC bus are synchronized.

A.16 BR0#(I/O), BR[3:1]# (I)

The BR[3:0]# pins are the physical bus request pins that drive the BREQ[3:0]# signals in the system. The BREQ[3:0]# signals are interconnected in a rotating manner to individual processor pins. Table 48 gives the rotating interconnect between the processor and bus signals.

Table 48. BR[3:0]# Signals Rotating Interconnect

Bus Signal	Agent 0 Pins	Agent 1 Pins	Agent 2Pins	Agent 3 Pins
BREQ0#	BR0#	BR3#	BR2#	BR1#
BREQ1#	BR1#	BR0#	BR3#	BR2#
BREQ2#	BR2#	BR1#	BR0#	BR3#
BREQ3#	BR3#	BR2#	BR1#	BR0#

During power-up configuration, the central agent must assert the BR0# bus signal. All symmetric agents sample their BR[3:0]# pins on active-to-inactive transition of RESET#. The pin on which the agent samples an active level determines its agent ID. All agents then configure their pins to match the appropriate bus signal protocol, as shown in Table 49.

Table 49. BR[3:0]# Signal Agent IDs

Pin Sampled Active on RESET#	Agent ID
BR0#	0
BR3#	1
BR2#	2
BR1#	3

A.17 BREQ[3:0]# (I/O)

The BREQ[3:0]# signals are the Symmetric-agent Arbitration Bus signals (called bus request). A symmetric agent n arbitrates for the bus by asserting its BREQn# signal. Agent n drives BREQn# as an output and receives the remaining BREQ[3:0]# signals as inputs.

The symmetric agents support distributed arbitration based on a round-robin mechanism. The rotating ID is an internal state used by all symmetric agents to track the agent with the lowest priority at the next arbitration event. At power-on, the rotating ID is initialized to three, allowing agent 0 to be the highest priority symmetric agent. After a new arbitration event, the rotating ID of all symmetric agents is updated to the agent ID of the symmetric owner. This update gives the new symmetric owner lowest priority in the next arbitration event.

A new arbitration event occurs either when a symmetric agent asserts its BREQn# on an Idle bus (all BREQ[3:0]# previously inactive), or the current symmetric owner de-asserts BREQm# to release the bus ownership to a new bus owner n. On a new arbitration event, based on BREQ[3:0]#, and the rotating ID, all symmetric agents simultaneously determine the new symmetric owner. The symmetric owner can park on the bus (hold the bus) provided that no other symmetric agent is requesting its use. The symmetric owner parks by keeping its BREQn# signal active. On sampling active BREQm# asserted by another symmetric agent, the symmetric owner de-asserts BREQn# as soon as possible to release the bus. A symmetric owner stops issuing new requests that are not part of an existing locked operation upon observing BPRI# active.

A symmetric agent can not deassert BREQn# until it becomes a symmetric owner. A symmetric agent can reassert BREQn# after keeping it inactive for one clock.

On observation of active AERR#, RESET#, or BINIT#, the BREQ[3:0]# signals must be deasserted in the next clock. BREQ[3:0]# can be reasserted in the clock after sampling the RESET# active-to-inactive transition or three clocks after sampling BINIT# active and RESET# inactive. On AERR# assertion, if bus agent n is in the middle of a bus-locked operation, BREQn# must be re-asserted after two clocks, otherwise BREQ[3:0]# must stay inactive for at least 4 clocks.

A.18 D[63:0]# (I/O)

The D[63:0]# signals are the data signals. They are driven during the Data Phase by the agent responsible for driving the data. These signals provide a 64-bit data path between various Pentium Pro processor bus agents. 32-byte line transfers

require four data transfer clocks with valid data on all eight bytes. Partial transfers require one data transfer clock with valid data on the byte(s) indicated by active byte enables BE[7:0]#. Data signals not valid for a particular transfer must still have correct ECC (if data bus ECC is selected). If BE0# is asserted, D[7:0]# transfers the least significant byte. If BE7# is asserted, D[63:56]# transfers the most significant byte.

The data driver asserts DRDY# to indicate a valid data transfer. If the Data Phase involves more than one clock the data driver also asserts DBSY# at the beginning of the Data Phase and de-asserts DBSY# no earlier than on the same clock that it performs the last data transfer.

A.19 DBSY# (I/O)

The DBSY# signal is the Data-bus Busy signal. It indicates that the data bus is busy. It is asserted by the agent responsible for driving the data during the Data Phase, provided the Data Phase involves more than one clock. DBSY# is asserted at the beginning of the Data Phase and may be deasserted on or after the clock on which the last data is driven. The data bus is released one clock after DBSY# is deasserted.

When normal read data is being returned, the Data Phase begins with the Response Phase. Thus the agent returning read data can assert DBSY# when the transaction reaches the top of the In-order Queue and it is ready to return response on RS[2:0]# signals. In response to a write request, the agent driving the write data must drive DBSY# active after the write transaction reaches the top of the In-order Queue and it sees active TRDY# with inactive DBSY# indicating that the target is ready to receive data. For an implicit writeback response, the snoop agent must assert DBSY# active after the target memory agent of the implicit writeback asserts TRDY#. Implicit writeback TRDY# assertion begins after the transaction reaches the top of the In-order Queue, and TRDY# de-assertion associated with the write portion of the transaction, if any is completed. In this case, the memory agent guarantees assertion of implicit writeback response in the same clock in which the snooping agent asserts DBSY#.

A.20 DEFER# (I)

The DEFER# signal is the defer signal. It is asserted by an agent during the Snoop Phase to indicate that the transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory agent or I/O agent. For systems that involve resources on a system bus other than the Pentium Pro processor bus, a bridge agent can accept the DEFER# assertion responsibility on behalf of the addressed agent.

When HITM# and DEFER# are both active during the Snoop Phase, HITM# is given priority and the transaction must be completed with implicit writeback response. If HITM# is inactive, and DEFER# active, the agent asserting DEFER# must complete the transaction with a Deferred or Retry response.

If DEFER# is inactive, or HITM# is active, then the transaction is committed for in-order completion and snoop ownership is transferred normally between the requesting agent, the snooping agents, and the response agent.

If DEFER# is active with HITM# inactive, the transaction commitment is deferred. If the defer agent completes the transaction with a retry response, the requesting agent must retry the transaction. If the defer agent returns a deferred response, the requesting agent must freeze snoop state transitions associated with the deferred transaction and issues of new order-dependent transactions until the corresponding deferred reply transaction. In the meantime, the ownership of the deferred address is transferred to the defer agent and it must guarantee management of conflicting transactions issued to the same address.

If DEFER# is active in response to a newly issued bus-lock transaction, the entire bus-locked operation is re-initiated regardless of HITM#. This feature is useful for a bridge agent in response to a split bus-locked operation. It is recommended that the bridge agent extend the Snoop Phase of the first transaction in a split locked operation until it can either guarantee ownership of all system resources to enable successful completion of the split sequence or assert DEFER# followed by a Retry Response to abort the split sequence.

A.21 DEN# (I/0)

The DEN# signal is the defer-enable signal. It is driven to the bus on the second clock of the Request Phase on the EXF1#/Ab4# pin. DEN# is asserted to indicate that the transaction can be deferred by the responding agent.

A.22 DEP[7:0]# (I/O)

The DEP[7:0]# signals are the data bus ECC protection signals. They are driven during the Data Phase by the agent responsible for driving D[63:0]#. The DEP[7:0]# signals provide optional ECC protection for the data bus. During power-on configuration, DEP[7:0]# signals can be enabled for either ECC checking or no checking.

The ECC error correcting code can detect and correct single-bit errors and detect double-bit or nibble errors. The *Pentium® Pro Processor Developer's Manual, Volume 1: Specifications* (Order Number 242690) provides more information about ECC.

DEP[7:0]# provide valid ECC for the entire data bus on each data clock, regardless of which bytes are valid. If checking is enabled, receiving agents check the ECC signals for all 64 data signals.

A.23 DID[7:0]# (I/O)

The DID[7:0]# signals are Deferred Identifier signals. They are transferred using A[23:16]# signals by the request initiator. They are transferred on Ab[23:16]# during the second clock of the Request Phase on all transactions, but only defined for deferrable transactions (DEN# asserted). DID[7:0]# is also transferred on Aa[23:16]# during the first clock of the Request Phase for Deferred Reply transactions.

The deferred identifier defines the token supplied by the request initiator. DID[7:4]# carry the request initiators' agent identifier and DID[3:0]# carry a transaction identifier associated with the request. This configuration limits the bus specification to 16 bus masters with each one of the bus masters capable of making up to sixteen requests.

Every deferrable transaction issued on the Pentium Pro processor bus which has not been guaranteed completion (has not successfully passed its Snoop Result Phase) will have a unique Deferred ID. This includes all outstanding transactions which have not had their snoop result reported, or have had their snoop results deferred. After a deferrable transaction passes its Snoop Result Phase without DEFER# asserted, its Deferred ID may be reused. Similarly, the deferred ID of a transaction which was deferred may be reused after the completion of the snoop window of the deferred reply.

DID[7]# indicates the agent type. Symmetric agents use 0. Priority agents use 1. DID[6:4]# indicates the agent ID. Symmetric agents use their arbitration ID. The Pentium Pro processor has four symmetric agents, so does not assert DID[6]#. DID[3:0]# indicates the transaction ID for an agent. The transaction ID must be unique for all transactions issued by an agent which have not reported their snoop results.

Table 50. DID[7:0]# Encoding

DID[7]	DID[6:4]	DID[3:0]
Agent Type	Agent ID	Transaction ID

The Deferred Reply agent transmits the DID[7:0]# (Ab[23:16]#) signals received during the original transaction on the Aa[23:16]# signals during the Deferred Reply transaction. This process enables the original request initiator to make an identifier match and wake up the original request waiting for completion.

A.24 DRDY# (I/O)

The DRDY# signal is the Data Phase data-ready signal. The data driver asserts DRDY# on each data transfer, indicating valid data on the data bus. In a multi-cycle data transfer, DRDY# can be deasserted to insert idle clocks in the Data Phase. During a line transfer, DRDY# is active for four clocks. During a partial 1-to-8 byte transfer, DRDY# is active for one clock. If a data transfer is exactly one clock, then the entire Data Phase may consist of only one clock active DRDY# and inactive DBSY#. If DBSY# is asserted for a 1-to-8 byte transfer, then the data bus is not released until one clock after DBSY# is deasserted.

A.25 DSZ[1:0]# (I/O)

The DSZ[1:0]# signals are the data-size signals. They are transferred on REQb[4:3]# signals in the second clock of Request Phase by the requesting agent. The DSZ[1:0]# signals define the data transfer

capability of the requesting agent. For the Pentium Pro processor, DSZ#= 00, always.

A.26 EXF[4:0]# (I/O)

The EXF[4:0]# signals are the Extended Function signals and are transferred on the Ab[7:3]# signals by the request initiator during the second clock of the Request Phase. The signals specify any special functional requirement associated with the transaction based on the requester mode or capability. The signals are defined in Table 51.

Table 51. EXF[4:0]# Signal Definitions

EXF	NAME	External Functionality	When Activated
EXF4#	SMMEM#	SMM Mode	After entering SMM mode
EXF3#	SPLCK#	Split Lock	The first transaction of a split bus lock operation
EXF2#	Reserved	Reserved	
EXF1#	DEN#	Defer Enable	The transactions for which Defer or Retry Response is acceptable.
EXF0#	Reserved	Reserved	

A.27 FERR# (O)

The FERR# signal is the PC Compatibility group Floating-point Error signal. The Pentium Pro processor asserts FERR# when it detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel387™ coprocessor. FERR# is included for compatibility with systems using DOS-type floating-point error reporting.

A.28 FLUSH# (I)

When the FLUSH# input signal is asserted, the Pentium Pro processor bus agent writes back all internal cache lines in the Modified state and invalidates all internal cache lines. At the completion of a flush operation, the Pentium Pro processor issues a Flush Acknowledge transaction to indicate that the cache flush operation is complete. The Pentium Pro processor stops caching any new data while the FLUSH# signal remains asserted.

FLUSH# is an asynchronous input. However, to guarantee recognition of this signal following an I/O write instruction, FLUSH# must be valid along with RS[2:0]# in the Response Phase of the corresponding I/O Write bus transaction. In FRC mode, FLUSH# must be synchronous to BCLK.

On the active-to-inactive transition of RESET#, each Pentium Pro processor bus agent samples FLUSH# to determine its power-on configuration. See Table 44.

A.29 FRCERR (I/O)

The FRCERR signal is the Error group Functional-redundancy-check Error signal. If two Pentium Pro processors are configured in an FRC pair, as a single “logical” processor, then the checker processor asserts FRCERR if it detects a mismatch between its internally sampled outputs and the master processor’s outputs. The checker’s FRCERR output pin is connected to the master’s FRCERR input pin.

For point-to-point connections, the checker always compares against the master’s outputs. For bussed single-driver signals, the checker compares against the signal when the master is the only allowed driver. For bussed multiple-driver Wire-OR signals, the checker compares against the signal only if the master is expected to drive the signal low.

FRCERR is also toggled during the Pentium Pro processor’s reset action. A Pentium Pro processor asserts FRCERR for approximately 1 second after RESET’s active-to-inactive transition if it executes its built-in self-test (BIST). When BIST execution

completes, the Pentium Pro processor de-asserts FRCERR if BIST completed successfully and continues to assert FRCERR if BIST fails. If the Pentium Pro processor does not execute the BIST action, then it keeps FRCERR asserted for approximately 20 clocks and then de-asserts it.

The Pentium® Pro Processor Developer's Manual, Volume 1: Specifications (Order Number 242690) describes how a Pentium Pro processor can be configured as a master or a checker.

A.30 HIT# (I/O), HITM# (I/O)

The HIT# and HITM# signals are Snoop-hit and Hit-modified signals. They are snoop results asserted by any Pentium Pro processor bus agent in the Snoop Phase.

Any bus agent can assert both HIT# and HITM# together for one clock in the Snoop Phase to indicate that it requires a snoop stall. When a stall condition is sampled, all bus agents extend the Snoop Phase by two clocks. The stall can be continued by reasserting HIT# and HITM# together every other clock for one clock.

A caching agent must assert HITM# for one clock in the Snoop Phase if the transaction hits a Modified line, and the snooping agent must perform an implicit writeback to update main memory. The snooping agent with the Modified line makes a transition to Shared state if the original transaction is Read Line or Read Partial, otherwise it transitions to Invalid state. A Deferred Reply transaction may have HITM# asserted to indicate the return of unexpected data.

A snooping agent must assert HIT# for one clock during the Snoop Phase if the line does not hit a Modified line in its writeback cache and if at the end of the transaction it plans to keep the line in Shared state. Multiple caching agents can assert HIT# in the same Snoop Phase. If the requesting agent observes HIT# active during the Snoop Phase it can not cache the line in Exclusive or Modified state.

On observing a snoop stall, the agents asserting HIT# and HITM# independently reassert the signal after one inactive clock so that the correct snoop result is available, in case the Snoop Phase terminates after the two clock extension.

A.31 IERR# (O)

The IERR# signal is the Error group Internal Error signal. A Pentium Pro processor asserts IERR# when it observes an internal error. It keeps IERR# asserted until it is turned off as part of the Machine Check Error or the NMI handler in software, or with RESET#, BINIT#, and INIT# assertion.

An internal error can be handled in several ways inside the processor based on its power-on configuration. If Machine Check Exception (MCE) is enabled, IERR# causes an MCE entry. IERR# can also be directed on the BERR# pin to indicate an error. Usually BERR# is sampled back by all processors to enter MCE or it can be redirected as an NMI by the central agent.

A.32 IGNNE# (I)

The IGNNE# signal is the Intel Architecture Compatability group Ignore Numeric Error signal. If IGNNE# is asserted, the Pentium Pro processor ignores a numeric error and continues to execute non-control floating-point instructions. If IGNNE# is deasserted, the Pentium Pro processor freezes on a non-control floating-point instruction if a previous instruction caused an error.

IGNNE# has no effect when the NE bit in control register 0 is set.

IGNNE# is an asynchronous input. However, to guarantee recognition of this signal following an I/O write instruction, IGNNE# must be valid along with RS[2:0]# in the Response Phase of the corresponding I/O Write bus transaction. In FRC mode, IGNNE# must be synchronous to BCLK.

During active RESET#, the Pentium Pro processor begins sampling the A20M#, IGNNE# and LINT[1:0] values to determine the ratio of core-clock frequency to bus-clock frequency. See Table 44. After the PLL-lock time, the core clock becomes stable and is locked to the external bus clock. On the active-to-inactive transition of RESET#, the Pentium Pro processor latches A20M# and IGNNE# and freezes the frequency ratio internally. Normal operation on the two signals continues two clocks after RESET# inactive is sampled.

A.33 INIT# (I)

The INIT# signal is the Execution Control group initialization signal. Active INIT# input resets integer registers inside all Pentium Pro processors without affecting their internal (L1 or L2) caches or their floating-point registers. Each Pentium Pro processor begins execution at the power-on reset vector configured during power-on configuration regardless of whether INIT# has gone inactive. The processor continues to handle snoop requests during INIT# assertion.

INIT# can be used to help performance of DOS extenders written for the Intel 80286 processor. INIT# provides a method to switch from protected mode to real mode while maintaining the contents of the internal caches and floating-point state. INIT# can not be used in lieu of RESET# after power-up.

On active-to-inactive transition of RESET#, each Pentium Pro processor bus agent samples INIT# signals to determine its power-on configuration. Two clocks after RESET# is sampled deasserted, these signals begin normal operation.

INIT# is an asynchronous input. In FRC mode, INIT# must be synchronous to BCLK.

A.34 INTR (I)

The INTR signal is the Interrupt Request signal. The INTR input indicates that an external interrupt has been generated. The interrupt is maskable using the IF bit in the EFLAGS register. If the IF bit is set, the Pentium Pro processor vectors to the interrupt handler after the current instruction execution is completed. Upon recognizing the interrupt request, the Pentium Pro processor issues a single Interrupt Acknowledge (INTA) bus transaction. INTR must remain active until the INTA bus transaction to guarantee its recognition.

INTR is sampled on every rising BCLK edge. INTR is an asynchronous input but recognition of INTR is guaranteed in a specific clock if it is asserted synchronously and meets the setup and hold times. INTR must also be deasserted for a minimum of two clocks to guarantee its inactive recognition. In FRC mode, INTR must be synchronous to BCLK. On power-up the LINT[1:0] signals are used for power-on-configuration of clock ratios. Both these signals must be software configured by programming the APIC register space to be used either as NMI/INTR or LINT[1:0] in the BIOS. Because APIC is enabled after reset, LINT[1:0] is the default configuration.

A.35 LEN[1:0]# (I/O)

The LEN[1:0]# signals are data-length signals. They are transmitted using REQb[1:0]# signals by the request initiator in the second clock of Request Phase. LEN[1:0]# define the length of the data transfer requested by the request initiator as defined in Table 52. The LEN[1:0]#, HITM#, and RS[2:0]# signals together define the length of the actual data transfer.

Table 52. LEN[1:0]# Data Transfer Lengths

LEN[1:0]#	Request Initiator's Data Transfer Length
00	0-8 Bytes
01	16 Bytes
10	32 Bytes
11	Reserved

A.36 LINT[1:0] (I)

The LINT[1:0] signals are the Execution Control group Local Interrupt signals. When APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a non-maskable interrupt. INTR and NMI are backward compatible with the same signals for the Pentium processor. Both signals are asynchronous inputs. In FRC mode, LINT[1:0] must be synchronous to BCLK.

During active RESET#, the Pentium Pro processor continuously samples the A20M#, IGNNE# and LINT[1:0] values to determine the ratio of core-clock frequency to bus-clock frequency. See Table 44. After the PLL-lock time, the core clock becomes stable and is locked to the external bus clock. On the active-to-inactive transition of RESET#, the Pentium Pro processor latches the ratio internally.

Both these signals must be software configured by programming the APIC register space to be used either as NMI/INTR or LINT[1:0] in the BIOS. Because APIC is enabled after reset, LINT[1:0] is the default configuration.

A.37 LOCK# (I/O)

The LOCK# signal is the Arbitration group bus lock signal. For a locked sequence of transactions, LOCK# is asserted from the first transaction's Request Phase through the last transaction's Response Phase. A locked operation can be prematurely aborted (and LOCK# deasserted) if AERR# or DEFER# is asserted during the first bus transaction of the sequence. The sequence can also be prematurely aborted if a hard error (such as a hard failure response or AERR# assertion beyond the retry limit) occurs on any one of the transactions during the locked operation.

When the priority agent asserts BPRI# to arbitrate for bus ownership, it waits until it observes LOCK# deasserted. This enables symmetric agents to retain bus ownership throughout the bus locked operation and guarantee the atomicity of lock. If AERR# is asserted up to the retry limit during an ongoing locked operation, the arbitration protocol ensures that the lock owner receives the bus ownership after arbitration logic is reset. This result is accomplished by requiring the lock owner to reactivate its arbitration request one clock ahead of other agents' arbitration request. LOCK# is kept asserted throughout the arbitration reset sequence.

A.38 NMI (I)

The NMI signal is the Non-maskable Interrupt signal. It is the state of the LINT1 signal when APIC is disabled. Asserting NMI causes an interrupt with an internally supplied vector value of 2. An external interrupt-acknowledge transaction is not generated. If NMI is asserted during the execution of an NMI service routine, it remains pending and is recognized after the IRET is executed by the NMI service routine. At most, one assertion of NMI is held pending.

NMI is rising-edge sensitive. Recognition of NMI is guaranteed in a specific clock if it is asserted synchronously and meets the setup and hold times. If asserted asynchronously, active and inactive pulse widths must be a minimum of two clocks. In FRC mode, NMI must be synchronous to BCLK.

A.39 PICCLK (I)

The PICCLK signal is the Execution Control group APIC Clock signal. It is an input clock to the Pentium Pro processor for synchronous operation of the APIC bus. PICCLK must be synchronous to BCLK in FRC mode.

A.40 PICD[1:0] (I/O)

The PICD[1:0] signals are the Execution Control group APIC Data signals. They are used for bi-directional serial message passing on the APIC bus.

A.41 PWRGOOD (I)

PWRGOOD is driven to the Pentium Pro processor by the system to indicate that the clocks and power supplies are within their specification. See Section 3.9 for additional details. This signal will not affect FRC operation.

A.42 REQ[4:0]# (I/O)

The REQ[4:0]# signals are the Request Command signals. They are asserted by the current bus owner in both clocks of the Request Phase. In the first clock, the REQa[4:0]# signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second clock, REQb[4:0]# signals carry additional information to define the complete transaction type. REQb[4:2]# is reserved. REQb[1:0]# signals transmit LEN[1:0]# (the data transfer length information). In both clocks, REQ[4:0]# and ADS# are protected by parity RP#.

All receiving agents observe the REQ[4:0]# signals to determine the transaction type and participate in the transaction as necessary, as shown in Table 53.

Table 53. Transaction Types Defined by REQa#/REQb# Signals

	REQa[4:0]#					REQb[4:0]#				
Transaction	**4**	**3**	**2**	**1**	**0**	**4**	**3**	**2**	**1**	**0**
Deferred Reply	0	0	0	0	0	X	X	X	X	X
Rsvd (Ignore)	0	0	0	0	1	X	X	X	X	X
Interrupt Acknowledge	0	1	0	0	0	DSZ#		X	0	0
Special Transactions	0	1	0	0	0	DSZ#		X	0	1
Rsvd (Central agent response)	0	1	0	0	0	DSZ#		X	1	X
Branch Trace Message	0	1	0	0	1	DSZ#		X	0	0
Rsvd (Central agent response)	0	1	0	0	1	DSZ#		X	0	1
Rsvd (Central agent response)	0	1	0	0	1	DSZ#		X	1	X
I/O Read	1	0	0	0	0	DSZ#		X	LEN#	
I/O Write	1	0	0	0	1	DSZ#		X	LEN#	
Rsvd (Ignore)	1	1	0	0	X	DSZ#		X	X	X
Memory Read & Invalidate	ASZ#		0	1	0	DSZ#		X	LEN#	
Rsvd (Memory Write)	ASZ#		0	1	1	DSZ#		X	LEN#	
Memory Code Read	ASZ#		1	D/C#=0	0	DSZ#		X	LEN#	
Memory Data Read	ASZ#		1	D/C#=1	0	DSZ#		X	LEN#	
Memory Write (may not be retried)	ASZ#		1	W/WB#=0	1	DSZ#		X	LEN#	
Memory Write (may not be retried)	ASZ#		1	W/WB#=1	1	DSZ#		X	LEN#	

A.43 RESET# (I)

The RESET# signal is the Execution Control group reset signal. Asserting RESET# resets all Pentium Pro processors to known states and invalidates their L1 and L2 caches without writing back Modified (M state) lines. For a power-on type reset, RESET# must stay active for at least one millisecond after $V_{CC}P$ and CLK have reached their proper DC and AC specifications. On observing active RESET#, all bus agents must deassert their outputs within two clocks.

A number of bus signals are sampled at the active-to-inactive transition of RESET# for the power-on configuration. The configuration options are described in the *Pentium® Pro Processor Developer's Manual, Volume 1: Specifications (Order* Number 242690) and in the pertinent signal descriptions in this appendix.

Unless its outputs are tristated during power-on configuration, after active-to-inactive transition of RESET#, the Pentium Pro processor optionally executes its built-in self-test (BIST) and begins program execution at reset-vector 0_000F_FFF0H or 0_FFFF_FFF0H.

A.44 RP# (I/O)

The RP# signal is the Request Parity signal. It is driven by the request initiator in both clocks of the Request Phase. RP# provides parity protection on ADS# and REQ[4:0]#. When a Pentium Pro processor bus agent observes an RP# parity error on any one of the two Request Phase clocks, it must assert AERR# in the Error Phase, provided "AERR# drive" is enabled during the power-on configuration.

A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This definition allows parity to be high when all covered signals are high.

A.45 RS[2:0]# (I)

The RS[2:0]# signals are the Response Status signals. They are driven by the response agent (the agent responsible for completion of the transaction at the top of the In-order Queue). Assertion of RS[2:0]# to a non-zero value for one clock completes the Response Phase for a transaction. The response encodings are shown in Table 55. Only certain response combinations are valid, based on the snoop result signaled during the transaction's Snoop Phase.

The RS[2:0]# assertion for a transaction is initiated when all of the following conditions are met:

- All bus agents have observed the Snoop Phase completion of the transaction.
- The transaction is at the top of the In-order Queue.
- RS[2:0]# are sampled in the Idle state

The response driven depends on the transaction as described below:

- The response agent returns a hard-failure response for any transaction in which the response agent observes a hard error.
- The response agent returns a Normal with data response for a read transaction with HITM# and DEFER# deasserted in the Snoop Phase, when the addressed agent is ready to return data and samples inactive DBSY#.
- The response agent returns a Normal without data response for a write transaction with HITM# and DEFER# deasserted in the Snoop Phase, when the addressed agent samples TRDY# active and DBSY# inactive, and it is ready to complete the transaction.

Table 54. Transaction Response Encodings

RS[2:0]	Description	HITM#	DEFER#
000	Idle State.	N/A	N/A
001	Retry Response. The transaction is canceled and must be retried by the initiator.	0	1
010	Defer Response. The transaction is suspended. The defer agent will complete it with a defer reply	0	1
011	Reserved.	0	1
100	Hard Failure. The transaction received a hard error. Exception handling is required.	X	X
101	Normal without data	0	0
110	Implicit WriteBack Response. Snooping agent will transfer the modified cache line on the data bus.	1	X
111	Normal with data.	0	0

- The response agent must return an Implicit writeback response in the next clock for a read transaction with HITM# asserted in the Snoop Phase, when the addressed agent samples TRDY# active and DBSY# inactive.
- The addressed agent must return an Implicit writeback response in the clock after the following sequence is sampled for a write transaction with HITM# asserted:
  1. TRDY# active and DBSY# inactive
  2. Followed by TRDY# inactive
  3. Followed by TRDY# active and DBSY# inactive
- The defer agent can return a Deferred, Retry, or Split response anytime for a read transaction with HITM# deasserted and DEFER# asserted.
- The defer agent can return Deferred, Retry, or Split response when it samples TRDY# active and DBSY# inactive for a write transaction with HITM# deasserted and DEFER# asserted.

A.46 RSP# (I)

The RSP# signal is the Response Parity signal. It is driven by the response agent during assertion of RS[2:0]#. RSP# provides parity protection for RS[2:0]#.

A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. During Idle state of RS[2:0]# (RS[2:0]#=000), RSP# is also high since it is not driven by any agent guaranteeing correct parity.

Pentium Pro processor bus agents can check RSP# at all times and if a parity error is observed, treat it as a protocol violation error. If the BINIT# driver is enabled during configuration, the agent observing RSP# parity error can assert BINIT#.

A.47 SMI# (I)

System Management Interrupt is asserted asynchronously by system logic. On accepting a System Management Interrupt, the Pentium Pro processor saves the current state and enters SMM mode. It issues an SMI Acknowledge Bus transaction and then begins program execution from the SMM handler.

A.48 SMMEM# (I/O)

The SMMEM# signal is the System Management Mode Memory signal. It is driven on the second clock

of the Request Phase on the EXF4#/Ab7# signal. It is asserted by the Pentium Pro processor to indicate that the processor is in System Management Mode and is executing out of SMRAM space.

A.49 SPLCK# (I/O)

The SPLCK# signal is the Split Lock signal. It is driven in the second clock of the Request Phase on the EXF3#/Ab6# signal of the first transaction of a locked operation. It is driven to indicate that the locked operation will consist of four locked transactions. Note that SPLCK# is asserted only for locked operations and only in the first transaction of the locked operation.

A.50 STPCLK# (I)

The STPCLK# signal is the Stop Clock signal. When asserted, the Pentium Pro processor enters a low-power state, the stop-clock state. The processor issues a Stop Clock Acknowledge special transaction, and stops providing internal clock signals to all units except the bus unit and the APIC unit. The processor continues to snoop bus transactions and service interrupts while in stop clock state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock.

STPCLK# is an asynchronous input. In FRC mode, STPCLK# must be synchronous to BCLK.

A.51 TCK (I)

The TCK signal is the System Support group Test Clock signal. TCK provides the clock input for the test bus (also known as the test access port). Make certain that TCK is active before initializing the TAP.

A.52 TDI(I)

The TDI signal is the System Support group test-data-in signal. TDI transfers serial test data into the Pentium Pro processor. TDI provides the serial input needed for JTAG support.

A.53 TDO (O)

The TDO signal is the System Support group test-data-out signal. TDO transfers serial test data out from the Pentium Pro processor. TDO provides the serial output needed for JTAG support.

A.54 TMS (I)

The TMS signal is an additional System Support group JTAG-support signal.

A.55 TRDY (I)

The TRDY# signal is the target Ready signal. It is asserted by the target in the Response Phase to indicate that the target is ready to receive write or implicit writeback data transfer. This enables the request initiator or the snooping agent to begin the appropriate data transfer. There will be no data transfer after a TRDY# assertion if a write has zero length indicated in the Request Phase. The data transfer is optional if an implicit writeback occurs for a transaction which writes a full cache line (the Pentium Pro processor will perform the implicit writeback).

TRDY# for a write transaction is driven by the addressed agent when:

- When the transaction has a write or writeback data transfer
- It has a free buffer available to receive the write data
- A minimum of 3 clocks after ADS# for the transaction
- The transaction reaches the top-of-the-In-order Queue
- A minimum of 1 clock after RS[2:0]# active assertion for transaction “n-1”. (After the transaction reaches the top of the In-order Queue).

TRDY# for an implicit writeback is driven by the addressed agent when:

- The transaction has an implicit writeback data transfer indicated in the Snoop Result Phase.
- It has a free cache line buffer to receive the cache line writeback

- If the transaction also has a request initiated transfer, that the request initiated TRDY# was asserted and then deasserted (TRDY# must be deasserted for at least one clock between the TRDY# for the write and the TRDY# for the implicit writeback),
- A minimum of 1 clock after RS[2:0]# active assertion for transaction “n-1”. After the transaction reaches the top of the In-order Queue).

TRDY# for a write or an implicit writeback may be deasserted when:

- Inactive DBSY# and active TRDY# are observed.
- DBSY# is observed inactive on the clock TRDY# is asserted.
- A minimum of three clocks can be guaranteed between two active-to-inactive transitions of TRDY#
- The response is driven on RS[2:0]#.
- Inactive DBSY# and active TRDY# are observed for a write, and TRDY# is required for an implicit writeback.

A.56 TRST (I)

The TRST# signal resets the JTAG logic.