

MOS GP Computer

by R. K. BOOHER

*North American Rockwell Corporation
Anaheim, California*

INTRODUCTION

When the 2-phase, 20-bit shift registers using P-channel enhancement mode MOS-FET's were first introduced on the market many of us did not have the foggiest idea of what a MOS-FET was. Logical designers were intrigued by the functional complexity which the technology appeared to offer. System designers were pleased with the prospect of lower power and fewer package requirements. Semiconductor manufacturers predicted that MOS would be forgotten sooner than the tunnel diode.

Autonetics studied the potential and the problems associated with direct coupled and 2-phase MOS circuits and promptly devised the 4-phase system which solved many of the problems of the 2-phase system. The first MOS-LSA using the 4-phase system was the Autonetics DDA Integrator. The first completely operational unit was produced during February 1966. This device has approximately 800 MOS-FET'S.

After gaining considerable experience with the DDA and other 4-phase MOS-LSA circuits, we felt we were ready to design a general purpose computer suitable for navigation applications.

At this point I would like to state that this computer, using MOS-LSA's, is fully operational. The computer was designed to satisfy the general requirements of a navigation computer, consequently it is neither the world's fastest nor the most versatile computer, but it does represent a quantum jump in the technology which produced it. The components are the most advanced in the industry. Numerous trade-offs had to be made before the logical equations for the machine could be written. Trade-offs were made between functional requirements, computer organization, MOS speed, IC size, IC complexity, number of leads per IC, number of IC types, and total number of IC's.

To give you a feel for the class of computer which has been built, I will touch on some of its salient features (Chart 1).

250 KC CLOCK RATE
PARALLEL, SINGLE ADDRESS ORGANIZATION
24 BIT WORD SIZE - INSTRUCTIONS & DATA
3 INDEX REGISTERS
4 INTERRUPT CHANNELS - WITH LOCKOUT
35 INSTRUCTIONS - MOST INDEXABLE
8 SEC ADD INSTRUCTION TIME
108 SEC MULTIPLY INSTRUCTION TIME
4K MEMORY - EXPANDABLE TO 32K
4 SEC MEMORY CYCLE TIME
24 IC'S IN CENTRAL PROCESSOR UNIT
8 IC TYPES IN CPU

CHART 1—MOS-GP characteristics

We were quite conservative when we evaluated the speed capability of the MOS circuits. In particular, our design was based on a 250 kHz clock rate using a patented 4-phase gating scheme. The gating scheme allows fairly complex logic equations to be evaluated at each level of gating but only allows, at most, four levels of gating during each clock time.

The machine operates in parallel with the conventional single address organization. A serial

machine was under consideration at one time, but it was abandoned for two reasons; it was slower and, surprisingly, it was more complex. The word size is 24 bits for both instructions and data. This came about principally from its intended use as a navigation computer. Three hardware index registers are provided, although one is pre-empted for use by the interrupt system. Four interrupt channels with programmable lock-out are provided. They operate on a rotational priority basis. They operate on a rotational priority basis. Thirty-five instructions are provided, including a 108 μ sec multiply, a 108 μ sec sum of products multiply, and a 112 μ sec divide. Most of the other instructions require 8 μ sec. The main exceptions are the shift type instructions which are of variable duration.

The computer is designed to address a 32K word memory, however, we currently are using a 4K word core memory. This core memory happens to have a 2 μ sec cycle time, although the computer really only requires a memory with a 4 μ sec cycle time to meet the stated instruction execution times. In the not too distant future we expect to operate the MOS-LSA's at 1 MHz clock rate, at which time we will require a memory with a 1 μ sec cycle time. The central processor unit is mechanized with 24 MOS-LSA's of 8 types (Chart 2).

The computer organization is fairly conventional, using an accumulator, a lower accumulator, an operand buffer register, a program counter,

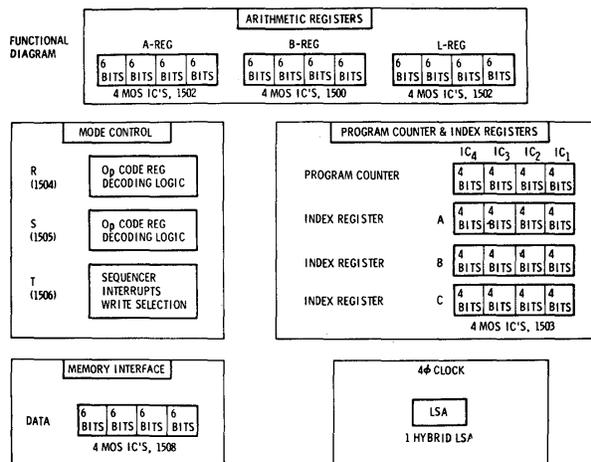


CHART 2—Arithmetic and control section, MOS-GP

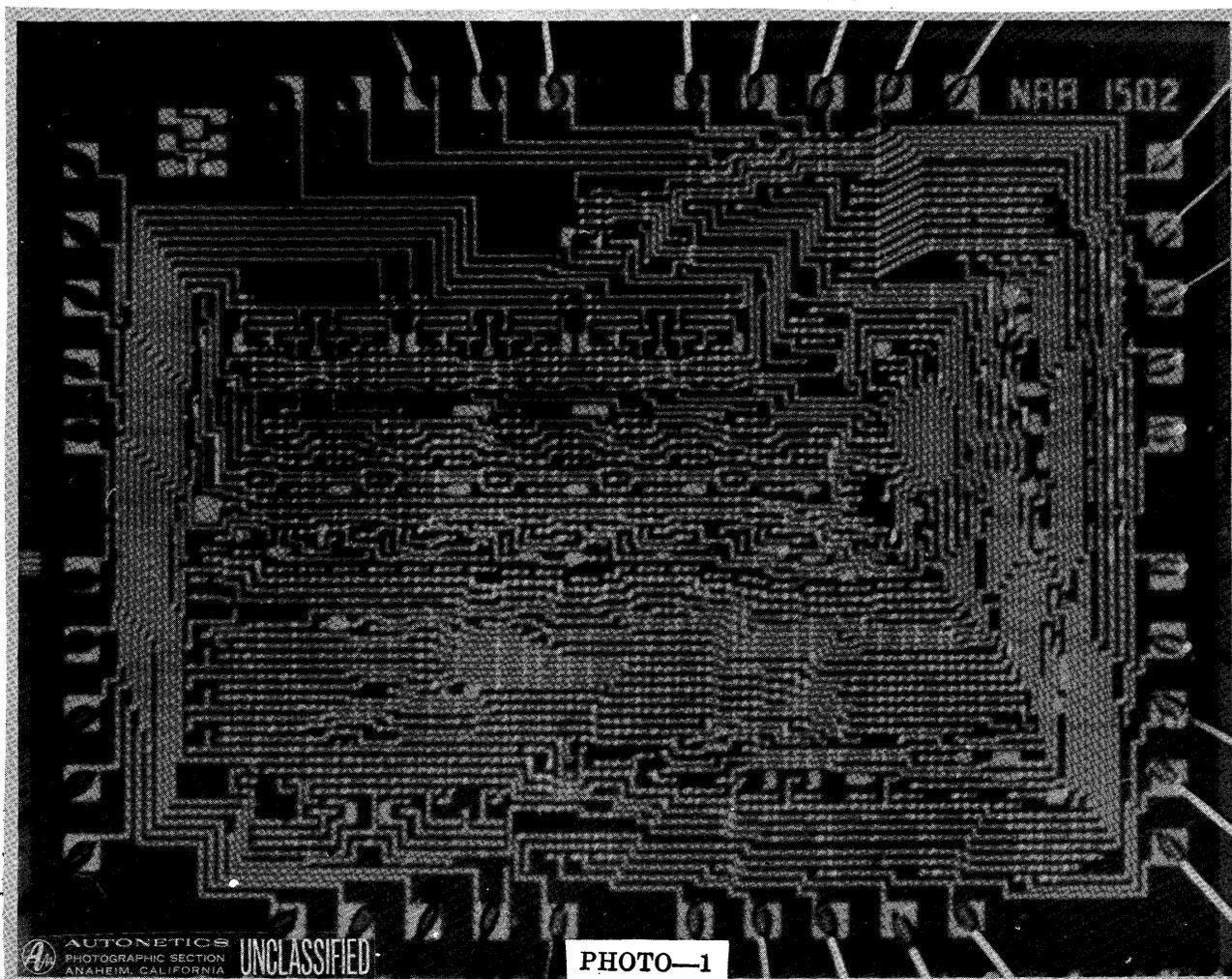
and three index registers. Four 1502 LSA's are used to mechanize the 24-bit accumulator. Four more 1502 LSA's mechanize the 24-bit lower accumulator. Four 1500 LSA's mechanize the 24-bit buffer register. Four 1503 LSA's mechanize a 16-bit program counter and three 16-bit index registers. One each of the 1504, 1505, and 1506 LSA's mechanize the mode control. These 19 LSA's really constitute the arithmetic and control portion of the computer. In addition to these LSA's, the Central Processor Unit (CPU) card also has four 1508 LSA's to mechanize a core memory interface function and one hybrid LSA to mechanize the 4-phase clock.

The 1502 (Photo #1) mechanizes 6 bits of an accumulator and is used in this machine to mechanize both the A and the L registers. It has four control inputs with signals which are exclusive; that is, the signals do not occur simultaneously. The ADD control causes the 1502 to add the number presented on a first set of operand input lines to the number held in the 1502's internal register. The sum is left shifted one binary place as it is inserted into the 1502's internal register. This somewhat peculiar operation was designed to optimize the multiply and divide instructions.

The add and subtract instructions require a compensating right shift which is the function of the SAR (shift A right) control line. In addition to the ADD and SAR control lines a CLR (clear) control line will clear the register to zero, and CPY (copy) control line will cause the register to copy the number presented on a second set of

operand input lines. The latter function was included principally to provide certain transfers of data between registers during multiply and divide operations.

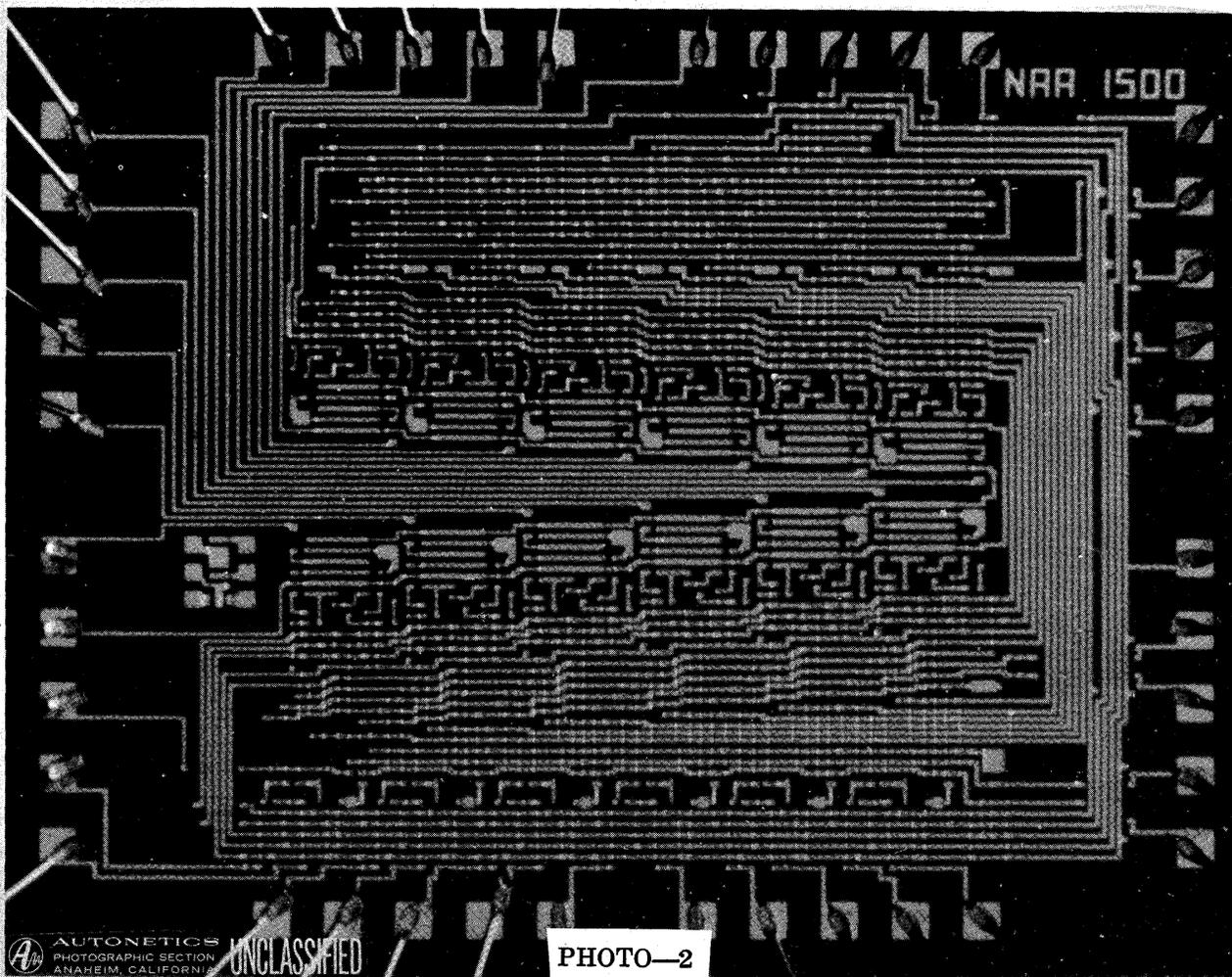
The compensating right shift which is required when executing an add instruction is performed before the left-shifted add, rather than after the left-shifted add. This provides the time required to complement the operand during the execution of a subtract instruction. The actual complementing is done in the 1500 LSA's. The 1502 also mechanizes a "look-ahead" carry scheme. The actual add (left-shifted) is performed in one clock time—that is four levels of gating. In fact, during divide operations the computer develops quotient bits at the rate of one per clock time. The 1502 LSA has 658 MOS-FET's. The die size is 110 mils by 140 mils.



The 1500 LSA, (Photo #2), mechanizes 6 bits of the buffer register. The buffer register copies memory and supplies operands to both the A and the L registers. For instructions where masking is required, the masking is performed as the operand is copied into the buffer register. For instructions where complementing of the operand is required, the complementing is performed between the buffer register and the drivers which supply the operand to the A register or the drivers which

supply the operand to the L register.

In addition to these functions, certain "dummy" operands are supplied to the A and/or L registers at certain times. One example of this is when the L register is made to act like an up/down counter during multiply operations by supplying a "dummy" operand of +1 or -1 unit. The 1500 LSA has 393 MOS-FET's. The die size is 110 mils by 140 mils.



The 1503 LSA (Photo #3) mechanizes four bits of the program counter and four bits of each of the three index registers. The functions performed by the 1503 LSA are tied in very closely to the overall structure of the machine. Its main function is to provide the addressing information required to operate the memory. The program counter takes care of instruction addressing by counting as required and by copying the appropriate address when a transfer instruction is executed. Operand addressing is simply a matter of copying the contents of the address field of the instruction word if no indexing is required. When indexing is required, the contents of the appro-

priate index register is subtracted from the contents of the address field of the instruction word. Each of the three index registers can be loaded, read out, tested for zero and decremented, and loaded with the complement of the contents of the program counter. The last function is used to set up a subroutine linkage.

In addition to these functions, the 1503 LSA provides memory addressing during a bootstrap fill mode and cooperates with input/output LSA's to set up the interrupt address when an interrupt request is honored. The 1503 LSA has 1053 MOS-FET's. The die size is 160 mils by 170 mils.

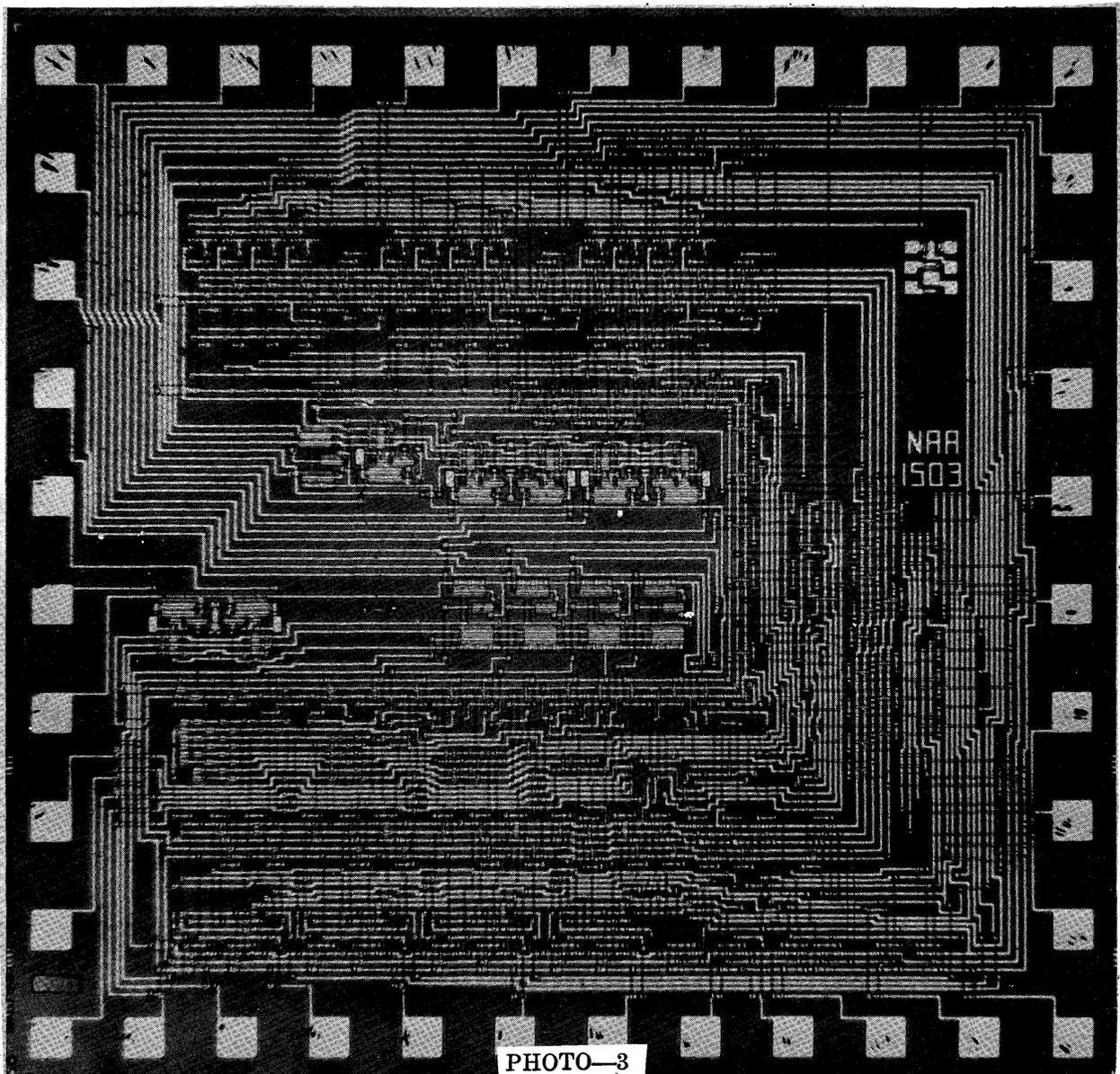


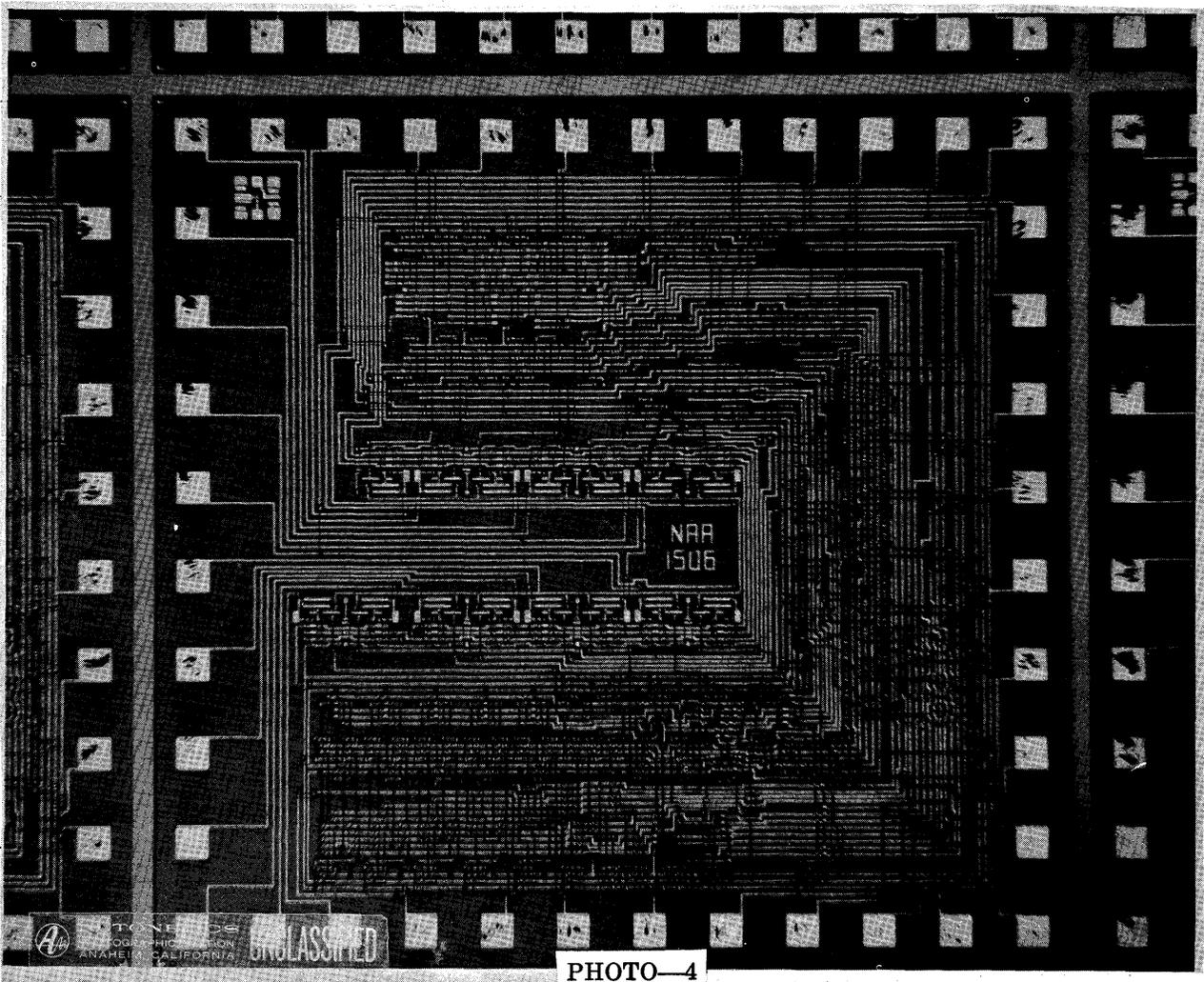
PHOTO-3

The 1506 (Photo #4) mechanizes the basic control signals required for timing. A five stage counter is used to provide the timing for long instructions such as multiply, divide, and the shifts. All other instructions have only a first clock time of execute and a last clock time of execute. Indexed instructions have an indexing clock time inserted before their first clock time of execute.

The 1506 LSA also mechanizes four interrupt channels with programmable lock-out. Simul-

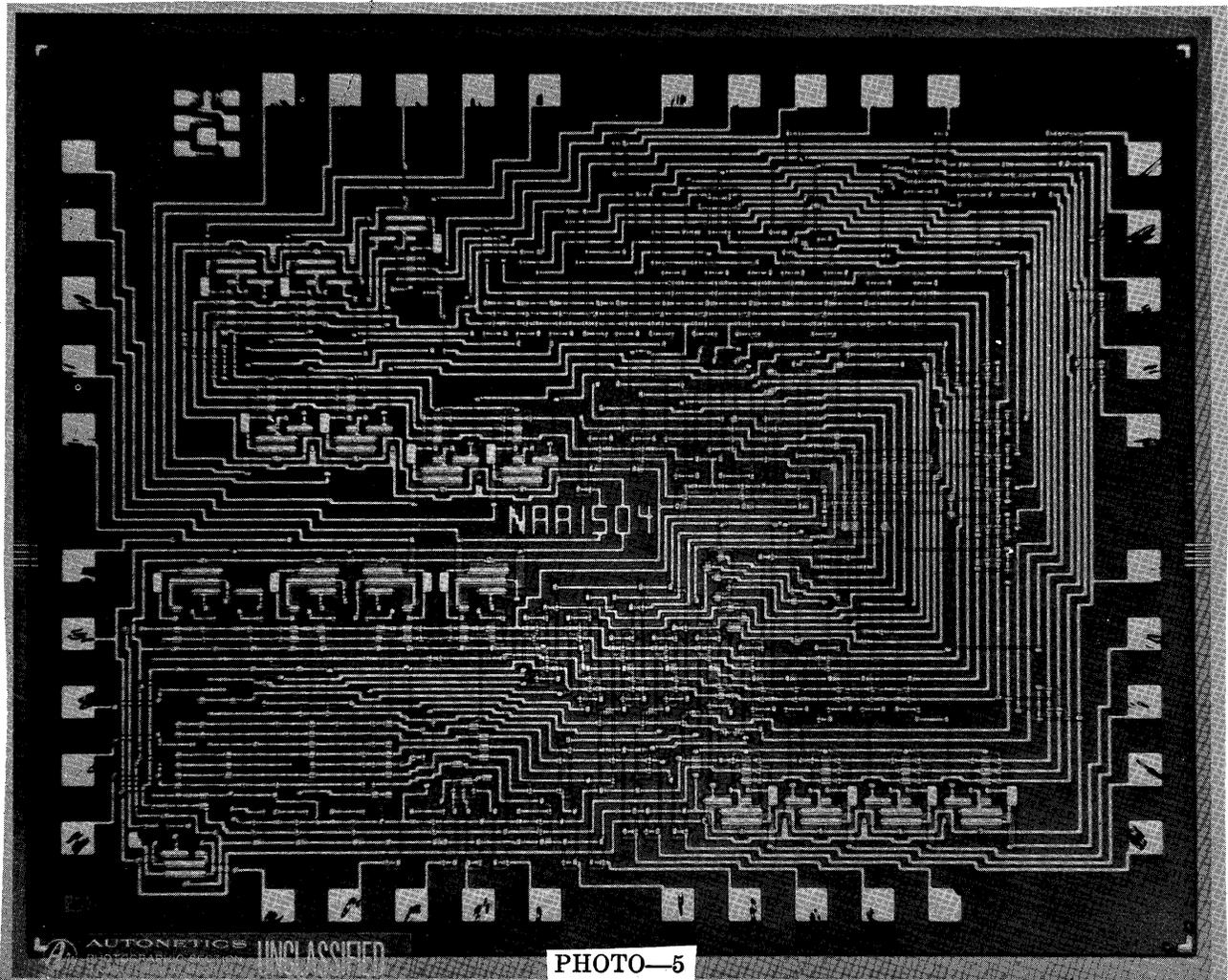
taneous interrupt requests are resolved by using a rotational priority scheme. When an interrupt request is honored, the appropriate channel is enabled and an interrupt which is timed to the current instruction sequence is issued.

The 1506 LSA also mechanizes a number of miscellaneous control signals. The memory write-select signals are included in this group. The 1506 LSA has 1016 MOS-FET's. The die size is 160 mils by 170 mils.



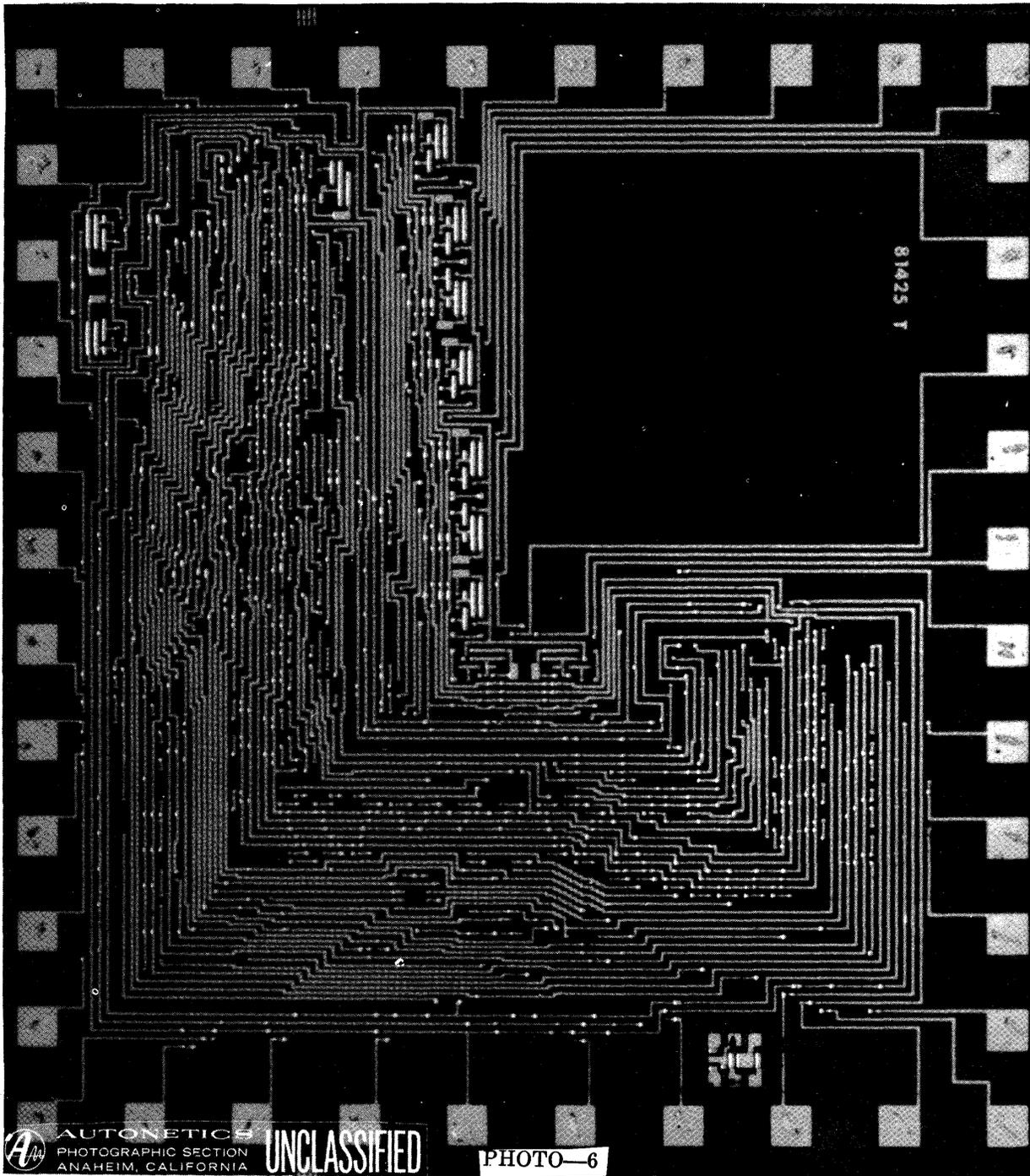
The 1504 LSA (Photo #5) generates some of the basic mode control signals related to indexing, writing into memory, and executing transfer instructions. In addition, it generates some control

signals related to the execution of arithmetic instructions. The 1504 LSA has 614 MOS-FET's. The die size is 110 mils by 140 mils.



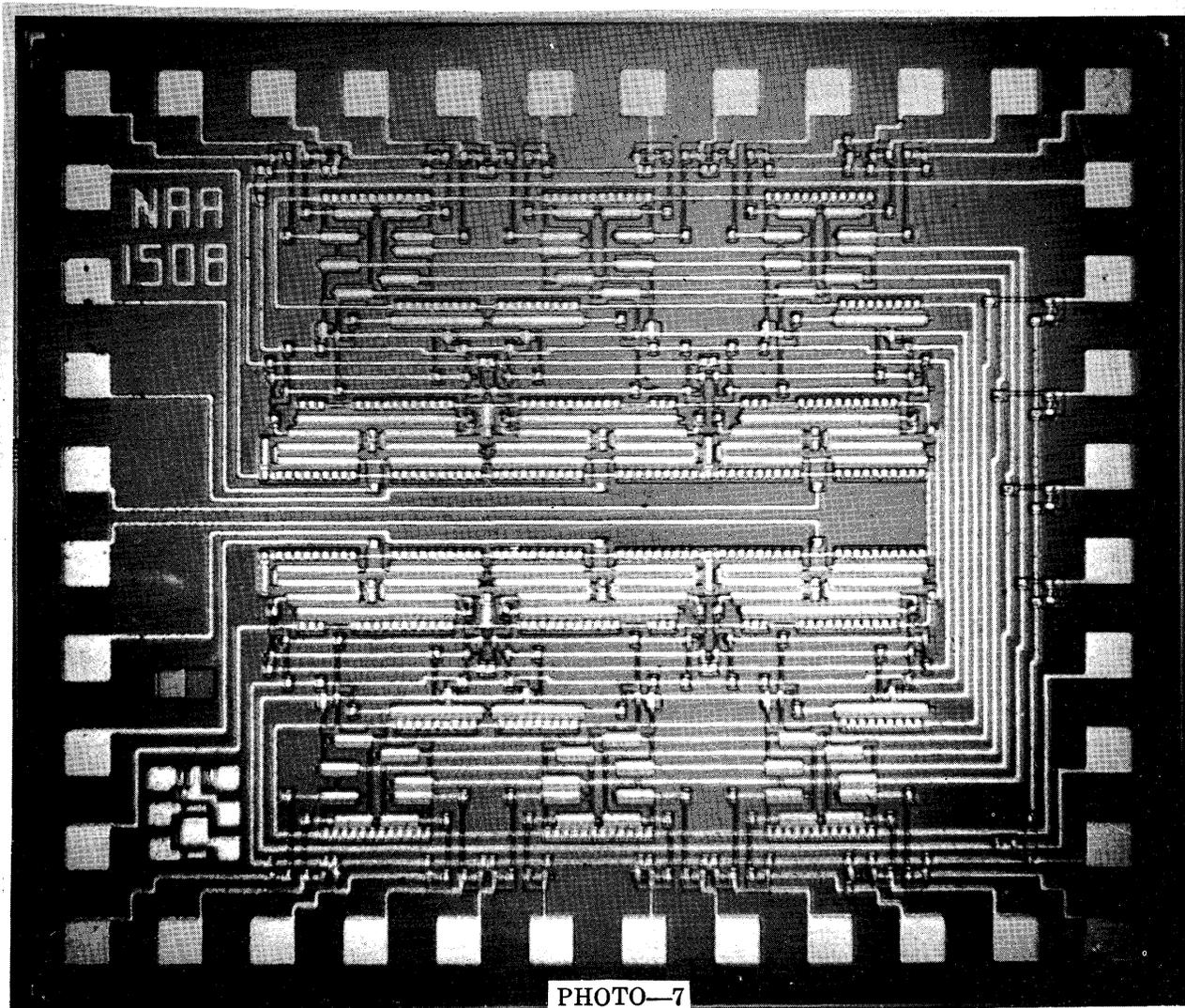
The 1505 LSA (Photo #6) generates most of the control signals related to the execution of arithmetic and shift type instructions. It also generates the low order carry data required for arithmetic operations in the A and L registers.

In addition, it processes the high and low order data bits of the A and L registers for arithmetic and shift type instructions. The 1505 LSA has 838 MOS-FET's. The die size is 160 mils by 170 mils.



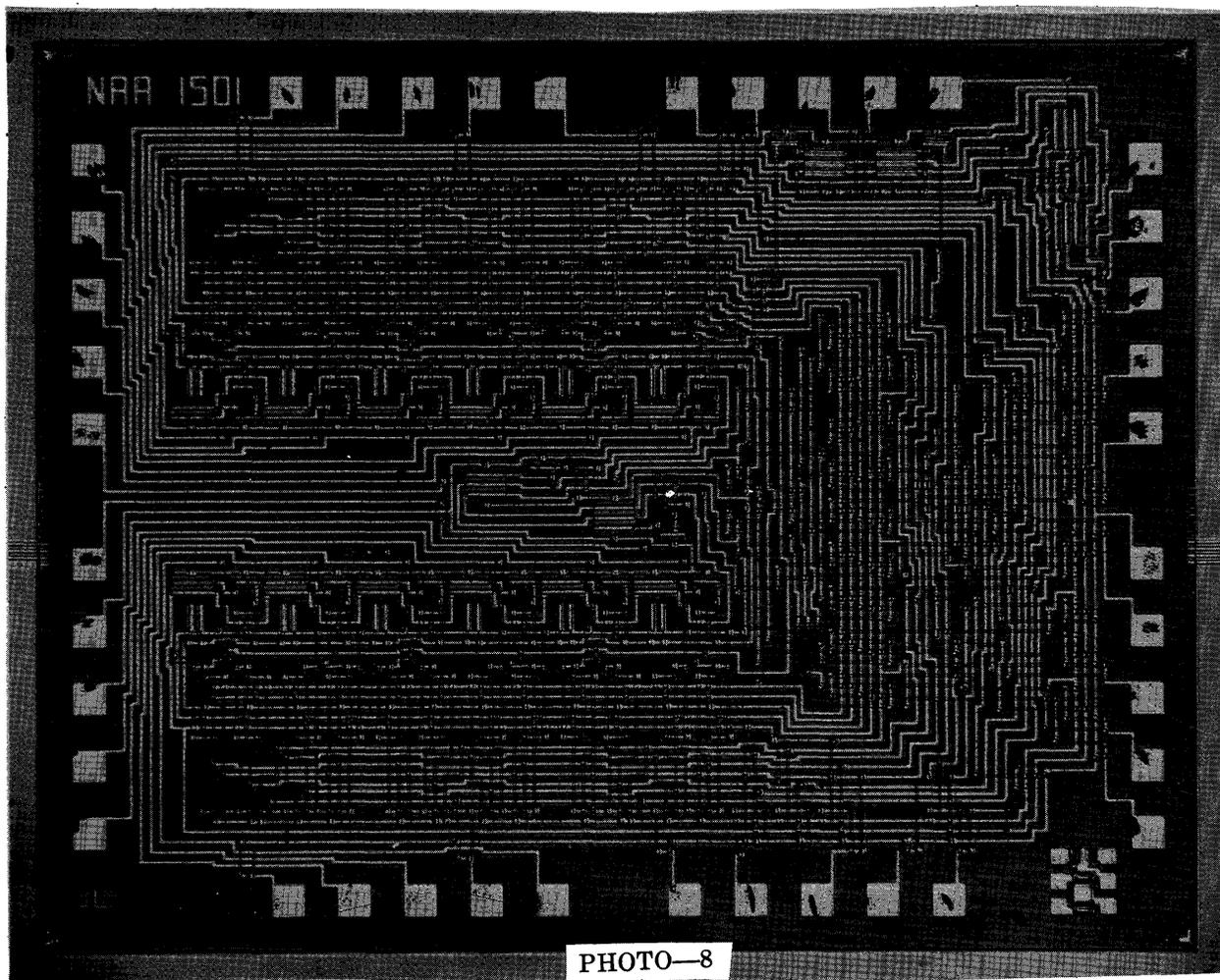
The 1508 LSA (Photo #7) mechanizes six bit positions of a core memory interface. The circuits employed are considerably different from the 4-phase circuits used in the other LSA's. The 1508 LSA performs a selection of one of four data sources. A sample and hold function is then performed to demodulate the 4-phase type signal. A

level shift function is then performed to make the signal compatible with the current bi-polar levels. Finally, the 1508 LSA provides the drive required by the bi-polar system and at the same time provides the capability for inverting the output. The 1508 LSA has 142 MOS-FET's. The die size is 88 mils by 104 mils.



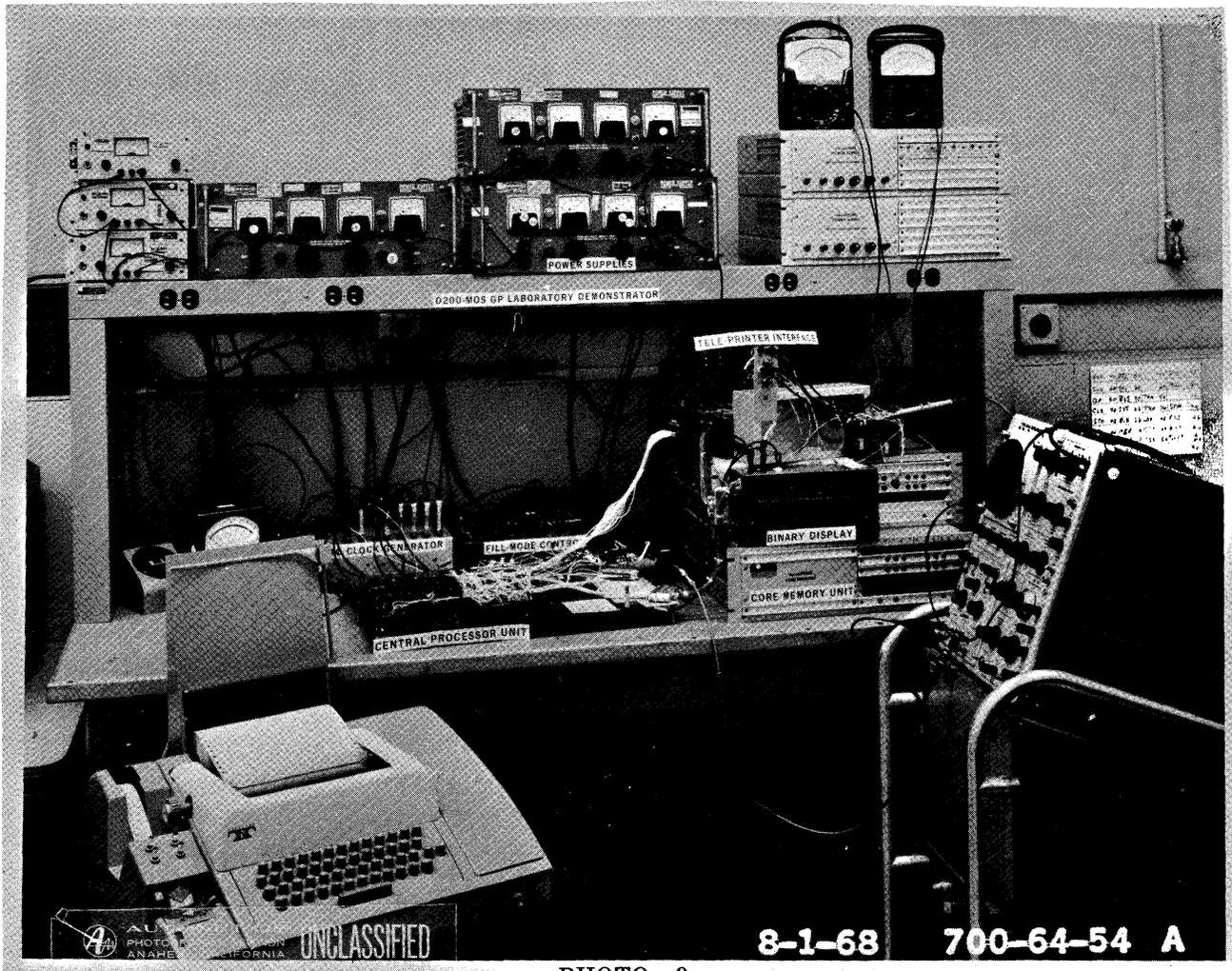
Currently, not much has been done in the input/output area, however, one LSA has been developed specifically for the input area. In particular, two 1501 LSA's (Photo #8) mechanize a buffered input channel. This circuit was included with the development of the CPU, since it was required to

load programs and data into the memory. The 1501 LSA has 732 MOS-FET's. The die size is 110 mils by 140 mils. No specific output circuits have been developed, however, a few existing circuit types have been successfully applied to satisfy current output requirements.



The breadboard computer (Photo #9) is small, and, like most breadboards, it is a bit of a hodge-podge. Most of the bulk is made up of lab power supplies, commercial memories, and miscellaneous

boxes. The central processor, together with one input channel, consists of one large board with interconnected LSA's.

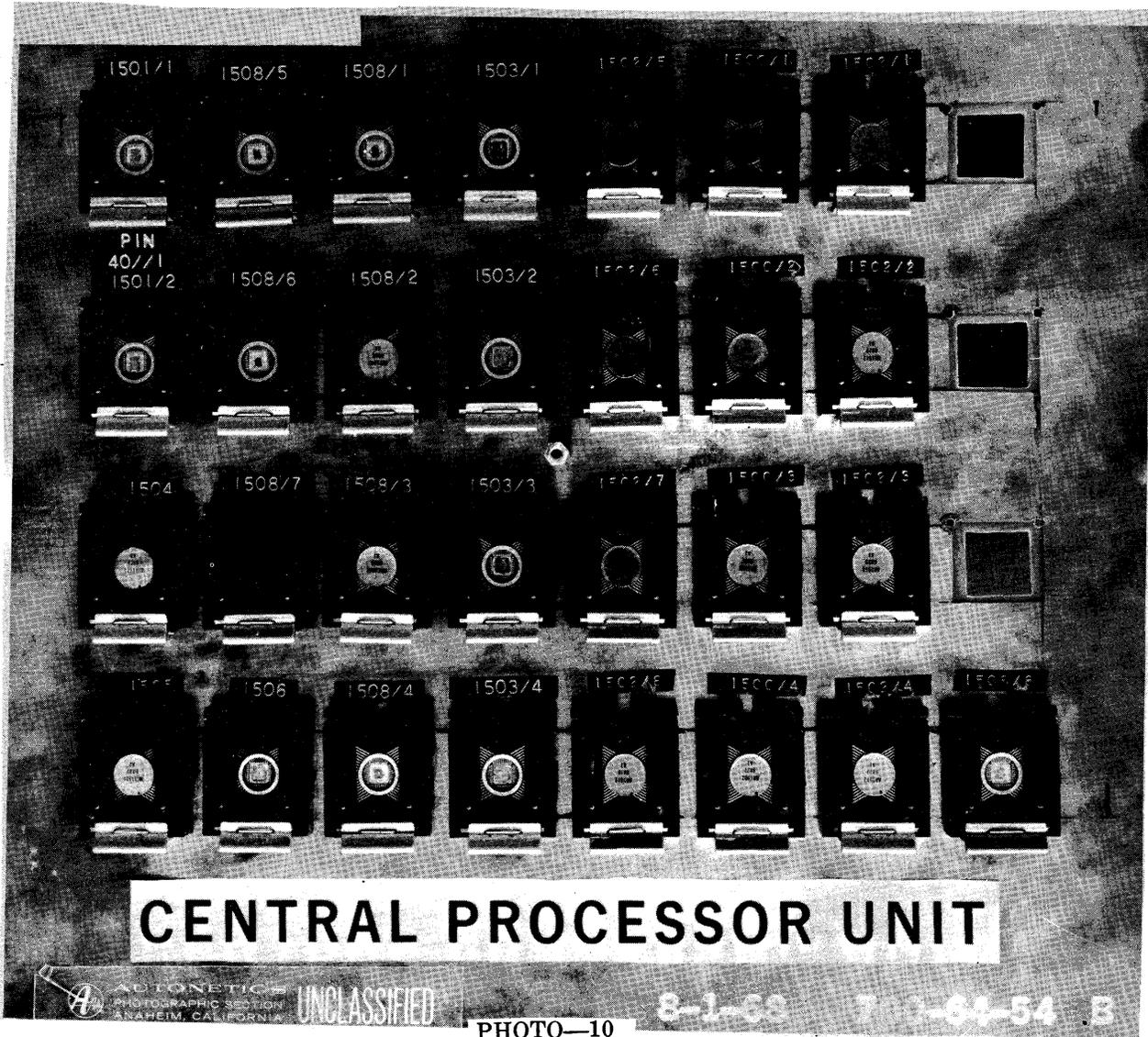


PHOTO—9

The LSA's are clamped into holders (Photo #10).

puter will be packaged for cockpit mounting in its initial application.

A mock-up (Photo #11) shows how the com-



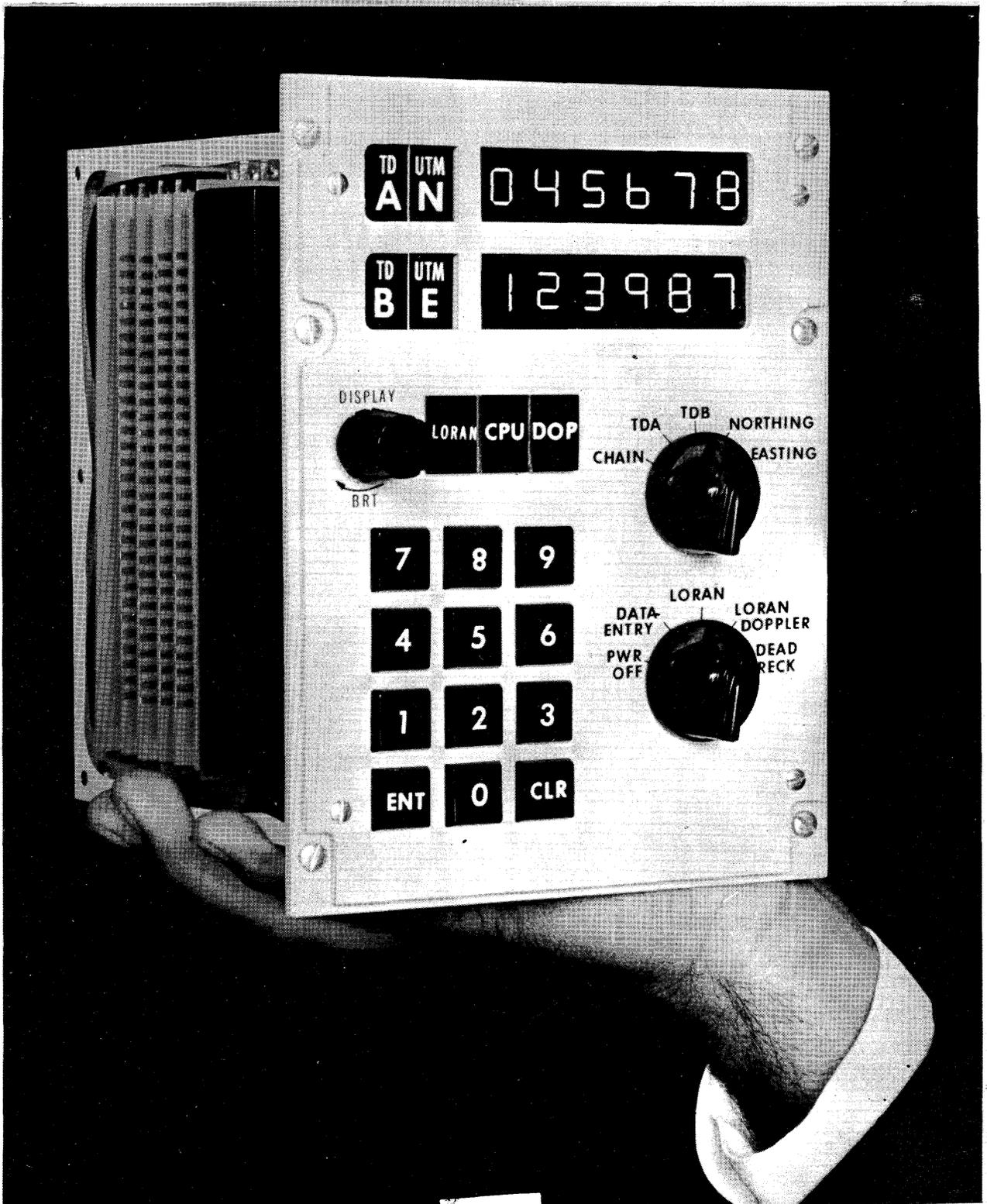


Photo #11

