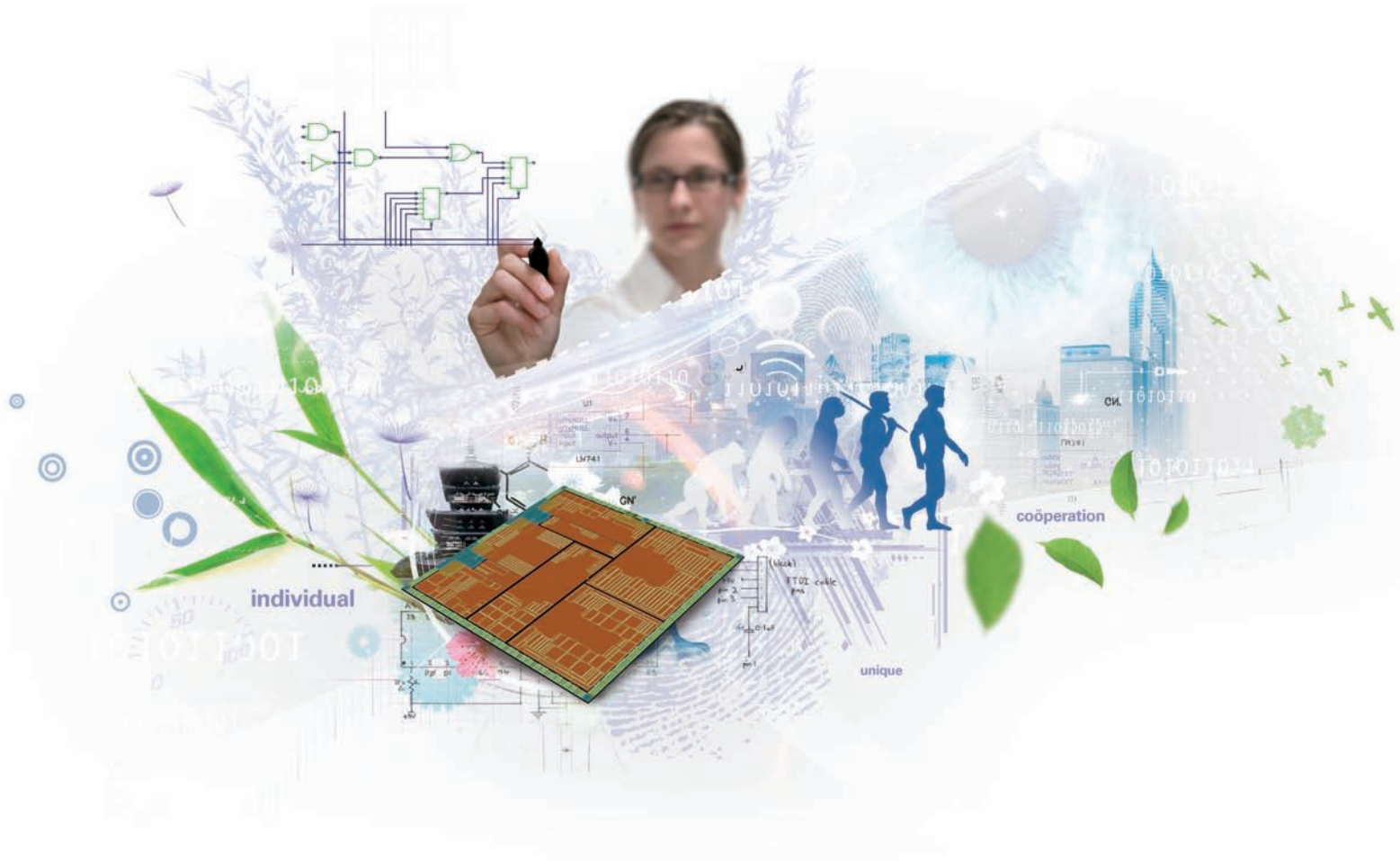# ASIC
Product Overview

IP Macro Blocks

CPU Cores

- Renesas Electronics: V850E family
- ARM: ARM7TDMI-STM
  ARM966E-STM, ARM946E-STM, ARM926EJ-STM, ARM946E-S Supermacro,
  ARM1136J(F)-S™, ARM1156T2(F)-S™, ARM11 MP Core,
  ARM Cortex™ family (M0, M3, R4, R4F, A5, A8, A9)
- MIPS Technologies: Renesas Vr compliant cores, 4KEc™, 24KEm™, 24KEc™, 24KEf™, and 74Kf™
- x86 compliant: V30MZ

System Integration Cores

- SRAM, muliported SRAM
- ROM
- UART, Timer, Interrupt Contoller, I²C, PWM, SSI, SPI, etc.
- Memory controller (DDR-SDRAM, SDRAM, SRAM, ROM, Flash)
- DMA controller, LCD controller
- PCI, PCI-X, PCI-Express
- AMBA™ bus architecture

Multimedia Cores

- IEEE1394-a LINK layer and PHY
- USB1.1, USB2.0
- JPEG
- MPEG
- Cryptographic cores

Networking Cores

- High-speed serial interfaces and SerDes cores
- From 120 Mbps up to 6.4 Gbps
- Various interface options: LVDS, LVDSS, pCML, pECL
- XAUI, 1G/10G Ethernet, FibreChannel, Serial-ATA, sRIO
- SPI 4.2, POS L3
- 10/100 M Ethernet MAC and PHY
- 10/100/1000 M Ethernet MAC
- 8B/10B coder/decoder
- UTOPIA interface
- CAN
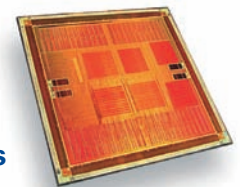
Technology Specific Cores

- A/D converter, D/A converter
- Analogue PLLs
- Embedded DRAM, CMOS-compatible

ASIC Technology Overview

Gate Array ASICs

- Very low-cost technology – ideally suited for cost-saving FPGA replacements
- Simple and fast design flow

*Product	Gate Length [μm] (drawn)	Core Supply Voltage (Options) [V]	Interface Voltage Options [V]	Metal Layers [# of Layers] (Options)	Max. Capacity [Raw Gates*1]
CMOS-N5	0.5	5/3.3	5/3.3	2	123 K
CMOS-9HD	0.35	3.3	5/3.3	3/4	2.5 M
EA-9HD	0.35	3.3	5/3.3	3/4	2.5 M*1
CMOS-12M	0.13	1.5	1.5/2.5/3.3	5/6	4 M*2

*1 Offers the usage of high-density, cell-based IC type SRAM
*2 plus up to 2.7 Mbit embedded SRAM

Cell-based IC (Standard Cell ASICs)

- Highest performance/extremely low power for highest complexity designs
- Optimum silicon efficiency
- Rich IP portfolio

Product	Node Length (acc. to ITRS)	Gate Length [μm] (drawn)	Core Supply Voltage [V]	Max. Capacity [Raw Gates]
CB-12	150 nm	0.13	1.5	32 M
CB-130	130 nm	0.095	1.2	52 M
CB-90	90 nm	0.065	1.0	90 M
CB-55	55 nm	0.050	1.0/1.2	200 M
CB-40	10 nm	0.040	1.0/1.1	400 M

Customizable Microcontrollers

- High performances and High flexibility
- Very simple and fast development
- Low unit price

Product	CPU	Performance	Node length [μm]	Core Supply Voltage [V]	Max capacitiy [K Gates]
SoC Lite+	ARM7TDMI-S	133 MHz	0.25	2.5	250/440
PfESiP EP-1	V850E2S	430 Mips (@200 MHz)	150	1.5	240
PfESiP EP-3	V850E2M	600 Mips (@400 MHz)	90	1.0	600

Subsystems

|	
SoC Lite+	SDRAM controller, 10/100 Ethernet MAC, UART
PfESiP EP-1	Memory controller, USB2.0 H&F, UARTs, A/D Converter
PfESiP EP-3	Memory controller, USB2.0 HS H&F, UARTs, A/D & D/A Converters, CAN, Ethernet MAC

ASIC Packaging Solutions

QFP (Quad Flat Pack)

- Well-established, general purpose packages
- 44 to 376 pins
- 0.4 mm to 1mm pin pitch
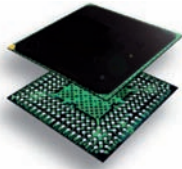- 1 or 2.7 mm package height

FPBGA (Fine Pitch Ball Grid Array)

- Small-footprint, low-height and low-weight chip-size package
- 48 to 1024 balls
- 0.4 to 1 mm ball pitches available
- 4.38 x 4.38 mm to 19 x 19 mm body sizes
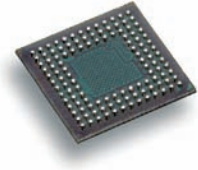
PBGA (Plastic Ball Grid Array)

- High-ball count, low-cost BGA package
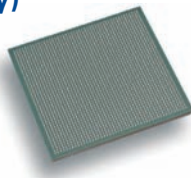- 225 to 672 balls
- 1.27 mm ball pitch

QFN (Quad-Flat Pack)

- Very small footprint
- Cost optimized
- 28 to 52 pins
- 0.5 mm lead pitch

FCBGA (Flip Chip Ball Grid Array)

- Optimum thermal and electrical characteristics
- 600 to 3000 balls
- 1 or 1.27 mm ball pitch

MCP (Multi Chip Package)/SIP (System In Package)

- Multiple chips/dies in one single package
- For cost/area balancing

ASIC Design Implementation

Design Services

Designing an ASIC together with Renesas Electronics offers you a broad range of services all the way from RTL hand-over to GDSII generation. Take advantage of the knowledge of our local European experts. We offer rapid design flow services of the highest quality, thus ensuring that your end product is ready for the market on time.

Highest Quality & Signal Integrity

Renesas has built impressive expertise in multi-million gate designs in deep sub-micron technologies. For the physical implementation, we use silicon proven methodology and "Best in Class" EDA software. Close cooperation with EDA companies allows us to evaluate and introduce the newest design tools up front.

Our comprehensive expertise in key areas of design implementation is based on a long history of designing ASICs. All known deep sub-micron effects are identified, analyzed and fixed in the course of the highly sophisticated design flow in order to provide best possible signal integrity. The European Technology Centre (ETC) supports both established and advanced technologies.

All our customers know they can rely on Renesas expertise and implementation schedules. The sophisticated software from Renesas and third parties runs on powerful computer farms, controlled by automated scripts adapted to the demands of each design.

Flexible Customer Interface

We offer very flexible data interfaces, including an RTL handover for synthesis by Renesas, a gate-level netlist interface, or previously placed and floorplanned interface data. A local European support team of ASIC specialists provides support with your specific requirements, putting you firmly on the road to success.
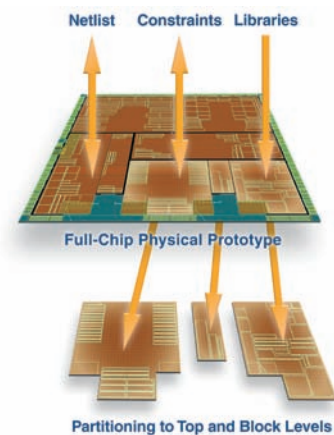
Design Implementation Example

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