Early Digital Computers at Bell Telephone Laboratories

M.M. Irvine

This article relates highlights from the digital computer development activities at Bell Telephone Laboratories for roughly the period 1937–1958. The history begins with a researcher using relays to build a binary adder on his home kitchen table, continues with relay computers designed for military use, and culminates with computers developed after Bell Labs invented the transistor.

It is my intent to convey the flavor of computer development at Bell Telephone Laboratories (Bell Labs) during the 20-some years following Bell Labs' entry into the digital computer era. In doing so, I describe various problems that Bell Labs was addressing and characteristics of the machines developed as solutions. During this period, Bell Labs was AT&T's research and development arm, and Western Electric was AT&T's manufacturing division. Western Electric and AT&T each owned 50 percent of Bell Labs, and AT&T owned 100 percent of Western Electric. The combination of AT&T, Western Electric, Bell Labs, and the telephone companies owned or controlled by AT&T was frequently referred to as the Bell System.

In what follows I will not attempt to distinguish between the terms calculator and computer. For example, one could take the position that the Model I was a calculator and not a computer because of its lack of a stored program and other deficiencies depending on one's exact definition of *computer*. Also, I will not discuss Bell Labs' telephone call-switching machines.

Figure 1. G.R. Stibitz's Model K binary adder. (Courtesy of the American Computer Museum.)

Model I

Bell Labs' entry into the digital computer era occurred in 1937 when a research mathematician, George R. Stibitz, noticed similarities between circuit paths through electromagnetic relays (used by telephone companies for switching telephone calls) and the mathematical binary notation for numbers. To explore this thought over a weekend, Stibitz used some relays to build a binary adder. This adder would give, as output, the binary digits for the sum of two one-digit binary numbers that were input to the device. He called it the Model K, the K referring to his kitchen where he constructed it. Figure 1 shows a replica of the Model K that Stibitz, shown in Figure 2, constructed in 1991 for George Keremedjiev, director of the American Computer Museum. When Stibitz demonstrated the device to his management the following week, they were unimpressed that relays could perform binary arithmetic.

However, in 1938, Stibitz was asked to design an electromechanical relay digital computer that could perform arithmetical calculations using complex numbers. Samuel B. Williams, a telephone system design engineer, was assigned to supervise its engineering and manufacturing. What had happened was that Stibitz's management had become aware that Bell Labs' computational staff was in an overload situation and felt that a Stibitz-designed relay machine could help alleviate the over-

 1058-6180/01/$10.00 © 2001 IEEE

load problem. At that time Bell Labs was using people with commercial mechanical calculators to solve problems, many involving complex numbers. Complex numbers have the form $a + ib$ where a and b are real numbers and i is the square root of minus 1. Complex number calculations were used extensively in designing the many electrical filters that made transcontinental telephony possible at that time.

The machine Stibitz designed was initially known as the Complex Number Calculator (CNC) and later as the Model I. Stibitz frequently referred to it as the Complex Calculator; others at Bell Labs referred to it as the Complex Number Computer. It became fully operational in early 1940 and was in constant use for about nine years.

The Model I used approximately 460 relays. It had three teletype terminals. (A teletype is a kind of typewriter device that was frequently used for sending messages over telephone and telegraph lines.) It had the capability to read and record on punched paper tape. To save computational time, the Model I had two parallel calculating units, which allowed the machine to simultaneously perform calculations on both parts of a complex number.

The Model I was the first digital computer to use multiple terminals. However, service was on a first come, first serve basis and the Model I could work on only the problem from a single terminal at a time. When that problem was finished, the machine immediately switched to the next problem in the queue.

The Model I was the first digital computer to demonstrate use from a remote location. The first occurrence took place at the September 1940 meeting of the American Mathematical Society at Dartmouth College in Hanover, New Hampshire. After Stibitz made his presentation explaining the details of his new machine, audience members were invited to submit problems to the computer via a teletype terminal in the room. This terminal was linked by a telegraph line to the computer, located at Bell Labs in New York City. Both John Mauchly (one of the ENIAC designers) and Norbert Wiener (a pioneer in cybernetics and coiner of the word) spent a great deal of time at the terminal that day testing the Model I's capabilities. It was able to give answers to problems in about a minute.

The total cost of the Model I was $20,000, which at that time was considered an extremely large expenditure (Stibitz called it "an astronomical sum"). Because of this high cost, Stibitz was unsuccessful in convincing his management to fund more advanced features he had designed for his machine.

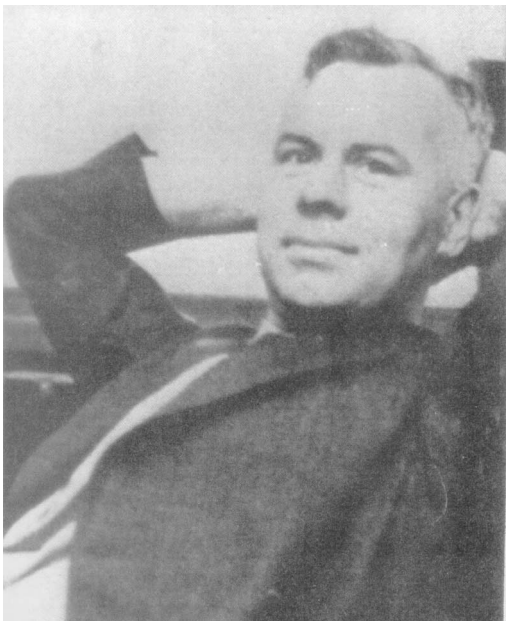

Figure 2. Inventor George R. Stibitz in the early 1940s. (*IEEE Spectrum*, Nov. 1974, © 1974 IEEE.)

Model II

With the advent of World War II, Bell Labs loaned Stibitz to the NDRC (National Defense Research Committee) to conduct studies in support of the war effort. One of the problems he worked on was how to develop a cost-effective method for testing designs for the M-9 analog antiaircraft gun director that Bell Labs was developing. A gun director used positional information, usually obtained from optical or radar sources, to compute the future position of an attacking aircraft. This information was then used to set the timing fuse of the shell and to point the gun to the proper aiming position for firing so that the shell exploded on or in close proximity to the aircraft. See

Editor's Note

Three prior articles focused on the early efforts at Bell Laboratories:

D. La Porte and G.R. Stibitz, "Eloge: E.G. Andrews, 1898–1980," *Annals of the History of Computing*, vol. 4, no. 1, Jan. 1982, pp. 4–5.

E.G. Andrews and H.W. Bode, "Use of the Relay Digital Calculator," *Annals of the History of Computing*, vol. 4, no. 1, Jan. 1982, pp. 5–13.

E.G. Andrews, "Telephone Switching and the Early Bell Laboratories Computers," *Annals of the History of Computing*, vol. 4, no. 1, Jan. 1982, pp. 13–19.

The Gypsy Computer

The computer used to conduct simulated flights of the B-68 under control of the XMH-3 TRADIC (transistorized airborne digital computer), although analog in nature, was a trailblazing machine, nicknamed Gypsy.

"Gypsy's" story began in 1940 when D.B. Parkinson and C.A. Lovell invented a pioneering electrical analog computer to be used for controlling antiaircraft guns.[1] It used shaped wire-wound potentiometers and vacuum-tube amplifiers to perform standard arithmetic operations.

This led directly to the development of the M-9 gun director to control the US Army's heavy antiaircraft guns. This is the gun director for which George Stibitz designed the Model II that was used for testing the M-9 during its development. The first production M-9 was delivered to the Army in December 1942. Although it served in many areas, probably its best-known achievement was its performance during the month of August 1944 when 89 of 91 V-1s ("buzz bombs") launched by the enemy from across the channel and aimed at London were shot down over the cliffs of Dover.

The success of the M-9 was such that Bell Labs was asked to develop a similar device for coastal defense guns used to protect US shores from enemy ships. The new task was simpler. Where the M-9 had to deal with high-speed, maneuverable targets in 3D space, the Coast Artillery had to deal with low-speed targets of minimal maneuverability constrained to the surface of the water.

For these reasons, the M-8 gun data computer (as the new device was called) was considerably simpler than the M-9 gun director. At that time it was customary to use the term *director* if the data processing equipment was in close proximity to the optical or radar source of data, and to use the term *computer* if the trajectory data came from a remote location as was the case with the M-8 data computer.

Quoting Fagan,[1] page 158 (emphasis in the following quote is mine):

> After the war, the technology developed for fire control, using the DC signal methods of the M-9 director and the M-8 computer, was applied, under the direction of Emory Lakatos, to the design of a very useful general-purpose analog computer (GPAC), nicknamed the "Gypsy," which was extensively used for over ten years for the solution of problems in many scientific and engineering areas. *This was the basis for the development of the analog computer industry.* The first Gypsy was built largely from unused components for M-8 computers leftover from the wartime development.

Gypsy was placed into service in 1949 and proved to be so useful that another was built a few years later. The two machines could be used separately for small problems or connected together to work on larger problems. These machines were donated to the Polytechnic Institute of Brooklyn in 1960 when their workload was assumed by a more modern, commercial analog computer. Figure A shows Gypsy.[2,3]

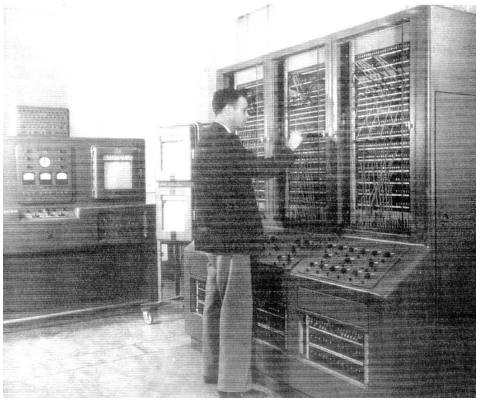

Figure A. Richard W. Hamming setting up a problem on Gypsy. (*A History of Eng. & Science in the Bell System Comm. Sciences* [*1925-1980*], courtesy AT&T Archives.)

References

1. M.D. Fagen, ed., *A History of Engineering & Science in the Bell System—National Service in War and Peace* (*1925-1975*), Bell Telephone Laboratories, New York, 1979.
2. A.A. Currie, "The General Purpose Analog Computer," *Bell Laboratories Record*, New York, Mar. 1951, pp. 101-108.
3. E. Lakatos, "Problem Solving with the Analog Computer," *Bell Laboratories Record*, New York,

the sidebar, "The Gypsy Computer," for additional M-9 information.

During the development process, Bell Labs found itself requiring test equipment that did not exist. This equipment would move the input knobs of the M-9, exactly as a person would move them, in tracking an attacking aircraft and check to determine if the signals issued by the M-9 would keep the gun accurately aimed.

Stibitz designed a dynamic tester for the M-

9 gun director. Using appropriate digital input data supplied by paper tape, the tester could simulate the aircraft's path in a form suitable for input for the M-9. Bell Labs was given the responsibility by NDRC to do the detailed design and to build the simulator. It used the same relay technology as the Model I and had approximately the same number of relays. The Model II took its program instructions and input data from punched paper tape. It had a repertoire of 31 instructions, and the output was a punched paper tape with trajectory data in a form suitable for input to the gun directors. When not being used to develop target data, the machine helped researchers solve a variety of other problems.

The simulator was installed at Bell Labs in New York City in September 1943. Stibitz had named it the Relay Interpolator, although that name was soon changed to the Model II. Near the war's end, Bell Labs moved the simulator to the Naval Research Laboratories in Washington, D.C., where it continued on active duty until 1961.

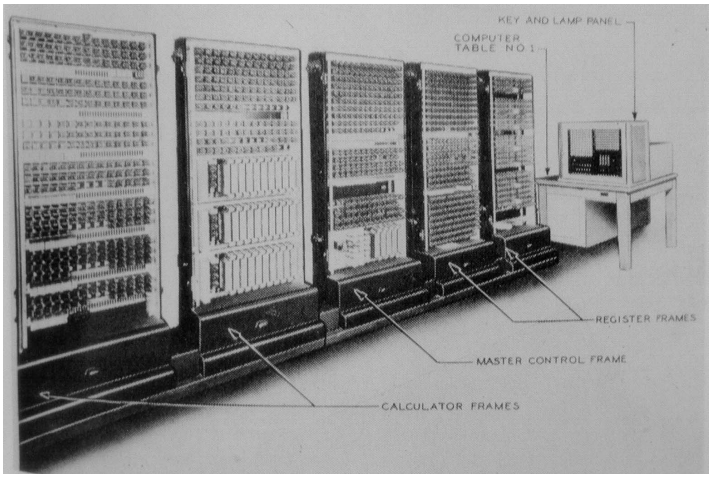

Figure 3. The Model III computer. ("A Review of the Bell Laboratories' Digital Computer Developments," ***Proc. Joint AIEE-IRE Computer Conf.,*** **© 1952 IEEE.)**

Model III

Because of the Model II's modest capabilities, Stibitz was unable to include all the calculations he wanted to incorporate into his simulator. Consequently, even before the Model II became operational, Stibitz had proposed a more sophisticated and powerful computer. This new computer also addressed the computationally intensive task of testing antiaircraft equipment. With its additional capability, it could simulate a shell's ballistic trajectory after the gun director had supplied the fusing and aiming information and after the gun was fired. Comparing the exploding shell's simulated detonation position with the plane's simulated position at the time of the detonation gave the miss distance and thus the effectiveness of the shot.

The Model III, shown in Figure 3, was commonly referred to as the Ballistic Computer. It used approximately 1,400 relays, three times as many as the Model I and II. It was installed at Camp Davis, North Carolina, in June 1944 and in 1948 moved to Fort Bliss, Texas, where it was upgraded with additional registers and served an additional 10 years working on various problems.

Model IV

Bell Labs built a Model IV for US Naval Ordnance. Much like the Model III, it was built to perform the same kinds of tasks. Additional circuits were added to account for the guns being mounted on the deck of a rolling, pitching ship. It was delivered to the Naval Research Laboratories in Washington, D.C., in 1945 and remained in service until 1961. The Navy referred to this machine as the Error Detector Mark 22.

Model V

The government's need for additional computer power continued. To help address this need, Bell Labs was awarded a contract in 1944 to use this relay technology to produce two new machines that would be markedly more powerful than their ancestors.

These new, more powerful machines were both known as the Model V. Although the design allowed for a total of six arithmetic units, these two machines were each equipped with only two units. The Model V could be divided into two independent machines to work on two different problems simultaneously or combined into one machine to handle larger problems. It was the first of the Stibitz machines to use the floating decimal point. Each of the Model Vs had about 9,000 relays, approximately 55 pieces of teletype equipment, and weighed about 10 tons. The Model I was built for a cost of $20,000; in contrast, each Model V cost about $500,000.

The Model V could be programmed to solve a wide variety of mathematical problems. These included solving problems in probability theory, solving systems of simultaneous equations, solving both ordinary and partial differential equations, performing integration, and simulating physical systems.

Stibitz and others often described the

Table 1. Design characteristics of Models I to VI, adapted and modified from work by Andrews.[9]

	Complex Number Calculator					
Design features	**Model I**	**Model II**	**Model III***	**Model IV**	**Model V**	**Model VI**
Number of built-in routines	2	0	0	0	4	200
Decimal point: fixed or floating	Fix	Fix	Fix	Fix	Float	Float
Multiplication	Yes	**	Yes	Yes	Yes	Yes
Division	Yes	No	Yes	Yes	Yes	Yes
Square root	No	No	No	No	Yes	Yes
Special trig features	No	No	***	***	Yes	No
Special log features	No	No	No	No	Yes	No
Self-checking (%)	No	90	100	99	100	100
Number of relays	460	490	1,400	1,425	9,000	4,600
Pieces of teletype equipment	4	5	7	7	55	16
Digits per number	8	2 to 5	1 to 6	1 to 6	1 to 7	3,6,10
Multiplication time in seconds per five-digit number	N/A	N/A	1	1	0.8	0.8
Number of problem stations	3	1	1	1	3 and 4	2
Arranged for unattended	No	No	Yes	Yes	Yes	Yes

* *This column applies to the Model III before its modification in 1949.*
** *With multiplier specified in program.*
*** *Very limited application.*

machines' useful work by estimating how many people, while using desk calculators, would be necessary to perform the equivalent amount of work. Stibitz estimated that the Model III did the work of 25–40 people, depending on the type of problem being solved, and that the Model V did the work of 225 people.

The first Model V was delivered to the National Advisory Committee for Aeronautics at Langley Field, Virginia, in 1946; the second one was delivered to the Ballistic Research Laboratories, Aberdeen, Maryland, in 1947. The Aberdeen machine was later sent to an army site at Fort Bliss, Texas, and after a period of use was donated to the University of Arizona.

In 1958 the first Model V was donated to Texas Technological College. While on its way to Texas, however, the truck transporting it tipped over, critically damaging the machine. The damaged Model V served out the rest of its life as spare parts for its twin at the University of Arizona.

Model VI

Bell Labs built one last machine of this series for its own use. Named the Model VI, it was a simplified version of the Model V. It had only one arithmetic unit and about half the number of relays as its predecessor (4,600 versus 9,000). Additional features included the capability to handle 10-digit numbers in contrast to the Model V's seven-digit capability.

The Model VI was installed at Bell Labs in 1950 where researchers used it to solve a large variety of Bell Labs' research and development problems. It was the first digital computer I ever saw in operation. In 1956, Bell Labs donated it to the Polytechnic Institute of Brooklyn where it was used for research and instructional purposes. In March 1960, it was given to the Bihar Institute of Technology in India where, I was told, it was India's first digital computer.

These relay machines had high reliability and high accuracy, and they were able to run for long periods of time unattended. During their entire working life, only two errors were ever reported from all three Model V and Model VI machines as a result of machine failure.

Stibitz[1] has given a delightful account of his involvement with these computers, and Andrews[2] has published a review of them. An excellent account of the machines' design and use can be found in Williams's book.[3] For still more details, see the literature for specific information on the respective models.[4-8]

Table 1 lists some of the machines' characteristics. Figure 4 shows the Model VI, and Figure 5 shows one of the remote operating stations.

The AMA computer

The success of these early relay machines encouraged Bell Labs to apply the same technology to an area vital to AT&T—the billing of telephone customers for calls made.

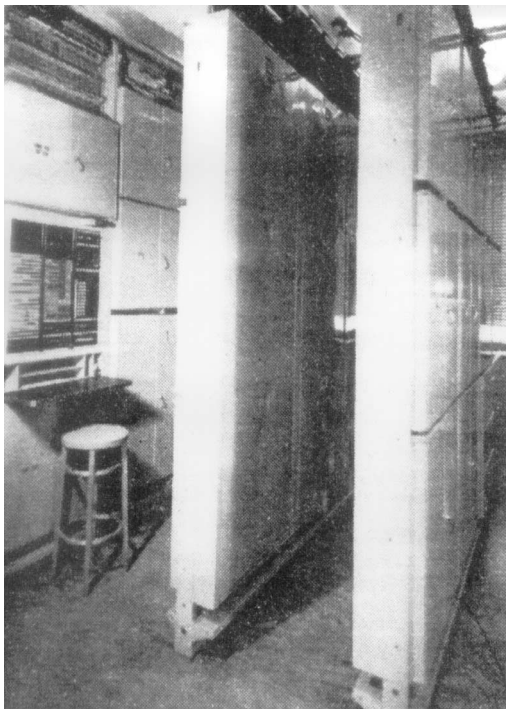

Figure 4. Frame equipment of the Model VI computer. ("A Review of the Bell Laboratories' Digital Computer Developments," ***Proc. Joint AIEE-IRE Computer Conf.,*** **© 1952 IEEE.)**

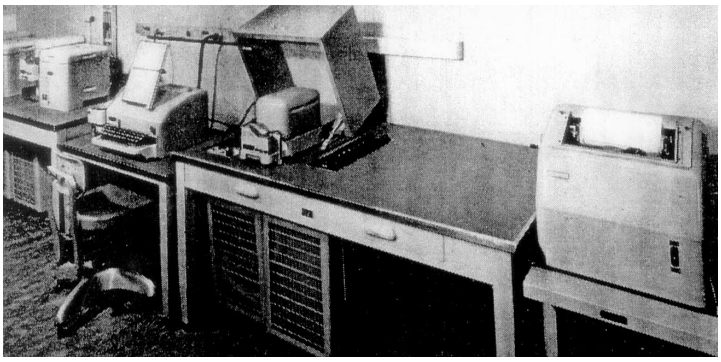

Figure 5. Remote operating station and storage input tables for the Model VI, which was originally installed at the Murray Hill, New Jersey, laboratory in 1949. ("Bell Laboratories Digital Computers," ***Bell Laboratories Record,*** **Mar. 1957, courtesy AT&T Archives.)**

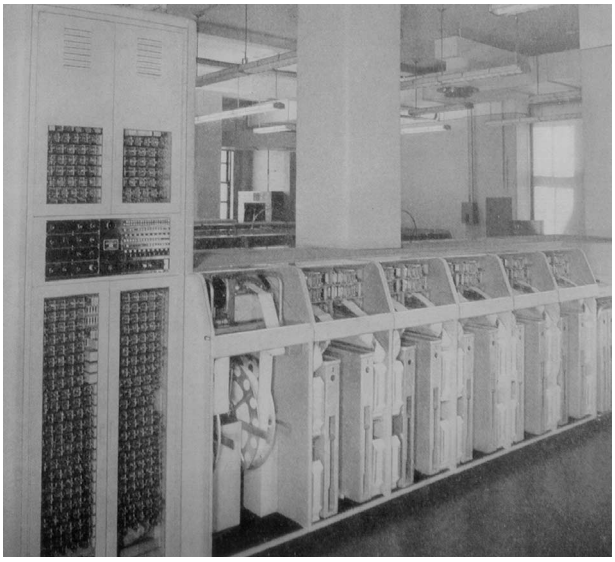

Figure 6. The assembler integrated a paper tape reader, relay logic, and tape perforators for processing telephone call data. ("The AMA Assembler," ***Bell Laboratories Record,*** **May 1952, courtesy AT&T Archives.)**

In this system, a data recorder—located at the switching machine handling the calls—captured the necessary data. The recorder used oil-impregnated, three-inch-wide, perforated paper tape. There was space for 28 holes across the tape allowing recording of six digits, each representing a single item. Adjacent rows were about one-tenth of an inch apart. Four or six rows were required per call depending on the type of call (local, long distance, and so on).[10]

One recorder would handle 100 telephone lines, and data for a particular call would be interspersed with data from other calls. Data recorded on the tapes included calling and called number, start and stop times of the call, the call type, and so forth. These tapes were periodically shipped, usually daily, to an automatic message accounting center for processing. At the AMA center, the tapes were read into an elaborate perforated tape operation called assembly. The collection of equipment doing this task was known as the assembler, shown in Figure 6. It consisted of a paper tape reader, relay logic, and 10 tape perforators.

The assembly operation was a two-stage tape sorting process that resulted in all the data for a particular call appearing on physically adjacent rows of the tape. This assembly operation also arranged the call data into a format suitable for input into the AMA computer. Drew gives a detailed account of this assembly operation and equipment.[11]

The AMA computer was a relay digital computer that performed the arithmetical operations necessary for customer billing. The computer's output consisted of perforated paper tapes that were used as input to four more stages of paper tape sorting (to put the call data in numerical order by phone number). The paper tapes resulting from this operation were used as input to a printer that printed the call data in a form readable by the billing clerks who prepared the final bill. This somewhat

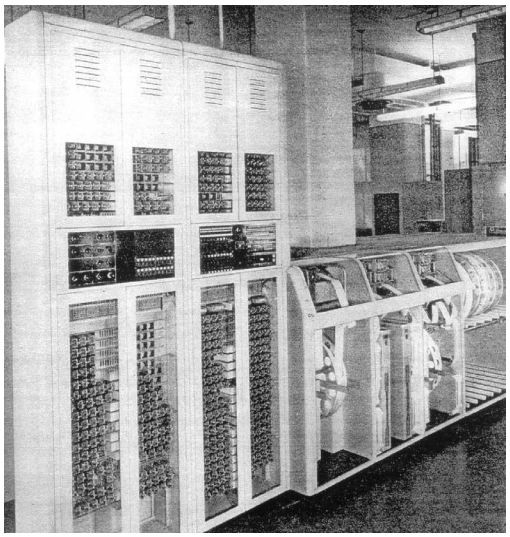

Figure 7. The AMA computer, showing four cabinets of control equipment, a tape reader, and several of the 14 tape perforators. ("The AMA Computer," *Bell Laboratories Record*, July 1952, courtesy AT&T Archives.)

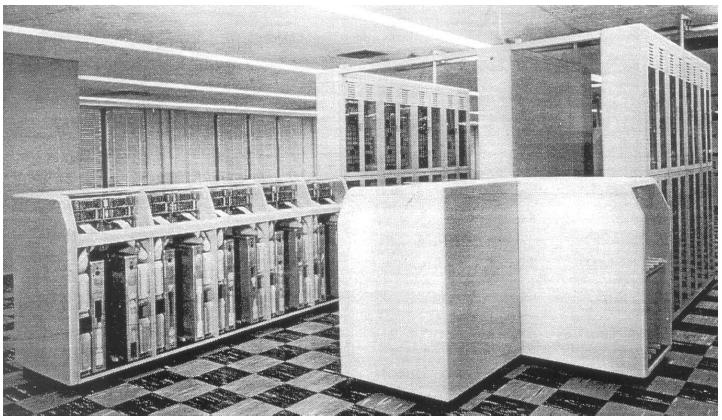

Figure 8. The assembler-computer, which consisted of 11 relay bays, one tape reader, and up to 14 tape perforators. ("The AMA Assembler-Computer," *Bell Laboratories Record*, Oct. 1957, courtesy AT&T Archives.)

cumbersome tape sorting system might seem strange today. However, it was not until the Bell System Data Processing project (more about that later) that Bell Labs decided to computerize the sorting operation.

The AMA computer, shown in Figure 7, consisted of four cabinets of relay equipment with lamps and control panels, a tape reader, and 14 tape perforators.[12]

Although the just-described system may seem overly complex and unwieldy, it worked well. At this time the Bell System had about 25 million customers making nearly 200 million calls per month. These calls had to be billed to the customer, accurately and on time. At the same time, the billing system had to be a low-cost operation to add only a negligible amount to the billable phone call (65 percent of which were 15 cents or less). The first AMA center opened in Philadelphia in 1948.[13]

The AMA assembler-computer

As the demand grew for additional processing capability, engineers studied the just-described system intensely for possible modifications. These studies resulted in the development of the AMA assembler-computer, a new relay computer that performed the tasks of both the earlier tape assembler and AMA computer. One assembler-computer used less floor space and replaced about three of the tape assemblers and AMA computers. This computer consisted of 11 relay bays, one tape reader, and up to 14 AMA tape perforators contained in seven cabinets. Figure 8 shows the assembler-computer.

Storage for the start and stop times of 100 calls was accomplished by means of a memory composed of 1,000 dry-reed relays (a glass-enclosed, hermetically sealed, magnetically actuated contact). An additional 2,300 wire-spring relays were used for the logic and control portions of the machine.

The inventor of this machine was Amos E. Joel Jr., and the invention's patent was the largest one issued in the US up to that time (1960). It contained about 250 claims and drawings.

More than 100 assembler-computers were built. They served chiefly until the late 1960s, when they were largely replaced by commercial computers.[14]

The throwdown machine

In developing the call-switching machines, Bell Labs conducted extensive simulations of proposed designs to determine how well they would perform under various telephone calling patterns and traffic loads. These simulations enabled the design engineers to locate bottlenecks in the system and better optimize their call-switching design. The input to these simulations was various calling patterns and traffic loads.

To test the operation of a new switching machine called the No. 5 crossbar, a manual simulation was run by a team using card files, ledgers, and written records. Dice would be thrown down during the simulation to make random decisions, which led to the following machine's being called the throwdown machine.

In 1949, William Keister, Alistair Ritchie,

and G.R. Frost mechanized this manual simulation by developing the throwdown machine,[15] shown in Figure 9. This was often referred to as the KRF machine after the initials of the developers' last names.

This special-purpose machine could handle all the significant elements of a No. 5 crossbar installation, small or large. Engineers used the data obtained from these simulations to make design modifications to the No. 5 crossbar, which improved traffic throughput and enabled determination of load-handling capacities for various configurations.

The throwdown machine was composed chiefly of telephone relays and rotary stepping switches. It had about 800 relays and 57 switches—47 of the 22-position, 6-circuit type and 10 of the 44-position, 3-circuit type. In addition, there were 60 cords with plugs and 509 jacks. Simulations were run with the aid of four operators. By the mid-1950s, electronic computers were used for these kinds of simulations.

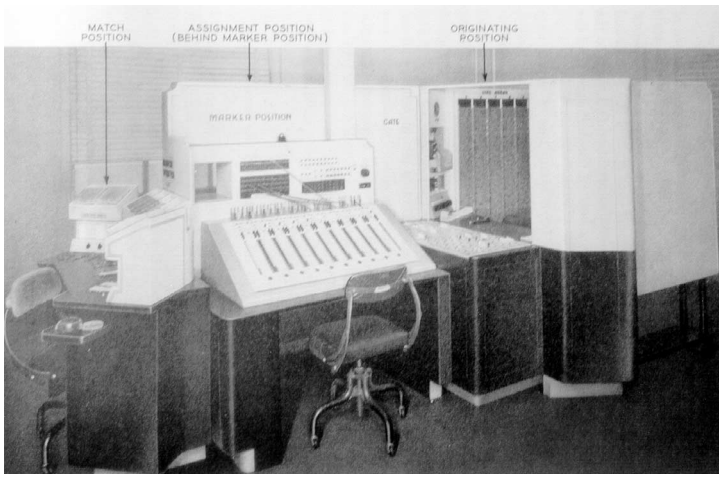

Figure 9. The throwdown machine, often called the KRF machine after the initials of the developers' last names. ("A Throwdown Machine for Telephone Traffic Studies," *The Bell System Tech. J.*, Mar. 1953, courtesy AT&T Archives.)

Gunnery system simulator

During World War II, the Navy Bureau of Ordnance asked Bell Labs to develop a number of fire control radars to provide defense for their combatant ships. The air defense system had a search radar that scanned the skies looking for enemy aircraft. When an attacking aircraft was detected, the system transferred positional data to a narrower beam tracking radar that would start tracking the object to develop data for calculating gun orders. With these data, a gun director would calculate aiming and firing data for the gun, including fuze settings. This system controlled dual-purpose gun batteries able to fire against both surface and air targets.

As the war progressed, the speeds of attacking aircraft steadily increased, making the air defense task more difficult by allowing less time for a response. Ironically, an additional complication for the air defense arose from improvements to the tracking accuracy of the fire control radars. The improved tracking accuracy was achieved by increasing the radar frequency, thereby decreasing the radar's beam width. This narrower beam width made it more difficult for the tracking radar—using the considerably less accurate search radar data on a rolling, pitching ship—to acquire an attacking aircraft target.

Because of these problems, in the closing days of the war, the Navy asked Bell Labs to undertake a system study of the entire problem, from search radar detection until the burst of the projectile against (or in close proximity to) the aircraft. The postulated air threat was a coordinated attack by substantial numbers of aircraft traveling at speeds up to 1,500 knots, allowing little time to organize the air defense. A further complication was that, under air attack, a ship would take violent evasive action, thus continually changing the effective arcs of fire of its guns.

The study was carried out over a two-year period, by a team composed of Walter A. MacNair, Bernard D. Holbrook, Alexis A. Lundstrom, and Walter H. MacWilliams. The team issued its "Naval AA" report in July 1947. The report proposed automatic track-while-scan of the skies with search radars and use of the track coordinates to simplify the acquisition of attacking aircraft by the tracking radars. In an automatic track-while-scan system, a search radar continually scanned the sky to obtain 3D positional data on aircraft within radar range. The data processing system would first associate new radar data with established stored aircraft tracks, then initiate new tracks on aircraft not presently being tracked. Next, it calculated the velocities of all the aircraft and predicted their future positions.

In this proposal, the mechanics of assigning incoming aircraft to gun directors would be simplified by use of a display and switching console. This combination was identified by the acronym TEWA, for Target Evaluator and Weapon Assigner. Further, the study proposed that a computer be designed to analyze the tactical situation and automatically generate assignments subject to manual override. This use of a computer to control the air defense was

termed ATEWA (Automatic Target Evaluator and Weapon Assigner).

Thus, officers would conduct the air defense by using sophisticated displays and switching facilities, with the possibility of carrying out the defense automatically, using the ATEWA computer but subject to manual override. It was further proposed that a gunnery system simulator (GSS) be built to simulate the attack and the defense response in order to compare the effectiveness of manual and automatic defenses against the postulated attacks. The Bureau of Ordnance agreed with the recommendations, and Bell Labs designed and built both the ATEWA and the GSS.

The GSS had the capability of simulating attacks of up to 10 aircraft against a defense installation of four tracking radars and gun directors, and four gun mounts. Target flight paths were input by teletypewriter punched paper tapes. The targets would then be prioritized, either manually or automatically, by estimated time to reach the ship. The most threatening targets would be assigned (manually or automatically) to the tracking radars and to the gun mounts that were most favorably situated to engage them.

The real-time ATEWA computer consisted of multicontact relays and implemented defense strategies based on quantifying the threats of individual targets and the availability of tracking radars and gun mounts. Once an incoming aircraft was assigned to a particular tracking radar and gun mount, simulated gunfire would start. The simulated gunfire began after an appropriate slewing time delay, which represented the time required to move the gun mount from its initial position to the position necessary to fire on the attacking aircraft.

The effects of gunfire on the attacking aircraft were simulated as well. A probability of kill for each shot, represented by the symbol p, was established based on the aircraft's flight path and the distance of the target from the ship at that instant. A single-shot kill probability computer calculated the probability that each individual shot would destroy the aircraft being fired at, as a function of the aircraft's range for that shot. A separate computer, the Electronic Dice Thrower, determined, on a probabilistic basis, whether each particular shot would destroy its attacking aircraft based on the computed kill probability of that shot. Data were accumulated on the success of that particular simulated attack, and the attacks were replicated to obtain statistical significance. No gun mount would be eligible for reassignment until destruction of the attacking aircraft was assured.

As remarked earlier, the simulated defense could be carried out either manually or automatically. Manual override of automatic decisions could always be made, thus permitting comparison between manual and automatic control of the defense.

The GSS consisted of about 40 racks of equipment and was probably one of the largest aggregates of electronic equipment up to that time.

The simulations carried out in 1950 and 1951 proved to be very valuable, and, as a result, the Navy asked Bell Labs to build a system for the *USS Northampton* based on the preceding work. The equipment, called the Gun Fire Control System Mark 65, was installed in the ship and received extensive shipboard testing.

Although the equipment did an excellent job in controlling the gunnery defense, antiaircraft guns gave way to surface-to-air missiles. Bell Labs modified the defensive system to control surface-to-air missiles, with one or two missile launchers per ship, keeping the track-while-scan elements. Over a period of some 20 years, weapon director systems for air defense were installed in 74 US combatant ships and in 20 ships of seven foreign navies.[16] The systems first used Terrier and later Tartar missiles.

Walter MacWilliams, in a 7 November 1999 letter to me, relates that an important bit of serendipity occurred during these simulation runs:

> The Simulator contained a great many vacuum tubes and electronic components and of course many component failures occurred, causing time lost in locating and replacing the failed parts. We became very sensitive to downtime resulting from component failures! As a result, the design of the equipment that was to be installed in ships was subjected to a painstaking process of scrutiny. Electronic components were used at well below their rated voltages and power dissipations to minimize the chance of failure. In addition, account was taken of over-voltages that could occur from component failures, so that in many cases a circuit would not be disabled by even a single (unlikely) component failure. As a result, the equipment that was installed aboard ships had an unparalleled record of reliability, leading to demonstrative affection on the part of fire control personnel.

The transistor gating matrix

The GSS contained, as one of its components, the first use anywhere of transistors to perform a circuit function other than one characterizing its electrical properties. It came about in this way: MacWilliams, who had proposed

the design and construction of the GSS, also designed some of its components, one of which was a matrix of gates that channeled pulses representing gunnery projectiles to circuits that computed the appropriate single-shot kill probability, as a function of the range to the aircraft being fired on. This matrix was called the gun-to-*p*-computer switching matrix.

MacWilliams had designed a perfectly satisfactory gun-to-*p*-computer matrix circuit using triode vacuum tubes. However, Bell Labs had announced the invention of the transistor, and several engineers obtained experimental transistors to explore their applicability for various applications. Jean H. Felker, a colleague of MacWilliams, was one of these recipients. MacWilliams persuaded Felker to get him some of the preproduction units so that he could explore whether transistors would be useful for his application. Using these samples, MacWilliams designed and built a 4×10 transistor gate matrix (one transistor per gate) that worked well. He then incorporated the design into the GSS itself, where it performed satisfactorily over the life of the simulator. Figure 10 shows the transistor matrix.[17]

I have related this first application of the transistor here because of its association with the gunnery system simulator. However, from here on, the transistor holds center stage with respect to Bell Labs' computer development.

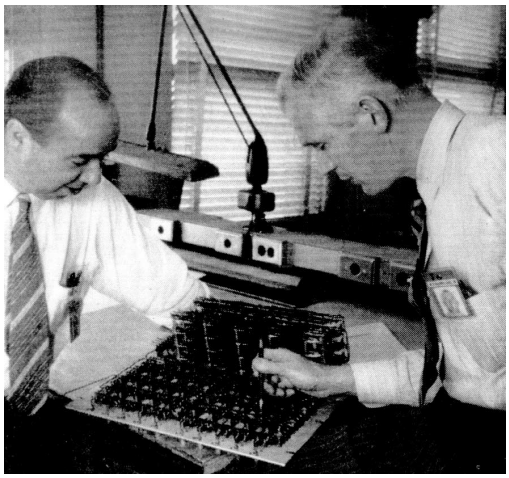

Figure 10. The transistor gating matrix, with Robert C. Winans at left and Walter H. MacWilliams at right. (Courtesy W.H. MacWilliams.)

The beginning of the transistor era

With Bell Labs' invention of the transistor in 1947, Bell Labs' management recognized the transistor's immense importance and devoted extensive laboratory effort to understanding all facets of transistor physics and technology. As that understanding grew, Bell Labs made it a policy to share this information with other scientists and engineers. Many symposia and conferences were held for scientists and engineers from the military, universities, and business.

Bell Labs summarized its development knowledge in November 1951 by publishing 5,500 copies of *The Transistor,* a 792-page book. It was affectionately called the Gray book because of its cover's color and, interestingly, now commands up to $625 on the secondhand book market. In 1958, a three-volume, 1,778-page book—*Transistor Technology*[18]—was published, elaborating on the work accomplished since the Gray book's publication. Its cover was also gray.

Much of this technology was developed in a small department led by Jack A. Morton, staffed by scientists and engineers from many disciplines. The department's responsibility was to convert the fledgling transistor into a consistent, manufacturable device that was understood at the engineering level and applicable to real problems. By mid-1950, several exploratory analog and digital applications were being pursued under a contract that the military's Joint Services sponsored and the US Army Signal Corps administered. Three of the digital projects were a six-digit angular position encoder, a four-digit reversible binary counter, and a serial adder with a pair of shift registers.

A shift register can receive a set of digits in time sequence or in parallel, hold the digits indefinitely, and move the digits in response to a signal. A serial adder produces a sum and carries digits when numbers to be added are fed into it. James Harris designed this five-digit shift register and two-word serial adder.[19,20] Figure 11 (next page) shows Harris holding the adder-register, which is now in the AT&T Archives. I believe it to be the oldest surviving piece of solid-state computing equipment in existence.

Most of the early computing components and computers built at Bell Labs were scrapped. I sadly admit that I signed off for scrapping several of the computers used in the first ballistic missile defense systems developed by Bell Labs. The adder-register is a rare exception to this fate.

After completing the adder-register in 1950 and it having served its purpose, Harris offered it to the Signal Corps, which had supported this work. Neither the Corps nor Bell Labs was interested in keeping it, but Harris was too proud of this machine he had constructed to put it on the scrap pile, so he took it home and stored it in his attic. There it remained until 1983 when he again offered to donate it to Bell Labs and this

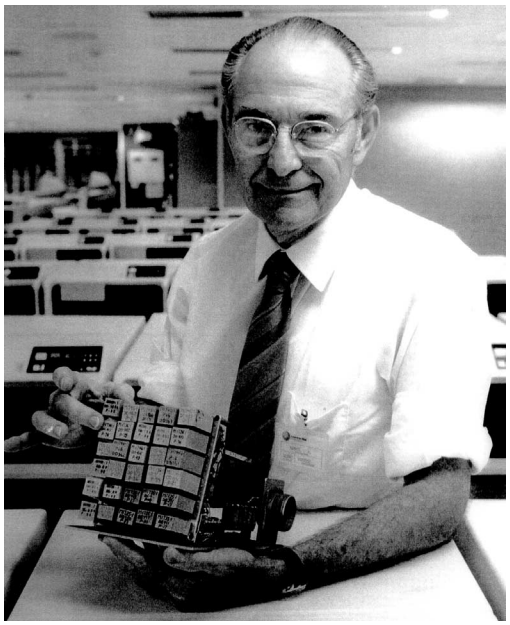

Figure 11. James R. Harris with the adder-register he built in 1950. (AT&T Archives photo, 1983.)

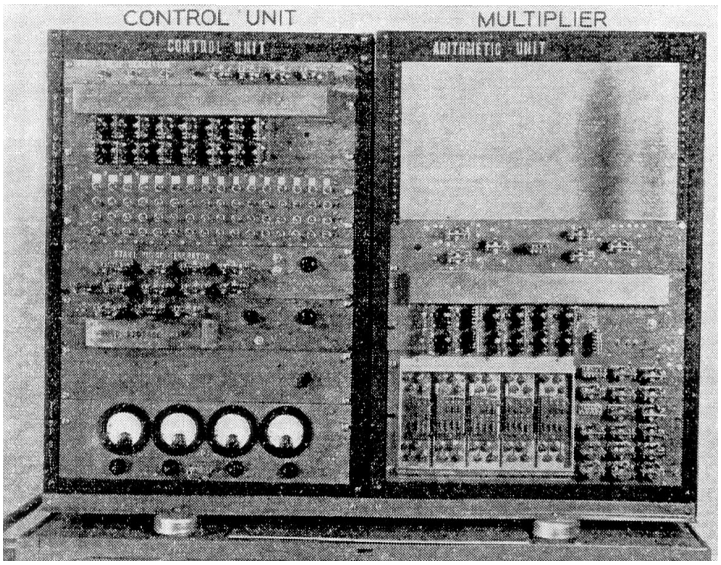

Figure 12. Jean H. Felker's multiplier and control unit. (*Proc. IRE*, Nov. 1952, p. 1596, © 1952 IEEE.)

time they accepted. Bell Labs in turn loaned it to the Smithsonian Institution where it was to go on public display in an exhibit the Smithsonian was designing. After some months, it became apparent that the proposed exhibit would not take place, so the device was returned and placed in the AT&T Archives.

The device and its builder were reunited in Bozeman, Montana, on 4 September 1999, when Harris was presented with the 1999 George R. Stibitz Computer Pioneer Award in a ceremony sponsored by the American Computer Museum and Computer Science Department of Montana State University. AT&T Archives very graciously loaned the adder-register to the American Computer Museum for the occasion.

Other engineers within Bell Labs also obtained sample transistors and experimented to determine what could be accomplished with this new, exciting device. Jean H. Felker, (who had given MacWilliams the transistors used in the GSS), received a new point-contact transistor that had been fabricated by Bell Labs' transistor development group. He first tried to build a linear amplifier with it but could not prevent it from oscillating. Finally, he decided that if he couldn't prevent it from oscillating, he would see if he could use it in that mode.

Felker then built a blocking oscillator that, when triggered, caused a simple pulse to occur. On examining the pulse output, he observed that it was very fast (for that time), rising and falling in a few hundredths of a microsecond and requiring a very small amount of power.

Bell Labs' lore relates that Felker then became notorious for roaming the halls and various offices, showing people the device and asking if they could possibly use it in their work. Unlike the usual development scenarios, he had a solution and was looking for a problem. The end result of his search was the birth of TRADIC (transistorized airborne digital computer) when he realized that his circuit could serve as a regenerative amplifier as part of a high-speed clocked circuit in a fast, lightweight, solid-state digital computer using low power.

Felker[21] proceeded to show how this regenerative amplifier could be used as the basis for a set of building blocks in a serial computer operating at a megahertz rate. These building blocks included OR, AND, INHIBIT, DELAY, and MEMORY (bit storage cell).

Felker built a multiplier to demonstrate the building blocks. Figure 12 shows his multiplier and its control unit. The multiplier contained 38 amplifier packages and could multiply two 16-digit binary numbers in 272 microseconds. The control unit on the left side of Figure 12 contained 35 amplifier packages and developed the numbers handled by the multiplier. It also provided test facilities. Each transistor package was mounted on a separate plug, and all packages were interchangeable. The dc power for the entire apparatus was obtained from a power supply that used semiconductor rectifiers. Part of this work was sponsored by the Navy Bureau of Ordnance.

After listening to Felker's presentations of

the new technology, the US Air Force agreed that a transistorized digital computer would be a major improvement over the analog control units in their bombing and navigational systems. Felker emphasized four points in his presentations: solid-state digital computers would have lower power consumption, require less cubic feet of space, weigh less, and be more reliable than the technology then in use by the military. In one meeting, Felker dramatized the last point by declaring, "We will give you a computer that is as reliable as a hammer!"[20]

Accordingly, in 1951, Felker led a group that began work on TRADIC, with Air Force sponsorship, to examine the feasibility of constructing a transistorized airborne digital computer.

At the same time that the TRADIC work was started, Bell Labs found a second application for transistor digital computers. In a brief digression, I will first describe the second application before returning to the TRADIC story.

The prediction computer

This second application was a transistorized digital computer to be used in a Navy track-while-scan shipboard radar system. In 1951, the Navy authorized Bell Labs to develop this computer, known as the prediction computer. The system requirement was to simultaneously track 50 aircraft. In doing so, the data processing system first associated new radar data with established stored aircraft tracks and initiated new tracks on aircraft not presently being tracked. The system then calculated the velocities of all the aircraft and predicted their future positions.

Two separate computers were to perform these two tasks, but for several reasons only the computer to calculate velocities and predictions was built. First, there was a shortage of transistors to construct two machines; next, there was a shortage of engineering personnel; finally, the velocity and prediction task was deemed the more demanding task. The prediction computer performed coordinate conversion, velocity computations, data smoothing, and prediction of future positions. These functions required a program of about 100 steps.

The prediction computer was a serial, synchronous machine that operated at a 3-MHz bit rate. It used diode-resistor logic and high-speed pulse amplifiers. A sequential access memory was provided by two 318-word quartz ultrasonic delay lines. A third 318-word delay line handled buffering.

Five programs altogether, at a maximum size of 168 steps each, were wired into the machine. The programs included two diagnostics for test purposes, one simulation program for generating test data, and two programs for the track-while-scan application. Addition time was 4 microseconds; multiplications required 48 microseconds.

The development work was directed by Arthur W. Horton Jr. This computer was completed, extensively tested, and demonstrated in 1957. Figure 13 shows an oblique view of the prediction computer. Table 2 details the machine's characteristics.[16,22,23]

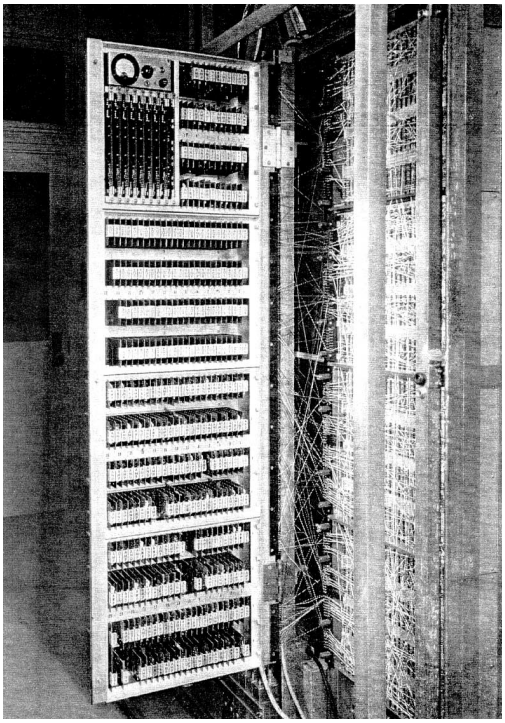

Figure 13. Oblique view of the prediction computer. ("A Special-Purpose Solid-State Computer Using Sequential Access Memory," *Proc. Western Joint AIEE-IRE Computer Conf.*, © 1959 IEEE.)

Table 2 . The prediction computer was a special-purpose, digital computer that used diode-resistor logic and high-speed pulse regenerative transistor amplifiers.

Feature	Specification
Word length	12 binary bits
Number of transistors	Approximately 1,000 (point contact)
Number of diodes	Approximately 12,000 (germanium)
Internal memory	636 words; two ultrasonic delay lines
Buffer memory	318 words, one ultrasonic delay line
Program control	168-step magnetic-core stepping switch
Addition time	4 microseconds
Multiplication time	48 microseconds
Output	Cathode ray tube (aircraft tracks), and pen recorder (for test purposes)

Table 3. TRADIC computers and the names they have been known by.

Computer	Also known as
TRADIC Phase One computer	Feasibility Model TRADIC
	TRADIC
Flyable TRADIC	TRADIC Phase Two
	TRADIC Flyable Model
	Flyable Model TRADIC
	Flyable Research Model TRADIC
	TRADIC
Leprechaun	Second TRADIC Feasibility Computer
XMH-3 TRADIC	Control Unit for XMH-3 System
	Flyable TRADIC
	XMH-3 Computer

Table 4. The TRADIC Phase One Computer. Germanium point-contact diodes were used for logic operations and other circuit functions. Point contact transistors were used in circuits to reshape pulses distorted by the logic networks.

Component	Description
Number of transistors	684 Bell Labs Type 1734 Type A cartridge transistors
Number of diodes	10,358 germanium point-contact diodes
Word size	16 bits-serial. Each word was stored in a separate electrical delay line 16 microseconds long.
Number storage	16 addressable electrical delay lines. Constants were input using toggle switches.
Addition or subtraction time	16 microseconds
Multiplication or division time	Less than 300 microseconds
Digital-to-analog converters	Two that converted numbers to voltages
Clock	30 watts at 1 megacycle supplied by an electron tube because no transistors were available which could supply this much power at this frequency.

Although this machine did not go into production, the knowledge gained during its design and construction was applied to the Nike Zeus Acquisition Radar Data Processing System (a track-while-scan system). That system used special-purpose reporter-sorter and track-initiator computers. A general-purpose computer handled the remaining track-while-scan functions such as data smoothing and tracking, a satellite test, impact point prediction, and handover of targets to a precision target-tracking radar.

The TRADIC project

The other project begun in 1951, with more long-lasting and far-reaching impact, was TRADIC. This Air Force-sponsored development program called for four versions of Bell Labs' solid-state computers.

TRADIC Phase One was developed to explore the feasibility, in the laboratory, of using transistors in a digital computer that could be used to solve aircraft bombing and navigation problems.

Flyable TRADIC was used to establish the feasibility of using an airborne solid-state computer as the control element of a bombing and navigation system.

Leprechaun was a second-generation laboratory research transistor digital computer designed to explore the capabilities of new solid-state devices for airborne computers. It was also used to demonstrate that a stored-program control machine could be built using transistors and to conduct programming and logical design research for digital computers to be used in real-time control loops in weapon systems.

XMH-3 TRADIC was to be a solid-state computer meeting military environmental specifications as the control unit for a bombing and navigational system to be installed in a to-be-developed Air Force plane, the B-68.

Each of these four computers has been referred to by different names, as listed in Table 3, and that has led to some confusion.

The naming confusion extends to the acronym TRADIC as well. Its origin is transistorized airborne digital computer; frequently, transistorized is changed to transistor.

Many Bell Labs personnel, including Morton, for example, detested the word transistorized. To them it implied that transistors were merely substituted for vacuum tubes in older circuit designs. Of course, the solid-state machines were completely new designs.

The TRADIC Phase One computer

The TRADIC Phase One computer was built to demonstrate successful laboratory operation of a high-speed, general-purpose, solid-state digital computer together with input-output (I/O) equipment representative of its use as the control unit of an aircraft bombing and navigation system.[24,25] *General purpose* here means the computer can add, subtract, multiply, and divide numbers and move them among its internal units and I/O equipment, all under control of any program that has been prepared for and inserted into it. The programs, which controlled the machine, were introduced via a removable plugboard. Table 4 gives a summary of some of its characteristics.

Felker led the development team and Harris was the supervisor reporting to Felker. The TRADIC Phase One computer was completed in January 1954. It was the first large transistor digital computer. Also, it was probably the

largest equipment unit in terms of the number of transistors used—684—up to that time.

One of the major decisions made early in the design stage was to use solid-state diodes for the logic circuits. Bell Labs already had a strong background in diode logic. Beginning in the late 1930s, Bell Labs had conducted an intensive review of various technologies that were potentially useful for future telephone call switching systems, and the solid-state diode was one of those studied. This investigation led to new and useful diode configurations for performing logical operations. Two of the most-used diode logic circuits, the AND gate and the OR gate, were invented by H.T. Holden[26] and Arthur W. Horton.[27]

Given these achievements, diode logic circuitry was well understood and very reliable in 1951 when TRADIC Phase One was being designed. The use of this proven technology limited the risk of failure in this new machine. Bell Labs decided that a follow-on computer (Leprechaun) would be developed to explore transistor logic as a main objective.

TRADIC Phase One had a 1-MHz clock using transistors for pulse shaping and amplification, and it used 10,358 germanium point-contact diodes. About one-third of the diodes were used for the logic circuits. The remainder had circuit functions such as isolation, pulse shaping, and clamping plus some functions peculiar to the use of point-contact transistors.

The computer performed additions and subtractions in 16 microseconds; multiplication and division, in less than 300 microseconds. Number storage was accomplished with 16 addressable electrical delay lines.

The 30 watts of power for the 1-MHz clock was supplied by a vacuum tube supply because no transistors were available that could supply this much power at this frequency. Logic circuits used 60 watts of dc power provided by precisely regulated, all solid-state power supplies. The only adjustable elements in the computer were in the power and clock supplies, and the computer operators used them to adjust the dc voltage and clock phase to standard values.

Programs for the computer were set up on removable plugboards. Each plugboard could handle a program of 64 machine steps, together with one subroutine, recallable as needed, also of up to 64 steps.

For two years—May 1954 to May 1956—TRADIC Phase One ran 24 hours a day in a reliability study. For some results from the study, see the "Highlights from TRADIC Summary Report" sidebar (next page).

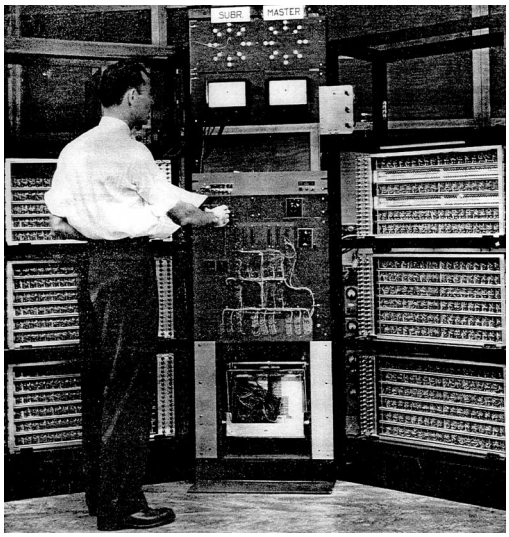

Figure 14. James R. Harris at the control unit of the TRADIC Phase One. ("TRADIC: The First Phase," *Bell Laboratories Record*, Sept. 1958, courtesy AT&T Archives.)

One of the hallmarks of the early Bell Labs' transistor digital computers was the extensive use of margin checking, which let the computer operators determine the machine's health. To perform margin checking, the operators would vary the power supply voltage to the computer from nominal during operation. If the machine continued to operate normally, all was well. However, if the computer started making errors, that was a warning that one or more components had deteriorated and that perhaps the machine would fail if preventive action were not taken to locate and replace the weak component. Margin checking proved highly effective in early identification of weak components.

Harris introduced margin checking into the TRADIC design. In his earlier work on telegraph equipment as an engineer with the C&P Telephone Co. of Virginia, he had observed that traditional margin checking was a very powerful maintenance tool that greatly enhanced system reliability (1999, private email communication). Figure 14 shows Harris with the TRADIC Phase One.

The Flyable TRADIC computer

The Flyable TRADIC computer was developed as a flying testbed to establish the feasibility of using a transistorized digital computer as a real-time control element in a bombing and navigation system.

In the early 1950s, Bell Labs developed the Bombing and Navigation System, Optical and Radar, Type K-5, and Western Electric pro-

Highlights from TRADIC Summary Report

The following three sections—Abstract, Project Goals, and History—are reproduced verbatim from the *TRADIC, Computer Research Program, Summary Engineering Report 32*. This report was issued 1 June 1957, Contract AF33(600)-21536 for the US Air Force, Air Materiel Command, prepared by Bell Telephone Laboratories on behalf of Western Electric Company.

Abstract

This report summarizes the TRADIC Computer Research Program for the development of a solid-state technology for airborne weapon-control computers. Among the major items covered are: direct-coupled transistor logic circuitry, transistor-driven magnetic-core memory, time encoding and decoding equipment and the philosophy of their use, and the system design of the digital weapon-control computer. Evaluations of these and competing techniques are included where appropriate.

The summary proper is accompanied by two auxiliary Volumes, of which Supplement I is a compilation of all TRADIC work on direct-coupled transistor logic circuitry. Supplement II is in the nature of a quarterly report, and presents the details of work completed during the twelfth quarter of the TRADIC computer research project.

Project Goals

The object of the computer research program has been to develop a digital-computer technology which exploits the most recent advances in the solid-state art and is tailored to meet current airborne weapon-control problems. Achievement of this objective required work in several areas including weapon-system studies, programming, logical design, input-output systems, large-scale memory systems, digital building blocks, and device work, e.g., work on transistors and magnetic cores.

History of the Project

The potential importance of the transistor in the design of military equipment was unmistakably clear at an early stage of transistor development. Programs for evaluation of the feasibility of the use of transistors for military applications were inevitable. The prospect of relatively complex systems operating at low power and occupying less volume and weighing less than corresponding vacuum-tube systems was attractive enough to arouse the interests of many people, particularly those concerned with airborne systems. TRADIC (coined from the words transistor airborne digital computer) was set up as one of the first projects to explore the application of transistors to a particular weapons problem.

Before transistors entered the picture, computers for bombing and navigation systems had almost universally used analog techniques. An early study concluded, however, that with available point-contact transistors an analog computer offered fewer dividends than a digital computer to perform this function. As a result, the first aim of the TRADIC project was to determine the feasibility of the use of point-contact transistors in a digital computer of the type required in the K-5 bombing and navigation system which was under development at the Bell Telephone Laboratories.

TRADIC was set up to include two phases. The goal of phase one was to develop a set of digital building blocks suitable for the construction of a complete computer and to build a small computer from these building blocks capable of solving part of the bombing and navigation problems. In addition to the demonstration of feasibility, it was expected that this computer would provide valuable information on the use of a relatively large numbers of transistors, particularly with respect to their reliability.

The building blocks developed in phase one used semiconductor diodes to perform the logic. Transistor synchronous pulse amplifiers were used to provide gain and pulse regeneration. The circuits were designed to operate at a pulse repetition rate of 1 megacycle. The transistors were germanium point-contact switching transistors which were the developmental predecessors of the Type 2N67. The phase one computer was constructed using 684 transistors and 10,614 [sic] diodes. It was first demonstrated in January 1954, and is believed to have been the first transistorized digital computer ever built.

The phase one computer, although limited in size, was capable of solving the simple bombing problem and did indeed demonstrate that these techniques were suitable for a bombing and navigation computer. In addition, the phase one computer has provided some interesting lifetest data. In 17,103 hours of operation, 8 out of 684 transistors were replaced and 9 out of 10,614 diodes were replaced, giving failure rates of 0.07 percent and 0.005 percent per thousand hours, respectively. Of the eight transistors replaced, five were detected by marginal checking before they caused a failure of the computer.

duced 65 of these systems for the Air Force's B-66B aircraft. The control units were vacuum tube analog computers. The Flyable TRADIC computer was to be flight-tested with the radar portion of this system, with Flyable TRADIC replacing the vacuum tube analog computer as the control unit.

To achieve this objective, the Bell Labs engineers reconfigured the TRADIC Phase One machine to withstand the aircraft's environmental conditions, including vibration, shock, and humidity, for example. Design changes to the TRADIC I/O circuits were necessary so that the TRADIC computer could interface correctly with the radar portion of the K-5 system. Other changes assured reliable operation in the

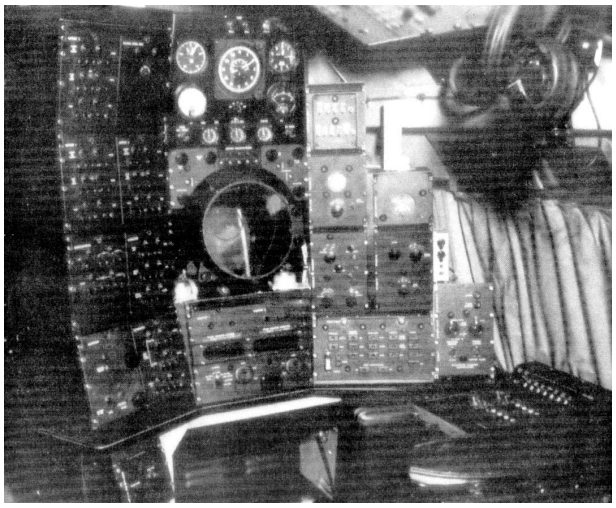

Figure 15. Flyable TRADIC's operator's position. (*TRADIC Flyable Research Model Program Summary Eng. Report,* US Air Force, 1958.)

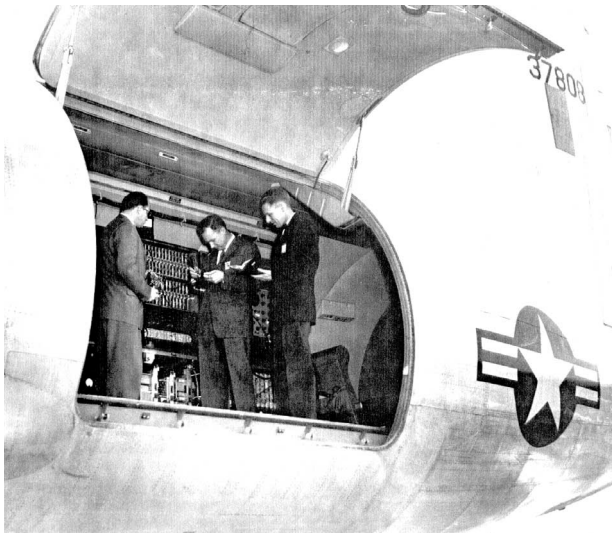

Figure 16. Flyable TRADIC installed in the EC-131B aircraft. (From AT&T Archives press release.)

harsher environment. For example, the plugboards for entering programs into the TRADIC Phase One computer would be unreliable in aircraft operation and also too complex with the longer program. Consequently, George G. Smith developed a new storage mechanism for programs by using a Mylar sheet with punched holes, a system reminiscent of punched-card storage.

Two Flyable TRADIC machines were constructed, one for flight-testing purposes aboard a loaned Air Force EC-131B cargo plane and the other for program development and debugging in the laboratory. The operator's position is shown in Figure 15. Figure 16 shows the EC-131B cargo plane with the equipment installed. Table 5 gives some of the characteristics of Flyable TRADIC.

Louis C. Brown, who did much of the Flyable TRADIC's programming and flight testing, has written an *Annals* article giving a detailed account of the system and of the issues encountered during its development.[28]

Table 5. The Flyable TRADIC computer was a synchronous, binary, serial computer with parallel multiplication.

Feature	Specification
Number of transistors	2269 (WECO 2N67)
	416 (WECO GA-52996)
Number of diodes	10,740
Word size	16 serial bits
Number of storage slots (variable)	52 serial delay-line storage slots
Number of storage slots (constant)	80 fixed constant-storage slots
Program store	Mylar sheet with punched holes
Addition or subtraction time	16 microseconds
Multiplication time	64 microseconds
Division time	304 microseconds
Program solution time	50 milliseconds
Input/output	8 shaft-angle inputs
	6 incremental inputs (slew and track)
	16 manual inputs (hand set and track)
	28 outputs (meters, servos, radar)
Clock	4 phase, 1.036 MHz
Weight	1,193 pounds (excluding air conditioning)
Size	39.5 cubic feet
Power	450 watts

Leprechaun

Leprechaun, a second-generation TRADIC computer, enabled Bell Labs engineers to further explore the capabilities of solid-state devices for use in airborne computers. Much time was devoted to programming and logical design research for computers to be used in military real-time control loops.

Initially, Felker led the development team and Harris, a supervisor then, reported to him. Later, Felker was reassigned to another Bell Labs computer project and was replaced by Jack A. Baird. Six months later, Harris was transferred to the same project as Felker, and shortly after that, Jack A. Githens was appointed Harris' replacement.

Leprechaun does not fit any discernible pattern, compared to the naming origins of other TRADIC computers, and the reason behind it

Table 6. The Leprechaun computer.

Feature	Specification
Number of transistors	5,500 (Raytheon CK761, GE 2N137, Philco Surface Barrier SB100, Western Electric GA52830)
Memory	18,000 coincident-current magnetic cores
Memory capacity	1,024 18-digit words including parity check bit and sign bit
Addition or subtraction time	48 microseconds
Multiplication time	350 microseconds
Division time	430 microseconds
Primary input	Ferranti photoelectric reader and paper tape
Primary output	Teletype high-speed punch
Optional output	Electric typewriter
Size	15 cubic feet, not including I/O equipment
Power	250 watts

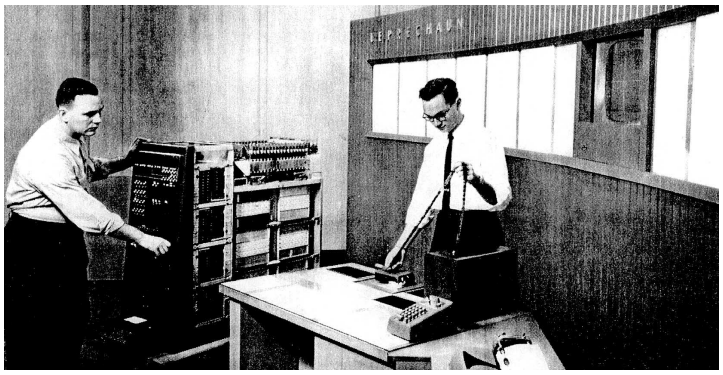

Figure 17. F.W. Hodde (right) feeds a problem into Leprechaun while N.J. Powell prepares the machine for operation. ("Military Applications," *Bell Laboratories Record,* June 1958, courtesy AT&T Archives.)

bears telling. Because this new computer would have the ability to run much longer programs than the TRADIC Phase One, the Bell Labs development group started referring to it as the Long Program computer. One day, while in the shower, Robert A. Kudlich—who was responsible for Leprechaun's system and logical design—starting musing on how to make an acronym from those three words. He started with LONPROCOM. As he repeated that name it sounded to him like Leprechaun (1999, private phone-call communication). Later, the rest of the group felt it was appropriate and the name stuck. Githens[29] has related why he felt the name particularly suited this machine:

> For when one turns to Webster, as everyone must to check the spelling, one finds that it is a very appropriate name. Leprechaun is from the Middle Irish *lu*, meaning "little" and from *corpan*, diminutive of *corp*; *corp* is from the Latin *corpus* meaning "body." Little body—that is just what we were after when we started designing this machine. Further, the dictionary reveals that in Irish folklore a leprechaun is a little fairy generally conceived as a tricky old man, who if caught may reveal the hiding place of treasure. After about a year of struggle, we have caught our Leprechaun, although we are still seeking the treasure.

A coincident-current magnetic memory served as storage. The logic functions were implemented by direct-coupled transistor logic circuitry (DCTL). Although Philco invented this circuitry, Harris named it. Leprechaun was a binary, parallel, asynchronous machine. The operation code provided all the common arithmetic, logical, and transfer operations—a total of 28 operations. Table 6 summarizes Leprechaun's main characteristics. A more detailed description of Leprechaun has been given by Jack Githens[29] and later by Jack Baird.[30] An exhaustive, 812-page review of Leprechaun's details was prepared and edited by Githens and Gilmartin.[31]

Figure 17 shows Leprechaun at its Bell Labs' Whippany, New Jersey, location. Leprechaun became operational in 1956 and, after extensive use at Bell Labs, was delivered to the Air Force. It was installed at the Wright-Patterson Air Development Center at Dayton, Ohio, in 1959, where it was used in evaluating Air Force weapons systems.

Harris has recently given an assessment of the historical significance of this machine (private communication, letter, 27 September 1999):

> The Leprechaun computer was a very significant advance in three major areas.
>
> First, this machine was the earliest solid-state computer to use true stored-program control, sometimes called von Neumann architecture. To put this a little differently, Leprechaun was the first solid-state computer to employ software!
>
> Second, Leprechaun was the first computer to use junction transistors. It was known from the very early days of the transistor that the junction type had the potential to be much superior to the point-contact type. Why? The point-contact device was inherently difficult to understand and analyze and duplicate. In contrast, the junction device, when it became available, lent itself to analysis and prediction at all levels, that is, device design, device manufacture, and circuit application.

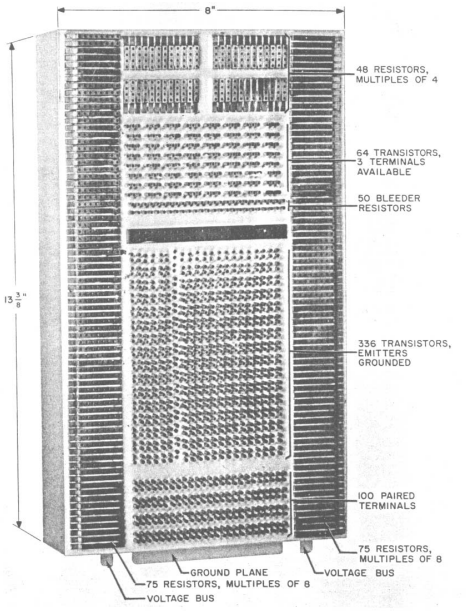

Figure 18. Direct coupled transistor logic (DCTL) plate (top view). (*TRADIC Computer Research Program Supplement I, A Handbook of Direct-Coupled Transistor Logic Circuitry,* US Air Force, 1957.)

> Finally, Leprechaun was a direct precursor of the integrated logic circuit that is now the engine of world economy. The machine used as a building block a DCTL (Direct Coupled Transistor Logic) logic plate containing only transistors and resistors, a scheme perfectly adapted to be realized later in the form of an integrated circuit. A DCTL logic plate is shown in Figure [18]. The plate was built in universal form, without wiring, and then was wired to realize a specific logic design. In this sense the DCTL plate foreshadowed the silicon master slice.

DCTL has been described by Harris[32] and discussed in depth (21 papers by 13 authors) in Supplement 1 (*A Handbook of Direct-Coupled Transistor Logic Circuitry*).[31]

TRADIC Summary Engineering Report

As the research phase of the TRADIC development program reached completion, a *Summary Engineering Report*[33] was issued that reviewed the project history, outlining what had been learned and giving suggestions for future research.

To convey the flavor of the development of these three machines and to give the developers' thoughts in their own words, the "Highlights from TRADIC Summary Report" sidebar reproduces the Abstract, Project Goals, and History sections of that report written in 1957.

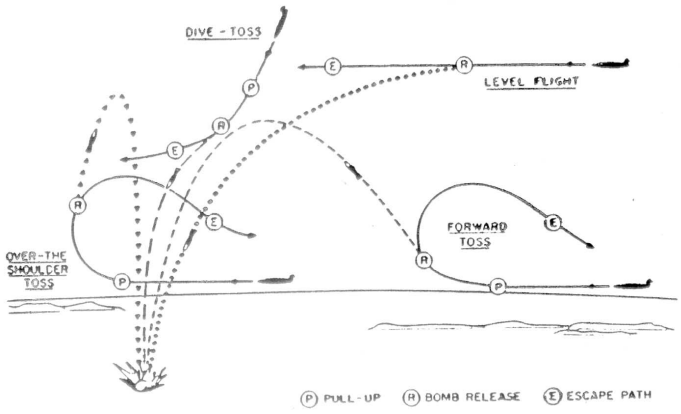

Figure 19. 302A Weapon System weapon-delivery modes. (*XHM-3 System Third Interim Eng. Report,* US Air Force, 1956.)

The XMH-3 TRADIC

Although ultimately never brought to completion, XMH-3 TRADIC was a solid-state computer to be built to military specifications and used as the control unit of the XMH-3 Bombing and Navigation System. This system was to be installed in a two-person, to-be-developed high-speed tactical bomber (B-68) that would be effective within a radius of 1,000 nautical miles at all hours and in all weather. The Air Force selected two aircraft companies, Douglas and Martin, for the design competition for the B-68 development contract. The airframe, with all of its equipment and payload, was known as the 302A Weapon System.

The XMH-3 Bombing and Navigation System was quite sophisticated for its time. It featured an inertial data generator (for inertial guidance), a bombing and navigation radar set, a three-beam radar terrain avoidance system, and a photographic unit.

The mission profile called for the plane to fly at high altitudes over friendly terrain (to conserve fuel) and, upon entering hostile territory, descend to a low altitude (100 to 200 feet) to avoid radar detection and radar-directed weapons' fire.

On reaching the target, the aircraft would execute one of several bomb release maneuvers as shown in Figure 19. The entire flight was under the XMH-3 TRADIC computer's control.

These were to be highly briefed missions, and a photographic unit would take pictures along the way, compare those pictures with briefing photos, and the navigator made any necessary position corrections to the system.

Simulated flights of the B-68 under the control of the XMH-3 TRADIC computer were conducted on an analog computer (see the

Table 7. The XMH-3 TRADIC computer's proposed characteristics. Five computers were to be built: one laboratory breadboard model, one flight test model, and three deliverable models for the B-68.

Feature	Specification
Program storage	Punched-card storage as used in Flyable TRADIC
Flight-plan storage	Ferrite-core memory made nondestructible by the placement of permanent magnets near each core that should show a "1". This type of memory was referred to as a Shachell Store. Stored in this memory would be up to four flight paths in a flight plan, using a maximum of 30 fix-and-aim points. Each fix or aim point required 161 bits.
Variable memory storage	Ferrite-core memory, minimum capacity of 256 18-bit words
Logic circuitry	DCTL as used in Leprechaun, although where Leprechaun used about 5,500 transistors, this would be 10,000 transistors.
Computing cycle	0.25 second or less. Operation would be asynchronous between start and completion.
Operation and address size	17-bit word (5 bits specify operations, 11 bits specify addresses and constants, and 1 bit indicates a program step that the computer cannot modify)
Weight	273 pounds
Size	10,560 cubic inches of space
Power	160 watts

"Gypsy" sidebar) by Bell Labs' Mathematics Research Department. A favorite exercise was to fly low over the English Channel toward the White Cliffs of Dover, which gave the terrain avoidance component a good workout.

The XMH-3 TRADIC design relied heavily on the experience gained during development of TRADIC Phase One, Flyable TRADIC, and Leprechaun. Major changes had to be made to meet the size and weight requirements as well as the military specifications covering, for example, humidity, temperature, and vibration. The computer's major characteristics are listed in Table 7.

The Air Force, in April 1956, delivered a C-131B to Bell Labs to be used in initial flight testing of the XMH-3 Bombing and Navigation System. In the fall of that year, the Air Force cancelled the 302A Weapon System project for budgetary reasons. Additional information on the XMH-3 TRADIC can be found in the *Third Interim Engineering Report*.[34]

The digital technology developed on this project and the projects discussed earlier were used as the basis for a series of new digital computers, developed in partnership with Univac. These new computers were used on the Nike Zeus, Nike X, Sentinel, and Safeguard intercontinental ballistic missile defense systems.

The Bell System data processing computer

When transferred from the Leprechaun project, Felker was appointed systems engineering director of a project charged with developing a computer for the Bell System telephone companies' use in business operations. This computer, initially envisioned as a replacement for the assembler-computer, would use magnetic tape instead of perforated paper tape to capture the call data. Later, under Felker's leadership, the charter was broadened to include some of the telephone companies' business operations.

The organization to carry out the development work was established in 1956, and the computer under development was called the Bell System Data Processing (BSDP). Initially, a separate computer was to be used for the four-stage tape-sorting operation discussed earlier. However, as the work progressed it became clear that the sorting operation could be accomplished in the BSDP and a separate computer would be unnecessary. Personnel were drawn from the Bell System telephone companies to aid in establishing the requirements for the new computer. Many of the Bell Labs engineers who had experience with the earlier computers were reassigned to the project, and this is the project to which Harris was transferred from the Leprechaun project.

The requirements were established and the machine's major components' design was under way when, in 1958, Bell Labs management made the decision to cancel the project. A survey of soon-to-be-available commercial computers convinced management that the telephone companies' needs could best be met by using commercially available machines.

A footnote to this history is that shortly after the cancellation of the BSDP computer (it had never had another name), Felker was transferred from Bell Labs to AT&T and later served as operations vice president of New Jersey Bell before he retired to Spain to paint.

Bell Labs then established an organization, reporting to a vice president, called Business Information Systems-Programs (BISP) for the purpose of developing software for commercially available computers for the telephone companies' business operations. Once again, engineers from the telephone companies were assigned to Bell Labs to aid in establishing system requirements, and Felker was coaxed out

of retirement to be the VP heading up the BISP development effort.

Epilogue

The military supported much of Bells Labs' computer research and development work. Although many other organizations also received strong support from the same source, Bell Labs was in a somewhat unique position. At this time, AT&T was a highly regulated company and had no legal right to develop computers for other than its own internal or government use. This fact shaped computer development at Bell Labs during the time period being discussed.

The Bell System was an appreciable market for computers, as evidenced by the approximately 100 assembler-computer machines delivered to the telephone companies. So it was natural that, when Bell Labs determined the telephone companies' computing demands were sufficiently great to warrant development of a suitable follow-on computer, the BSDP project was established.

In my opinion, the decisive moment for the future of computer research and development at Bell Labs occurred in 1958 when management decided that suitable commercial computers would be available in the near future and canceled the BSDP project. Bell Labs further emphasized its withdrawal from the field by forming a partnership with Univac for developing computers for ballistic missile defense systems.

However, the various telephone call switching machines that Bell Labs designed and Western Electric manufactured are truly special-purpose computers optimized for call switching. These switching machines were produced by the hundreds. Several other small more general computers were also built.

Acknowledgments

It is with a great deal of pleasure that I acknowledge all the help I have received from Louis C. Brown and Walter H. MacWilliams. They have been very generous with their time in discussing their activities on the computer systems discussed here. They also shared with me critical documentation including photographs and copies of their papers. And it was a lot of fun reliving events with them of those long-ago days.

I owe special thanks to J.R. Harris whom I pestered constantly during the preparation of this article. Jim always responded promptly to my questions, whether they were about dates, people, events, or technology, with thoughtful, well-researched answers.

Figures A, 5 to 9, 14, and 17 are the property of AT&T Archives and are reprinted with permission of AT&T.

I would also like to express my appreciation to the *Annals* editors for their patience with me while they transformed this article into publishable form.

References and notes

1. G.R. Stibitz, "The Relay Computers at Bell Labs," *Datamation*, vol. 13, nos. 4 and 5, Apr. and May 1967, pp. 35-49.
2. E.G. Andrews, "A Review of the Bell Laboratories' Digital Computer Developments," *Proc. Joint AIEE-IRE Computer Conf.*, Dec. 1951, Feb. 1952. (Reprinted in *Bell Telephone System Monograph No. 1972*.)
3. M.R. Williams, *A History of Computing Technology,* 2nd ed., Chapter 6, IEEE Computer Soc. Press, Los Alamitos, Calif., 1997, pp. 221-234.
4. O. Cesaroo, "The Relay Interpolator," *Bell Laboratories Record*, vol. 24, no. 12, Dec. 1946, pp. 457-460; *Relay Interpolator,* final tech. report to the National Defense Research Council, Bell Telephone Laboratories, New York, 31 Oct. 1945; *The Relay Interpolator,* report no. R-3177, Naval Research Laboratory, Washington, D.C., 25 Sept. 1947.
5. J. Juley, "The Ballistic Computer," *Bell Laboratories Record*, New York, vol. 25, no. 1, Jan. 1947, pp. 5-9.
6. *Computer Mark 22, Model 0*, report 178-45, United States Navy, Washington, D.C., 12 Dec. 1945.
7. S.B. Williams, "A Relay Computer for General Application," *Bell Laboratories Record*, New York, vol. 25, no. 2, Feb. 1947, p. 49; S.B. Williams, "A Bell Telephone Laboratories Relay Computing System," *Annals*, Harvard Computation Laboratory, Cambridge, Mass., vol. 16, 1947, p. 41; F.L. Alt, "A Bell Telephone Laboratories Computing Machine," *Mathematical Tables and Other Aids to Computation*, National Research Council, Washington, D.C., vol. 3, no. 21, part 1, Jan. 1948, pp. 1-13, and part 2, no. 22, April 1948, pp. 69-89; Additional pictures of Aberdeen installation, *Bell Laboratories Record*, New York, vol. 26, no. 5, 1948, p. 208; H.W. Bode and E.G. Andrews, "Use of the Relay Digital Computer," *Electrical Eng.*, New York, vol. 69, no. 2, Feb. 1950, pp.158-163.
8. E.G. Andrews, "The Bell Computer Model VI," *Annals*, Harvard Computation Laboratory, Cambridge, Mass., vol. 26, 1951, p. 20; E.G. Andrews, "The Bell Computer Model VI," *Electrical Engineering*, New York, vol. 68, no. 9, Sept. 1949, pp. 751-756.
9. E.G. Andrews, "Bell Laboratories Digital Computers," *Bell Laboratories Record*, New York, Mar. 1957, p. 82.
10. H.D. Cahill, "Recording on AMA Tape in Central

Offices," *Bell Laboratories Record*, New York, Dec. 1951, pp. 565-570.
11. G.G. Drew, "The AMA Assembler," *Bell Laboratories Record*, New York, May 1952, pp. 227-232.
12. A.E. Hague, "The AMA Computer," *Bell Laboratories Record*, New York, July 1952, pp. 289-294.
13. J. Meszar, "Basic Features of the AMA Center," *Bell Laboratories Record*, New York, Feb. 1952, pp. 70-74.
14. T.C. Rehm, "The AMA Assembler-Computer," *Bell Laboratories Record*, New York, Oct. 1957, pp. 423-427.
15. G.R. Frost, W. Keister, and A.E. Ritchie, "A Throwdown Machine for Telephone Traffic Studies," *The Bell System Tech. J.*, vol. 32, no. 2, Mar. 1953, pp. 292-359.
16. M.D. Fagen, ed., *A History of Engineering & Science in the Bell System—National Service in War and Peace (1925-1975)*, Bell Telephone Laboratories, New York, 1978.
17. W.H. MacWilliams, "A Transistor Gating Matrix for a Simulated Warfare Computer," *Bell Laboratories Record*, New York, Mar. 1957, pp. 94-99.
18. *Transistor Technology*, H.E. Bridgers, J.H. Scaff, and J.N. Shive, eds., vols. 1, 2, and 3, Van Nostrand, New York, 1958.
19. J.R. Harris, "A Transistor Shift Register and Serial Adder," *Proc. Inst. of Radio Engineers (IRE)*, New York, Nov. 1952, pp. 1597-1602.
20. J.R. Harris, "The Earliest Solid-State Digital Computers," *IEEE Annals of the History of Computing*, vol. 21, no. 4, 1999, pp. 49-54.
21. J.H. Felker, "Regenerative Amplifier for Digital Computer Applications," *Proc. IRE*, Nov. 1952, pp. 1584-1596.
22. J.A. Baird, "Military Applications," *Bell Laboratories Record*, June 1958, pp. 221-225.
23. W.A. Cornell, "A Special-Purpose Solid-State Computer Using Sequential Access Memory," *Proc. Western Joint AIEE-IRE Computer Conf.*, Mar. 1959, pp.74-79.
24. J.H. Felker, "Performance of TRADIC Transistor Digital Computer," *Proc. Eastern Joint AIEE-IRE Computer Conf.*, "Performance of TRADIC Transistor Digital Computer," *Computers and Automation*, vol. 4, no. 1, Jan. 1955, p. 16 (abstract).
25. J.R. Harris, "TRADIC: The First Phase," *Bell Laboratories Record*, vol. 36, Sept. 1958, pp. 330-334.
26. W.H.T. Holden, US Patent No. 2,299,898; Patent and Trademark Office, Washington, D.C., filed 16 Oct. 1941; issued 27 Oct. 1942.
27. A.W. Horton, US Patent No. 2,244,700; Patent and Trademark Office, Washington, D.C., filed 21 Sept. 1939; issued 10 June 1941.
28. L.C. Brown, "Flyable TRADIC—The First Airborne Transistorized Digital Computer," *IEEE Annals of the History of Computing*, vol. 21, no. 4, Oct.-Dec. 1999, pp. 55-61.
29. J.A. Githens, "The TRADIC Leprechaun Computer," *Proc. Eastern Joint AIEE-IRE Computer Conf.*, 1956, pp. 29-33.
30. J.A. Baird, "Leprechaun Computer," *Bell Laboratories Record*, New York, Feb. 1960, pp. 58-63.
31. "TRADIC Computer Research (Second Stage)," *Summary Eng. Report 1*, Dec. 1958, AD-208621, J.A. Githens and M. J. Gilmartin, eds.; TRADIC Computer Research (Second Stage)," *Summary Eng. Report, Supplement*: *Leprechaun, A Solid-State Digital Computer,* 1 Dec. 1958, Contract AF33(600)-34977, U.S. Air Force, Air Materiel Command, AD-208622, J.A. Githens and M. J. Gilmartin, eds. Also, *Tradic Computer Research Program Supplement I, A Handbook of Direct-Coupled Transistor Logic Circuitry*, 1 June 1957, Reporting Period 1 Feb. 1954 to 31 Dec. 1956, Contract AF33(600)-21536, US Air Force, Air Materiel Command.
32. J.R. Harris, "Direct Coupled Transistor Logic Circuitry," *IRE Trans. Electronic Computers*, vol. EC-7, no. 1, Mar. 1958.
33. J.A. Baird et al., "TRADIC Computer Research Program," *Summary Eng. Report*, US Air Force, Air Materiel Command, Washington, D.C., 1 June 1957.
34. Bell Telephone Laboratories, *XHM-3 System Third Interim Engineering Report*, Air Materiel Command, USAF, Washington, D.C., 15 Nov. 1956, AD-115 302.

M.M. Irvine retired from Bell Labs in 1984, which he joined in 1955 after teaching physics at Lehigh University, following service in World War II as a radio officer for the merchant marine. His responsibilities at Bell Labs focused on software development for various ballistic missile defense systems and, later, for the Bell System operating companies. He served on the editorial board of the *Bell Laboratories Record* from 1978 to 1983. Irvine received a BS in engineering physics from Montana State College and an MS and a PhD in physics from Lehigh University. He is a Senior Life member of the IEEE, a member of the American Physical Society, and of the American Association of Physics Teachers.

Contact M.M. Irvine at 511 South Willson Ave., Bozeman, MT 59715; email mmirvine@montanadsl.net.