Research article

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On-chip optical parity checker using silicon photonic integrated circuits

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Abstract: The optical parity checker plays an important role in error detection and correction for high-speed, large-capacity, complex digital optical communication networks, which can be employed to detect and correct the error bits by using a specific coding theory such as introducing error-detecting and correcting codes in communication channels. In this paper, we report an integrated silicon photonic circuit that is capable of implementing the parity checking for binary string with an arbitrary number of bits. The proposed parity checker consisting of parallel cascaded N micro-ring resonators (MRRs) is based on directed logic scheme, which means that the operands applied to MRRs to control the switching states of the MRRs are electrical signals, the operation signals are optical signals, and the final operation results are obtained at the output ports in the form of light. A 3-bit parity checker with an operation speed of 10 kbps, fabricated on a silicon-on-insulator (SOI) platform using a standard commercial complementary metal-oxide-semiconductor (CMOS) process, was experimentally and successfully demonstrated.

Keywords: integrated optics; optical switching devices; optical logic devices; resonators; photonic integrated circuits.

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1 Introduction

With the shrinking feature size of electronic transistors, the development of silicon electronics has been confronted with some serious challenges, such as limited bandwidth source, thermal power consumption, and complicated metal interconnects. Indeed, it is hard to further improve the performance of silicon electronics devices, along with the Moore's law, and silicon electronics has already entered the era after Moore. Light is regarded as a promising candidate as information carrier to realize high-speed, large-capacity information processing due to its high propagation speed, ultra-high bandwidth source, and parallelism [1–5]. In fact, optical information processing is commonly used in various occasions such as rack-to-rack, board-to-board, chip-to-chip, and even on-chip interconnect communications [6–9]. With the fast-developing optical information processing technology, signal error detecting and correcting have attracted extensive attention, both of which are very powerful binary manipulation in optical communication and coding community [10]. Errors of signal bits, which can be added, deleted, or flipped, may occur in various ways. Therefore, how to detect the error bits is the first challenge. The optical parity checker is a promising candidate for error bit detection, which can be used to identify the parity of the number of logic 1s or logic 0s in binary sequence signals and verify whether the signal bits are transmitted in the communication channels correctly [11, 12].

At present, various parity checking schemes have been proposed and demonstrated successfully [13–16]. Generally, the reported optical parity checkers are based on all-optical schemes such as third-order nonlinear optical materials, semiconductor optical amplifiers, etc. [17]. The all-optical scheme can be compatible with the all-optical network very well and does not need extra electrical control signals. However, a very strong pump light signal with the intensity of GW/cm^2 order is required to realize the correct operation in order to generate a nonlinear effect of material [18–21]. Therefore, it is difficult for an all-optical scheme to achieve large-scale integration on a single chip.

In this work, we propose and demonstrate a silicon photonic circuit that can perform the function of the parity checker based on parallel cascaded micro-ring resonators (MRRs). The proposed optical parity checker consisting of parallel cascaded N MRRs can realize binary string with an arbitrary number of bits, even checking and odd checking simultaneously. Here, MRR is employed to form the optical switching element of the photonic circuit considering its unique advantages such as compact size, low power consumption, high response speed, and large-scale integration [22–27]. The electrical signals regarded as binary operands are applied to the MRRs to control switching states, and the parity checking results are directed to the output port in the form of light. The overall latency of the proposed device is very low, as each MRR is independent from each other and all MRRs can perform their operations simultaneously. In contrast, the gate delays of electronic logic circuits are accumulated to a large overall latency [28, 29]. We designed and fabricated a 3-bit parity optical checker using standard commercial complementary-metal-oxide-semiconductor (CMOS) on a silicon-on-insulator (SOI), and the 3-bit parity checker is finally demonstrated successfully with a speed of 10 kbps.

2 Device principle

The schematic of the optical parity checker consisting of parallel cascaded N MRRs is shown in Figure 1A. We define N as an odd number to ensure that the even checking result of the binary string with an arbitrary number of bits is directed to the bus waveguide and the odd checking result is directed to the drop waveguide. Here, each MRR acts as an optical switch, and all optical switches are cascaded to form the optical switch network, which can implement the function of the arbitrarily bit optical parity checker. Micro-heaters fabricated on the top of corresponding MRRs are employed to tune MRRs for implementing the function of optical switch. Three ports of the circuit are defined as input, even-parity, and odd-parity according to their functions for conveniently introducing the operation principle of the device. Monochromatic continuous wave (CW) light with a working wavelength of λ_w is coupled into the input port by the commercial lensed fiber and then modulated by N independent electrical pulse sequences A_1, A_2, … A_{N-1} and A_N applied to corresponding MRRs, respectively. Logic 0 and 1 in the electrical domain is defined by the low and high levels of the electrical pulse sequences applied to the MRRs, respectively. Similarly, logic 0 and 1 in the optical domain is represented by the low and high levels of the optical power at the output ports. In the proposed device, each MRR is on-resonance at λ_w when the applied voltage is at high level (logic 1), and then the optical switch is at ON state, the light coupled from input port can be downloaded to the drop port of MRR. On the contrary, MRR is off-resonance at λ_w when the applied voltage is at low level (logic 0), and then the optical switch is at OFF state, the light from input port is directed to the through port of MRR without disturbances. The path of light in the MRR at

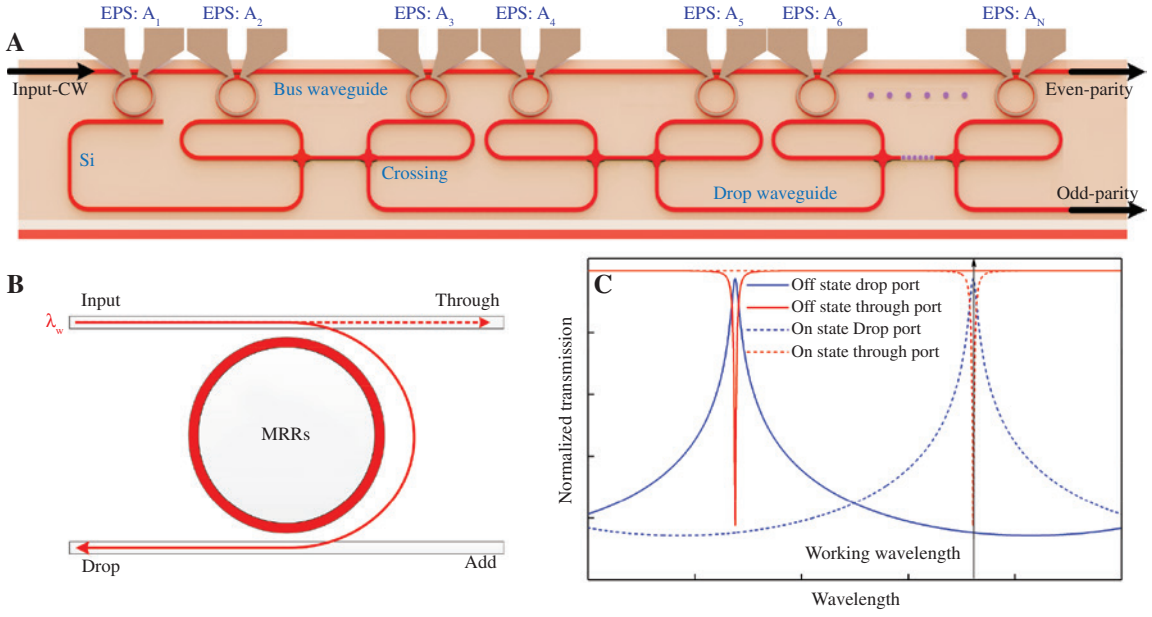

Figure 1: Schematic of the proposed device and switching element.
(A) Schematic of the proposed optical parity checker (CW, continuous wave; MRR, micro-ring resonator; EPS, electrical pulse sequences; N, an odd number). (B) The path of light in the MRR at ON state (the solid line) and OFF state (the dotted line). (C) Normalized transmissions at the drop and through ports. The black solid line indicates the working wavelength.

different work states is shown in Figure 1B. When the MRR is switched from the OFF state to the ON state, the resonance would be red-shifted from the initial position because of the thermal-optical effect (Figure 1C). Based on the working state definition of MRR, when the number of logic 1s (representing a high level of electrical signal) applied to MRRs is an odd number, there would be an odd number of MRRs, which are on-resonance. Thus, light is downloaded to the drop waveguide by the active MRRs for an odd number of times, and light bypasses the other inactive MRRs directly. Consequently, light is finally directed to the odd-parity port and logic 1 (representing a high level of light) is achieved at the odd-parity port. When the number of logic 1s applied to MRRs is an even number, there would be an even number of MRRs that are on-resonance. In this case, light is downloaded to the drop waveguide by the active MRRs for an even number of times, and light is finally directed to the even-parity port and logic 0 is achieved at the odd-parity port. In other words, if the obtained result is logic 1 at the odd-port, the number of logic 1s of the operand bits should be an odd number, or else it should be an even number. Therefore, the odd-parity port of proposed device can be used for implementing the function of odd checking correctly. For example, if the optical parity checker consists of parallel cascaded five MRRs. When three MRRs are on-resonance (defined as MRR_1, MRR_3, and MRR_5) and two MRRs are off-resonance (defined as MRR_2 and MRR_4), the light with the working wavelength of λ_w coupled into the device is downloaded to the drop port of MRR_1 firstly and bypasses MRR_2 directly. Light is directed to the add port of MRR_3 and is downloaded through the port of MRR_3. Then light is directed through the port of MRR_4 and downloaded to the drop port of MRR_5. Light is directed to odd-parity port at last, and thus logic 1 is achieved at the odd-parity port (Figure 2A). When two MRRs are on-resonance (defined as MRR_2 and MRR_4) and three MRRs are off-resonance (defined as MRR_1, MRR_3, and MRR_5), the light with the working wavelength of λ_w coupled into the device bypasses MRR_1 and is downloaded to the drop port of MRR_2. The light bypasses the MRR_3 and is directed to the add port of MRR_4. Then the light is downloaded to the through port of MRR_4 and bypasses MRR_5 directly. The light is directed to even-parity port at last and thus logic 0 is achieved at the odd-parity port (Figure 2B). The above description method for the odd-parity port is also effective for the even-parity port, and the function of even parity checking could be performed in this port: the logic signals are correct (logic 1) for an even number of logic 1s, while an odd number of logic 1s will lead to an error (logic 0). Based on the above elaboration, the truth table shown in Table 1 can be achieved for the proposed device. It is clear that the proposed logic circuit can perform the function of N-bit parity checker. Meanwhile, the resonant wavelengths of non-working MRRs can be shifted far from the working wavelengths of the circuit through thermal tuning to realize arbitrary-bit parity checking. Furthermore, the results of odd-parity checking and even-parity checking can be carried out at two different output ports simultaneously.

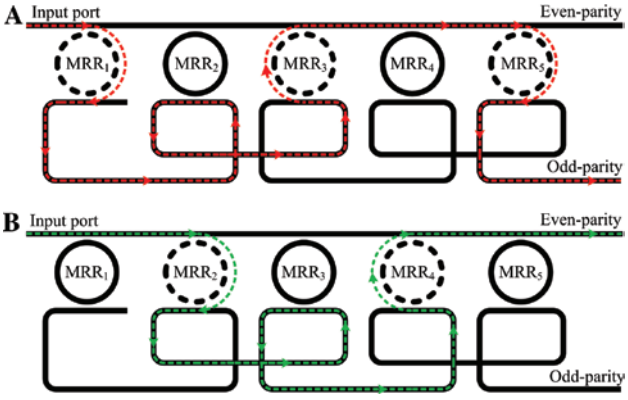

Figure 2: Two pathways of light propagating from input port to the corresponding output port.
(A) Odd-parity port and (B) even-parity port, respectively (the solid line ring denotes that MRR off-resonance at λ_w, the dot line ring denotes that MRR on-resonance at λ_w).

Table 1: Truth table of the proposed N-bit optical parity checker.

N-bit binary sequence	Odd-parity	Even-parity
00…000	0	1
00…001	1	0
00…011	0	1
00…010	1	0
…	…	…
11…111	1	0

3 Device fabrication

We fabricated a 3-bit optical parity checker using silicon photonic integrated circuits. The proposed device is fabricated on an 8-in. (20.3 cm) SOI wafer with 220-nm-thick top silicon-layer and 2-μm-thick buried SiO_2 layer at the Institute of Microelectronics, Singapore. The microscope image of the fabricated device is shown in Figure 3, and the efficient footprint of the fabricated device is about 600×300 μm^2. The thermo-optic modulating scheme is adopted because of its very wide tuning range, less complex device layer structure, and easier fabrication steps. The rib waveguides with 400 nm in width, 220 nm in height, 90 nm in slab thickness, and 130 nm in rid thickness are

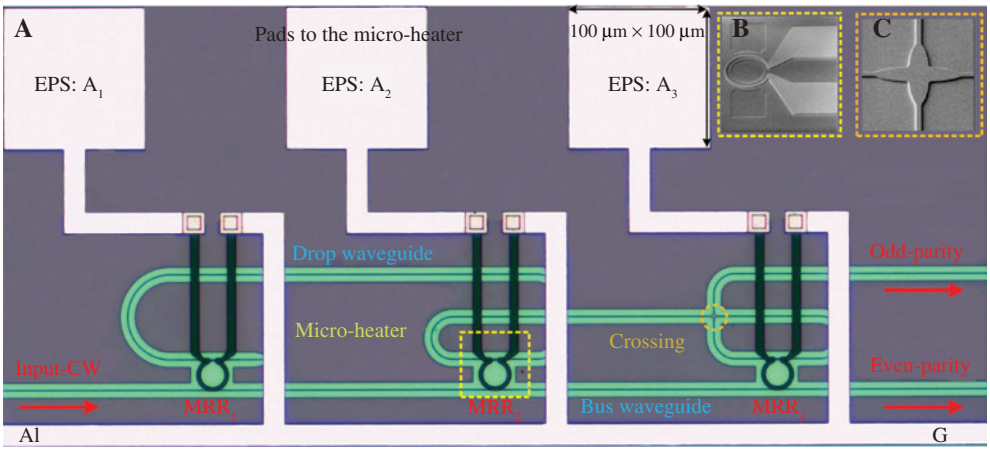

Figure 3: The proposed device is fabricated based on the CMOS process.
(A) Micrograph of the fabricated 3-bit optical parity checker. (B) and (C) Scanning electronic micrograph (SEM) of Ω-shaped TiN micro-heater and elliptical structure, respectively.

employed to form the device, which only support the quasi-TE fundamental mode. Compared to the strip waveguide with similar dimensions, the rib waveguide has less sidewall area, which can reduce the scattering loss on the waveguide sidewall, and thus, the transmission loss is less than the strip waveguide with similar dimensions and a similar fabrication process. The three MRRs are designed with identical physical parameters, and the radii of MRRs are 10 μm, with gaps of 400 nm between all ring waveguides and straight waveguides. An elliptical structure (short axis = 1.5 μm and long axis = 6.25 μm) is adopted to reduce the transmission loss and scattering of the waveguides crossings (Figure 3C). Two-hundred-forty-eight-nanometer-deep ultraviolet (UV) photolithography was used to define the device pattern. Inductively coupled plasma etching process was used to etch the top silicon layer. In order to enhance the coupling efficiency between the lensed fibers and the waveguides, spot size converters (SSCs) were integrated on the input and output terminals of the waveguides. The SSC is a 200-μm-long linearly inversed taper with a 180-nm-wide tip. The top cladding oxide with a thickness of 2 μm was deposited on top of an MRR by plasma enhanced chemical vapor deposition (PECVD), and then titanium nitride (TiN) with a thickness of 120 nm was used to create the Ω-shaped heaters (Figure 3B). Aluminum wires and pads were formed for wire bonding, seeing the white areas in Figure 3.

4 Experimental results

4.1 Static response spectra

An amplified spontaneous emission source (ASE, Hoyatek, HY-ASE-C-N-13-BA-FA, Shenzhen, Guangdong, China), three

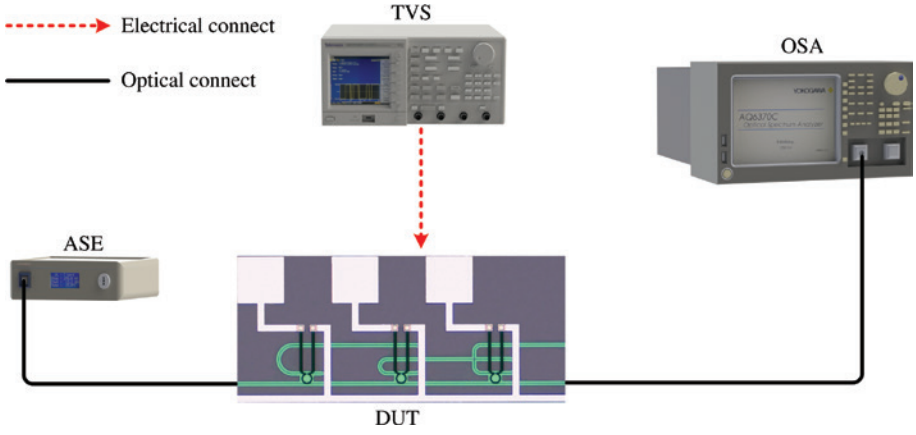

Figure 4: Experiment schematic for the static response of the device (ASE, amplified spontaneous emission source; TVS, tunable voltage source; OSA, optical spectral analyzer; DUT, device under test).

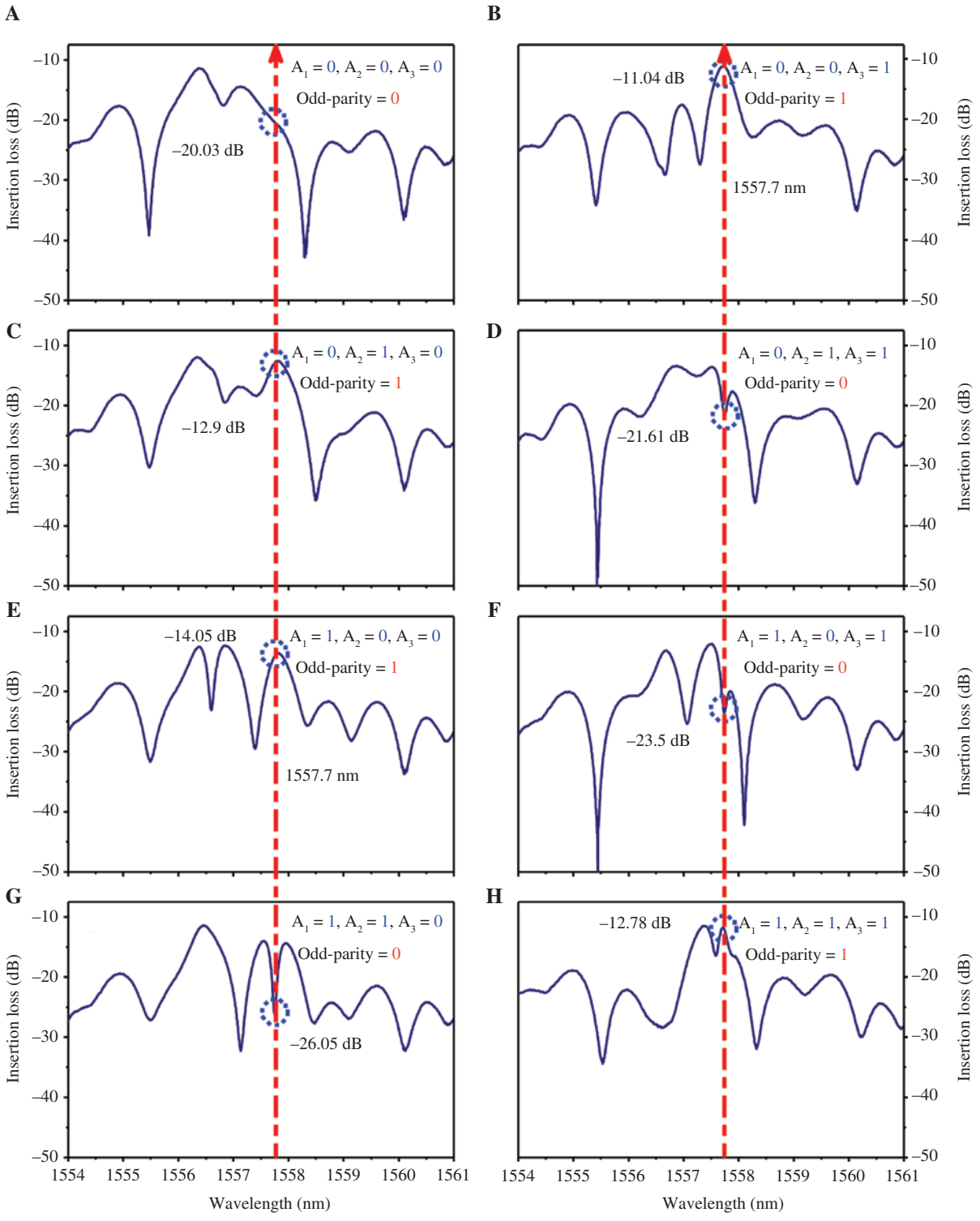

Figure 5: Response spectra in the odd-parity port under different combinations of voltages.
In (A)–(H), the logic 1 (0) of each signal represent that the corresponding voltage is at high (low) level. The high levels of voltage applied to the micro-heaters above MRR_1, MRR_2, and MRR_3 are 2.82 V, 2.30 V, and 2.62 V, respectively, while the low levels are all at 0 V.

tunable voltage sources (TVSs, GWinstek, GPD-3303S, Taipei, Taiwan, China), and optical spectrum analyzer (OSA, Yokogawa, AQ6370C, Tokyo, Japan) were firstly employed to characterize the static response of the device (Figure 4). Meanwhile, the working wavelength and voltages of each electrical pulse sequences were determined

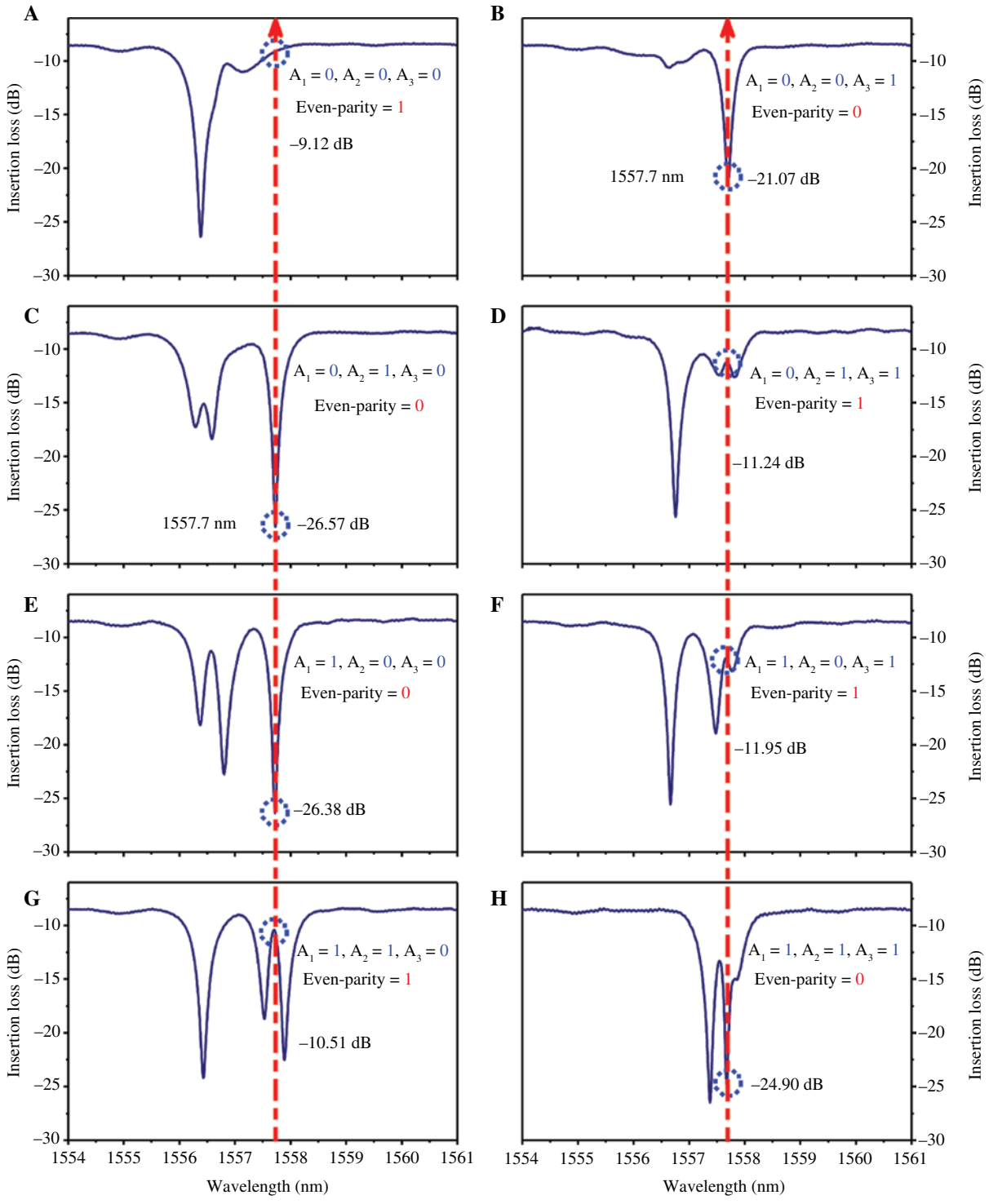

Figure 6: Response spectra in the even-parity port under different combinations of voltages.
In (A)–(H), logic 1 (0) of each signal represent that the corresponding voltage is at high (low) level. The high levels of voltage applied to the micro-heaters above MRR_1, MRR_2, and MRR_3 are 2.82 V, 2.30 V, and 2.62 V, respectively, while the low levels are all at 0 V.

by device's static characterization. Broadband light generated by ASE was coupled into the input port of the device through a lensed fiber, and the output light was fed into the OSA through another lensed fiber. Three TVSs were employed to tune three TiN micro-heaters above the corresponding MRRs, respectively. When the MRR is heated up, the refractive index of the silicon increases basing on thermo-optic effect and the resonant wavelength of the

Table 2: Measured truth table of the proposed 3-bit optical parity checker.

Voltages applied to the corresponding MRRs			Measured output results		Logical results	
A_1 (V)	A_2 (V)	A_3 (V)	Odd-parity (dB)	Even-parity (dB)	Odd-parity	Even-parity
0	0	0	−20.03	−9.12	0	1
0	0	2.62	−11.04	−21.07	1	0
0	2.30	0	−12.90	−26.57	1	0
0	2.30	2.62	−21.61	−11.24	0	1
2.82	0	0	−14.05	−26.38	1	0
2.82	0	2.62	−23.50	−11.95	0	1
2.82	2.30	0	−26.05	−10.51	0	1
2.82	2.30	2.62	−12.78	−24.90	1	0

MRR will red-shift. Although the three MRRs are designed to have the same radius (10 μm), they are slightly different in resonant wavelengths due to the limited manufacturing accuracy (Figure 6A). In principle, any wavelength at the right of the dip located at 1557.14 nm can be chosen as λ_w. In order to achieve a sufficiently large extinction ratio and relatively low power consumption, λ_w is chosen to be 1557.70 nm. The resonant wavelengths of MRR_1, MRR_2, and MRR_3 can be tuned to 1557.70 nm when the amplitudes of applied voltages are 2.82 V, 2.30 V, and 2.62 V, respectively, which means that the applied voltages of A_1, A_2, and A_3 for being on-resonance are 2.82 V, 2.30 V, and 2.62 V, respectively.

The response spectra of the device at the odd-parity port are shown in Figures 5A–H. When all MRRs are off-resonance at 1557.70 nm, this means that there is no logic 1 for input signals ($A_1=0$, $A_2=0$, and $A_3=0$). The light bypasses three MRRs and is directed to the even-port through the bus waveguide at last. Therefore, the optical power at the odd-parity port is at low level (odd-parity port result = 0, Figure 5A). When one MRR is on-resonance and the other two MRRs are off-resonance, this means that there is one logic 1 for input signals ($A_1=0$, $A_2=0$, and $A_3=1$; $A_1=0$, $A_2=1$, and $A_3=0$; $A_1=1$, $A_2=0$, and $A_3=0$). The light is downloaded by the on-resonance MRR while it bypasses two off-resonance MRRs and is directed to the odd-parity port directly through the drop waveguide. Therefore, the optical power at the odd-parity port is at high level (odd-parity port result = 1, Figure 5B, C, E). When two MRRs are on-resonance and one MRR is off-resonance, this means that there are two logic 1s for input signals ($A_1=0$, $A_2=1$, and $A_3=1$; $A_1=1$, $A_2=0$, and $A_3=1$; $A_1=1$, $A_2=1$, and $A_3=0$). The light is downloaded by the two on-resonance MRRs while it bypasses one off-resonance MRR and is directed to the even-parity port directly through the bus waveguide. Therefore, the optical power at the odd-parity port is at low level (odd-parity port result = 0, Figure 5D, 5F, 5G). When all MRRs are on-resonance, this means that there are three logic 1s for input signals ($A_1=1$, $A_2=1$, and $A_3=1$). The light is downloaded by three MRRs and directed to the odd-parity port through the drop waveguide at last. Therefore, the optical power at the odd-parity port is at a high level (odd-parity port result = 1, Figure 5H). From the above discussion, the odd-parity port of the proposed logic circuit can show that logic signals are correct for an odd number of logic 1s, while an error exists in the logic signals for an even number of logic 1s.

The response spectra of the device at the even-parity port are shown in Figures 6A–H. In the same way as that mentioned above, we can obtain the results of even-port at the wavelength of 1557.70 nm. The even-port of the proposed logic circuit can show that logic signals are correct for an even number of logic 1s, while an error exists in the logic signals for an odd number of logic 1s. Based on the above elaboration, the results of the proposed parity checker at the wavelength of 1557.70 nm can be listed in Table 2.

4.2 Dynamic operation results

The dynamic performance of the optical parity checker is further demonstrated. The experimental schematic for the device's dynamic response is shown in Figure 7. According to the static response spectra of the device, the input working wavelength is chosen to be 1557.70 nm, and the high levels of voltages applied on MRR_1, MRR_2, and MRR_3 are 2.82 V, 2.30 V, and 2.62 V, respectively, while the low levels are all at 0 V. Monochromatic CW light generated by tunable laser diode (TLD, EXFO, FLS-2800, Auckland, New Zealand) with the wavelength of 1557.70 nm is coupled into the input port of the proposed device. The proposed device is designed to support only TE mode; therefore, the polarization controller (PC, Fiberlogix, Watford, UK) is required to control the polarization of the signal light in order to obtain the maximum power of the output signal

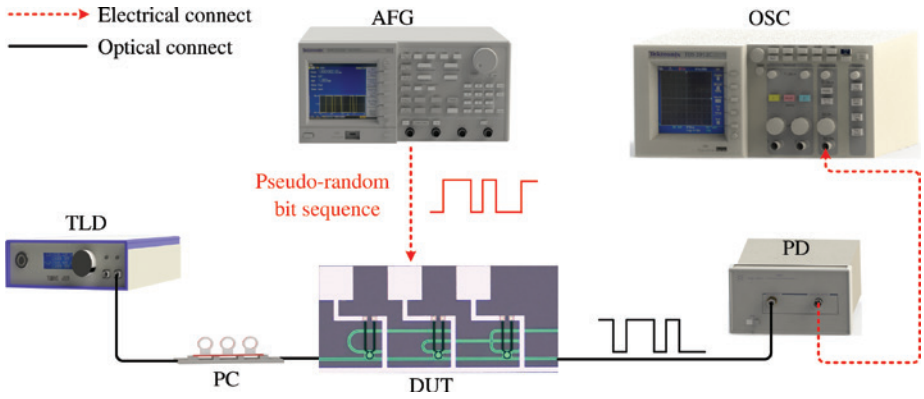

Figure 7: Experiment schematic for the dynamic response characterization of the device (TLD, tunable laser diode; PC, polarization controller; AFG, arbitrary function generator; PD, photodetector; OSC, oscilloscope; DUT, device under test).

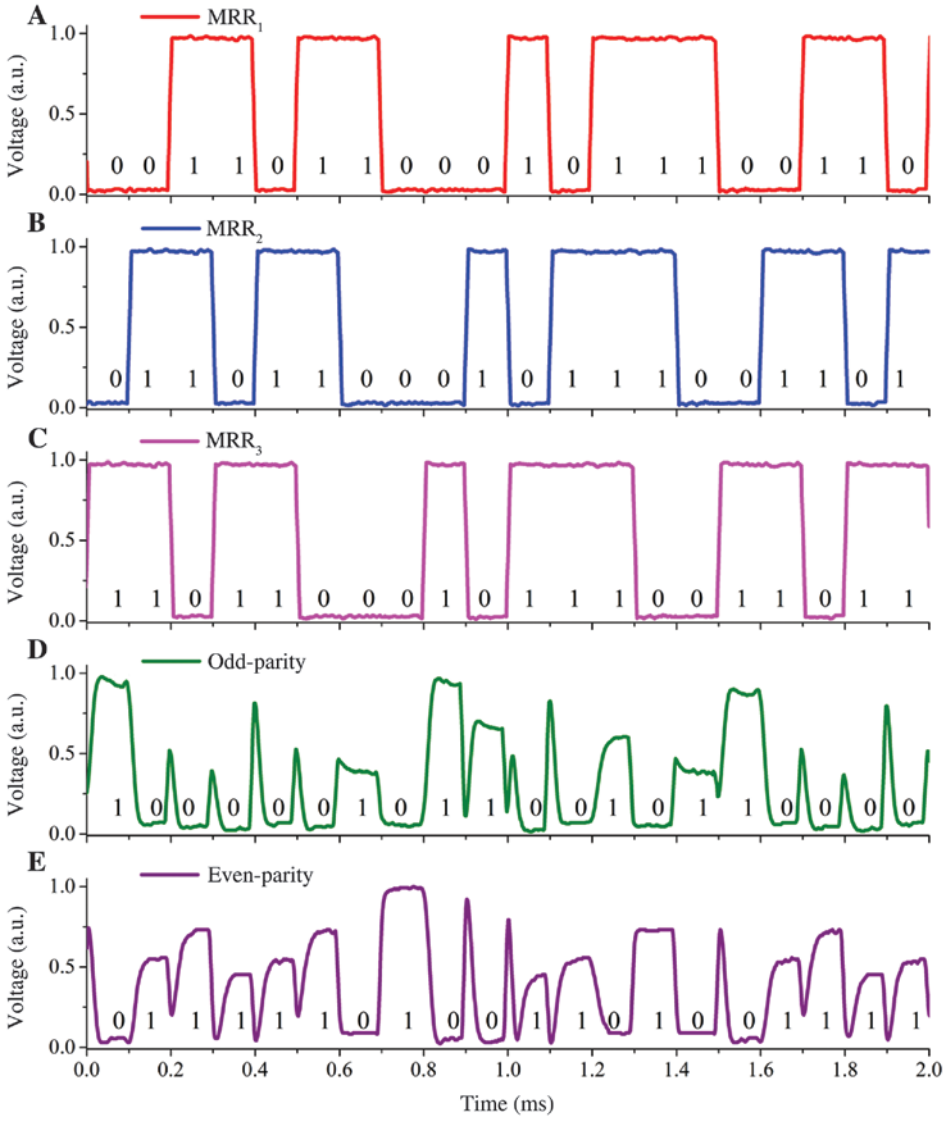

Figure 8: The dynamic performances of the device are measured.
(A)–(C) are signals applied to MRR_1, MRR_2, and MRR_3, respectively. (D) is the result at the odd-parity port. (E) is the result at the even-parity port.

from the device. Three continuous binary sequences generated by three arbitrary function generators (AFG, Tektronix, AFG3102C, Beaverton, OR, USA) with specific high and low levels of voltages at 10 Kbps are applied to the three MRRs, respectively. The applied sequences are with periods of 15 bits, and each bit is 0.1 ms in length. The output light at the odd-parity port and the even-parity port of the device are fed into a high-speed photodetector (PD, Agilent, 11982A, CA, USA) one by one. The electrical signals output from the PD and the three electrical signals applied to the MRRs are fed into an oscilloscope (OSC, Tektronix, TDS2012C, Beaverton, OR, USA) for waveform observation. The dynamic performance of the proposed device is shown in Figure 8. As shown in Figure 8D, the optical power at odd-parity port is correct (logic 1) for an odd number of logic 1s, while an error (logic 0) exists in the logic signals for an even number of logic 1s. Meanwhile, the optical power at even-parity port is correct (logic 1) for an even number of logic 1s, while an error (logic 0) exists in the logic signals for an odd number of logic 1s (Figure 8E). Note that the power levels for logic 1 are different at both odd-parity port and even-parity port in different cases, which mainly results from the transmission loss and scattering of the waveguides crossings. The light passes through different numbers of the cross structure in different working states, which leads to different steps of power levels for logic 1s. This similar phenomenon can also be observed in the static response spectra (Figure 5 and Figure 6). However, this does not hinder the implementation of the parity checker function of the device. Some small sharp dips and peaks can be found in Figures 8D and E, which originate from the transition of the different operation states [30].

5 Conclusion

In conclusion, we proposed an arbitrary-bit optical parity checker that can realize arbitrary-bit parity checking. The results of binary string with an arbitrary number of bits odd checking and even checking can be carried out at two different output ports simultaneously. We fabricate and experimentally realize a 3-bit optical parity checker using silicon photonic integrated circuits to prove the concept. The static response spectra and dynamic results of the device were successfully demonstrated. To achieve faster operations, we can employ other advanced modulation schemes, such as the plasma dispersion effect or graphene integrated modulation schemes, to modulate the MRRs [31, 32]. Further efforts should be made to construct large-scale directed logic circuits in the electro-optic manner.

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