IMX258 Application Note

IMX258-0AQH5
Software Reference Manual

Ver.1.0.1
2017/07/03
Mobile Imaging System Business Division
Sony Semiconductor Solutions Corporation

Revision History

Version	Date	Description
0.0.1	2015.03.11	First release
0.0.2	2015.04.22	Figure 4 1 Physical alignment of imaging pixel array - Correction of all pixel number(3182 -> 3192) Table 5 19 Sub-sampling mode setting - Correction of Y_ODD_INC[3:0] description Figure 9 13 Communication control and timing with shared CCI Bus - Correction IMX258(Slave) 2ND_CCI ACK setting(enable -> disable) Figure 9 15 Communication control and timing with separated CCI Bus - Correction IMX258(Slave) 2ND_CCI ACK setting(disable -> enable) Note, 5.7.1. Shield Pixel - Removing about reference document(Software Reference Manual for PDAF) 5.7.2. Shield Pixel Correction(SPC) - Changing reference document name (Software Reference Manual for PDAF -> PDAF Module Calibration Manual) 5.5 Gain setting - Range of Gains table is added ALL - Correction of Typographical Error
0.0.3	2015.05.18	6.1.3/6.2.2 Constraints of XCLR - Removing these section 5.5.2. Digital gain settings - Removing digital gain constraint in HDR capture mode 5.7.2. Shield Pixel Correction (SPC) - The explanation of SPC control register is added 10.4. LSC data structure - The explanation of OTP address was added. Figure 10 8 - Add this figure 9.8.7 Restriction of dual/multi camera usage - Add this section
0.0.4	2015.06.12	Note - Add the reference of Register default value 2.1. 2-wire serial communication operation specifications - Modify I2C Bus mode name (Fast-mode Plus) 2.3.2. Secondary slave address Table 2 4 2nd CCI ACK control register Figure 9 13 Communication control and timing with shared CCI Bus Figure 9 15 Communication control and timing with separated CCI Bus - Add SLAVE_ADD_EN_2ND and SLAVE_ADD_ACKEN_2ND 2.3.3. Second CCI slave address for synchronous dual sensor operation

		- Modify reference information (Dual camera) 2.6. 2-wire serial communication register update timing - Add register type (double buffered) - Modify the description of register update timing Figure 2 14 2-wire serial communication register update timing diagram (v-latched or double buffered type registers) - Add register type (double buffered) Figure 2 15 Pre-latch timing - Add Note (communication prohibited period) 2.7.3. Example of using grouped parameter hold continuously - Modify the description of GPH 5.1.1. Clock system diagram - Add Note (IVTCK PLL) Figure 5 1 Clock system diagram (PLL single mode) Figure 5 2 Clock system diagram (PLL dual mode) - Modify clock tree Table 5 17 HDR capture mode setting - Modify the description (HDR_RESO_REDU_H, HDR_RESO_REDU_V) Table 5 19 Sub-sampling mode setting - Add FORCE_FD_SUM 5.5.3. Change in output pixel level depending on binning mode - Modify reference information (BINNING_WEIGHTING) 5.7.1. Shield Pixel - Modify the description of shield pixel 5.7.2. Shield Pixel Correction (SPC) - Modify the description of SPC Figure 6 1 Start up sequence with 2-wire serial communication (external reset) - Add Note (Presence of INCK during Power Off) Table 7 5 List of registers to be set only in SW-standby as mode transition. - Add Range of PLL_IVT_MPY (Single PLL mode) 8. Settings related to HDR capture mode picture quality - Modify the description of the signal required by HDR system Table 8 1 Integration time control and analogue gain control for HDR capture mode - Add ANA_GAIN_GLOBAL, ST_ANA_GAIN_GLOBA Table 9 16 Monitor Setting example case 2 - Remove case 3 (OIS Pulse, Flash Strobe, V sync) Table 9 17 Monitor Setting example case 3 - Add this table ALL - Correction of Typographical Error
0.0.5	2015.06.30	4.6.1.2.3. Supplemental description of AF Window MANUAL_MODE - A mistake of an AF_WINDOW arithmetic expression was corrected. 3.1. MIPI transmitter

		- Correction of CSI-2 version(1.01.00 -> 1.10) 4.6.1.2. AF Window Specification - Correction of AF_WINDOW support mode(1/2 Binning -> 1/2 Sub-Sampling) 2.3.1. First slave address - Adjust position of Table 2 3.
0.0.6	2015.07.21	4.6.1.2.3. Supplemental description of AF Window MANUAL_MODE - A mistake of an AF_WINDOW arithmetic expression was corrected. 4.6. Output image format - The Embedded line number is changed to “2”.
0.0.7	2015.08.21	4.6.1.2.3. Supplemental description of AF Window MANUAL_MODE - A mistake of an AF_WINDOW arithmetic expression was corrected. Before : af _sta_x = block_sta_x + block_size_x – ((crop_sta_x - block_sta_x) % block_size_x) After : af _sta_x = crop_sta_x + block_size_x – ((crop_sta_x - block_sta_x) % block_size_x) Table 9 20 Control Register for Master and Slave mode Correction of 0x4635 description Figure 4 15 Shield pixel output variation (BYTE2 Full/HDR) Figure 1-16 Shield pixel output variation (BYTE2 V 1/2 Sub-sampling) Figure 4 18 Shield pixel output timing(BYTE2) - Addition these figure
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0.0.9	2015.10.26	Figure 5 1 Clock system diagram (PLL single mode) - Modification of Clock system diagram Figure 5 2 Clock system diagram (PLL dual mode) - Modification of Clock system diagram Table 4 8 AF Window setting - Correction of bit size description (Y_OUT_SIZE[12:8] -> Y_OUT_SIZE[11:8]) Table 5 22 Output crop setting - Correction of bit size description (Y_OUT_SIZE[12:8] -> Y_OUT_SIZE[11:8]) Table 5 35 Optical black level clamp related registers and descriptions - Correction of I2C Address description (MANUAL_DATA_PEDESTAL_ENABLE 0x30c2 -> 0x3090) (MANUAL_DATA_PEDESTAL_VALUE[9:8] 0x30c2 -> 0x3092) (MANUAL_DATA_PEDESTAL_VALUE[7:0] 0x30c3 -> 0x3093) Table 7 5 List of registers to be set only in SW-standby as mode transition. - Correction of I2C Address description (SHORT_FRAME_RS 0x3030 -> 0x3003) Table 7 9 Fast mode transition related register - Correction of I2C Address description (SHORT_FRAME_RS 0x0303-> 0x3003) Table 8 1 Integration time control and analogue gain control for HDR capture mode - Correction of bit size description ST_COARSE_INTEG_TIME -> ST_COARSE_INTEG_TIME[15:8] and

		ST_COARSE_INTEG_TIME[7:0] ANA_GAIN_GLOBAL -> ANA_GAIN_GLOBAL[8] and ANA_GAIN_GLOBAL[7:0] ST_ANA_GAIN_GLOBAL -> ST_ANA_GAIN_GLOBAL[8] and ST_ANA_GAIN_GLOBAL[7:0] Table 9 6 Long exposure mode related registers - Correction of I2C Address description (CIT_LSHIFT 0x3028 -> 0x3002) Table 9 20 Control Register for Master and Slave mode - Correction of I2C Address description (VDMY1_STA 0x5490 -> 0x5a90) (VDMY1_WID 0x5492 -> 0x5a92) (VDMY2_WID 0x5493 -> 0x5a93)
0.1.0	2016.02.09	Table 5-31 Digital gain setting - Correction of register upper byte range 5.5.2 Digital gain settings - Correction of calculating formula
0.1.1	2016.02.17	Table 9-20 Control Register for Master and Slave mode - Correction of register name and I2C Address description (MSTSLV 0x5A5C -> MASTER_SLAVE_SEL 0x3004) Figure 9-13 Communication control and timing with shared CCI Bus Figure 9-15 Communication control and timing with separated CCI Bus - Correction of register name description (MSTSLV -> MASTER_SLAVE_SEL) 9.8.2.CCI communication setting - Correction of CCI Address description
0.1.2	2016.02.24	9.8.5. Restriction of Dual camera usage with shared CCI bus - Correction of Dual camera setting description
1.0.0	2016.10.17	3.1.1 CSI lane mode − Add to description Table 3-3 CSI data format registers − Add to description Table 4-1 Imaging area determining registers − Add to horizontal direction analog cropping recommended value Table 4-4 Register that determine frame size. Table 5-24 Integration time setting register Table 7-3 List of corrupted frame causing registers Table 9-6 Long exposure mode related registers − Add to description 5.1.1 Clock system diagram − Add to description Table 5-12 Typical image output of main capture modes (3) Table 5-13 Typical image output of main capture modes (4)

		− Correction of image size 5.2.1 Image size related settings. − Add to description 5.2.5 Image size related functions − Correction of Scaling function 5.4.2. Integration time calculation − Add to LINE_LENGTH_PCK recommended value Table 5-32 Digital gain setting reference (0 to 23.9[dB]) − Correction of upper/lower value(2 times, 7 times and 10 times)
1.0.1	2017.07.03	Table 7-12 - Correction of analog gain value(Range : 0 to 480)

Note

In this specification, it covers the major F/W or H/W registers with functionality explanation, however the default value which set by Sony is not written. Because H/W or F/W defaults value is sometimes updated faster than document update timing. See "Register setting" (Excel sheet) for the latest default value shown as "Global Setting".

There are two types of “default value”.

- H/W default value: is a default value that is embedded with metal wiring into the silicon. It is decided in very early stage of device design and cannot be changed afterward. These values can be found in the Register Map.
- S/W default value: is a default valued that is recommended value and/or bug fix values to be externally over writing H/W default values after evaluation of engineering samples. These values are shown in “Register Setting”. Sony recommended register setting table or customer unique register setting table will be supplied upon request.

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Glossary

- **Color X-Talk**: the leakage of electron from mainly 4 nearby normal pixels of different color filter.
- **Contrast Value**: the value of strength of high-frequency component
- **CRA**: Chief Ray Angle
- **DAC value**: the value of digital analog converter of lens actuator(= the distance from image sensor to lens)
- **Defocus**: the degree of how blurred the image is (= the degree of how far the lens is from in-focus position)
- **Defocus Conversion Coefficient**: coefficient made in module manufacturing to convert phase difference to lens move amount (unit: DAC/pix)
- **DPC**: Defect Pixel Correction
- **Image Height**: the distance from optical light axis on image sensor
- **I2C**: Inter-Integrated Circuit (= serial bus description)
- **LSC**: Lens Shading Correction
- **MIPI**: Mobile Industry Processor Interface
- **OCL**: On Chip Lens
- **OTP**: One Time Programmable ROM
- **OIS**: Optical Image Stabilization(= the lens shifting function for avoiding blurring the image by hand shake)
- **PDAF**: Phase Detection Auto Focus
- **Register**: a small amount of storage in digital processor
- **Shield Pixel:** a pixel shielded nearly half with metal
- **SPC**: Shield Pixel Correction
-

1. System Outline

This sensor is a diagonal 5.867mm (Type1/3.06) 13Mega-pixel CMOS active pixel type stacked image sensor with a square pixel array. It adopts Exmor-RS™ technology to achieve high speed image capturing by column parallel ADC circuits and high sensitivity and low noise image.

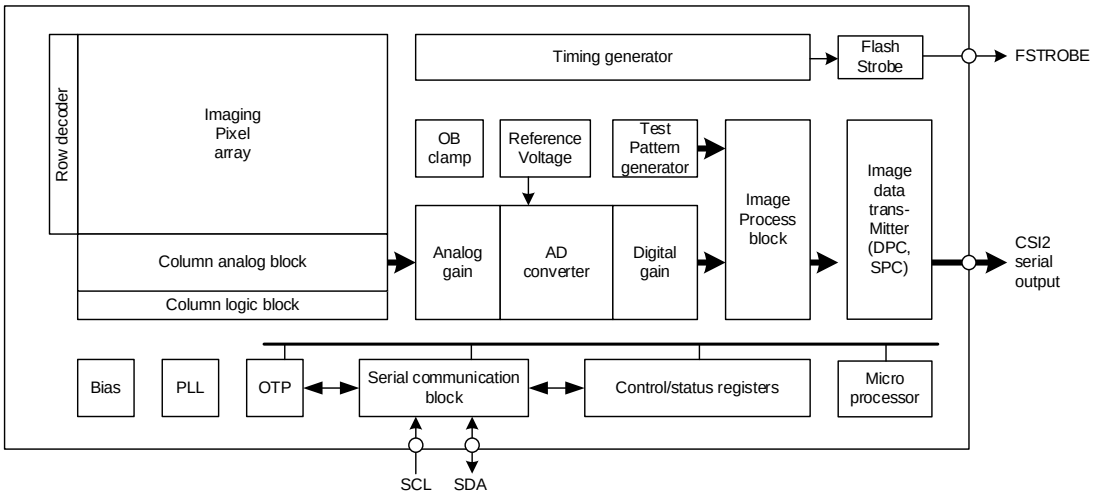

Figure 1-1 System block diagram

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2. Control Register Settings by Serial Communication

This sensor can use the 2-wire serial communication method for sensor control.

In this chapter, specification, method of 2-wire serial communication between the master device and this sensor is described.

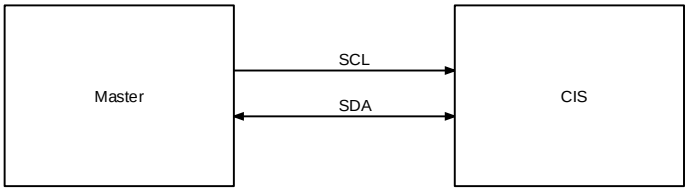

Figure 2-1 2-wire serial communication

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2.1. 2-wire serial communication operation specifications

The 2-wire serial communication method conforms to the camera control interface (CCI). CCI is an I2C Fast-mode Plus compatible interface, and the data transfer protocol is I2C standard.

This 2-wire serial communication circuit can be used to access the control-registers and status-registers of this sensor.

Table 2-1 Description of 2-wire serial communication pins

Pin name	Description
SDA	Serial data input/output pin
SCL	Serial clock input pin

The control registers and status registers of this sensor are mapped on the 16-bit address space. The register categories are shown below. Detail register information is shown in each chapter/section in this document and in Register Map.

Table 2-2 Abstract of register address map for 2-wire serial communication

	Address range	Description	Note
I^2C register	0x0000 - 0x0fff	Configuration register Read only and read/write dynamic register	
	0x1000 - 0x1fff	Reserved	

	0x2000 - 0x2fff	Reserved	
	0x3000 - 0x31ff	Manufacturer specified register	SONY customer register
	0x3200 - 0xffff	Manufacturer specified register	SONY internal register

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2.2. Communication protocol

2-wire serial communication supports a 16-bit register address and 8-bit data message type.

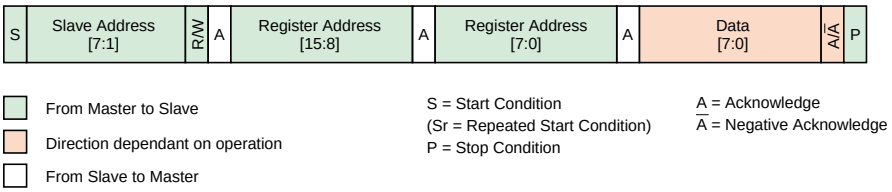

Figure 2-2 2-wire serial communication protocol

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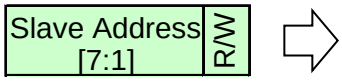
2.3. Default CCI slave address configuration

2.3.1. First slave address

This sensor has a default Camera Control Interface (CCI) or 1st I2C slave address shown below. When called by this slave address, the serial communication interface is activated. Duplication of the address on the same bus must be prevented. This slave address is controlled by hardware connection of SLASEL pin.



Slave Address (Read or Write) * See Table 2-3 for R/W bit	SLASEL (pin#43)
MSB LSB 0 0 1 1 0 1 0 R/W	L or NC
MSB LSB 0 0 1 0 0 0 0 R/W	H

R/W shows the direction of communication.

Figure 2-3 CCI (I2C) Slave address

Table 2-3 R/W bit

R/W bit	Direction of communication	Address
0	Write (master → sensor)	0: 0x34 or 0x20
1	Read (sensor → master)	1: 0x35 or 0x21

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2.3.2. Secondary slave address

In this sensor, 2nd I2C Slave address is available also. This value is fixed as 0x6c (0x6d in case of read timing). It can be switched On/Off by ”SLAVE_ADD_EN_2ND” and “SLAVE_ADD_ACKEN_2ND” for ACK to 2nd CCI. Refer to the table below.

Table 2-4 2nd CCI ACK control register

	Address	Bit	Name	Description
I2C register	0x3006	[0]	SLAVE_ADD_EN_2ND	2nd Slave Address Enable 0: disable 1: enable
	0x3007	[0]	SLAVE_ADD_ACKEN_2ND	2nd Slave Address Ack Enable 0: disable 1: enable

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2.3.3. Second CCI slave address for synchronous dual sensor operation

Two sensors are capable to be differently controlled by one host. In this case two sensors could be operated in parallel with even different integration time and gain while keeping synchronization each other. This kind of dual camera application requires having different first slave address and the same second address at the same time between the two sensors.

See “9.8 Dual camera” for more detail.

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2.4. Specification of communication bus state

2.4.1. Idle state

Idle state is specified as follows; neither master nor slave device drives the SDA or SCL, and these bus lines are pulled up to VDD via register.

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2.4.2. Issue “Start condition”

While the 2-wire communication bus is in idle state, master device (ex. subsequent image processing LSI, etc.) issues the communication-start: Start condition S by driving SDA from “High” to “Low” level. Serial data are transmitted in 8-bit-unit MSB first format. For every 8-bit data transmission, the slave device issues acknowledge or negative acknowledge (explained later). A (acknowledge)/Ā (negative acknowledge).

Data (SDA) is transmitted in sync with the SCL cycle. SDA toggles while SCL is “Low “and holds the value while SCL is “High”.

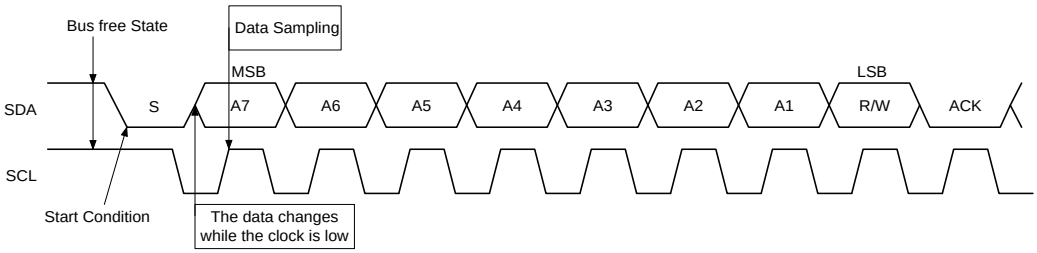

Figure 2-4 Start condition

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2.4.3. Issue “Stop condition”

After A (acknowledge)/Ā (negative acknowledge) and while SCL is High, master device issues communication-stop condition: “Stop condition” P by driving SDA from a low to high level. After issuing a “Stop condition”, master release 2-wire serial bus enters into an idle state.

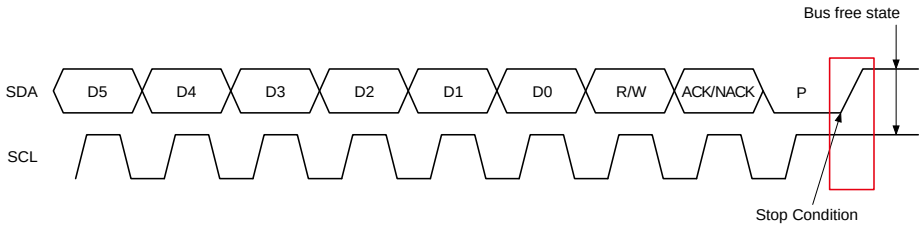

Figure 2-5 Stop condition

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2.4.4. Issue “Repeated start condition”

Master device can issue a start condition after previous transaction without issuing a stop condition. In this case this start condition is recognized as the “Repeated started condition” Sr.

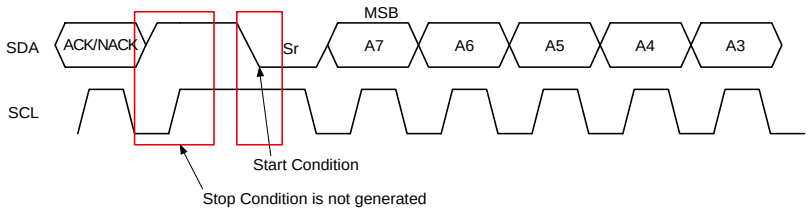

Figure 2-6 Repeated start condition

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2.4.5. Issue acknowledge/negative acknowledge

After transmitting each byte, a master or slave device issues an acknowledgement or negative acknowledgement and can release the bus to the idle state. When negative acknowledgement is issued, the master must issue the stop and terminate the communication immediately.

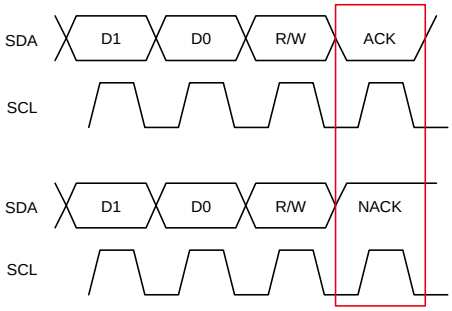

Figure 2-7 Acknowledge and negative acknowledge

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2.5. Read/write operation of 2-wire serial communication

This sensor has an index function that indicates which address is to be accessed. When reading/writing the value from/to a requested address, the master must set the address value to the index. Index value is designated by 2 bytes of dummy write operation after the slave address transmission. The index value is automatically incremented by “one” with the “Acknowledge/Negative Acknowledge” for the following data transfer.

This sensor supports four read modes and two write modes being compliant to Camera Control Interface (CCI).

Table 2-5 Read/Write operations supported by 2-wire serial communication

Access mode	1	CCI single read from random location (Single read from an arbitrary address)
	2	CCI single read from current location (Single read from the held address)
	3	CCI sequential read starting from random location (Sequential read starting from an arbitrary address)
	4	CCI sequential read starting from current location (Sequential read starting from the held address)
	5	CCI single write to random location (Single write to an arbitrary address)
	6	CCI sequential write starting from random location (Sequential write starting from an arbitrary address)

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2.5.1. CCI single read from random location

The upper part of the below figure below shows the sensor internal index value, and the lower part shows the SDA data flow. The master sets the sensor index value of M by designating the sensor slave address with a write request. Then the Master generates the Start condition. The Start condition is generated without generating the Stop condition, so it becomes the Repeated Start condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge followed immediately by the data at the index address on SDA. After the Master receives the data, it generates a Negative Acknowledge and the Stop condition to end the communication.

When reading single datum from the requested address register, the master device starts write-operation with the slave address of this sensor and by making 2 bytes of dummy write master sets the address value (M) to the index. After that master issues the “start condition” again instead of issuing a “stop condition”. This “start condition” is recognized as “repeated start condition”. Then transmitting the read request with the slave address, this sensor issues the “Acknowledge” and starts transmitting the register value from indexed address (M). Master issues the “Negative Acknowledge” and “stop condition” after receiving the transmission.

The figure below indicates the transition of index value and data on SDA line.

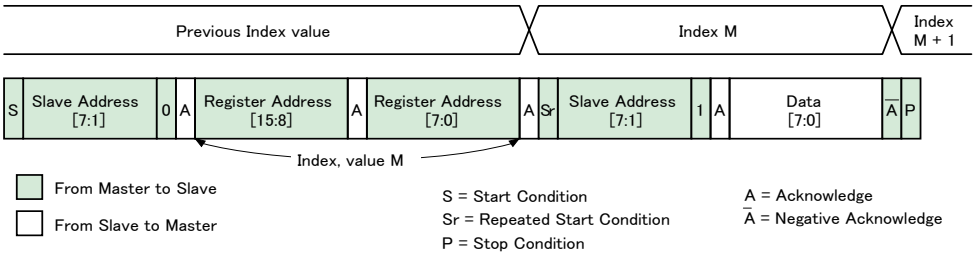

Figure 2-8 CCI single read from random location

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2.5.2. CCI single read from current location

When master transmits slave address, but does not designate an index, the previous value is held. And the index value is incremented at the “Acknowledge/Negative Acknowledge” after reading/writing the register value. When master knows the current index value is set to the requested address, master transmits the slave address and read request, then the value in the register appears on SDA line right after the “Acknowledge” issued by this sensor. Master issues the “Negative Acknowledge” and “Stop” and terminates the communication. Since the index value is incremented by “one” with this “Negative Acknowledge”, master can read the register value of the next address with the same procedure.

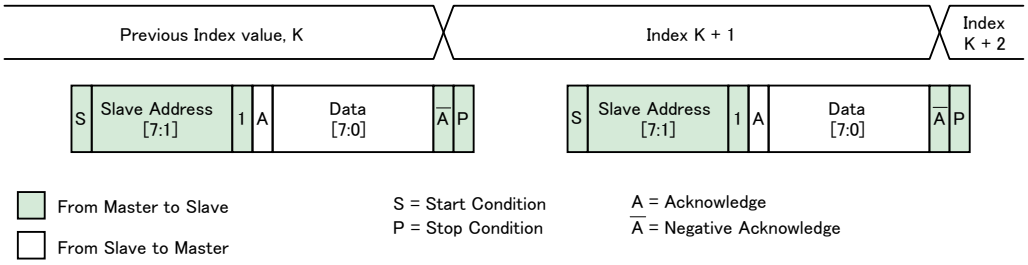

Figure 2-9 CCI single read from current location

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2.5.3. CCI sequential read starting from random location

When reading the data from an arbitrary address sequentially, master reads the first data by the similar procedure to “CCI single read from random location” but issues the “Acknowledge” instead of “Negative Acknowledge”, the index is incremented by “one” with this “Acknowledge” then master can

repeat the read operation. This operation is terminated when master issues the “Negative Acknowledge”, “Stop condition”, and the communication is terminated.

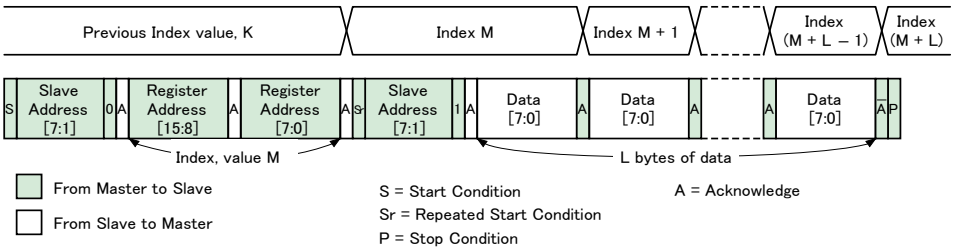

Figure 2-10 CCI sequential read starting from random location

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2.5.4. CCI sequential read starting from current location

When master knows the current index value is set to the requested address, master transmits the slave address and read request, then the value from the register appears on SDA line right after the “Acknowledge” issued by this sensor. Master issues the “Acknowledge” after receiving 1-byte of the data and this sensor continuously transmits the data from the next address of register since the index value is incremented by “one” with this “Acknowledge”. By repeating issue of the “Acknowledge” for every 1-byte reading, master can read the data sequentially. After reading necessary bytes of data, master issues “Negative Acknowledge” and “stop condition” and then terminates the communication.

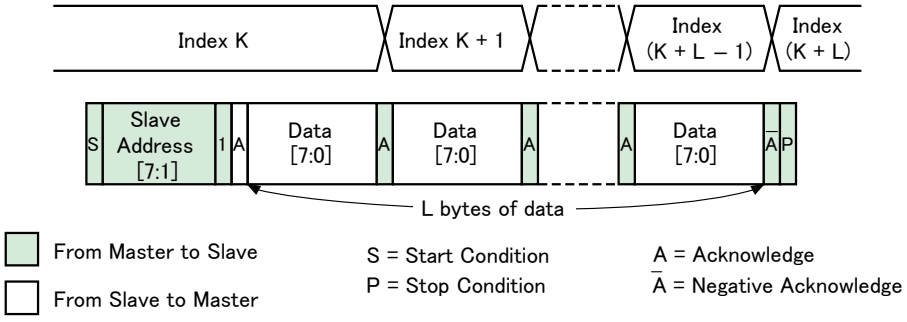

Figure 2-11 CCI sequential read starting from current location

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2.5.5. CCI single write to random location

When writing single datum to a register of target address, the master device starts write-operation with the slave address of this sensor and by making 2-bytes of dummy write master sets the address value (M) to the index. And then master transmits the data to be written to the register addressed by index value. Master issues “stop condition” after it transmits the data and terminates the communication

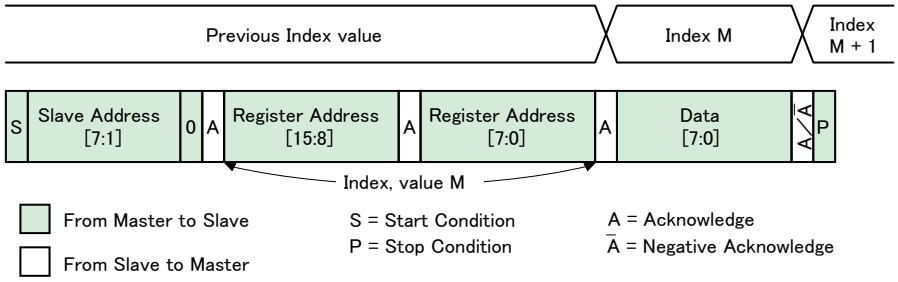

Figure 2-12 CCI single write to random location

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2.5.6. CCI sequential write starting from random location

When master writes the data sequentially from the requested address, master uses a similar procedure to do “CCI single write to random location” and without issuing a “stop condition” and continuously transmits the data after each “Acknowledge” issued. This sensor issues “Acknowledge” for each 1-byte write operation. After transmitting necessary data, master issues a “stop condition” and terminates the communication.

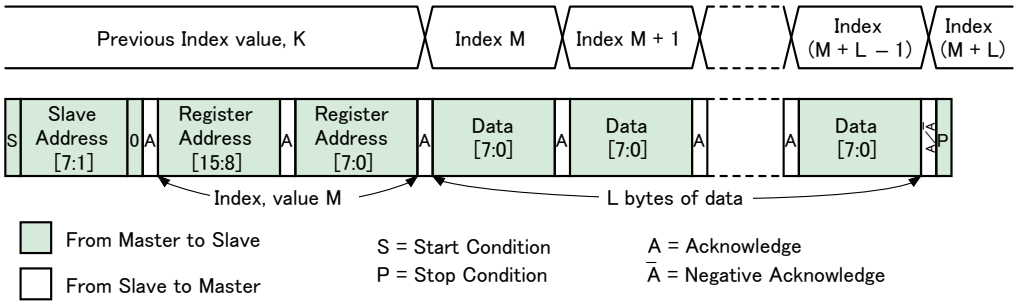

Figure 2-13 CCI sequential write starting from random location

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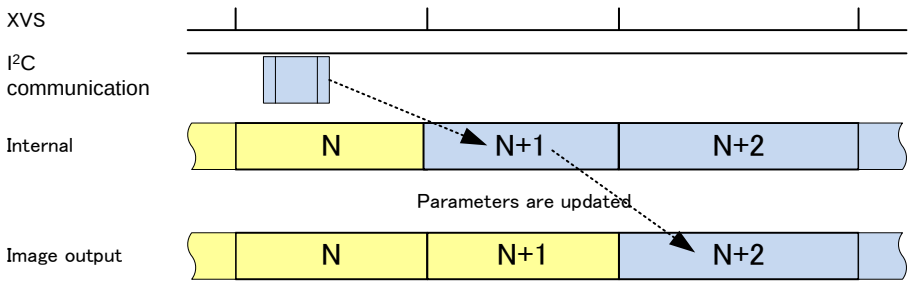
2.6. 2-wire serial communication register update timing

There are two types of registers in terms of the update timing of the transmitted data: the immediate type and the double buffered type. For immediate type registers, the transmitted data will be written to the registers immediately. As for the v-latched or double buffered type registers, the actual update timing of the register contents are controlled to the proper timing and become valid in the next frame. Users can transmit the commands regardless of the internal update timing of this sensor. The registers of double buffered types are indicated with "○"mark at the "reflection" column of "IMX258 Register Map".



* Example of integration time change.

Figure 2-14 2-wire serial communication register update timing diagram (v-latched or double buffered type registers)

Regarding the use case based CCI communications and reflection timings, refer to each sections as follows:

For reflection timing of capture mode transition, see 7.2 Streaming mode transition

For reflection timing of exposure time and gain change, see 7.3.3 AE bracketing

Cautions on pre-latch timing of double buffered registers

Retimed registers are pre-latched before V-sync for internal transaction.

Pre-latch timing exists several lines ahead of the embedded data (FS), and the timing changes depending on the operating condition settings. Registers written ahead of the pre-latch timing are updated internally during the next frame, however registers afterwards are updated internally but may be delayed a frame in addition to the normal update timings. The data transmission to be updated shall be completed within the communication period outlined in Figure2-15 in order to internally update the settings for the target frame; first frame for non-GPH registers and second frame for GPH registers after register settings.

The same timing rule applies for GPH release setting too.

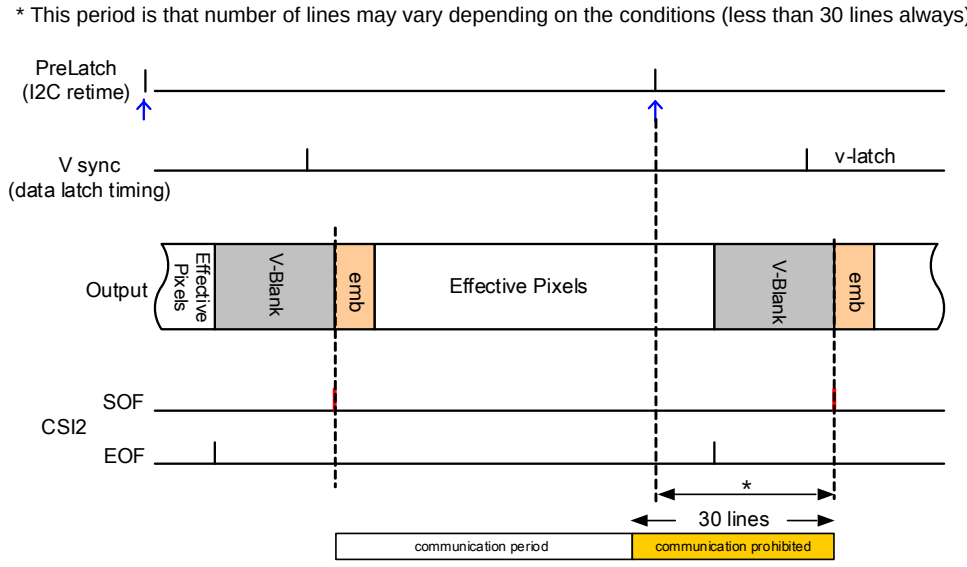


Figure 2-15 Pre-latch timing

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2.7. Grouped parameter hold function

2.7.1. Purpose and functional description of grouped parameter hold function

The image shooting parameters are assigned with many registers and they need to be changed within one frame period of the image. However the communication speed is limited and setting all of necessary registers might not be completed. So the double buffered type registers have the “grouped parameter hold” function to behave to be updated at once. While “grouped parameter hold” register is set to “1” the transmitted data are held in the buffer registers and after resets “grouped parameter hold” register to “0”, imaging parameter register values are updated as if they are transmitted at the same time and realize a smooth transition for changing the imaging condition.

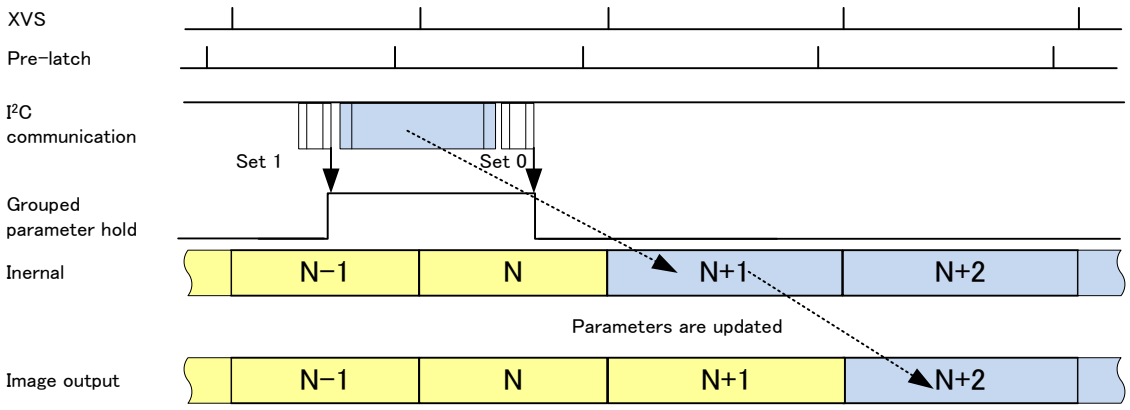
In this section, basic concept of the functionality and general ideas of application are explained. It is required to refer to individual sections for complete understanding on application. In such cases pointers to reference sections are also shown.

The register update timing using the “Group parameter hold function” is shown in Figure2-16. If the timing to set "Group parameter hold" from 1 to 0 is before the pre-latch timing, the register is updated internally during the next frame, however if it is afterwards, the update is delayed by 1 frame. It is

recommended to release GPH within the "communication period" outlined in Figure2-15 in order to update the register with the target timing.

Table 2-6 Grouped parameter hold function

	Address	Bit	Name	Description
I²C register	0x0104	[0]	GRP_PARAM_HOLD	This register is a hold control register for updating multiple parameters within the same frame. 0 : hold release 1 : hold



* Example of integration time change.

Figure 2-16 GRP_PARAM_HOLD function timing diagram

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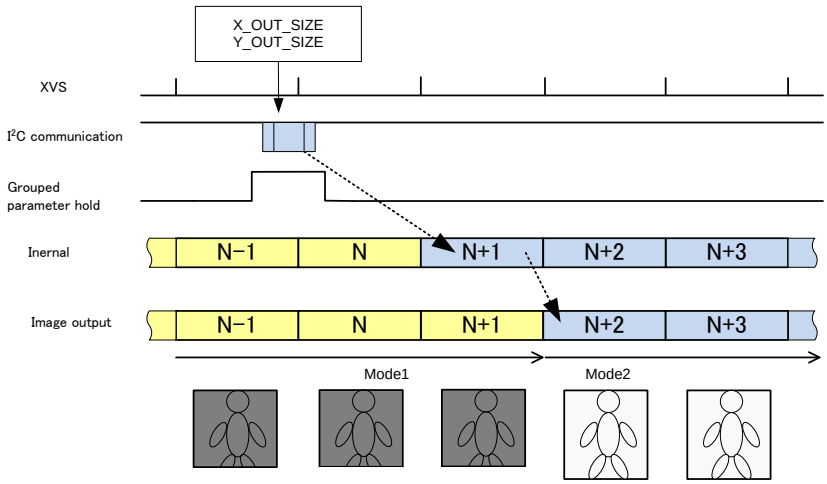
2.7.2. Example of mode transition using grouped parameter hold

An example of “On the fly” mode transition using "grouped parameter hold" is shown in the following chart. For more detail of “On the fly” mode transition, see section 7.2 and Appendix A-1.2



* Example of integration time change.

Figure 2-17 Mode transition using GRP_PARAM_HOLD

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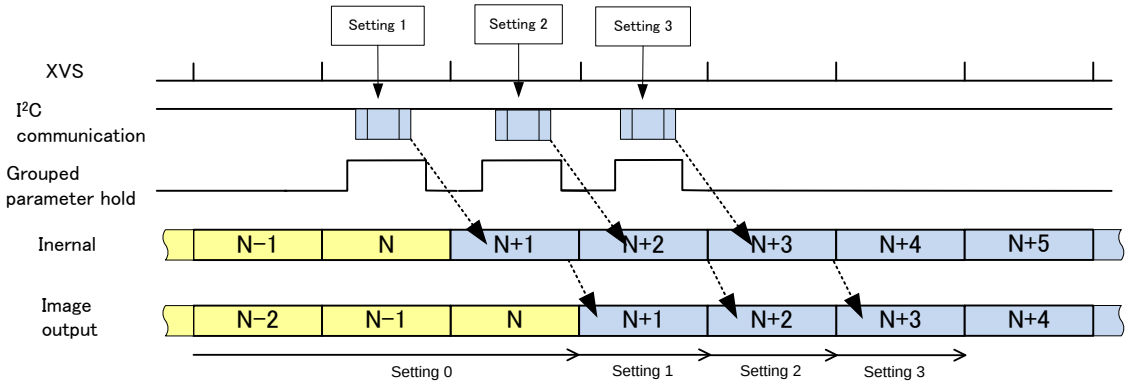
2.7.3. Example of using grouped parameter hold continuously

With this sensor, GPH can be used to update registers in continuous frames, unlikely from older product design. This is outlined in the following timing chart. Note that settings for both setting and resetting GPH must be completed within 1 frame ("communication period" shown in Figure2-15).



* Example of integration time change.

Figure 2-18 GRP_PARM_HOLD continuous frame register update

In 7.2 Streaming mode transition and gain feedback, you can find more about the grouped parameter function.

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3. Image Signal Interface

3.1. MIPI transmitter

This sensor outputs image signals by CSI2 high speed serial interface consisting of one pair of clock lines and four pairs of data lines. Refer to MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) version 1.10 and MIPI Alliance Specification for D-PHY version 1.1 for details. Because signals are transmitted in differential pairs, impedance (generally 100 Ω) between differential pairs near the receiver side during HS mode is required.

Otherwise, select a receiver with built-in impedance between differential pairs. Different delay times of differential pairs may reduce the input timing margin of ISP devices, which leads to malfunctions. Therefore, delay time within and among differential pairs must be as similar as possible in layout.

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3.1.1. CSI lane mode

Table 3-1 CSI lane mode register

	Address	Bit	Name	Description
I^2C register	0x0114	[1:0]	CSI_LANE_MODE	Number of lanes for CSI 0 : 1-lane *not supported 1 : 2-lane 2 : 3-lane *not supported 3 : 4-lane

* This sensor supports only 2Lane and 4Lane.

MIPI pins function as shown in the following table according to CSI_LANE_MODE.

If use 2-lane mode, please confirm with SONY.

Table 3-2 MIPI transmitter

	Pin name	2Lane	4Lane
MIPI transmitter	CKP/CKN	Clock lane	Clock lane
	D1P/D1N	Data lane 1	Data lane 1
	D2P/D2N	Data lane 2	Data lane 2
	D3P/D3N	Not used (LP only)	Data lane 3
	D4P/D4N	Not used (LP only)	Data lane 4

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3.1.2. CSI data format

The following register table specifies data format of the image output.

It sets data format from the options of output format as shown in the table below.

Table 3-3 CSI data format registers

	Address	Bit	Name	Description
I2C register	0x0112	[7:0]	CSI_DT_FMT_H [7:0]	The output data format for CSI CSI_DT_FMT_H : Uncompressed Data Bit Width CSI_DT_FMT_L : Compressed Data Bit Width 0x0808: RAW8 (Top 8 bits of pixel data) 0x0a0a: RAW10 Setup other than the above is forbidden. If use RAW8, please confirm with SONY.
	0x0113	[7:0]	CSI_DT_FMT_L [7:0]	

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3.1.3. CSI-2 bus

3.1.3.1. RAW8

The 8-bit Raw data transmission is performed by transmitting the pixel data over a CSI-2 bus. The following table specifies the packet size constraints for RAW8 packets. The length of each packet must be a multiple of the values in the table.

Table 3-4 Packet size constraints for RAW8 packet

Pixels	Bytes	Bits
1	1	8

Bit order in transmission follows the general CSI-2 rule, LSB first.

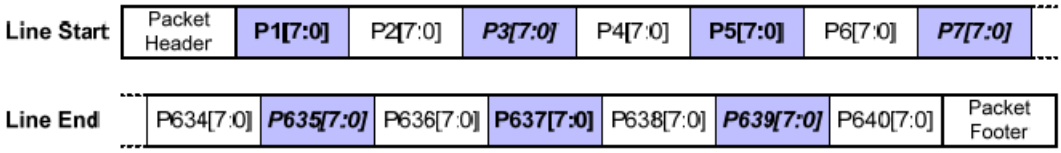

Figure 3-1 RAW8 transmission

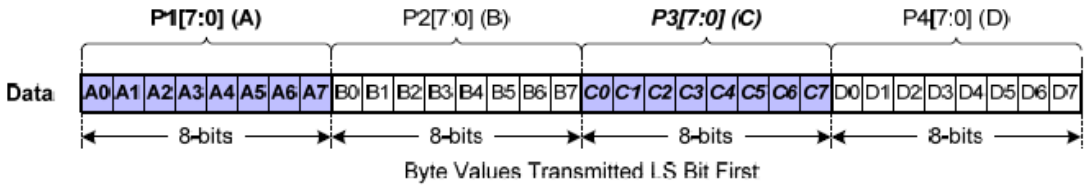

Figure 3-2 RAW8 data transmission on CSI-2 bus bitwise illustration

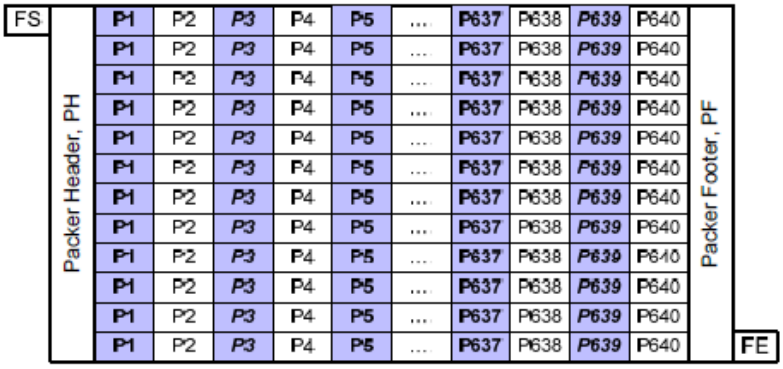

Figure 3-3 RAW8 frame format

3.1.3.2. RAW10

The transmission of 10-bit Raw data is accomplished by packing the 10-bit pixel data to look like 8-bit data format. The following table specifies the packet size constraints for RAW10 packets. The length of each packet must be a multiple of the values in the table.

Table 3-5 Packet size constraint for RAW10 packets

Pixels	Bytes	Bits
4	5	40

Bit order in transmission follows the general CSI-2 rule, LSB first.

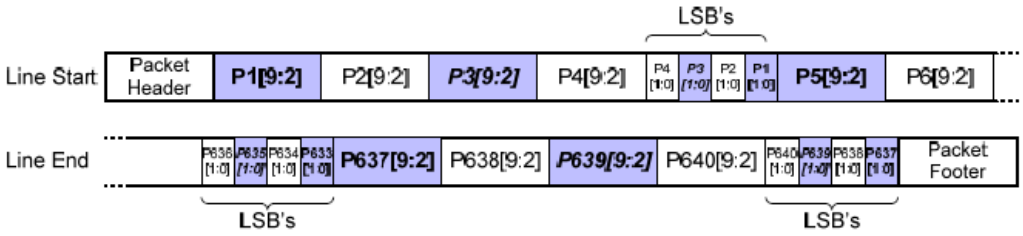

Figure 3-4 RAW10 transmission

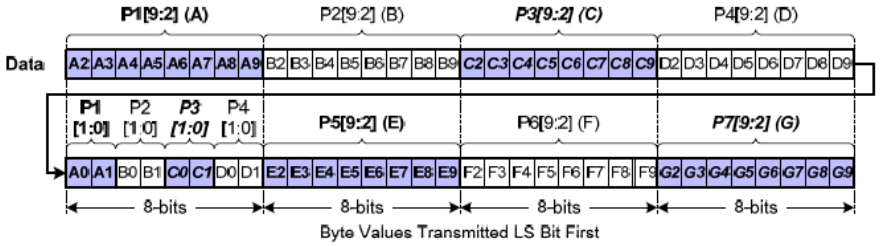

Figure 3-5 RAW10 data transmission on CSI-2 bus bitwise illustration

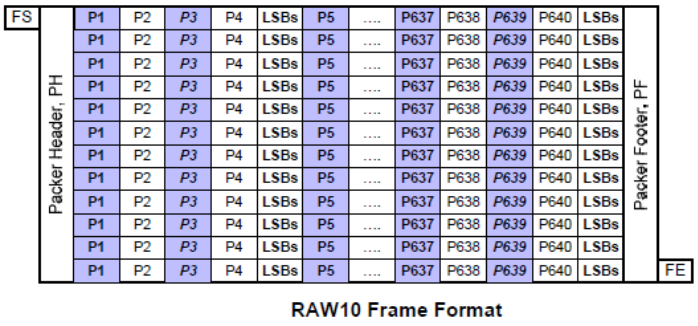

Figure 3-6 RAW10 frame format

3.1.3.3. BYTE2(only for Shield Pix data)

The transmission of 10-bit Shield pix data is accomplished by packing the 10-bit pixel data to look like 16-bit data format. One of Shield Pix data packet includes 6bit invalid “0” data. The following table specifies the packet size constraints for BYTE2 packets. The length of each packet must be a multiple of the values in the table.

Table 3-6 Packet size constraint for BYTE2 Shield Pix packets

Pixels	Bytes	Bits
4	8	64

Bit order in transmission follows the general CSI-2 rule, LSB first.

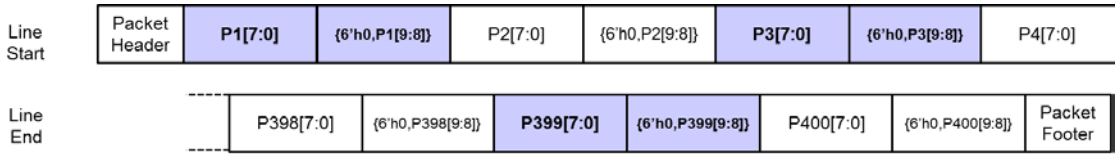

Figure 3-7 BYTE2 transmission

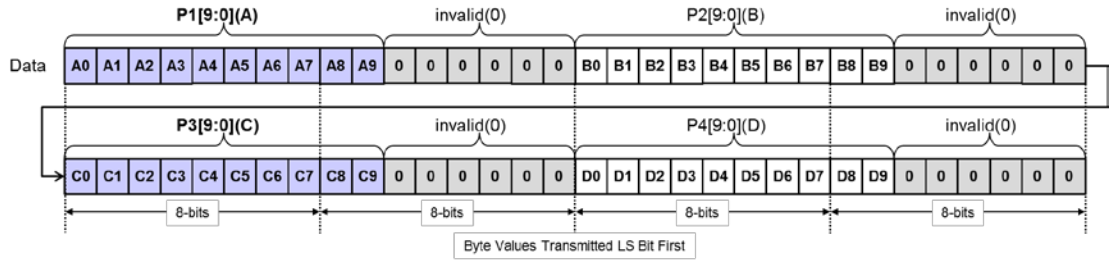

Figure 3-8 BYTE2 Shield Pix data transmission on CSI-2 bus bitwise illustration

3.1.4. MIPI Global Timing setting

MIPI Global Timing parameters are set with the registers below.

The setting method of MIPI Global Timing can be selected with the DPHY_CTRL register.

DPHY_CTRL=0, Use automatic control (Automatic Mode)

MIPI Global timing automatically set the appropriate value which is calculated by the below bitrate setting.

In case of PLL single mode (PLL_MULT_DRIV=0),

Bitrate = (PLL output frequency) / (OP Sys Clock Divider)

(PLL output frequency) = INCK × PLL_IVT_MPY / PREPLLCLK_VT_DIV

In case of PLL dual mode (PLL_MULT_DRIV=1)

Bitrate = (PLL output frequency) / (OP Sys Clock Divider)

(PLL output frequency) = INCK × PLL_IOP_MPY / PREPLLCK_OP_DIV

When externally set as DPHY_CTRL=1, MIPI Global Timing is automatically set using the values of REQ_LINK_BIT_RATE_MBPS and CSI_LANE_MODE.

Global Timing Setting is automatically set every time the setting of REQ_LINK_BIT_RATE_MBPS is changed.

The value of the REQ_LINK_BIT_RATE_MBPS can be obtained from the following relational equation.

REQ_LINK_BIT_RATE_MBPS = Output bitrate * (CSI_LANE_MODE +1)

Where Output bitrate = OPPXCK * CSI_DT_FMT_L[7:0]

* REQ_LINK_BIT_RATE[31:0] consist of integer part (REQ_LINK_BIT_RATE_MBPS[31:16]) and decimal part (REQ_LINK_BIT_RATE_MBS[15:0]).

* For IOPPXCK, more detail refers to “5.1.4 IOPPXCK Clock”.

When set as DPHY_CTRL=2, Global Timing must be set with registers from 0x080a to 0x0819 manually.

Table 3-7 MIPI Global timing setting

	Address	Bit	Name	Description
I²C register	0x0808	[1:0]	DPHY_CTRL	MIPI Global Timing control selection 0 : automatic control 1 : UI control 2 : register control 3 : reserved
	0x080a	[0]	TCLK_POST_EX [8]	MIPI Global Timing (Tclk)
	0x080b	[7:0]	TCLK_POST_EX [7:0]	
	0x080c	[0]	THS_PREPARE_EX [8]	MIPI Global Timing (Ths_prepare)
	0x080d	[7:0]	THS_PREPARE_EX [7:0]	
	0x080e	[0]	THS_ZERO_MIN_EX [8]	MIPI Global Timing (Ths_zero_min)
	0x080f	[7:0]	THS_ZERO_MIN_EX [7:0]	
	0x0810	[0]	THS_TRAIL_EX [8]	MIPI Global Timing (Ths_trail)
	0x0811	[7:0]	THS_TRAIL_EX [7:0]	
	0x0812	[0]	TCLK_TRAIL_MIN_EX [8]	MIPI Global Timing (Tclk_trail_min)
	0x0813	[7:0]	TCLK_TRAIL_MIN_EX [7:0]	
	0x0814	[0]	TCLK_PREPARE_EX [8]	MIPI Global Timing (Tclk_prepare)
	0x0815	[7:0]	TCLK_PREPARE_EX [7:0]	
	0x0816	[0]	TCLK_ZERO_EX [8]	MIPI Global Timing (Tclk_zero)
	0x0817	[7:0]	TCLK_ZERO_EX [7:0]	
	0x0818	[0]	TLPX_EX [8]	MIPI Global Timing (Tlpx)
	0x0819	[7:0]	TLPX_EX [7:0]	
	0x0820	[7:0]	REQ_LINK_BIT_RATE_MBPS[31:24]	Output Data Rate [Mbps] Bit[32:16] integer Bit[15:0] decimal
	0x0821	[7:0]	REQ_LINK_BIT_RATE_MBPS[23:16]	
	0x0822	[7:0]	REQ_LINK_BIT_RATE_MBPS[15:8]	
	0x0823	[7:0]	REQ_LINK_BIT_RATE_MBPS[7:0]	

3.1.5. CLK mode during Frame blanking

This is a function to stop the MIPI clock during Frame Blanking.

The details of the register and timing are shown below.

Table 3-8 CLK mode setting register during Frame Blanking

	Address	Bit	Name	Description
I²C register	0x4040	[0]	CLBLANKSTOP	CLBLANKSTOP Control RUN/STOP of CSI2 during Frame Blanking 0 : Stay in HS mode (Clock/Strobe output) during CLK Frame Blanking 1 : Transition to LP11 (Clock/Strobe stop) during CLK Frame Blanking Details are as follows: - When a valid frame starts, transition to HS-Clock status. - When the frame ends (after EOF output), transition from HS-Clock to LP11.

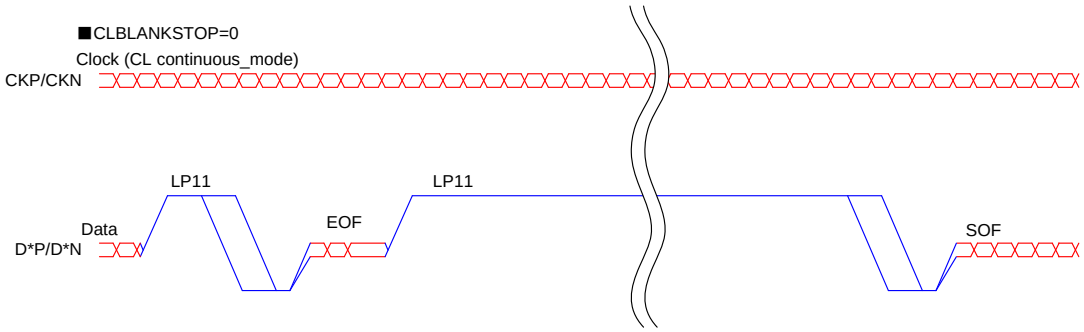

Figure 3-9 CLK mode during Frame Blanking (CLBLANKSTOP=0)

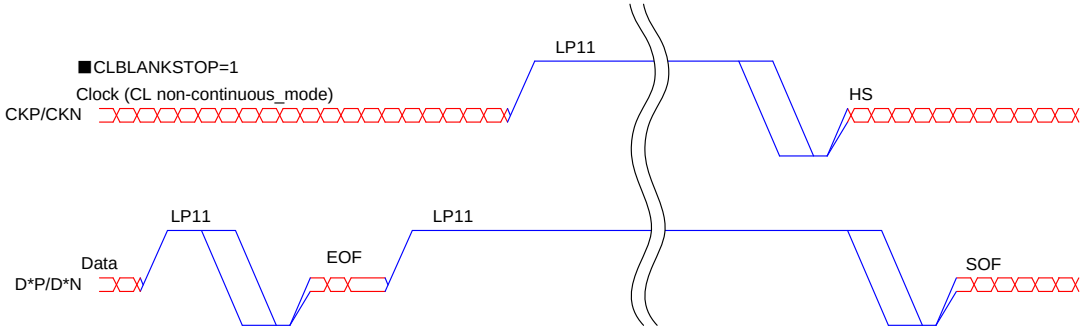

Figure 3-10 CLK mode during Frame Blanking (CLBLANKSTOP=1)

4. Image Readout Operation

In this chapter, you can find relations among imaging area, pixel readout orientation/readout and transmission frame/signal structure.

By setting the parameters of PLL, image size, start/end position of the imaging area, direction of reading image, binning, shutter mode, integration time, gain, and output format via 2-wire serial communication, this sensor outputs the image data.

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4.1. Physical alignment of imaging pixel array

The figure below shows the physical alignment of the imaging pixel array with pin #1 located at the upper left corner.

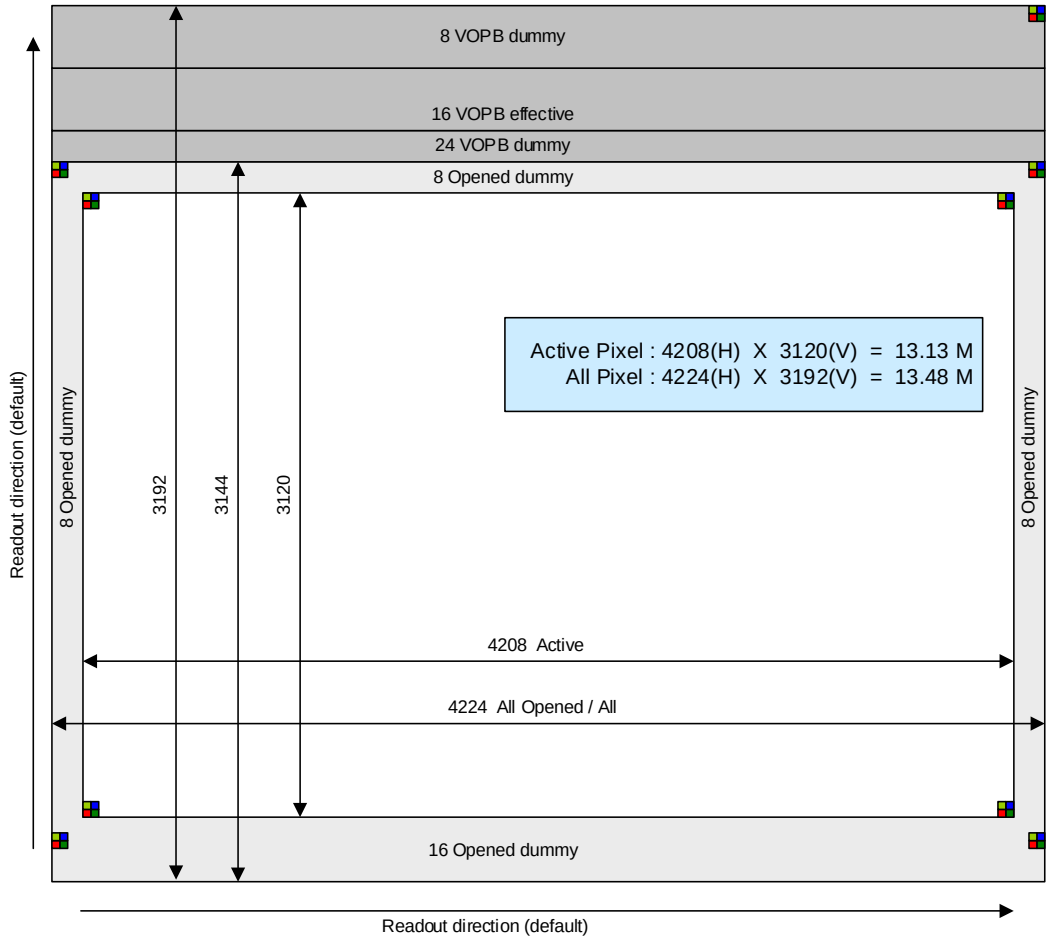

Figure 4-1 Physical alignment of imaging pixel array

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4.2. Color coding and order of reading image data

The original color filter arrangement of the sensor is shown in the figure below. Gr and Gb are the G signals shown at the same line as R signals and B signals respectively. The line with R & Gr signals and the line with Gb & B signals are output alternating one after the other.

In the case of HDR, Long Exposure line is read first.

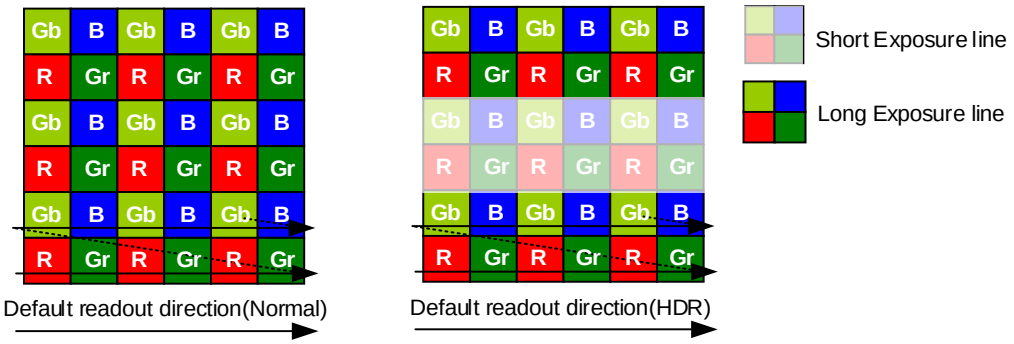

Figure 4-2 Color coding alignment

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4.3. Imaging area determination

Imaging area is specified on the output signal with physical coordinate with lower left as (0, 0) and determined by registers shown as below.

Table 4-1 Imaging area determining registers

	Address	Bit	Name	Description
I²C register	0x0344	[4:0]	X_ADD_STA [12:8]	Horizontal direction analog cropping start position within the active pixels area Unit : pixels Format : 13-bit unsigned integer * Note that this is the cropping end position when mirroring (IMG_ORIENTATION_H=1) * Recommended value is 0d. Any other value change require, please confirm with SONY.
	0x0345	[7:0]	X_ADD_STA [7:0]	
	0x0346	[3:0]	Y_ADD_STA [11:8]	Vertical direction analog cropping start position within the active pixels area Unit : pixels Format : 12-bit unsigned integer * Note that this is the cropping end position when flipping (IMG_ORIENTATION_V=1)
	0x0347	[7:0]	Y_ADD_STA [7:0]	
	0x0348	[4:0]	X_ADD_END [12:8]	Horizontal direction analog cropping end position within the active pixels area Unit : pixels Format : 13-bit unsigned integer * Note that this is the cropping start position when mirroring (IMG_ORIENTATION_H=1) * Recommended value is 4207d. Any other value change require, please confirm with SONY.
	0x0349	[7:0]	X_ADD_END [7:0]	
	0x034a	[3:0]	Y_ADD_END [11:8]	Vertical direction analog cropping end position within the active pixels area Unit : pixels Format : 12-bit unsigned integer * Note that this is the cropping start position when flipping (IMG_ORIENTATION_V=1)
	0x034b	[7:0]	Y_ADD_END [7:0]	

Above settings shall be always set based on full pixel basis even in binning mode.

There are capture mode and/or binning mode dependent restrictions in setting Imaging area as shown in the following table.

Table 4-2 Register setting Restrictions list for each mode

	Mode								
	Full-pixel (Normal)	H:2-scale V:2- sub (Normal)	H:2-scale, V:2-bin (Normal)	H:4 - scale, V:2- bin& 2-sub (Normal)	H:4-scale. V:4-bin (Normal)	H:8 scale, V:4- bin& 2-sub (Normal)	H:3-scale V:3-bin (Normal)	H:3-scale V:3-b (Normal)	Full-pixel (HDR)
Y_ADD_STA	multiples of 2	multiples of 4	multiples of 4	multiples of 8	multiples of 8	multiples of 16	multiples of 4	multiples of 4	multiples of 4
Y_ADD_END – Y_ADD_STA+ 1	multiples of 2	multiples of 4	multiples of 4	multiples of 8	multiples of 8	multiples of 16	multiples of 6	multiples of 6	multiples of 4
X_ADD_STA	multiples of 2	multiples of 2	multiples of 2	multiples of 2	multiples of 2	multiples of 2	multiples of 2	multiples of 2	multiples of 2
X_ADD_END – X_ADD_STA + 1	multiples of 2	multiples of 2	multiples of 2	multiples of 2	multiples of 2	multiples of 2	multiples of 2	multiples of 2	multiples of 2

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4.4. Readout start position

Default readout position of this sensor starts from the lower left whenever PIN1 is placed at the upper left corner. Because the lens will invert the image both vertically and horizontally, the proper image can be achieved when PIN1 is placed at the upper left corner.

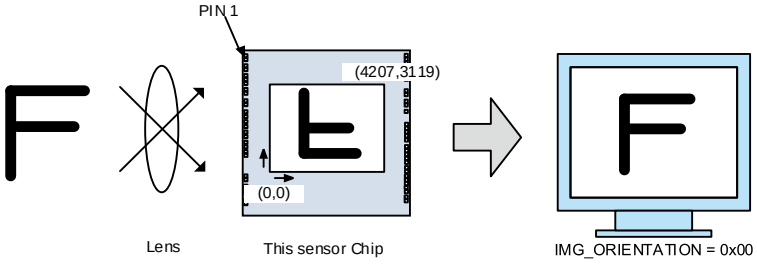
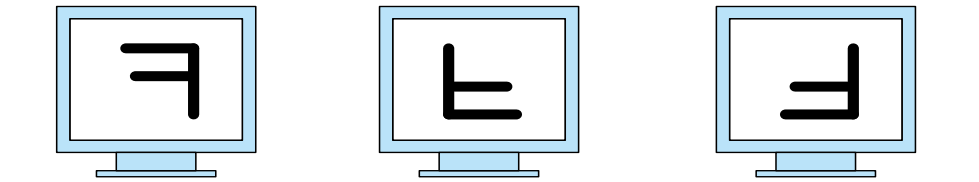


Figure 4-3 Readout start position

Vertical flip and horizontal mirror readout modes can be specified by the register below. When the readout direction is changed, the color of the first pixel (R/Gr/Gb/B) read out also changes with it.

Table 4-3 Vertical flip and horizontal mirror

	Address	bit	Name	Description
I²C register	0x0101	[1]	IMG_ORIENTATION_V	Image orientation for Vertical direction 0 : normal 1 : reverse
		[0]	IMG_ORIENTATION_H	Image orientation for Horizontal direction 0 : normal 1 : reverse



IMAGE_ORIENTATION = 0x01 IMAGE_ORIENTATION = 0x02 IMAGE_ORIENTATION = 0x03

Figure 4-4 Read out image for each combination of flip and mirror

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4.5. Frame structure

Each line of each image frame will be output according to the General Frame Format of CSI2 specification. A period of time from the line end sync code (Packet Footer (PF)) to the line start sync code (Packet Header (PH)) of the next line is called “line blanking”.

Similarly, a period of time from the frame end sync code (Frame End (FE)) to the frame start sync code (Frame Start (FS)) of the next frame is called “frame blanking”.

Frame size is determined by “FRM_LENGTH_LINES” in the vertical direction and “LINE_LENGTH_PCK” in the horizontal direction.

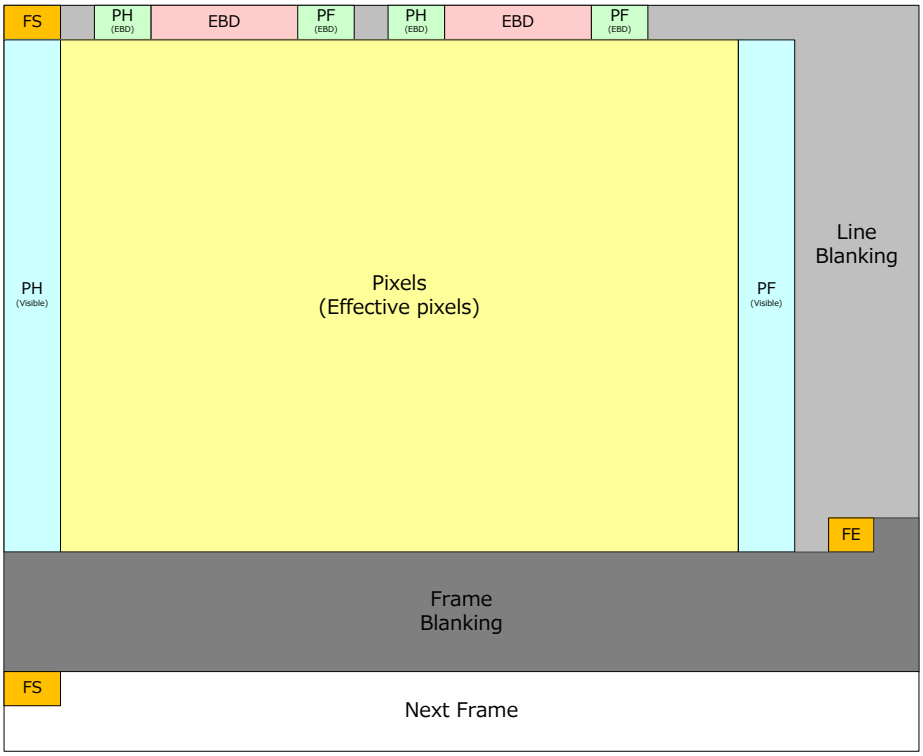

Figure 4-5 Frame structure (Normal)

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4.5.1. Registers that determine frame size

Table 4-4 Registers that determine frame size

	address	bit	name	description
I²C register	0x0340	[7:0]	FRM_LENGTH_LINES [15:8]	The length of frame Unit : lines Format : 16-bit unsigned integer *set value for given capture mode ≦ 65525d
	0x0341	[7:0]	FRM_LENGTH_LINES [7:0]	
	0x0342	[7:0]	LINE_LENGTH_PCK [15:8]	The length of line Unit : pixels Format : 16-bit unsigned integer * Set to 5352d. Any other value change require, please confirm with SONY.
	0x0343	[7:0]	LINE_LENGTH_PCK [7:0]	

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4.6. Output image format

This is the output image diagram of full pixel output mode, Image data is output from the upper left corner of the diagram.

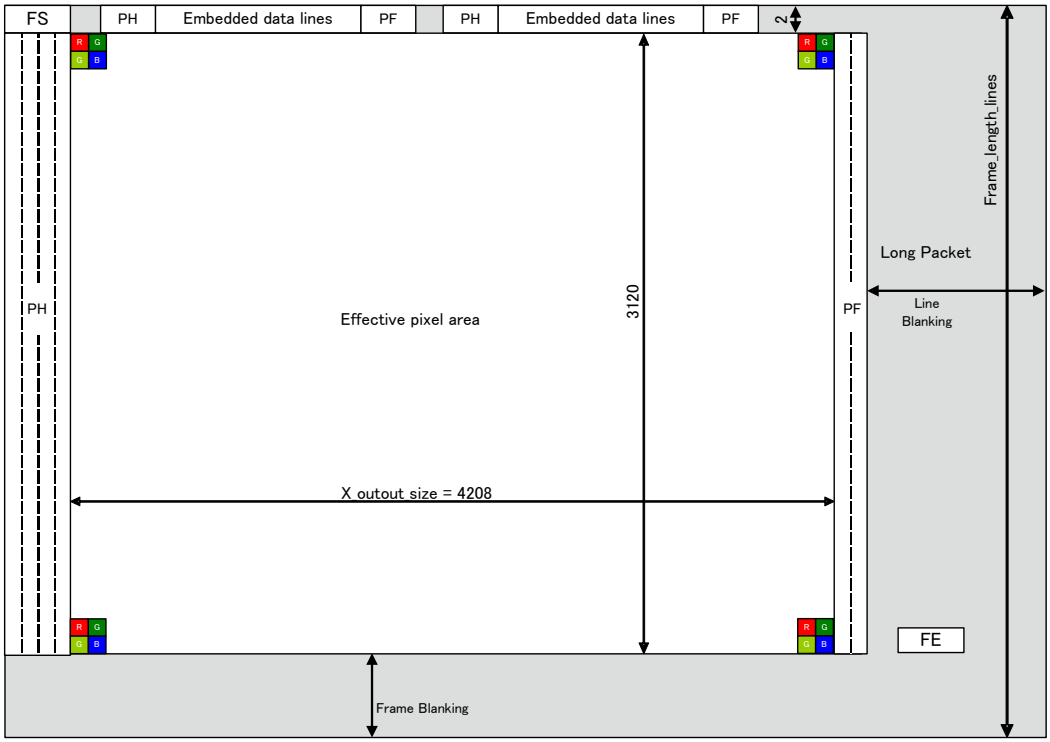

Figure 4-6 Full pixel output mode image data structure

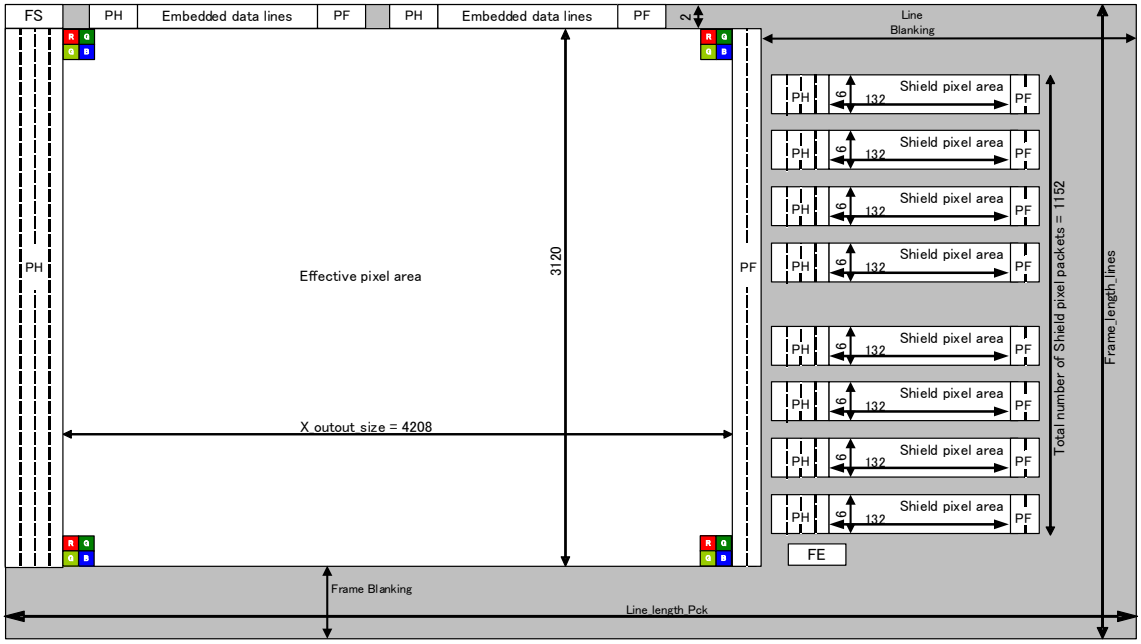

Figure 4-7 Full pixel output mode image data structure (ALL ON, RAW10 Shield pixel)

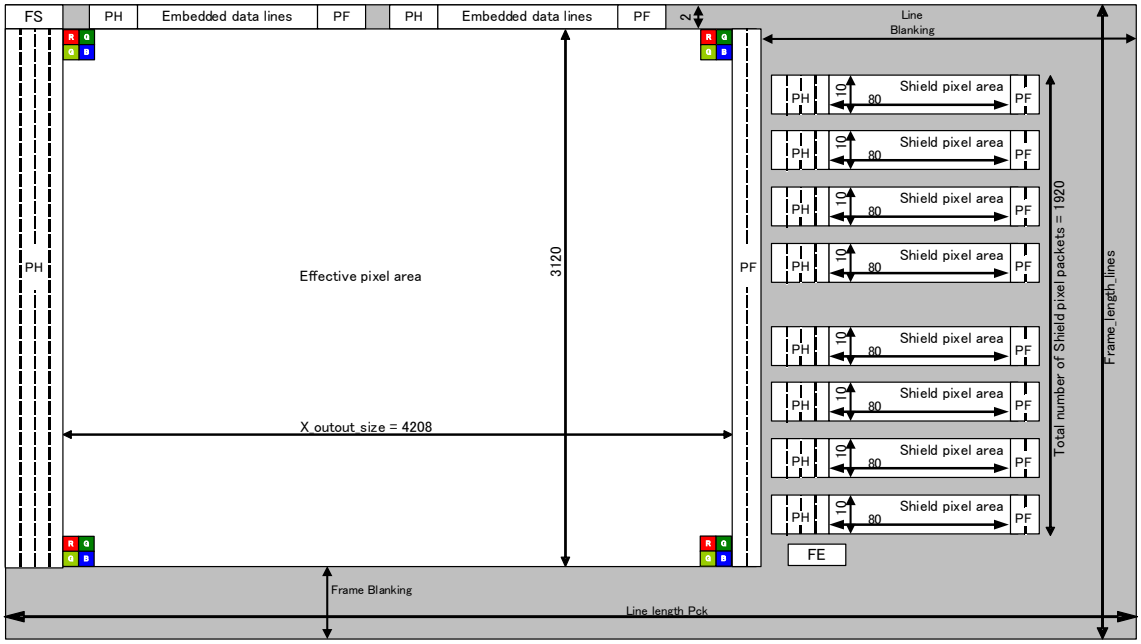

Figure 4-8 Full pixel output mode image data structure (ALL ON, BYTE2 Shield pixel)

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4.6.1. Shield Pixels data control

Shield pixels data can be output as a packet different from normal image data during the line blanking period. In addition, for outputting the Shield pixels data through MIPI, it is requested to set PHASE_PIX_OUTEN. It is possible to select Shield pixels data format(RAW10 or BYTE2) by set PDPIX_DATA_RATE.

Shield pixels data X Size is changed by Shield pixels data format. When RAW10, X Size is 132, When BYTE2 , X Size is 80. Y size is calculated automatically.

Table 4-5 Shield pixels data output control

	Address	bit	Name	Description
I²C register	0x3030	[0]	PHASE_PIX_OUTEN	Shield pixels data output ON/OFF control. *1 1:Enable (Output ON) 0:Disable (Output OFF)
	0x3032	[7:0]	PDPIX_DATA_RATE	Shield pixels data format 0:RAW10 1:BYTE2

*1 : Shield pixels data output is supported only Full-pix, HDR and V 1/2 Sub-sampling

It is not possible to set “1”(Enable) for PHASE_PIX_OUTEN during other mode.

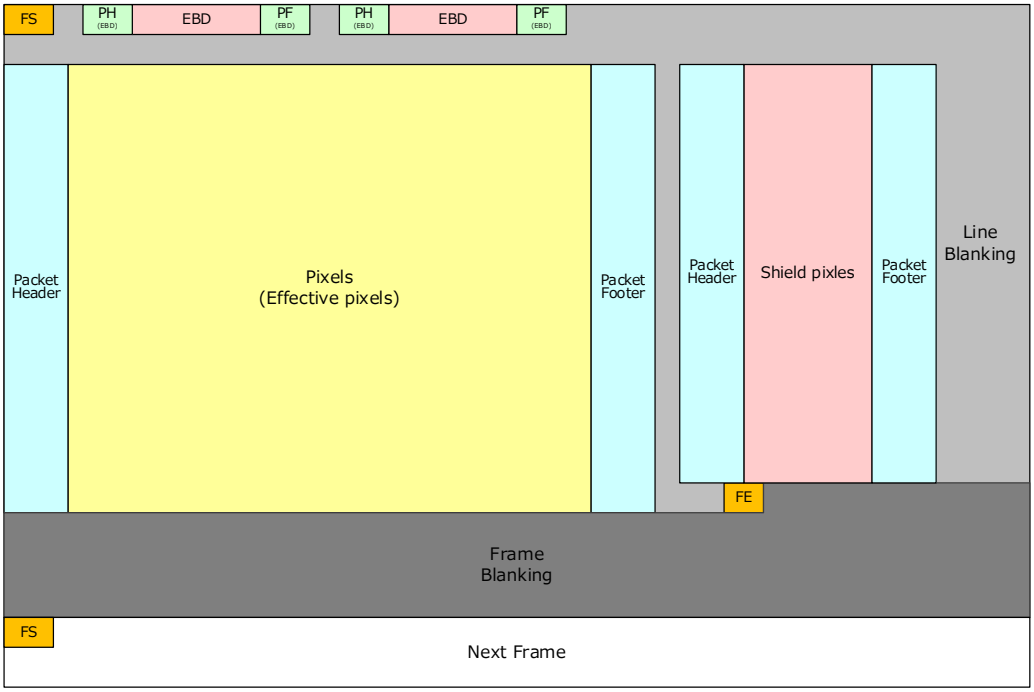


Figure 4-9 Frame Structure (Shield pixels data OUT)

Packet header (PH) of both left and right shield pixels are the same. Please judge left or right shield pixel from its physical arrangement

Shield pixels output in one line is divided into multiple packets. Number of shield pixels one packet can hold differs between RAW10 and BYTE2 format.

Table 4-6 Max number of Shield pixel in one packet

Shield pixels data format	Max number of Shield pixel in one packet
RAW10	132[pix]
BYTE2	80[pix]

If total number of Shield pixels in one line is larger than the number of Shield pixel that one packet can hold (i.e. Max number of Shield pixel in one packet), Shield pixel output will be divided into several packets. All packets have the same size adjusted by using padding data (padding data value is 0). See Figure 4-10 and Figure 4-11.

In case Shield Pixel output overlaps with each other, the latter packet will be delayed for one line. (See Figure 4-11)

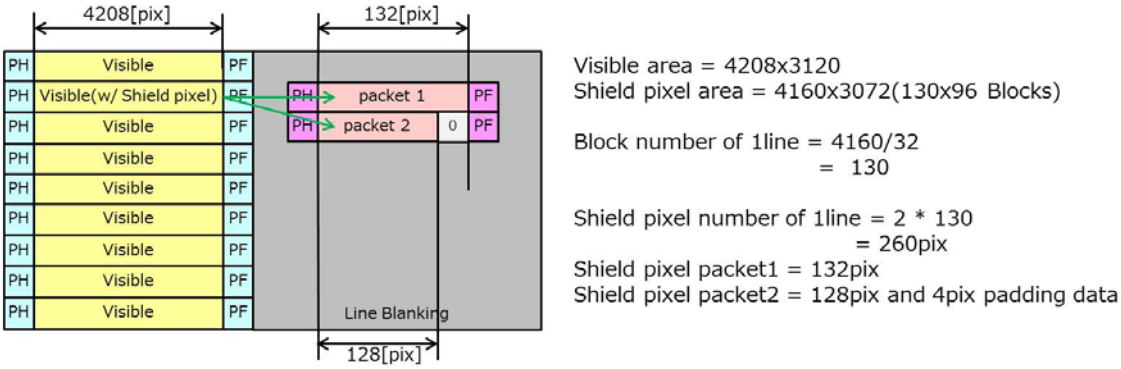


Figure 4-10 Shield pixel packet size(RAW10)

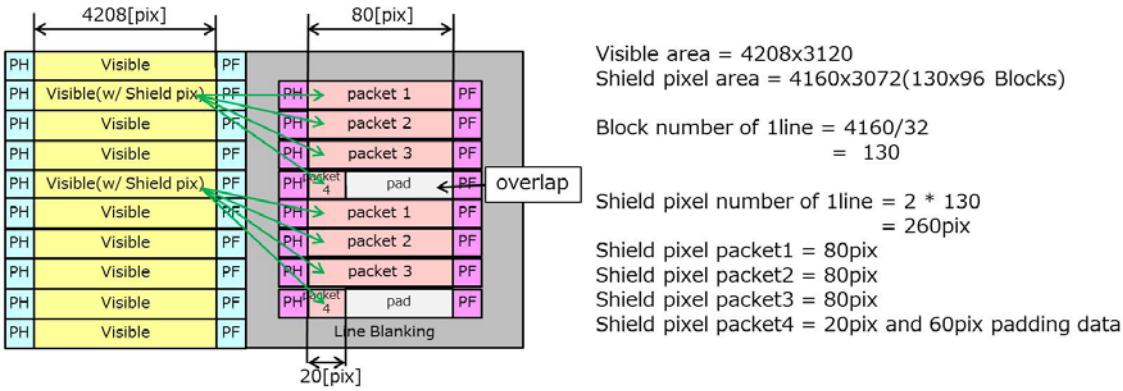
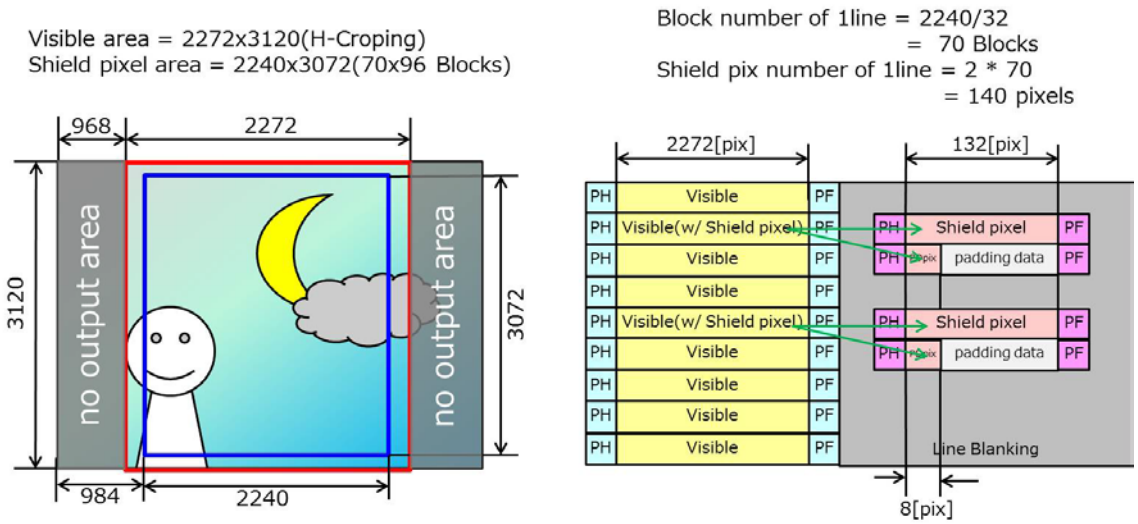


Figure 4-11 Shield pixel packet size(BYTE2)

Shield pixel number is changed by H-Cropping setting or AF Window[*1] setting. An example of Shield pixel packet size with H-Cropping and AF Window[*1] is shown as below.

*1 : See 4.6.1.2 AF Window Specification



Total Shield pix = 140pix(packet1 : 132 pix, packet2 : 8 pix)
Total number of visible packets = 2272
Total number of Shield pixel packets = 1152(96[blocks] * 2[Shield pix pixels] * 6[packets])
*include of all 0 packet(See 4.6.1.1 Output timing and data range)

Figure 4-12 Shield pixel output with H-Cropping and AF Window

No matter vertical readout direction flips, alignment of right and left Shield pixel packet will not change. (L -> R -> R -> L)

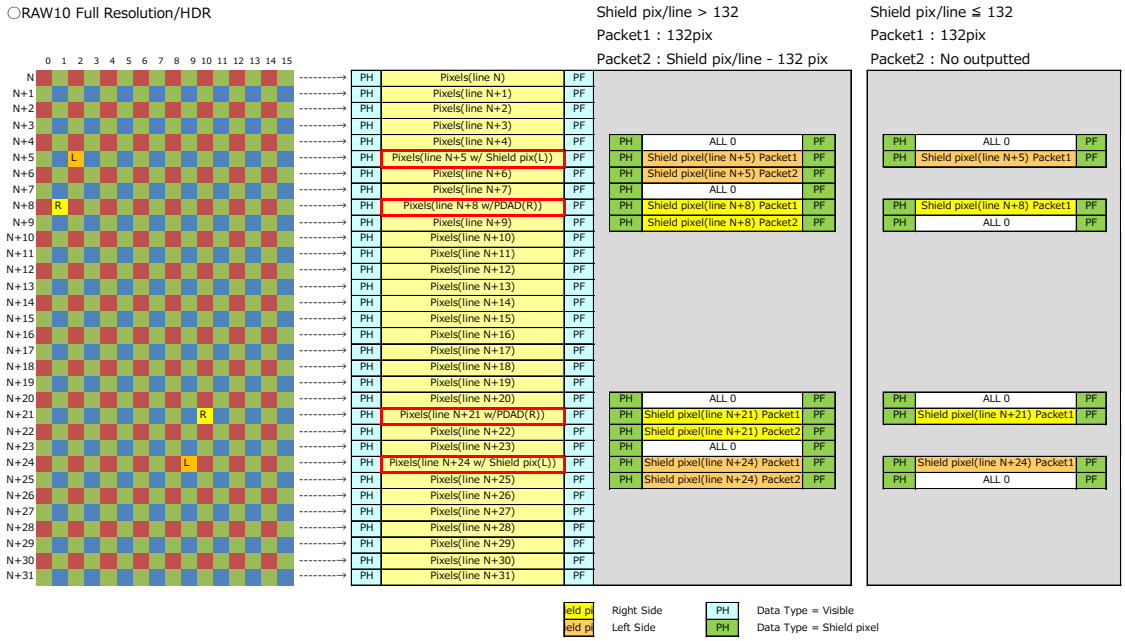


Figure 4-13　Shield pixel output variation (RAW10 Full/HDR)

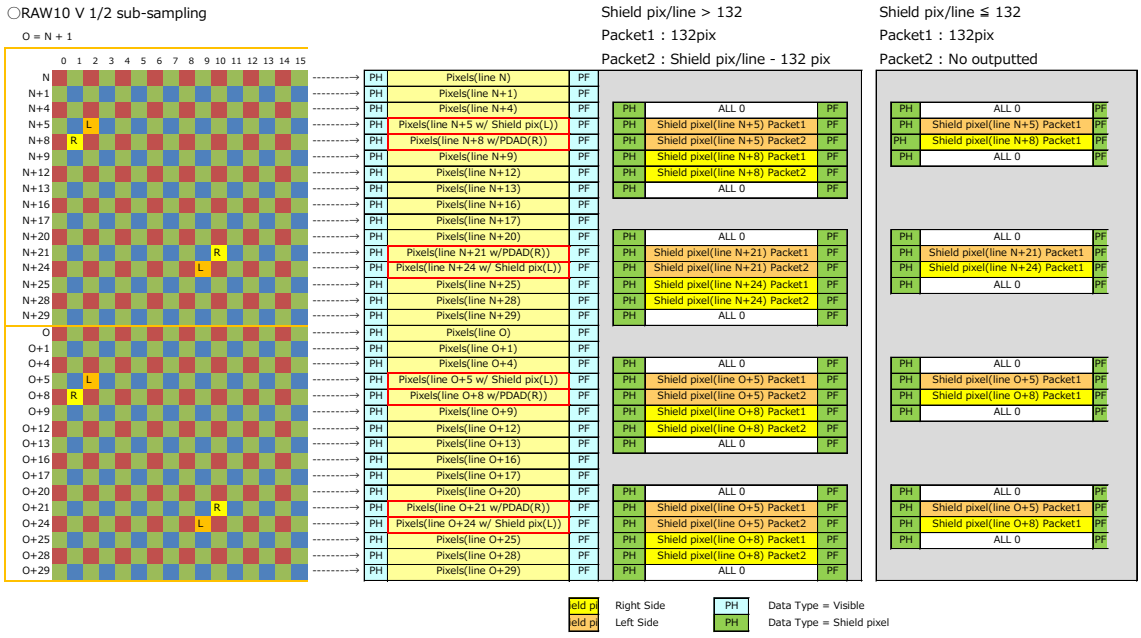


Figure 4-14　Shield pixel output variation (RAW10 V 1/2 Sub-sampling)

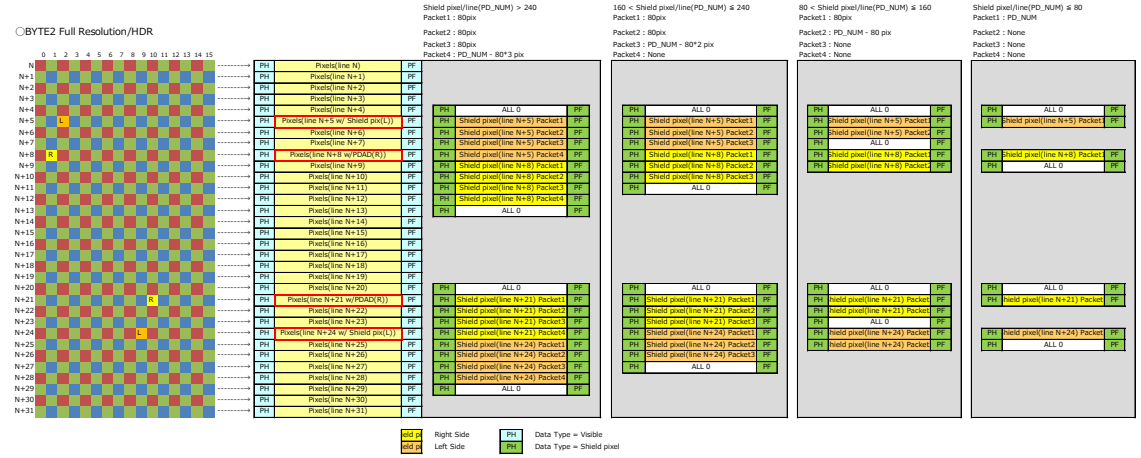


Figure 4-15 Shield pixel output variation (BYTE2 Full/HDR)

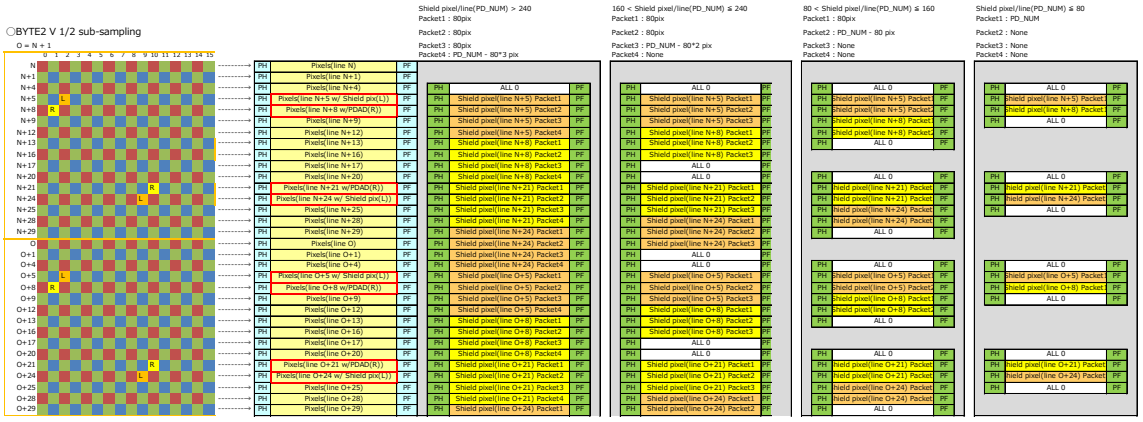


Figure 4-16 Shield pixel output variation (BYTE2 V 1/2 Sub-sampling)

4.6.1.1. Output timing and data range

This sensor begins output of Shield pixel packet only from tail of even(0,2,4…) visible packets and finishes output of Shield pixel packet only from tail of odd(1,3,5…) visible packets.

When Shield pixels exist in odd line, all tails of even and odd visible packets output 0.

If Shield pixel output is overlapped, all 0 packets output mentioned above will not occur. (See Figure 4-17)

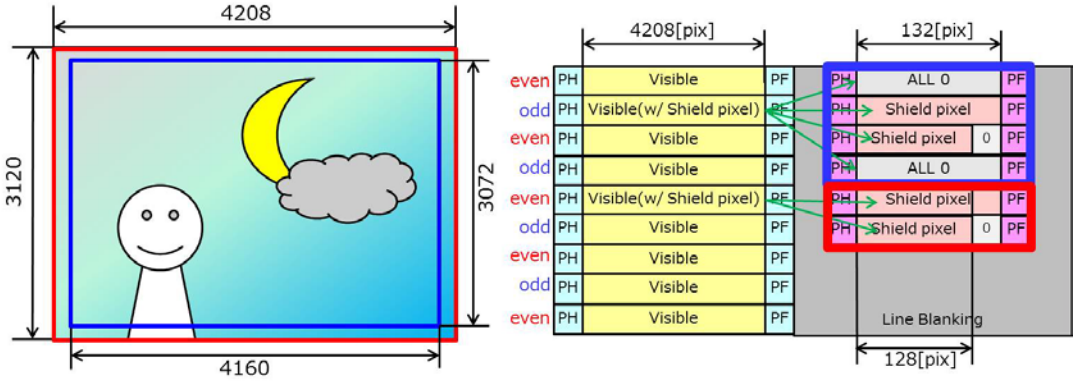


Figure 4-17 Shield pixel output timing(RAW10)

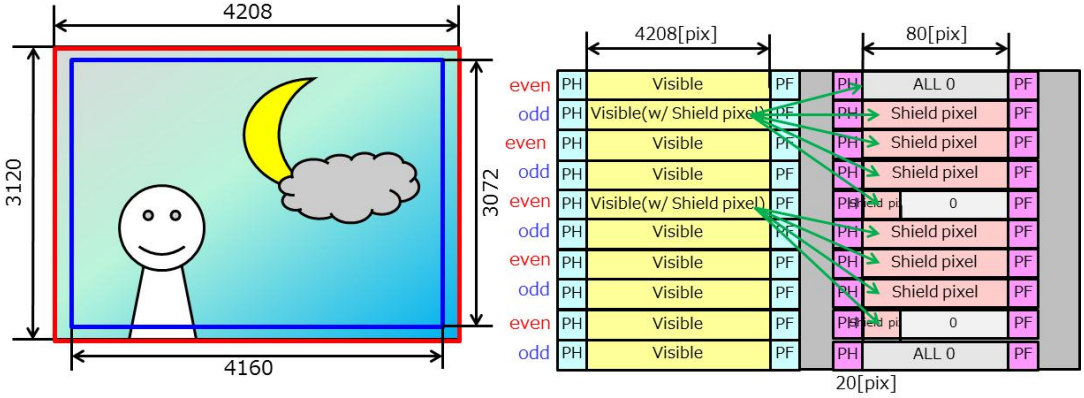


Figure 4-18 Shield pixel output timing(BYTE2)

Valid Shield pixel packet does not contain 0, (Valid Shield pixel data range is 1 – 1023).

Invalid Shield pixel packet and padding data will output 0 only.

If input data of Shield pixel comes 0, please ignore the data afterward in that packet.

4.6.1.2. AF Window Specification

The Shield pixels detecting area (AF window) can be set according to output images after cropping / binning.

AF window setting is necessary to fit the boundary of Shield pixel block.

Setting of the AF window is shown as below.

(1) AF Window is adjusted to fit boundary of Shield pixel block by calculation inside the sensor.
This is called “AUTO_MODE”

(2) AF Window is adjusted to fit boundary of Shield pix tile by User.
This is called “MANUAL_MODE”

Table 4-7 Setting of the AF window

Modes	AF Window setting	
	AUTO_MODE	MANUAL_MODE
Full Resolution	Available	Available
2 Sub-Sampling(V: 1/2)	Not available	Available
HDR	Available	Available

4.6.1.2.1. Shield pixel block arrangement

This sensor has 96x130 blocks including 8 shield pixels (4 pairs of left/right shield pixel) respectively.

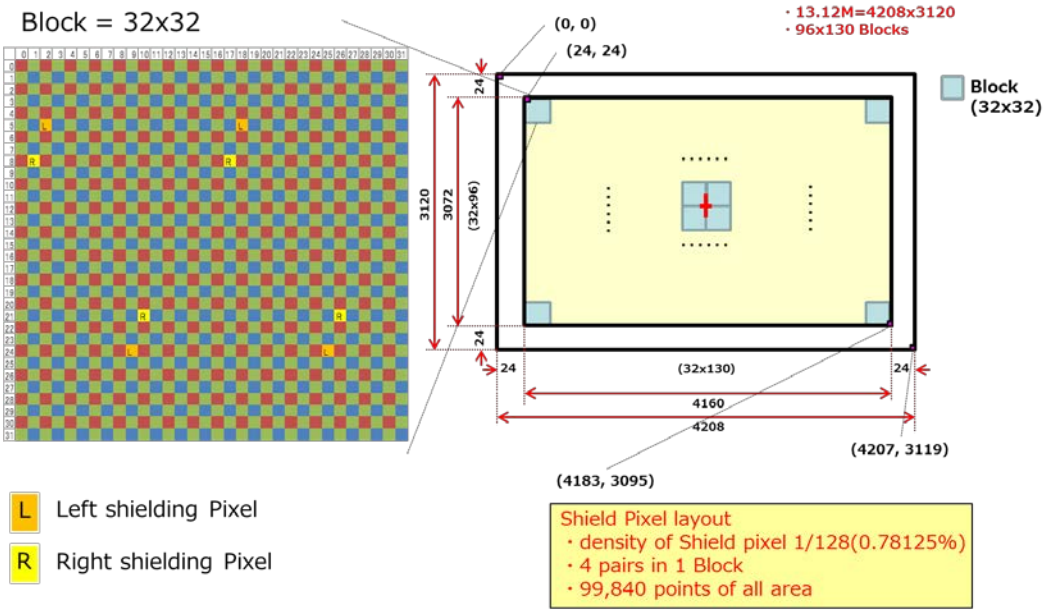


Figure 4-19 Shield Pixel Block Arrangement

4.6.1.2.2. Description of AF Window setting

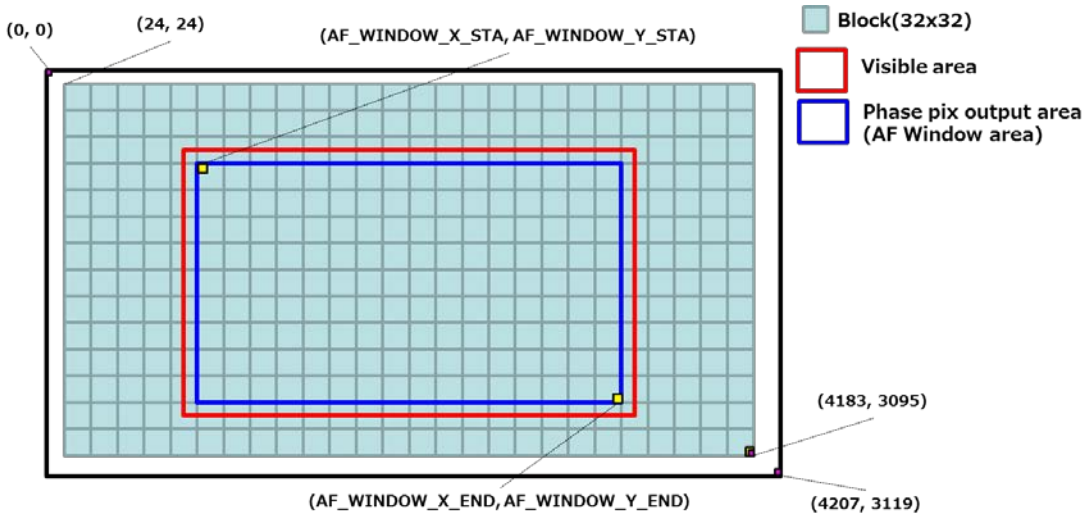


Figure 4-20 AF Window area

In case of AUTO_MODE, after the visible area (red rectangle) and AF window setting (green rectangle) is fixed, Shield pixels output area (blue rectangle) will be calculated by this sensor automatically.(See Figure 4-21)

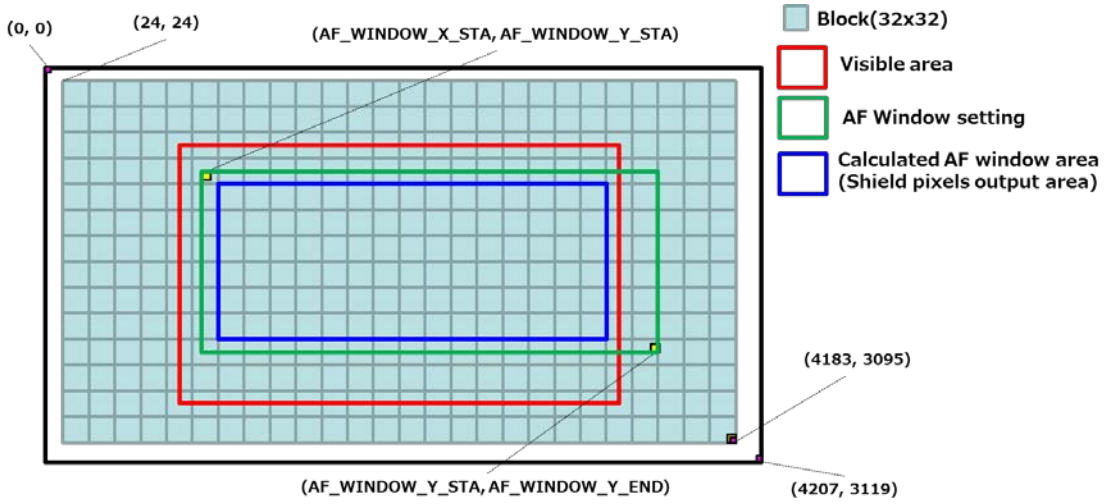


Figure 4-21 AUTO_MODE

In case of MANUAL_MODE, only AF Window (blue rectangle) setting is necessary. No internal calculations will be executed.

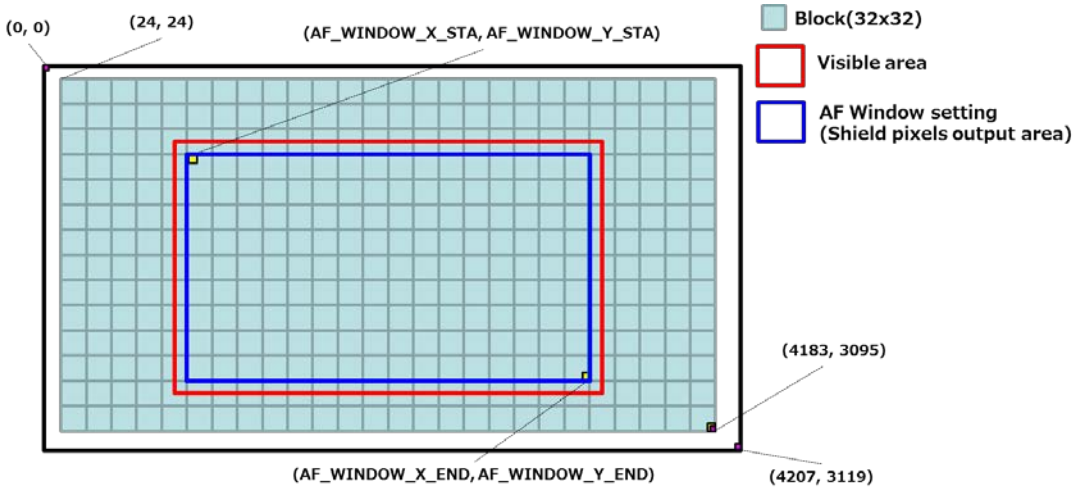


Figure 4-22 MANUAL_MODE

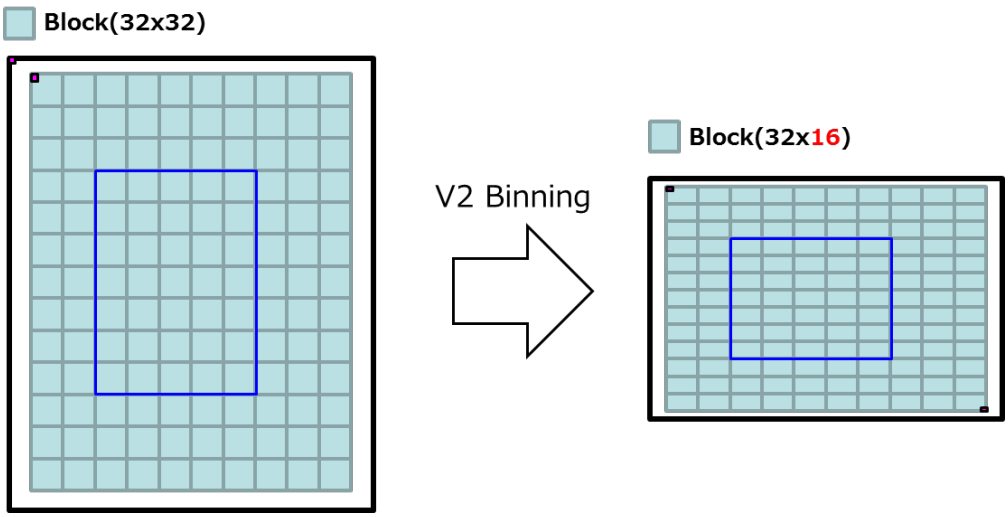


Figure 4-23 V2 binning of Shield pixel block

In 2 Sub-Sampling (V: 1/2) mode, Vertical Block size become half. It (V: 1/2) must be considered in AF Window Setting because only MANUAL_MODE is available in binning mode.

Table 4-8 AF Window setting

	Address	Bit	Name	Description
I²C register	0x3170	[4:0]	AF_WINDOW_X_STA[12:8]	AF_WINDOW horizontal start position
	0x3171	[7:0]	AF_WINDOW_X_STA[7:0]	
	0x3172	[4:0]	AF_WINDOW_X_END[12:8]	AF_WINDOW horizontal end position
	0x3173	[7:0]	AF_WINDOW_X_END[7:0]	
	0x3174	[3:0]	AF_WINDOW_Y_STA[11:8]	AF_WINDOW vertical start position
	0x3175	[7:0]	AF_WINDOW_Y_STA[7:0]	
	0x3176	[3:0]	AF_WINDOW_Y_END[11:8]	AF_WINDOW vertical end position
	0x3177	[7:0]	AF_WINDOW_Y_END[7:0]	
	0x7bcd	[0]	AF_WINDOW_MODE	AF Window calculate mode select 0 : AUTO_MODE 1 : MANUAL_MODE
	0x0408	[4:0]	DIG_CROP_X_OFFSET[12:8]	Offset from X_ADD_STA after binning and Sub-sampling
	0x0409	[7:0]	DIG_CROP_X_OFFSET[7:0]	
	0x040a	[3:0]	DIG_CROP_Y_OFFSET[11:8]	Offset from Y_ADD_STA after binning and Sub-sampling
	0x040b	[7:0]	DIG_CROP_Y_OFFSET[7:0]	
	0x040c	[4:0]	DIG_CROP_IMAGE_WIDTH[12:8]	Image width after digital cropping
	0x040d	[7:0]	DIG_CROP_IMAGE_WIDTH[7:0]	
	0x040e	[3:0]	DIG_CROP_IMAGE_HEIGHT[11:8]	Image height after digital cropping
	0x040f	[7:0]	DIG_CROP_IMAGE_HEIGHT[7:0]	
	0x0401	[1:0]	SCALE_MODE[1:0]	Scaling mode selection 0 : No Scaling 1 : Horizontal Scaling 2 : Horizontal & Vertical Scaling 3 : Reserved
	0x0404	[0]	SCALE_M[8]	Down scale factor M:
	0x0405	[7:0]	SCALE_M[7:0]	
	0x3038	[0]	SCALE_MODE_EXT	H-direction scaling ratio control enable independently with V-direction scaling ratio 0: Disable 1: Enable (only available SCALE_MODE=2)
	0x034c	[4:0]	X_OUT_SIZE[12:8]	The sensor output size of horizontal
	0x034d	[7:0]	X_OUT_SIZE[7:0]	
	0x034e	[3:0]	Y_OUT_SIZE[11:8]	The sensor output size of vertical
	0x034f	[7:0]	Y_OUT_SIZE[7:0]	

	0x0344	[4:0]	X_ADD_STA [12:8]	Horizontal direction analog cropping start position within the active pixels area * Note that this is the cropping end position when mirroring (IMG_ORIENTATION_H=1)
	0x0345	[7:0]	X_ADD_STA [7:0]	
	0x0346	[3:0]	Y_ADD_STA [11:8]	Vertical direction analog cropping start position within the active pixels area * Note that this is the cropping end position when flipping (IMG_ORIENTATION_V=1)
	0x0347	[7:0]	Y_ADD_STA [7:0]	
	0x0348	[4:0]	X_ADD_END [12:8]	Horizontal direction analog cropping end position within the active pixels area * Note that this is the cropping start position when mirroring (IMG_ORIENTATION_H=1)
	0x0349	[7:0]	X_ADD_END [7:0]	
	0x034a	[3:0]	Y_ADD_END [11:8]	Vertical direction analog cropping end position within the active pixels area * Note that this is the cropping start position when flipping (IMG_ORIENTATION_V=1)
	0x034b	[7:0]	Y_ADD_END [7:0]	

4.6.1.2.3. Supplemental description of AF Window MANUAL_MODE

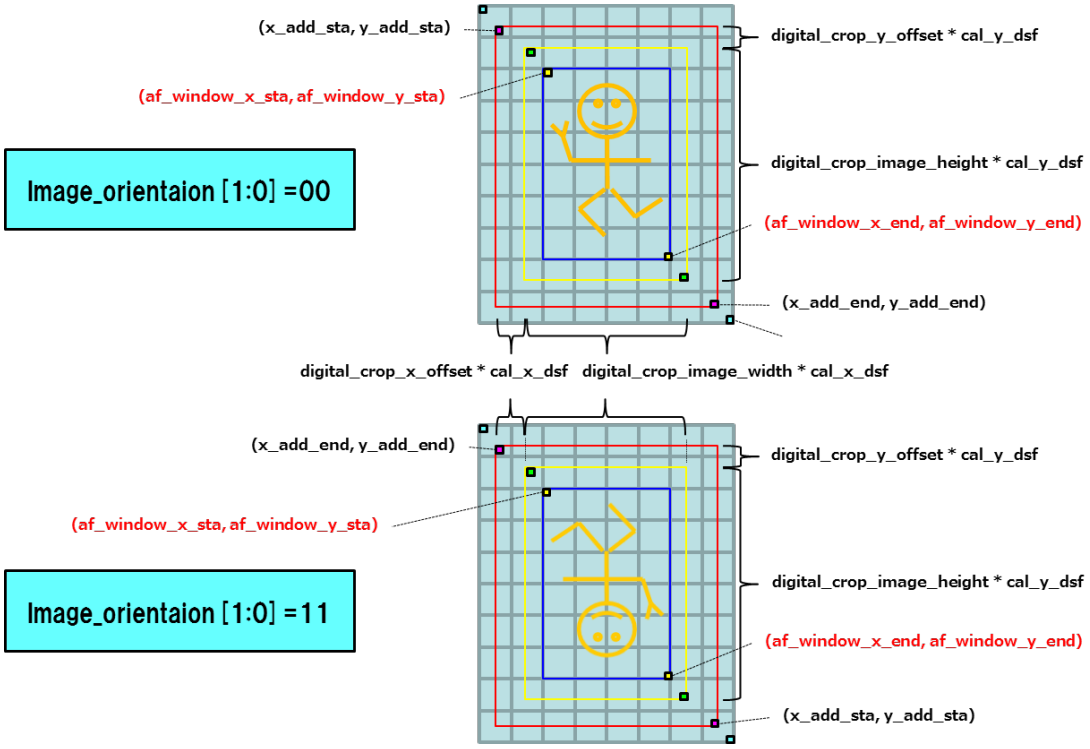


Figure 4-24 AF Window compensation function

cal_x_dsf, cal_y_dsf : Digital Scaling Factor

scale_dsf_h = (SCALE_MODE !=0) && (SCALE_M ≧16) ? SCAME_M : 16

cal_x_dsf = scale_dsf_h / 16

Table 4-9 cal_y_dsf calculation

Modes	**cal_y_dsf**
Full Resolution	1
1/2 Sub-Sampling(v 1/2)	2
HDR	1
Other	Not supported

dig_crop_sta_x, dig_crop_sta_y, dig_crop_end_x, dig_crop_end_y : Digital Crop Position

dig_crop_sta_x_pre0 = digital_crop_x_offset

dig_crop_sta_y_pre0 = digital_crop_y_offset

dig_crop_end_x_pre0 = (digital_crop_x_offset + digital_crop_width – 1)

dig_crop_end_y_pre0 = (digital_crop_y_offset + digital_crop_height – 1)

dig_crop_sta_x_pre1 = af_window_x_sta < *dig_crop_sta_x_pre0* ? *dig_crop_sta_x_pre0* : af_window_x_sta * *cal_x_dsf*

dig_crop_sta_y_pre1 = af_window_y_sta < dig_crop_sta_y_pre0 ? dig_crop_sta_y_pre0 : af_window_y_sta

dig_crop_end_x_pre1 = af_window_x_end < *dig_crop_end_x_pre0* ? af_window_x_end * *cal_x_dsf* : *dig_crop_end_x_pre0*

dig_crop_end_y_pre1 = af_window_y_end < *dig_crop_end_y_pre0* ? af_window_y_end : *dig_crop_end_y_pre0*

dig_crop_sta_x = *dig_crop_sta_x_pre1*

dig_crop_sta_y = *dig_crop_sta_y_pre1*

dig_crop_end_x = *dig_crop_end_x_pre1*

dig_crop_end_y = *dig_crop_end_y_pre1*

AF_WINDOW_X_STA, AF_WINDOW_Y_STA, AF_WINDOW_X_END, AF_WINDOW_Y_END

// Shield pixel block size

block_size_x = 32

block_size_y = 32/cal_y_dsf

// Shield pixel block start and end position

block_sta_x = 24

block_end_x = 4183

block_sta_y = 24 / *cal_y_dsf*

block_end_y = ROUNDUP (3095 / *cal_y_dsf*) - 1

//Analog crop position which considered AF Window

x_add_sta_afw = x_add_sta

x_add_end_afw = x_add_end

y_add_sta_afw = y_add_sta / *cal_y_dsf*

y_add_end_afw = (y_add_end+1) / *cal_y_dsf - 1*

//crop position which considered Image orientation

If (image_orientation[0] = 0)

crop_sta_x = x_add_sta_afw + dig_crop_sta_x

crop_end_x = x_add_sta_afw + dig_crop_end_x

Else

crop_sta_x = x_add_end_afw - dig_crop_end_x

crop_end_x = x_add_end_afw - dig_crop_sta_x

If (image_orientation[1] = 0)

crop_sta_y = y_add_sta_afw + dig_crop_sta_y

crop_end_y = y_add_sta_afw + dig_crop_end_y

Else

crop_sta_y = y_add_end_afw - dig_crop_end_y

crop_end_y = y_add_end_afw - dig_crop_sta_y

// af_window parameter without image orientation calculation

If (*crop_sta_x < block_sta_x***)**

af_sta_x = block_sta_x

Else

if (*(crop_sta_x - block_sta_x) % block_size_x = 0***)**

af _sta_x = crop_sta_x

else

af _sta_x = crop_sta_x + block_size_x - ((crop_sta_x - block_sta_x) % block_size_x)

If (*crop _end_x > block_end_x***)**

af_end_x = block_end_x

Else

if (*(block_end_x - crop _end_x) % block_size_x = 0***)**

af_end_x = crop _end_x

else

af_end_x = crop _end_x - block_size_x + ((block_end_x - crop _end_x) % block_size_x)

If (*crop_sta_y < block_sta_y***)**

af_sta_y = block_sta_y

Else

if(*(crop_sta_y - block_sta_y) % block_size_y = 0***)**

af_sta_y = crop_sta_y

else

af_sta_y = crop_sta_y + block_size_y - ((crop_sta_y - block_sta_y) % block_size_y)

If (*crop _end_y > block_end_y***)**

af_end_y = block_end_y

Else

if (*(block_end_y - crop _end_y) % block_size_y = 0***)**

af_end_y = crop_end_y

else

af_end_y = crop _end_y - block_size_y + ((block_end_y - crop_end_y) % block_size_y)

// User Setting AF window(considered image orientation)

If (image_orientation[0] = 0)

AF_WINDOW_X_STA = *af _sta_x - x_add_sta_afw*

AF_WINDOW_X_END = *af _end_x - x_add_sta_afw*

Else

AF_WINDOW_X_STA = *x_add_end_afw - af_end_x*

AF_WINDOW_X_END = *x_add_end_afw - af_sta_x*

If (image_orientation[1] = 0)

AF_WINDOW_Y_STA = *af _sta_y - y_add_sta_afw*

AF_WINDOW_Y_END = *af _end_y - y_add_sta_afw*

Else

AF_WINDOW_Y_STA = *y_add_end_afw - af_end_y*

AF_WINDOW_Y_END = *y_add_end_afw - af_sta_y*

4.6.2. Output order of various control data

All of enable or control setting of each function are set to 1 (enabled), Shield pixel data is output in series as shown below.

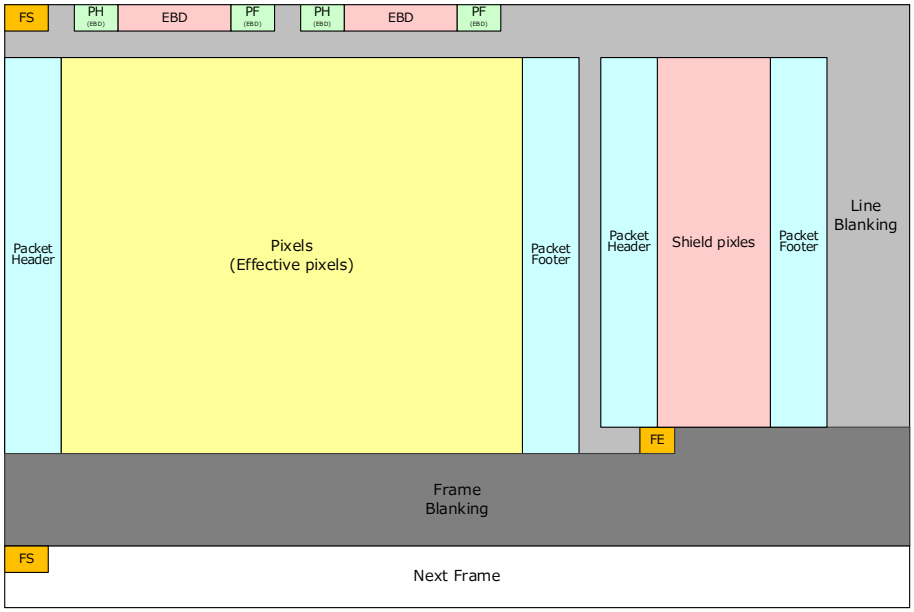


Figure 4-25 Frame Structure (ALL ON)

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4.6.3. Contents of packet header

The contents of the first byte in the packet header (data identifier) and the corresponding register settings are described in the table below.

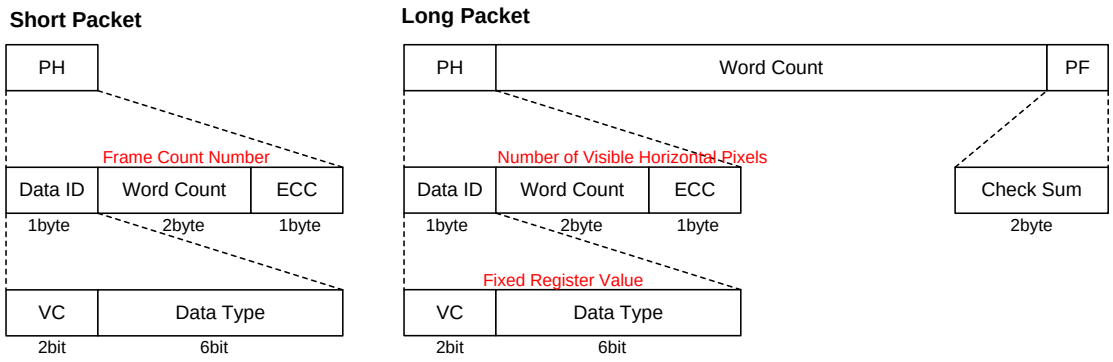

Figure 4-26 Short packet & long packet structures

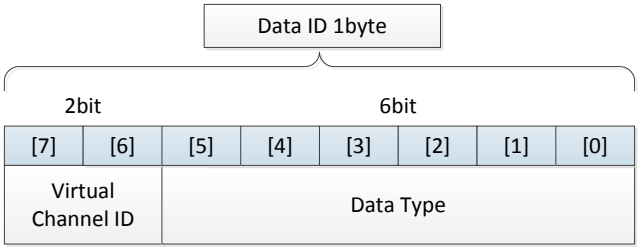

Figure 4-27 Configuration of Data ID

Table 4-10 Data Identifier

	Bit assignment	Value	Name	Corresponding registers (I2C)	Description
Packet header	[7:6] Virtual Channel ID	2'h0 (Default)	-	0x 0110 CSI_CH_ID [2:0]	Refers LSB 2bits
	[5:0] Data types	6'h00	Frame Start Code	NA	
		6'h01	Frame End Code	NA	
		6'h12	Embedded Data	NA	For embedded data line
		6'h2B	RAW10	NA	0x0112:CSI_DT_FMT_H=0x0a 0x0113:CSI_DT_FMT_L=0x0a
		6'h2A	RAW8	NA	0x0112:CSI_DT_FMT_H=0x08 0x0113:CSI_DT_FMT_L=0x08
		6'h2F (Default)	Shield Pix Data	NA	For Shield pixels data line

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4.6.4. Data type

Types of data in each line are shown below.

Table 4-11 Image pixel area and data type

Image pixel area	Data type
Embedded data lines	Embedded data
Effective pixels	RAW10, RAW8
Shield pixels data lines	Shield Pix Data

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4.6.5. Embedded data line control

It is possible to output certain 2-wire serial register contents on the 2 lines just after the FS sync code of the frame. Undefined value is output when not outputting embedded data. Regarding actual contents of the embedded data line are listed in Appendix.

Table 4-12 Embedded data line control

I^2C register	Address	Bit	Name	Description
	0x4041	[2:0]	EBD_SIZE_V	0 is no EBD 2 is EBD 2 line others are forbidden

The sequence of EBD in each output format is as shown in the figures below.

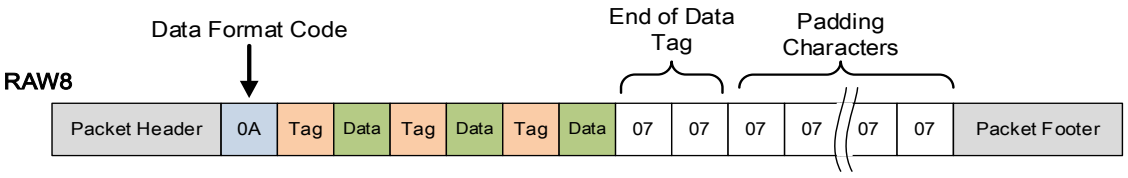

Figure 4-28 Embedded data lines alignment in RAW8 mode

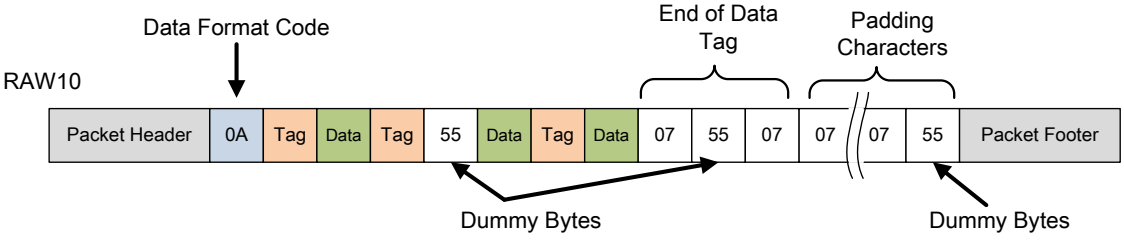

Figure 4-29 Embedded data lines alignment in RAW10 mode

Addresses and the end of register values are distinguished by “Tags” embedded in the data sequence.

Table 4-13 Embedded data line tag

Tag	Data byte description
00h	Illegal Tag. If found treat as end of Data
07h	End of Data (Data Byte Value = 07H)
aah	CCI Register Index MSB [15:8]
a5h	CCI Register Index LSB [7:0]
5ah	Auto increment the CCI index after the data byte – valid data Data byte contains valid CCI register data
55h	Auto increment the CCI index after the data byte – null data A CCI register does NOT exist for the current CCI index. The data byte value is the 07H
ffh	Illegal Tag. If found treat as end of Data

The definite data sequence is described in the table in the Appendix.

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5. Operation Mode Setting

5.1. Clock generation and PLL

This sensor is equipped with embedded oscillator and PLL to generate the necessary internal clocks and CSI2 transmission clocks. Set the related registers according to the operation conditions.

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5.1.1. Clock system diagram

This sensor is equipped with 2 PLLs, one to output VTCK for image processing, and the other to output IOPCK for MIPI output. The IVTCK PLL can output at 338 to 1300 MHz, and the IOPCK PLL can output at 338 to 1300 MHz, based on a clock input with the 6 to 27 MHz range.

The IVTCK PLL could be configured with divider of up to 1/1 to 1/4 range, and multiply in the 51 to 216 range.

The IOPCK PLL could be configured with divider of up to 1/1 to 1/4 range, and multiply in the 51 to 216 range.

This sensor normally recommend to make it operate in single PLL mode by driving just one PLL (IVTCK PLL), however can also operate in dual PLL mode by driving both PLLs from parameter setting flexibility point of view. If use dual PLL mode, please confirm with SONY.

In PLL single mode, PREPLLCK_VT_DIV and PLL_IVT_MPY are applied to IOPCK PLL, and PREPLLCK_OP_DIV and PLL_IOP_MPY are ignored.

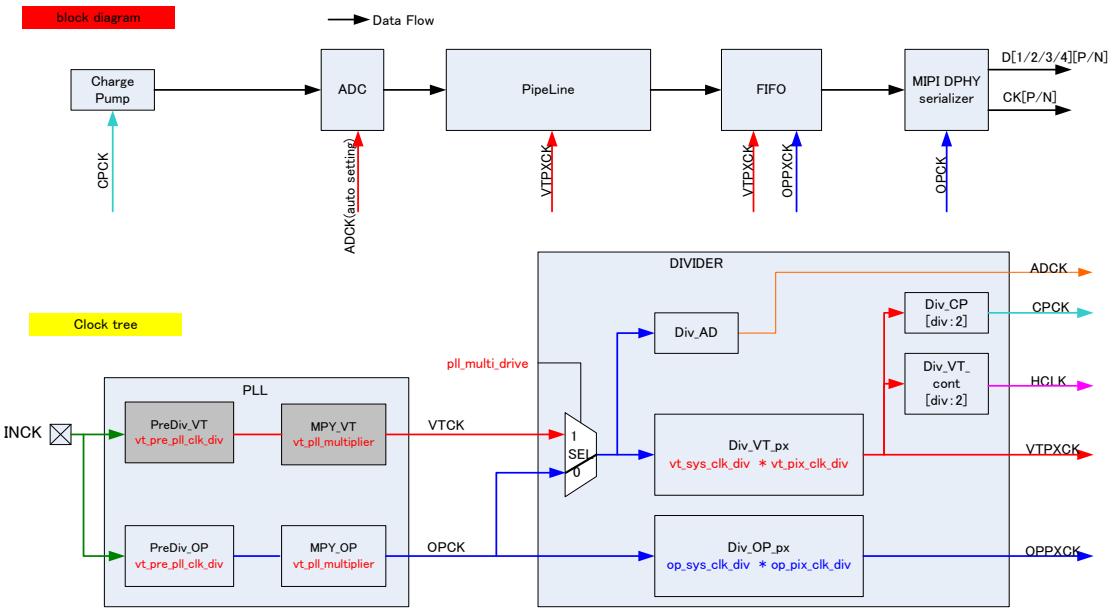

Figure 5-1 Clock system diagram (PLL single mode)

Table 5-1 PLL pre divider & multiplier setting (PLL single mode)

	Address	Bit	Name	Description	Setting constraint
I²C register	0x0305	[3:0]	PREPLLCK_VT_DIV	The pre-PLL Clock Divider for Internal Video Timing System Clock Range : 1 to 4 Step : 1 Format : 16-bit unsigned integer *Setup other than the above is forbidden.	INCK / PREPLLCK_VT_DIV = 6 to 12 MHz
	0x0306	[2:0]	PLL_IVT_MPY[10:8]	The PLL multiplier for Internal Video Timing System Clock Range : 51 to 216 Step : 1 Format : 16-bit unsigned integer *Setup other than the above is forbidden.	IVTCK & IOPCK = 338 to 1300 MHz
	0x0307	[7:0]	PLL_IVT_MPY[7:0]		

*PREPLLCK_OP_DIV and PLL_IOP_MPY are ignored

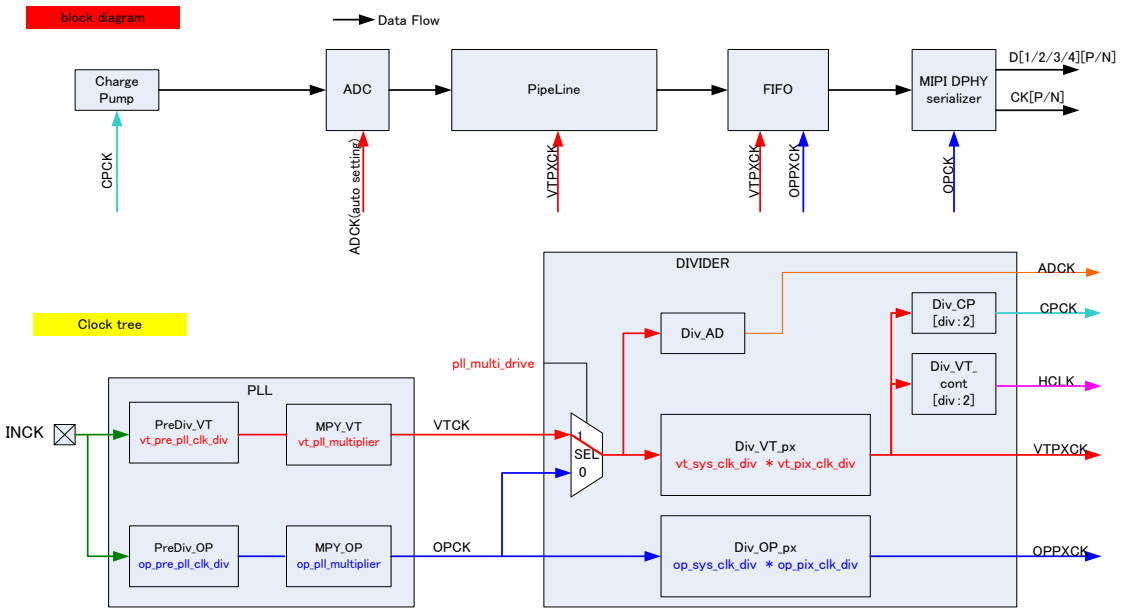

Figure 5-2 Clock system diagram (PLL dual mode)

Table 5-2 PLL pre divider & multiplier setting (PLL dual mode)

	Address	Bit	Name	Description	Setting constraint
I²C register	0x0305	[3:0]	PREPLLCK_VT_DIV	The pre-PLL Clock Divider for Internal Video Timing System Clock Range : 1 to 4 Step : 1 Format : 16-bit unsigned integer *Setup other than the above is forbidden.	INCK / PREPLLCK_VT_DIV = 6 to 12 MHz
	0x030d	[3:0]	PREPLLCK_OP_DIV	The pre-PLL Clock Divider for Internal Output Pixel System during "Dual PLL mode" (PLL_MULT_DRIV=1). Range : 1 to 4 Step : 1 Format : 16-bit unsigned integer *Setup other than the above is forbidden.	INCK / PREPLLCK_OP_DIV = 6 to 12 MHz
	0x0306	[2:0]	PLL_IVT_MPY [10:8]	The PLL multiplier for Internal Video Timing System Clock Range : 57 to 216 Step : 1 Format : 16-bit unsigned integer *Setup other than the above is forbidden.	IVTCK = 338 to 1300 MHz
	0x0307	[7:0]	PLL_IVT_MPY [7:0]		
	0x030e	[2:0]	PLL_IOP_MPY [10:8]	The PLL multiplier for Internal Output Pixel System "Dual PLL mode" (PLL_MULT_DRIV=1). Range : 51 to 216 Step : 1 Format : 16-bit unsigned integer *Setup other than the above is forbidden.	IOPCK = 338 to 1300 MHz
	0x030f	[7:0]	PLL_IOP_MPY [7:0]		

Table 5-3 INCK Frequency setting

	Address	Bit	Name	Description	Setting constraint
I²C register	0x0136	[7:0]	EXCK_FREQ[15:8]	External clock(INCK) frequency [MHz] Bit[15:8] integer Bit[7:0] decimal	INCK = 6 to 27 MHz The same setting as INCK frequency.
	0x0137	[7:0]	EXCK_FREQ[7:0]		

Table 5-4 PLL mode select

I²C register	Address	Bit	Name	Description	Notes
	0x0310	[0]	PLL_MULT_DRIV	PLL mode select 0 : Single PLL mode 1 : Dual PLL mode	

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5.1.2. Supplemental description of operation clocks

These clocks are the root of all the operation clocks in this sensor and it designates the data rate. CKP/CKN; CSI2 interface clock is generated from IOPCK by dividing into 1/2 (or1/4) frequency since the interface is operated in double data rate format.

5.1.2.1. IVTCK, IOPCK: PLL output(PLL single mode)

IOPCK = INCK frequency × *PreDivider setting* × *PLL multiple setting*

* *PreDivider setting* = 1/ PREPLLCK_VT_DIV

* *PLL multiple setting* = PLL_IVT_MPY

IVTCK = IOPCK

CKP, CKN = *OPCK* × *CSI2 divide* × (1/ OPSYCK_DIV)

* *CSI2 divide* = 1/2

5.1.2.2. IVTCK, OPCK: PLL output (PLL dual mode)

IVTCK = *INCK frequency* × *PreDivider setting* × *PLL multiple setting*

* *PreDivider setting* = 1/ PREPLLCK_VT_DIV

* *PLL multiple setting* = PLL_IVT_MPY

IOPCK = *INCK frequency* × *PreDivider setting* × *PLL multiple setting*

* *PreDivider setting* = 1/ PREPLLCK_OP_DIV

* *PLL multiple setting* = PLL_IOP_MPY

CKP, CKN = I*OPCK* × *CSI2 divide* × (1/ IOPSYCK_DIV)

* *CSI2 divide* = 1/2

5.1.2.3. Clock frequency configuration examples

Table 5-5 PLL frequency table IVTCK (include PLL single mode)

CLK	Input Clock (INCK)	Pre division	PLL Input frequency	Multiple	PLL Oscillation frequency
IVTCK	6 MHz	1	6.0 MHz	57	342.0 MHz
				166	996.0 MHz
				216	1296.0 MHz
	12 MHz	2	6.0 MHz	57	342.0 MHz
				166	996.0 MHz
				216	1296.0 MHz
	13.5 MHz	2	6.75 MHz	51	344.25 MHz
				148	999.0 MHz
				192	1296.0 MHz
	18 MHz	3	6.0 MHz	57	342.0 MHz
				166	996.0 MHz
				216	1296.0 MHz
	24 MHz	4	6.0 MHz	57	342.0 MHz
				166	996.0 MHz
				216	1296.0 MHz
	27 MHz	4	6.75 MHz	51	344.25 MHz
				148	999.0 MHz
				192	1296.0 MHz

Table 5-6 PLL frequency table IOPCK

CLK	Input Clock (INCK)	Pre division	PLL Input frequency	Multiple	PLL Oscillation frequency
IOPCK	6 MHz	1	6.0 MHz	57	342.0 MHz
				166	996.0 MHz
				216	1296.0 MHz
	12 MHz	2	6.0 MHz	57	342.0 MHz
				166	996.0 MHz
				216	1296.0 MHz
	13.5 MHz	2	6.75 MHz	51	344.25 MHz
				148	999.0 MHz

				192	1296.0 MHz
	18 MHz	3	6.0 MHz	57	342.0 MHz
				166	996.0 MHz
				216	1296.0 MHz
	24 MHz	4	6.0 MHz	57	342.0 MHz
				166	996.0 MHz
				216	1296.0 MHz
	27 MHz	4	6.75 MHz	51	344.25 MHz
				148	999.0 MHz
				192	1296.0 MHz

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5.1.3. IVTPXCK Clock

The clock for internal image processing is generated by dividing IVTCK into 1/10, 1/14, 1/16, 1/20, 1/28, 1/32, or 1/40 frequency. This clock is used as the base of integration time, frame rate, etc.

IVTPXCK clock frequency = I*VTCK* × I*VTPXCK clock division ratio*

* *IVTPXCK clock division ratio* = 1 / (IVTSYCK_DIV * IVTPXCK_DIV)

Table 5-7 IVTPXCK divider setting

	Address	Bit	Name	Description	Notes
I²C register	0x0303	[2:0]	IVTSYCK_DIV	The System Clock Divider for Internal Video Timing System Range : 2, 4 Format : 16-bit unsigned integer *Setup other than the above is forbidden.	
	0x0301	[4:0]	IVTPXCK_DIV	The Pixel Clock Divider for Internal Video Timing System Range : 4,5,7,8,10 Format : 16-bit unsigned integer *Setup other than the above is forbidden.	

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5.1.4. IOPPXCK Clock

The clock for internal image processing is generated by dividing IOPCK into 1/8, 1/10, 1/16, or 1/20 frequency according to the word length of the CSI2 interface. This clock designates the pixel rate etc.

IOPPXCK clock frequency = I*OPCK* × I*OPPXCK clock division ratio*

* *IOPPXCK clock division ratio* = 1 / (IOPSYCK_DIV * IOPPXCK_DIV)

Table 5-8 IOPPXCK divider setting

	Address	Bit	Name	Description	Notes
I²C register	0x030b	[1:0]	IOPSYCK_DIV	The System Clock Divider for Internal Output Pixel System Range : 1, 2 Format : 16-bit unsigned integer *Setup other than the above is forbidden.	
	0x0309	[4:0]	IOPPXCK_DIV	The Pixel Clock Divider for Internal Output Pixel System Range : 8, 10 (The setting value is decided by output bit width) Format : 16-bit unsigned integer *Setup other than the above is forbidden.	IOPPXCK_DIV is decided only by MIPI transmission format. Refer to Table 5-9

Table 5-9 IOPPXCK clock division ratio

Format	IOPSYCK_DIV setting	IOPPXCK_DIV setting	IOPPXCK clock division ratio
RAW10	1 or 2	10	1/10 or 1/20
RAW8	1 or 2	8	1/8 or 1/16

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5.2. Description of mode operation

Main modes of this sensor are Full resolution, Sub-sampling (V:1/2), Binning (V:1/3), and HDR (Full-resolution RAW output)

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5.2.1. Image size related settings

This sensor can output full size and/or re-sized (shrunk) images. Examples are shown in the table below.

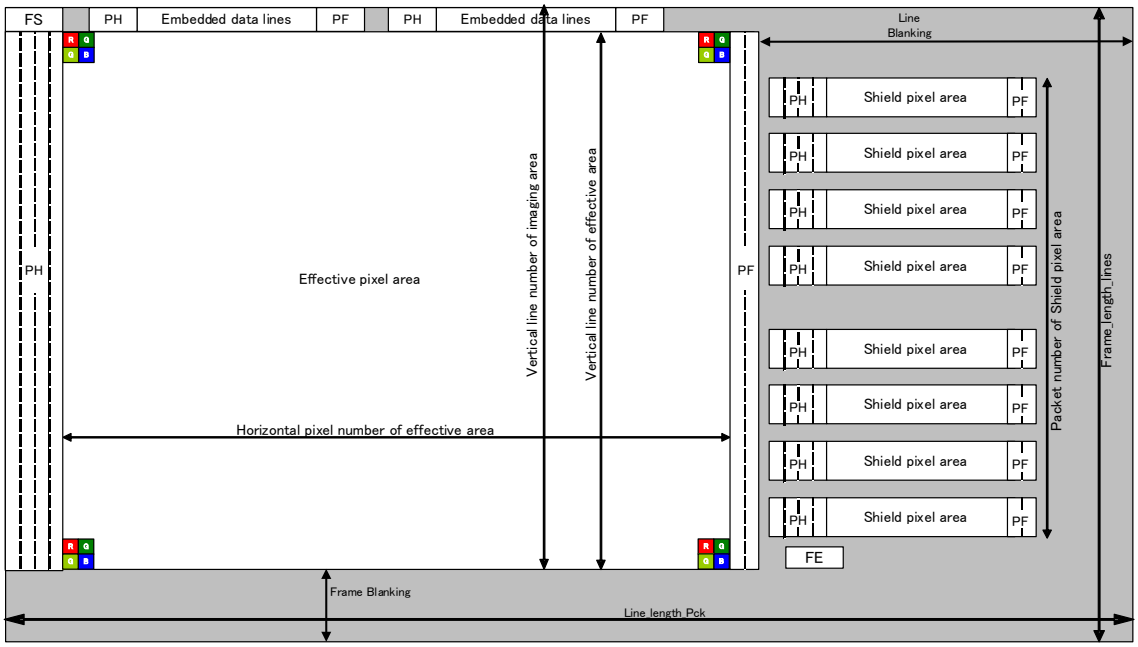


Figure 5-3 Image size parameter definition

Table 5-10 Typical image output of main capture modes (1)

		Modes					
		Full resolution HDR		2 Sub-sampling (V: 1/2)		3 Binning (V 1/3)	
Number of vertical lines in imaging area		3121		1561		753	
Number of horizontal pixels in effective area		4208		2100		1400	
Packet number of Shield pixel area	RAW10	1152		1152		Not support	
	BYTE2	1920		1538			
Number of lines and start position		Start position	Number of lines	Start Position	Number of lines	Start Position	Number of lines
Name of the areas	Frame start	1	1	1	1	1	1
	Embedded data lines	1	1	1	1	1	1
	Number of vertical pixels in effective area	2	3120	2	1560	2	752
	Frame end	3121	1	1561	1	753	1

Table 5-11 Typical image output of main capture modes (2)

Mode	Full (4:3)	Full (4:3)	Full 4K2K (16:9)	Full 4K2K (16:9)
Mode2	Normal	HDR	Normal	HDR
Analog Cropping	Non	Non	V crop	V crop
Binning	Non	Non	Non	Non
Skipping	Non	Non	Non	Non
Scaling	Non	Non	Non	Non
Number of horizontal pixels in effective area	4208	4208	4208	4208
Number of vertical lines in effective area	3120	3120	2352	2352
Max Frame rate	30fps	40fps	40fps	40fps
FOV	 H:4208 x V:3120	 H:4208 x V:3120	 H:4208 x V:2352	 H:4208 x V:2352
Output	 H:4208 x V:3120	 H:4208 x V:3120	 H:4208 x V:2352	 H:4208 x V:2352

Table 5-12 Typical image output of main capture modes (3)

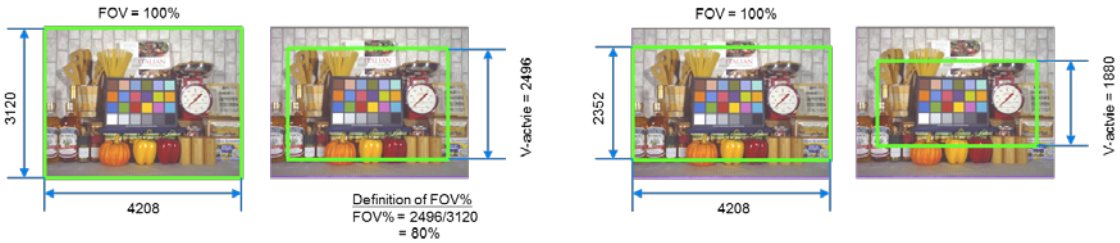
Mode	Full (16:9) 1080P	Full (16:9) 720P	Full/2(4:3)	Full/2(16:9) 1080P	Full/2(16:9) 720P
Mode2	Normal	Normal	Normal	Normal	Normal
Analog Cropping	V crop	V crop	Non	V crop	V crop
Binning	Non	Non	Non	Non	Non
Skipping	Non	Non	2Skipping	2Skipping	2Skipping
Scaling	HV 16/32	HV 16/48	H 16/32	H 16/32	H 16/48, V 16/24
Number of horizontal pixels in effective area	2100	1400	2100	2100	1400
Number of vertical lines in effective area	1172	780	1560	1176	780
Max Frame rate	40fps	40fps	60fps	80fps	80fps
FOV	 H:4208 x V:2352	 H:4208 x V:2352	 H:4208 x V:3120	 H:4208 x V:2352	 H:4208 x V:2352
Output	 H:2100 x V:1172	 H:1400 x V:780	 H:2100 x V:1560	 H:2100 x V:1176	 H:1400 x V:780

Table 5-13 Typical image output of main capture modes (4)

Mode	Full/3 (4:3)	Full/3 (16:9) 720P
Mode2	Normal	Normal
Analog Cropping	Non	V crop
Binning	3Binning	3Binning
Skipping	Non	Non
Scaling	H 16/48	H 16/48
Number of horizontal pixels in effective area	1400	1400
Number of vertical lines in effective area	1040	752
Max Frame rate	90fps	123fps
FOV	 H:4208 x V:3120	 H:4208 x V:2256
Output	 H:1400 x V:1040	 H:1400 x V:752

Table 5-14 FOV% vs FPS(Crop)

Binning	Aspect ratio	FOV %	Actual RAW size	Scaling (V)	Scaling (H)	Max. FPS
No(Full)	4:3	100	4208 x 3120	No	No	30
		75	3152 x 2340	No	No	40
		50	2100 x 1560	No	No	60
		32	1400 x 1024	No	No	90
		17	720 x 544	No	No	164
	16:9	100	4208 x 2352	No	No	40
		75	3152 x 1760	No	No	53
		50	2100 x 1176	No	No	79
		33	1400 x 784	No	No	116
		23	960 x 544	No	No	164



The following table shows the setting list for the supporting operation modes of capture mode.

Other settings are not supported in this sensor.

Table 5-15 Support list of operation mode of capture mode1

Operation mode	HDR setting		BINNING setting			Sub-sampling setting			
	0x0220 [5:0]	0x0222 [4:0]	0x0900 [0]	0x0901 [7:0]	0x300D [0]	0x0381 [1:0]	0x0383 [2:0]	0x0385 [1:0]	0x0387 [2:0]
	HDR_MODE [0]	EXPO_RATIO [4:0]	BINNING_MODE [0]	BINNING_TYPE_H [7:4]*1 BINNING_TYPE_V [3:0]	FORCE_FD_SUM [0]	X_EVN_INC [1:0]*2	X_ODD_INC [2:0]*2	Y_EVN_INC [1:0]	Y_ODD_INC [2:0]
HDR	See Table 5-16 *3		0	0x11	0	1(Fix)	1(Fix)	1	1
Full Resolution			0	x	0			1	1
2 Sub-sampling	0	x			0			1	3
2 Binning			1	0x12	0			1	1
2Binning + 2Sub-sampling					0			1	3
3Binning					1			3	3
4Binning				0x14	0			1	1
4Binning + 2Sub-sampling					0			1	3

*1 : BINNING_TYPE_H is fix value(1) in this sensor
*2 : X_EVN_INC and X_ODD_INC are fix value(1) in this sensor
*3 HDR and Full Resolution controlled by HDR_MODE & EXPO_RATIO. See Table 5-17

For 3 binning operation mode (V1/3), the output image quality may deteriorate, please use it under sufficient evaluation.

Table 5-16 Support list of operation mode of capture mode2

Operation mode	HDR setting				Comment
	0x0220 [5:0]			0x0222 [4:0]	
	HDR_MODE [0]	HDR_MODE [1]	HDR_MODE [5]	EXPO_RATIO [4:0]	
Full Resolution	0	x	x	x	Called “Full-Reso Type1” in this document
	1	0	0	1	Called “Full-Reso Type2” in this document
HDR		other			

5.2.2. HDR capture mode settings

Register settings for HDR capture mode are as follows.

This sensor outputs HDR pixels data without doing re-mosaic(HDR RAW output).

Table 5-17 HDR capture mode setting

	Address	Bit	Name	Description
I²C register	0x0112	[7:0]	CSI_DT_FMT_H[7:0]	The output data format for CSI Setting value: 0x0a0a See 3.1.2 CSI data format
	0x0113	[7:0]	CSI_DT_FMT_L[7:0]	
	0x0220	[5:0]	HDR_MODE[5:0]	Setting value: 0x01 or 0x03 or 0x23 Bit[0] HDR mode enable 0 : HDR disable 1 : HDR enable Bit[1] Gain mode select during HDR 0 : combined gain used 1 : separate gain used Bit[4:2] Reserved Bit[5] exposure mode select during HDR 0 : short exposure determined by ratio (controlled by EXPO_RATIO(0x0222)) 1 : short exposure controlled by direct control
	0x0221	[7:4]	HDR_RESO_REDU_H	Scaling factor during HDR 0x11 : HDR Full Pixel Other values are prohibited.
	0x0221	[3:0]	HDR_RESO_REDU_V	
	0x0222	[4:0]	EXPO_RATIO	Exposure_ratio [4:0] Defines exposure ratio between short and long exposure. Short exposure value = coarse_integration_time / Exposure_ratio 1,2,4,8,16(unsigned integer) can be set.

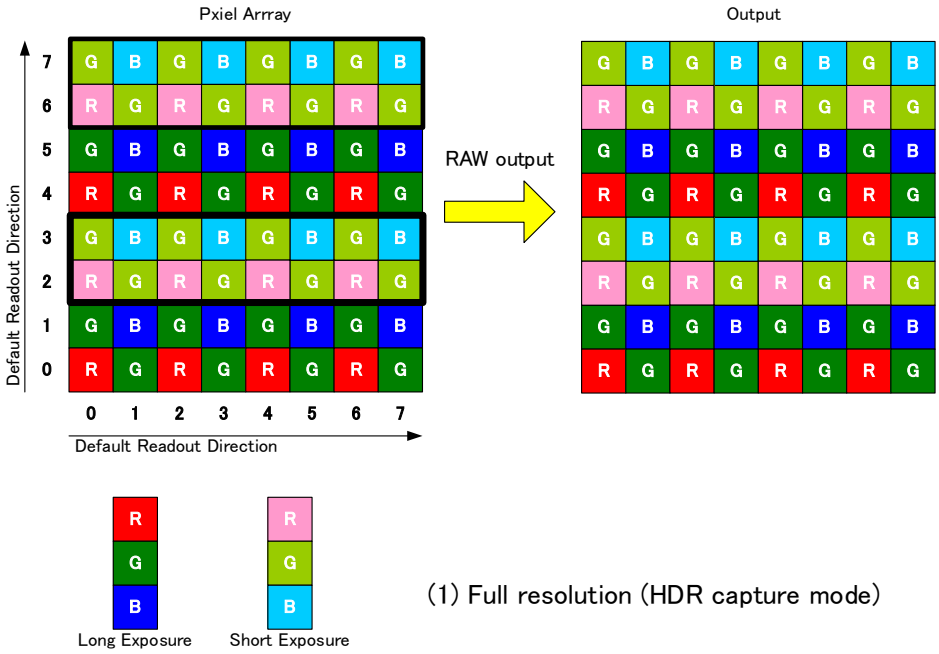


Figure 5-4 Image size parameter definition

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5.2.3. Normal capture mode settings (full and binning mode)

Register settings for Binning mode are as follows.

Table 5-18 Normal capture mode settings (full and binning mode)

	Address	Bit	Name	Description
I²C register	0x0220	[5:0]	HDR_MODE[5:0]	Setting value: 0x00 (HDR MODE OFF)
	0x0900	[0]	BINNING_MODE	Binning enable control 0=None 1=Enable
	0x0901	[7:4]	BINNING_TYPE_H[3:0]	BINNING_TYPE_H : Binning type selection for Horizontal BINNING_TYPE_V : Binning type selection for Vertical 0x12=2 or 3Binning for (V:1/2 or V 1/3) 0x14=4 Binning for (V:1/4, H:1/4) Other values are ignored.
	0x0901	[3:0]	BINNING_TYPE_V[3:0]	
	0x0902	[7:0]	BINNING_WEIGHTING[7:0]*1	Binning type selection for Horizontal 0 : additional average 1 : addition (summed) 2 : weighting additional average *Setup other than the above is forbidden.

* See 5.5.3 for the description of BINNING_WEIGHTING [7:0]

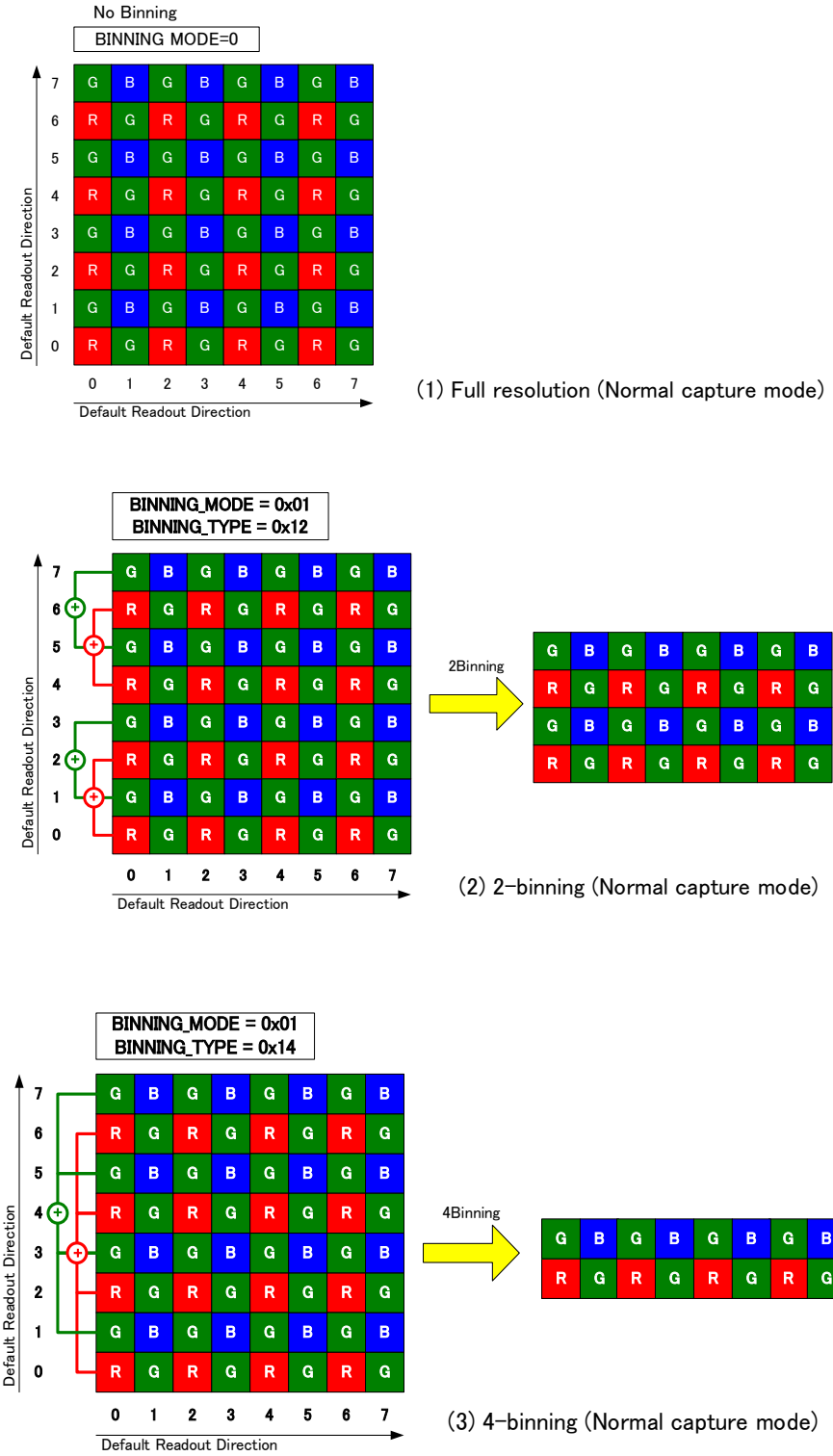

Figure 5-5 Binning mode image

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5.2.4. Normal capture mode settings (Sub-sampling mode)

By programming the x and y odd and even increment registers, the camera module can be configured to readout Sub-sampled pixel data in Normal capture mode. The Sub-sampling mode is not available in HDR capture mode.

Table 5-19 Sub-sampling mode setting

	Address	Bit	Name	Description
I²C register	0x0381	[2:0]	X_EVN_INC[2:0]	No. of pixels skipped from even number to odd number in Sub-sampling mode - Fix 1.
	0x0383	[2:0]	X_ODD_INC[2:0]	No. of pixels skipped from odd number to even number in Sub-sampling mode – Fix1
	0x0385	[3:0]	Y_EVN_INC[3:0]	No. of lines skipped from even number line to odd number line in Sub-sampling mode - 0, 2, 4 etc.
	0x0387	[3:0]	Y_ODD_INC[3:0]	No. of lines skipped from odd number line to even number line in Sub-sampling mode - 1, 3, 5 etc.
	0x300d	[0]	FORCE_FD_SUM	Force FD Addition Setting（Valid Only for Vertical Not Additional mode Bayer unit 1/3 Sub-sampling mode ） 0:Force FD Addition OFF 1:Force FD Addition ON

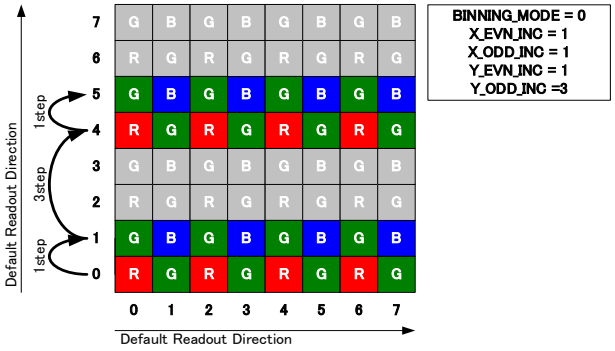

Figure 5-6 Sub-sampling mode (Normal capture mode)

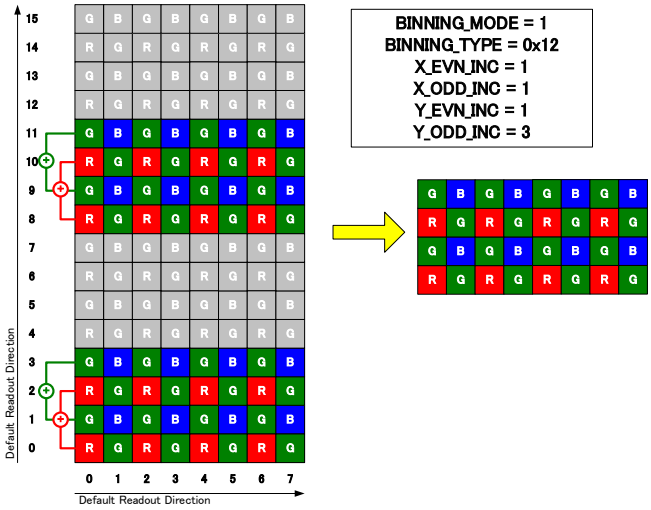

Figure 5-7 2 Binning + Sub-sampling

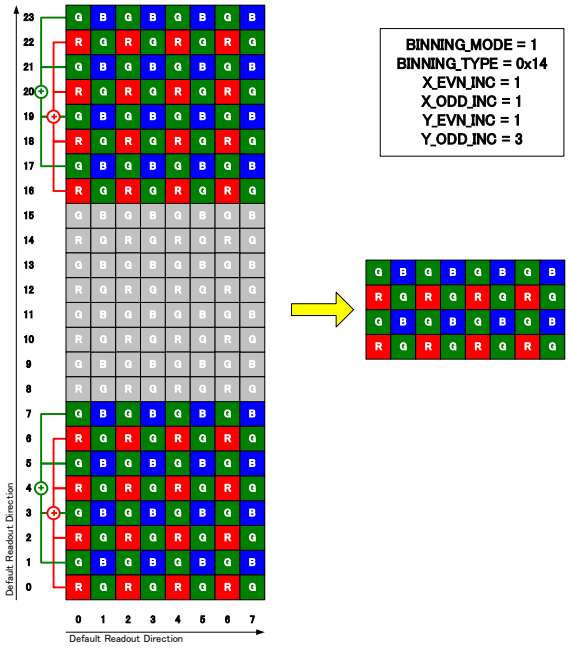

Figure 5-8 4 Binning + Sub-sampling

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5.2.5. Image size related functions

The relationships of image output size and the registers are shown below.

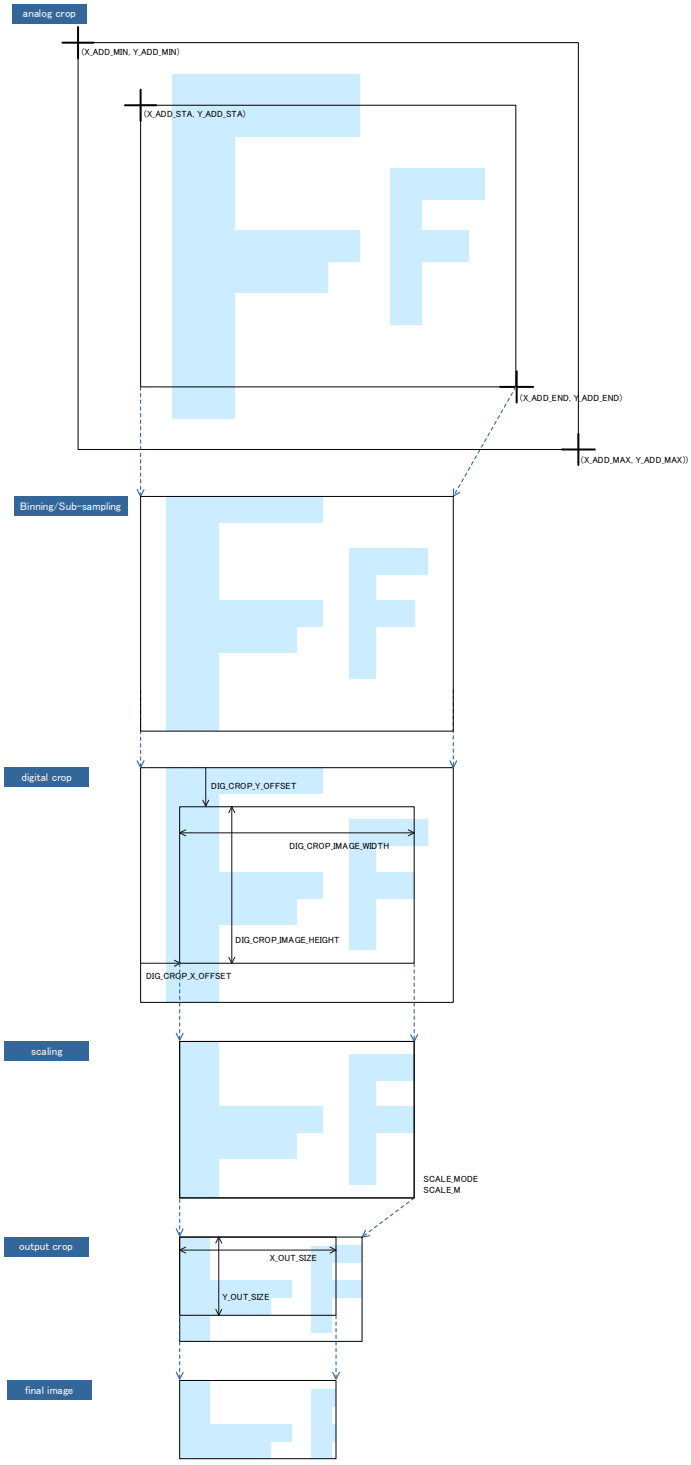

Figure 5-9 Image size related functions

Analog crop

Please refer to “4.3 Imaging area determination”.

Binning

Settings and see 5.2.3 Normal capture mode settings (full and binning mode) for details.

Digital crop

Digital crop is processed after image readout operation or in order of [Analog crop → Binning → Digital crop] and is common for Normal capture mode and HDR capture mode. The crop size (DIG_CROP_IMAGE_WIDTH and DIG_CROP_IMAGE_HEIGHT) must always be set properly even if cropping is not used.

Table 5-20 Digital crop setting

	Address	Bit	Name	Description
I²C register	0x0408	[4:0]	DIG_CROP_X_OFFSET[12:8]	Offset from X_ADD_STA after binning and Sub-sampling
	0x0409	[7:0]	DIG_CROP_X_OFFSET[7:0]	
	0x040a	[3:0]	DIG_CROP_Y_OFFSET[11:8]	Offset from Y_ADD_STA after binning and Sub-sampling
	0x040b	[7:0]	DIG_CROP_Y_OFFSET[7:0]	
	0x040c	[4:0]	DIG_CROP_IMAGE_WIDTH[12:8] *1	Image width after digital cropping Unit : pixels
	0x040d	[7:0]	DIG_CROP_IMAGE_WIDTH[7:0] *1	
	0x040e	[3:0]	DIG_CROP_IMAGE_HEIGHT[11:8] *1	Image height after digital cropping Unit : lines
	0x040f	[7:0]	DIG_CROP_IMAGE_HEIGHT[7:0] *1	

*1 (DIG_CROP_IMAGE_WIDTH and DIG_CROP_IMAGE_HEIGHT) must always be set properly even if cropping is not used.

Scaling

The horizontal and vertical scalar can be specified by scaling mode and down scale factor registers.

The down scale factor is determined by N/M ratio.

Scaling factor = N/M (N=16 fixed value)

Table 5-21 Scaling related registers

	Address	Bit	Name	Description
I²C register	0x0401	[1:0]	SCALE_MODE[1:0]	Scaling mode selection 0 : No Scaling 1 : Horizontal Scaling 2 : Horizontal & Vertical Scaling (only available PHASE_PIX_OUTEN = 0 and Operation mode isn't HDR)*1 3 : Reserved
	0x0404	[0]	SCALE_M[8]	Down scale factor M: Available M component: 16 - 511 Format: 9 bit unsigned integer
	0x0405	[7:0]	SCALE_M[7:0]	
	0x3038	[0]	SCALE_MODE_EXT	H-direction scaling ratio control enable independently with V-direction scaling ratio 0: Disable 1: Enable (only available SCALE_MODE=2)
	0x303a	[0]	SCALE_M_EXT[8]	H-direction : Scaling ratio Default 0x0010
	0x303b	[7:0]	SCALE_M_EXT[7:0]	

*1 In the case of PHASE_PIX_OUT_EN = 1, Vertical Scaling is unavailable

In the case of HDR operation mode, both of Horizontal and Vertical Scaling are unavailable

An example of picture sizes before and after scaling is as follows.

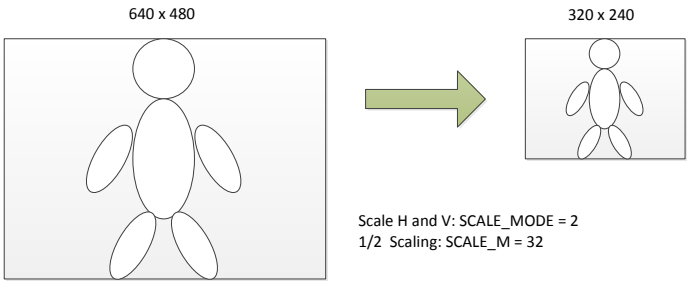

Figure 5-10 Scaling example

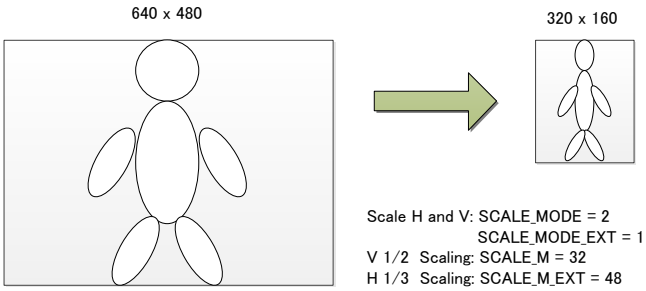

Figure 5-11 Scaling example (SCALE_MODE_EXT =1b)

Output crop

The width and height of the visible pixel area within the frame of data output from the sensor can be programmed by the “X_OUT_SIZE” and “Y_OUT_SIZE”.

Note that this function does not have “offset” setting just not like as Digital Crop’s Offset capability. So, the picture will not centered any more if the output size is trimmed with Out Crop function.

Table 5-22 Output crop setting

	Address	Bit	Name	Description
I²C register	0x034c	[4:0]	X_OUT_SIZE[12:8]	The sensor output size of horizontal Unit : pixels RAW8: multiple of 2 RAW10: multiple of 4
	0x034d	[7:0]	X_OUT_SIZE[7:0]	
	0x034e	[3:0]	Y_OUT_SIZE[11:8]	The sensor output size of vertical Unit : lines RAW8/RAW10: multiple of 2
	0x034f	[7:0]	Y_OUT_SIZE[7:0]	

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5.3. Frame rate calculation formula

The frame rate of the output image of this sensor can be calculated by the formula below.

Frame Rate [frame/s] = *Pixel_rate* [pixels/s] / *Total number of pixels* [pixels/frame]

Pixel rate [pixels/s] = I*VTPXCK* [MHz] * 4 (*Total number of IVTPX channel)*

Total number of pixels [pixels/frame]

= FRM_LENGTH_LINES [lines/frame] * LINE_LENGTH_PCK [pixels/line]

See 5.1.3 for the calculation formula for IVTPXCK.

See 5.1.1 for the descriptions of registers used for the calculation formula.

5.4. Electronic shutter and integration time settings

5.4.1. Registers related to integration time (electronic shutter setting)

The integration time setting registers are shown below.

Table 5-23 Electronic shutter setting register

	Address	Bit	Name	Description	Notes
I²C register	0x0202	[7:0]	COARSE_INTEG_TIME[15:8]	Coarse storage time Unit : lines Format : 16-bit unsigned integer	
	0x0203	[7:0]	COARSE_INTEG_TIME[7:0]		

Table 5-24 Integration time setting register

	Address	Bit	Name	Description	Notes
I²C register	0x0200	[7:0]	FINE_INTEG_TIME[15:8]	Fine storage time Unit : pixels Format : 16-bit unsigned integer	Read only
	0x0201	[7:0]	FINE_INTEG_TIME[7:0]		
	0x0342	[7:0]	LINE_LENGTH_PCK[15:8]	The length of line Unit : pixels Format : 16-bit unsigned integer * Set to 5352d. Any other value change require, please confirm with SONY.	
	0x0343	[7:0]	LINE_LENGTH_PCK[7:0]		
	0x0350	[0]	FRM_LENGTH_CTL	Frame length automatic tracking control Select whether or not the frame length is changed automatically when FRM_LENGTH_LINES < COARSE_INTEG_TIME + α (α = type-specific adjustment parameter, and is 10(d) for this type) 0 :no automatic tracking control of frame length 1 :automatic tracking control of frame length In this case, "COARSE_INTEG_TIME + α" operates instead of FRM_LENGTH_LINES	

5.4.2. Integration time calculation

The integration time or shutter time(T_{SH}) can be obtained from the following relational equation.

Tsh = ***Tline*** * (COARSE_INTEG_TIME [lines] + FINE_INTEG_TIME [pixels] / LINE_LENGTH_PCK [pixels/line])

Tline = LINE_LENGTH_PCK [pixels/line] * I*VTPXCK_period* / 4 (*Total number of image pipe lines*)

This relationship stands up regardless of the operating mode; full pixel mode, binning modes, Sub-sampling mode or combination of Sub-sampling and binning mode.

Settings and storage times are shown below.

* FINE_INTEG_TIME is a fixed value.

* LINE_LENGTH_PCK is a variable value.

(Recommended value of LINE_LENGTH_PCK is 5352. Any other value change require, please confirm with SONY.)

To set exposure time longer than 1 frame, you can either automatically extend it with the setting FRM_LENGTH_CTL=1 or perform truncation by frame length with the setting FRM_LENGTH_CTL = 0.

Table 5-25 Integration time setting (In case of FRM_LENGHT_CTL=0)

Parameter Setting		Frame time / Integration Time	
FRM_LENGTH_LINES [15:0]	COARSE_INTEG_TIME [15:0]	Frame time	Integration time (Tline stands for the duration of one line)
M	1	M Tline	(1+α)Tline
	2		(2+α)Tline
	…		...
	M-10		((M-10)+α)Tline
	(M-9) ~	prohibited	

* α =FINE_INTEG_TIME/LINE_LENGTH_PCK

* M: set value for given capture mode <= 65535

Table 5-23 Integration time setting(In case of FRM_LENGHT_CTL=1)

Parameter Setting		Frame time / Integration Time	
FRM_LENGTH_LINES [15:0]	COARSE_INTEG_TIME [15:0]	Frame time	Integration time (H stands for the duration of one line)
M	1	M Tline	(1+α) Tline
	2		(2+α) Tline
	…		…
	M-10		((M-10)+α) Tline
	M-9	(M+1) Tline	((M- 9)+α) Tline
	M-8	(M+2) Tline	((M- 8)+α) Tline
	…	…	…
	N	(N+10) Tline	(N +α) Tline

* α =FINE_INTEG_TIME/LINE_LENGTH_PCK

* M: set value for given capture mode <= 65535

* N: can be set with values greater than M <= 65525

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5.5. Gain setting

This sensor can apply analog gain on photo-electron signal and digital gain on digital signal after ADC.

Range of settable range is as follows.

Table 5-26 Range of Gains

	Max.	Note
Analog Gain	24dB	
Digital Gain	24dB	

5.5.1. Analog gain settings

The formula for analog gain is shown below.

Analog gain parameters are set with registers. Analog gain and digital gain are set separately.

$$Analog\ Gain = (m0 \times X + c0) / (m1 \times X + c1)$$

The variables of above equation are specified in the table below.

Table 5-27 Variables of analog gain settings

	Address	Bit	Name	Description	Notes
I²C register	0x008c	[7:0]	ANA_GAIN_M0 [15:8]	m0: fixed to 0	Read only static
	0x008d	[7:0]	ANA_GAIN_M0 [7:0]		
	0x0090	[7:0]	ANA_GAIN_M1 [15:8]	m1: fixed to -1	Read only static
	0x0091	[7:0]	ANA_GAIN_M1 [7:0]		
	0x008e	[7:0]	ANA_GAIN_C0 [15:8]	c0: fixed to 512	Read only static
	0x008f	[7:0]	ANA_GAIN_C0 [7:0]		
	0x0092	[7:0]	ANA_GAIN_C1 [15:8]	c1: fixed to 512	Read only static
	0x0093	[7:0]	ANA_GAIN_C1 [7:0]		
	0x0204	[0]	ANA_GAIN_GLOBAL [8]	X: Analog gain setting value	0 to 480
	0x0205	[7:0]	ANA_GAIN_GLOBAL [7:0]		

As a result, analog gain is calculated by the formula below.

$$Analog\ gain = 512 / (512 - X)$$

The relationship between the setting values X of ANA_GAIN_GLOBAL and the gain is shown in the following table. The ANA_GAIN_GLOBAL value is normally set in the range from 0 to 480 [0 dB to 24 dB].

Table 5-28 Analog gain setting reference [0 to 159]

Setting range: 0 - 480d

Setup other than the above is forbidden.

ana_gain_global	Gain(times)	Gain(dB)	ana_gain_global	Gain(times)	Gain(dB)	ana_gain_global	Gain(times)	Gain(dB)	ana_gain_global	Gain(times)	Gain(dB)
0	1.000	0.000	40	1.085	0.707	80	1.185	1.476	120	1.306	2.320
1	1.002	0.017	41	1.087	0.725	81	1.188	1.496	121	1.309	2.342
2	1.004	0.034	42	1.089	0.743	82	1.191	1.516	122	1.313	2.364
3	1.006	0.051	43	1.092	0.762	83	1.193	1.536	123	1.316	2.386
4	1.008	0.068	44	1.094	0.780	84	1.196	1.557	124	1.320	2.409
5	1.010	0.085	45	1.096	0.799	85	1.199	1.577	125	1.323	2.431
6	1.012	0.102	46	1.099	0.818	86	1.202	1.597	126	1.326	2.454
7	1.014	0.120	47	1.101	0.836	87	1.205	1.618	127	1.330	2.476
8	1.016	0.137	48	1.103	0.855	88	1.208	1.638	128	1.333	2.499
9	1.018	0.154	49	1.106	0.874	89	1.210	1.659	129	1.337	2.521
10	1.020	0.171	50	1.108	0.893	90	1.213	1.679	130	1.340	2.544
11	1.022	0.189	51	1.111	0.911	91	1.216	1.700	131	1.344	2.567
12	1.024	0.206	52	1.113	0.930	92	1.219	1.720	132	1.347	2.590
13	1.026	0.223	53	1.115	0.949	93	1.222	1.741	133	1.351	2.613
14	1.028	0.241	54	1.118	0.968	94	1.225	1.762	134	1.354	2.636
15	1.030	0.258	55	1.120	0.987	95	1.228	1.783	135	1.358	2.659
16	1.032	0.276	56	1.123	1.006	96	1.231	1.804	136	1.362	2.682
17	1.034	0.293	57	1.125	1.025	97	1.234	1.824	137	1.365	2.705
18	1.036	0.311	58	1.128	1.044	98	1.237	1.845	138	1.369	2.728
19	1.039	0.328	59	1.130	1.063	99	1.240	1.866	139	1.373	2.751
20	1.041	0.346	60	1.133	1.083	100	1.243	1.887	140	1.376	2.775
21	1.043	0.364	61	1.135	1.102	101	1.246	1.909	141	1.380	2.798
22	1.045	0.381	62	1.138	1.121	102	1.249	1.930	142	1.384	2.821
23	1.047	0.399	63	1.140	1.140	103	1.252	1.951	143	1.388	2.845
24	1.049	0.417	64	1.143	1.160	104	1.255	1.972	144	1.391	2.868
25	1.051	0.435	65	1.145	1.179	105	1.258	1.994	145	1.395	2.892
26	1.053	0.453	66	1.148	1.199	106	1.261	2.015	146	1.399	2.916
27	1.056	0.471	67	1.151	1.218	107	1.264	2.036	147	1.403	2.940
28	1.058	0.488	68	1.153	1.238	108	1.267	2.058	148	1.407	2.963
29	1.060	0.506	69	1.156	1.257	109	1.270	2.079	149	1.410	2.987
30	1.062	0.524	70	1.158	1.277	110	1.274	2.101	150	1.414	3.011
31	1.064	0.542	71	1.161	1.297	111	1.277	2.123	151	1.418	3.035
32	1.067	0.561	72	1.164	1.316	112	1.280	2.144	152	1.422	3.059
33	1.069	0.579	73	1.166	1.336	113	1.283	2.166	153	1.426	3.084
34	1.071	0.597	74	1.169	1.356	114	1.286	2.188	154	1.430	3.108
35	1.073	0.615	75	1.172	1.376	115	1.290	2.210	155	1.434	3.132
36	1.076	0.633	76	1.174	1.396	116	1.293	2.231	156	1.438	3.156
37	1.078	0.652	77	1.177	1.416	117	1.296	2.253	157	1.442	3.181
38	1.080	0.670	78	1.180	1.436	118	1.299	2.275	158	1.446	3.205
39	1.082	0.688	79	1.182	1.456	119	1.303	2.298	159	1.450	3.230

Table 5-29 Analog gain setting reference [160 to 319]

ana_gain_global	Gain(times)	Gain(dB)	ana_gain_global	Gain(times)	Gain(dB)	ana_gain_global	Gain(times)	Gain(dB)	ana_gain_global	Gain(times)	Gain(dB)
160	1.455	3.255	200	1.641	4.302	240	1.882	5.494	280	2.207	6.876
161	1.459	3.279	201	1.646	4.330	241	1.889	5.526	281	2.216	6.913
162	1.463	3.304	202	1.652	4.358	242	1.896	5.558	282	2.226	6.951
163	1.467	3.329	203	1.657	4.386	243	1.903	5.590	283	2.236	6.989
164	1.471	3.354	204	1.662	4.414	244	1.910	5.623	284	2.246	7.027
165	1.476	3.379	205	1.668	4.443	245	1.918	5.655	285	2.256	7.065
166	1.480	3.404	206	1.673	4.471	246	1.925	5.688	286	2.265	7.103
167	1.484	3.429	207	1.679	4.499	247	1.932	5.720	287	2.276	7.142
168	1.488	3.454	208	1.684	4.528	248	1.939	5.753	288	2.286	7.180
169	1.493	3.480	209	1.690	4.557	249	1.947	5.786	289	2.296	7.219
170	1.497	3.505	210	1.695	4.585	250	1.954	5.819	290	2.306	7.258
171	1.501	3.530	211	1.701	4.614	251	1.962	5.853	291	2.317	7.298
172	1.506	3.556	212	1.707	4.643	252	1.969	5.886	292	2.327	7.337
173	1.510	3.581	213	1.712	4.672	253	1.977	5.919	293	2.338	7.377
174	1.515	3.607	214	1.718	4.701	254	1.984	5.953	294	2.349	7.416
175	1.519	3.633	215	1.724	4.730	255	1.992	5.987	295	2.359	7.456
176	1.524	3.659	216	1.730	4.760	256	2.000	6.021	296	2.370	7.496
177	1.528	3.685	217	1.736	4.789	257	2.008	6.055	297	2.381	7.537
178	1.533	3.710	218	1.741	4.818	258	2.016	6.089	298	2.393	7.577
179	1.538	3.737	219	1.747	4.848	259	2.024	6.123	299	2.404	7.618
180	1.542	3.763	220	1.753	4.878	260	2.032	6.157	300	2.415	7.659
181	1.547	3.789	221	1.759	4.908	261	2.040	6.192	301	2.427	7.700
182	1.552	3.815	222	1.766	4.937	262	2.048	6.227	302	2.438	7.741
183	1.556	3.841	223	1.772	4.967	263	2.056	6.261	303	2.450	7.782
184	1.561	3.868	224	1.778	4.998	264	2.065	6.296	304	2.462	7.824
185	1.566	3.894	225	1.784	5.028	265	2.073	6.331	305	2.473	7.866
186	1.571	3.921	226	1.790	5.058	266	2.081	6.367	306	2.485	7.908
187	1.575	3.948	227	1.796	5.089	267	2.090	6.402	307	2.498	7.950
188	1.580	3.974	228	1.803	5.119	268	2.098	6.438	308	2.510	7.993
189	1.585	4.001	229	1.809	5.150	269	2.107	6.473	309	2.522	8.035
190	1.590	4.028	230	1.816	5.180	270	2.116	6.509	310	2.535	8.078
191	1.595	4.055	231	1.822	5.211	271	2.124	6.545	311	2.547	8.121
192	1.600	4.082	232	1.829	5.242	272	2.133	6.581	312	2.560	8.165
193	1.605	4.110	233	1.835	5.273	273	2.142	6.617	313	2.573	8.208
194	1.610	4.137	234	1.842	5.305	274	2.151	6.654	314	2.586	8.252
195	1.615	4.164	235	1.848	5.336	275	2.160	6.690	315	2.599	8.296
196	1.620	4.192	236	1.855	5.367	276	2.169	6.727	316	2.612	8.340
197	1.625	4.219	237	1.862	5.399	277	2.179	6.764	317	2.626	8.385
198	1.631	4.247	238	1.869	5.430	278	2.188	6.801	318	2.639	8.429
199	1.636	4.275	239	1.875	5.462	279	2.197	6.838	319	2.653	8.474

Table 5-30 Analog gain setting reference [320 to 480]

ana_gain_global	Gain(times)	Gain(dB)
320	2.667	8.519
321	2.681	8.565
322	2.695	8.610
323	2.709	8.656
324	2.723	8.702
325	2.738	8.749
326	2.753	8.795
327	2.768	8.842
328	2.783	8.889
329	2.798	8.936
330	2.813	8.984
331	2.829	9.032
332	2.844	9.080
333	2.860	9.128
334	2.876	9.177
335	2.893	9.226
336	2.909	9.275
337	2.926	9.325
338	2.943	9.374
339	2.960	9.424
340	2.977	9.475
341	2.994	9.525
342	3.012	9.576
343	3.030	9.628
344	3.048	9.679
345	3.066	9.731
346	3.084	9.783
347	3.103	9.836
348	3.122	9.889
349	3.141	9.942
350	3.160	9.995
351	3.180	10.049
352	3.200	10.103
353	3.220	10.157
354	3.241	10.212
355	3.261	10.267
356	3.282	10.323
357	3.303	10.379
358	3.325	10.435
359	3.346	10.492
360	3.368	10.549
361	3.391	10.606
362	3.413	10.664
363	3.436	10.722
364	3.459	10.780
365	3.483	10.839
366	3.507	10.898
367	3.531	10.958
368	3.556	11.018
369	3.580	11.079
370	3.606	11.140
371	3.631	11.201
372	3.657	11.263
373	3.683	11.325
374	3.710	11.388
375	3.737	11.451
376	3.765	11.515
377	3.793	11.579
378	3.821	11.643
379	3.850	11.708
380	3.879	11.774
381	3.908	11.840
382	3.938	11.907
383	3.969	11.974
384	4.000	12.041
385	4.031	12.109
386	4.063	12.178
387	4.096	12.247
388	4.129	12.317
389	4.163	12.387
390	4.197	12.458
391	4.231	12.530
392	4.267	12.602
393	4.303	12.674
394	4.339	12.748
395	4.376	12.822
396	4.414	12.896
397	4.452	12.971
398	4.491	13.047
399	4.531	13.124
400	4.571	13.201
401	4.613	13.279
402	4.655	13.358
403	4.697	13.437
404	4.741	13.517
405	4.785	13.598
406	4.830	13.679
407	4.876	13.762
408	4.923	13.845
409	4.971	13.929
410	5.020	14.013
411	5.069	14.099
412	5.120	14.185
413	5.172	14.273
414	5.224	14.361
415	5.278	14.450
416	5.333	14.540
417	5.389	14.631
418	5.447	14.723
419	5.505	14.816
420	5.565	14.910
421	5.626	15.005
422	5.689	15.101
423	5.753	15.198
424	5.818	15.296
425	5.885	15.395
426	5.953	15.495
427	6.024	15.597
428	6.095	15.700
429	6.169	15.804
430	6.244	15.909
431	6.321	16.016
432	6.400	16.124
433	6.481	16.233
434	6.564	16.344
435	6.649	16.456
436	6.737	16.569
437	6.827	16.684
438	6.919	16.801
439	7.014	16.919
440	7.111	17.039
441	7.211	17.160
442	7.314	17.283
443	7.420	17.408
444	7.529	17.535
445	7.642	17.664
446	7.758	17.795
447	7.877	17.927
448	8.000	18.062
449	8.127	18.199
450	8.258	18.338
451	8.393	18.479
452	8.533	18.622
453	8.678	18.768
454	8.828	18.917
455	8.982	19.068
456	9.143	19.222
457	9.309	19.378
458	9.481	19.538
459	9.660	19.700
460	9.846	19.865
461	10.039	20.034
462	10.240	20.206
463	10.449	20.381
464	10.667	20.561
465	10.894	20.743
466	11.130	20.930
467	11.378	21.121
468	11.636	21.316
469	11.907	21.516
470	12.190	21.720
471	12.488	21.930
472	12.800	22.144
473	13.128	22.364
474	13.474	22.590
475	13.838	22.821
476	14.222	23.059
477	14.629	23.304
478	15.059	23.556
479	15.515	23.815
480	16.000	24.082

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5.5.2. Digital gain settings

Digital gain of this sensor can be set by color. The registers for digital gain settings are shown in the table below.

Table 5-31 Digital gain setting

	Address	Bit	Name	Description	Notes
I²C register	0x020e	[7:0]	DIG_GAIN_GR [15:8]	Digital gain control code for GR Format : 16-bit unsigned iReal	range: 1 to 15
	0x020f	[7:0]	DIG_GAIN_GR [7:0]		range: 0 to 255
	0x0210	[7:0]	DIG_GAIN_R [15:8]	Digital gain control code for R Format : 16-bit unsigned iReal	range: 1 to 15
	0x0211	[7:0]	DIG_GAIN_R [7:0]		range: 0 to 255
	0x0212	[7:0]	DIG_GAIN_B [15:8]	Digital gain control code for B Format : 16-bit unsigned iReal	range: 1 to 15
	0x0213	[7:0]	DIG_GAIN_B [7:0]		range: 0 to 255
	0x0214	[7:0]	DIG_GAIN_GB [15:8]	Digital gain control code for GB Format : 16-bit unsigned iReal	range: 1 to 15
	0x0215	[7:0]	DIG_GAIN_GB [7:0]		range: 0 to 255

Each register is comprised of 2 bytes with the *upper_byte* [15:8] setting the integer portion and the *lower_byte* [7:0] setting the decimal portion of the gain. The gain for each color is obtained by the following formula.

Digital gain = *upper_byte* + *lower_byte* / 256 [times]

The unit of Digital gain is times. The upper byte can be set to a value ranging from 1 to 127 and the lower byte to a value ranging from 0 to 255. Therefore, the range of digital gain is shown as follows.

1 + 0/256 [times] (0 dB) ≤ *Digital gain* ≤ 15 + 255/256 [times] (≒24 dB)

When representing the gain by log-linear scale [dB], lower gain takes coarse steps and high gain takes fine steps for the incrimination of the register value. The table below indicates the register values in 0.1 dB steps for reference.

Table 5-32 Digital gain setting reference (0 to 23.9[dB])

Upper		Lower		Gain [times]	Gain [dB]	Upper		Lower		Gain [times]	Gain [dB]	Upper		Lower		Gain [times]	Gain [dB]	Upper		Lower		Gain [times]	Gain [dB]
dec	hex	dec	hex			dec	hex	dec	hex			dec	hex	dec	hex			dec	hex	dec	hex		
1	1	0	0	1	0	1	1	255	FF	2	6	3	3	251	FB	3.98	12	7	7	241	F1	7.94	18
1	1	3	3	1.01	0.1	2	2	5	5	2.02	6.11	4	4	7	7	4.03	12.1	8	8	9	9	8.04	18.1
1	1	6	6	1.02	0.2	2	2	11	B	2.04	6.21	4	4	19	13	4.07	12.2	8	8	33	21	8.13	18.2
1	1	9	9	1.04	0.3	2	2	17	11	2.07	6.3	4	4	31	1F	4.12	12.3	8	8	57	39	8.22	18.3
1	1	12	C	1.05	0.4	2	2	23	17	2.09	6.4	4	4	43	2B	4.17	12.4	8	8	81	51	8.32	18.4
1	1	15	F	1.06	0.49	2	2	29	1D	2.11	6.5	4	4	56	38	4.22	12.5	8	8	106	6A	8.41	18.5
1	1	18	12	1.07	0.59	2	2	35	23	2.14	6.59	4	4	68	44	4.27	12.6	8	8	131	83	8.51	18.6
1	1	21	15	1.08	0.68	2	2	42	2A	2.16	6.71	4	4	81	51	4.32	12.7	8	8	156	9C	8.61	18.7
1	1	25	19	1.1	0.81	2	2	48	30	2.19	6.8	4	4	93	5D	4.36	12.8	8	8	182	B6	8.71	18.8
1	1	28	1C	1.11	0.9	2	2	55	37	2.21	6.91	4	4	106	6A	4.41	12.9	8	8	207	CF	8.81	18.9
1	1	31	1F	1.12	0.99	2	2	61	3D	2.24	7	4	4	120	78	4.47	13	8	8	234	EA	8.91	19
1	1	35	23	1.14	1.11	2	2	68	44	2.27	7.1	4	4	133	85	4.52	13.1	9	9	4	4	9.02	19.1
1	1	38	26	1.15	1.2	2	2	74	4A	2.29	7.19	4	4	146	92	4.57	13.2	9	9	31	1F	9.12	19.2
1	1	41	29	1.16	1.29	2	2	81	51	2.32	7.3	4	4	160	A0	4.63	13.3	9	9	58	3A	9.23	19.3
1	1	45	2D	1.18	1.41	2	2	88	58	2.34	7.4	4	4	173	AD	4.68	13.4	9	9	85	55	9.33	19.4
1	1	48	30	1.19	1.49	2	2	95	5F	2.37	7.5	4	4	187	BB	4.73	13.5	9	9	113	71	9.44	19.5
1	1	52	34	1.2	1.61	2	2	102	66	2.4	7.6	4	4	201	C9	4.79	13.6	9	9	141	8D	9.55	19.6
1	1	55	37	1.21	1.69	2	2	109	6D	2.43	7.7	4	4	215	D7	4.84	13.7	9	9	169	A9	9.66	19.7
1	1	59	3B	1.23	1.8	2	2	116	74	2.45	7.79	4	4	230	E6	4.9	13.8	9	9	198	C6	9.77	19.8
1	1	63	3F	1.25	1.91	2	2	124	7C	2.48	7.9	4	4	244	F4	4.95	13.9	9	9	227	E3	9.89	19.9
1	1	66	42	1.26	1.99	2	2	131	83	2.51	8	5	5	3	3	5.01	14	10	A	0	0	10	20
1	1	70	46	1.27	2.1	2	2	138	8A	2.54	8.09	5	5	18	12	5.07	14.1	10	A	30	1E	10.12	20.1
1	1	74	4A	1.29	2.21	2	2	146	92	2.57	8.2	5	5	33	21	5.13	14.2	10	A	60	3C	10.23	20.2
1	1	78	4E	1.3	2.31	2	2	154	9A	2.6	8.3	5	5	48	30	5.19	14.3	10	A	90	5A	10.35	20.3
1	1	81	51	1.32	2.39	2	2	161	A1	2.63	8.4	5	5	64	40	5.25	14.4	10	A	121	79	10.47	20.4
1	1	85	55	1.33	2.49	2	2	169	A9	2.66	8.5	5	5	79	4F	5.31	14.5	10	A	152	98	10.59	20.5
1	1	89	59	1.35	2.59	2	2	177	B1	2.69	8.6	5	5	95	5F	5.37	14.6	10	A	183	B7	10.71	20.6
1	1	93	5D	1.36	2.69	2	2	185	B9	2.72	8.7	5	5	111	6F	5.43	14.7	10	A	215	D7	10.84	20.7
1	1	97	61	1.38	2.79	2	2	193	C1	2.75	8.8	5	5	127	7F	5.5	14.8	10	A	247	F7	10.96	20.8
1	1	101	65	1.39	2.89	2	2	201	C9	2.79	8.9	5	5	143	8F	5.56	14.9	11	B	23	17	11.09	20.9
1	1	106	6A	1.41	3.01	2	2	210	D2	2.82	9.01	5	5	160	A0	5.63	15	11	B	56	38	11.22	21
1	1	110	6E	1.43	3.1	2	2	218	DA	2.85	9.10	5	5	176	B0	5.69	15.1	11	B	90	5A	11.35	21.1
1	1	114	72	1.45	3.2	2	2	226	E2	2.88	9.2	5	5	193	C1	5.75	15.2	11	B	123	7B	11.48	21.2
1	1	118	76	1.46	3.29	2	2	235	EB	2.92	9.3	5	5	210	D2	5.82	15.3	11	B	157	9D	11.61	21.3
1	1	123	7B	1.48	3.41	2	2	244	F4	2.95	9.41	5	5	227	E3	5.89	15.4	11	B	192	C0	11.75	21.4
1	1	127	7F	1.5	3.5	2	2	252	FC	2.98	9.5	5	5	245	F5	5.96	15.5	11	B	227	E3	11.89	21.5
1	1	131	83	1.51	3.59	3	3	5	5	3.02	9.6	6	6	7	7	6.03	15.6	12	C	6	6	12.02	21.6
1	1	136	88	1.53	3.7	3	3	14	E	3.05	9.7	6	6	24	18	6.09	15.7	12	C	41	29	12.16	21.7
1	1	140	8C	1.55	3.79	3	3	23	17	3.09	9.8	6	6	42	2A	6.16	15.8	12	C	77	4D	12.3	21.8
1	1	145	91	1.57	3.90	3	3	32	20	3.13	9.9	6	6	61	3D	6.24	15.9	12	C	114	72	12.45	21.9
1	1	150	96	1.59	4.01	3	3	42	2A	3.16	10	6	6	79	4F	6.31	16	12	C	151	97	12.59	22
1	1	154	9A	1.6	4.09	3	3	51	33	3	10.1	6	6	98	62	6.38	16.1	12	C	188	BC	12.73	22.1
1	1	159	9F	1.62	4.2	3	3	60	3C	3.23	10.2	6	6	117	75	6.46	16.2	12	C	226	E2	12.88	22.2
1	1	164	A4	1.64	4.3	3	3	70	46	3.27	10.3	6	6	136	88	6.53	16.3	13	D	8	8	13.03	22.3
1	1	169	A9	1.66	4.4	3	3	80	50	3.31	10.4	6	6	155	9B	6.61	16.4	13	D	47	2F	13.18	22.4
1	1	174	AE	1.68	4.5	3	3	90	5A	3.35	10.5	6	6	175	AF	6.68	16.5	13	D	86	56	13.34	22.5
1	1	179	B3	1.7	4.6	3	3	99	63	3.39	10.6	6	6	195	C3	6.76	16.6	13	D	125	7D	13.49	22.6
1	1	184	B8	1.72	4.7	3	3	109	6D	3.43	10.7	6	6	215	D7	6.84	16.7	13	D	165	A5	13.64	22.7
1	1	189	BD	1.74	4.8	3	3	120	78	3.47	10.8	6	6	235	EB	6.92	16.8	13	D	206	CE	13.8	22.8
1	1	194	C2	1.76	4.9	3	3	130	82	3.51	10.9	7	7	0	0	7.00	16.9	13	D	247	F7	13.96	22.9
1	1	199	C7	1.78	5	3	3	140	8C	3.55	11	7	7	20	14	7.08	17	14	E	32	20	14.13	23
1	1	205	CD	1.8	5.11	3	3	151	97	3.59	11.1	7	7	41	29	7.16	17.1	14	E	74	4A	14.29	23.1
1	1	210	D2	1.82	5.2	3	3	161	A1	3.63	11.2	7	7	63	3F	7.25	17.2	14	E	116	74	14.45	23.2
1	1	215	D7	1.84	5.3	3	3	172	AC	3.67	11.3	7	7	84	54	7.33	17.3	14	E	159	9F	14.62	23.3
1	1	221	DD	1.86	5.41	3	3	183	B7	3.71	11.4	7	7	106	6A	7.41	17.4	14	E	203	CB	14.79	23.4
1	1	226	E2	1.88	5.5	3	3	194	C2	3.76	11.5	7	7	128	80	7.50	17.5	14	E	246	F6	14.96	23.5
1	1	232	E8	1.91	5.6	3	3	205	CD	3.8	11.6	7	7	150	96	7.59	17.6	15	F	35	23	15.14	23.6
1	1	237	ED	1.93	5.69	3	3	217	D9	3.85	11.7	7	7	172	AC	7.67	17.7	15	F	80	50	15.31	23.7
1	1	243	F3	1.95	5.8	3	3	228	E4	3.89	11.8	7	7	195	C3	7.76	17.8	15	F	125	7D	15.49	23.8
1	1	249	F9	1.97	5.9	3	3	239	EF	3.93	11.9	7	7	218	DA	7.85	17.9	15	F	171	AB	15.67	23.9
																		15	F	217	D9	15.85	24

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5.5.3. Change in output pixel level depending on binning mode

The output pixel level in Binning mode changes as shown in the table.

Table 5-33 Output pixel level according to binning modes

HDR_ MODE 0x0220[0]	BINNING_ MODE 0x0900	BINNING_ TYPE 0x0901	BINNING_ WEIGHTING 0x0902	Output Pixel Level Ratio	Max Analog Gain[dB]
0	0	x	x	1	24
	1	0x12	0x00	1	24
			0x01	2	24
			0x02	1	24
		0x14	0x00	1	24
			0x01	4	24
			0x02	1	24
		other	Not supported		
1	x	x	x	1	24

* Values in parentheses for pixel level are output pixel level to which pedestal level (0x40) is added.

Table 5-34 Binning mode determining registers

	Address	Bit	Name	Description
I²C register	0x0902	[7:0]	BINNING_WEIGHTING	Binning type selection for Horizontal 0 : additional average 1 : addition (summed) 2 : weighting addition average *Setup other than the above is forbidden.

*For BINNING_MODE and BINNING_TYPE see 5.2.3

As shown on Table 5-34, H/V weighting addition average is available by specifying BINNING_WEIGHTING as 0x02 with Binning mode. However it's not available on HDR capture mode. Thus, H/V weighting addition average is impossible on HDR capture mode.

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5.5.4. Bayer weighting function

Bayer weighting function optimizes the center of gravity of every color when using binning mode.

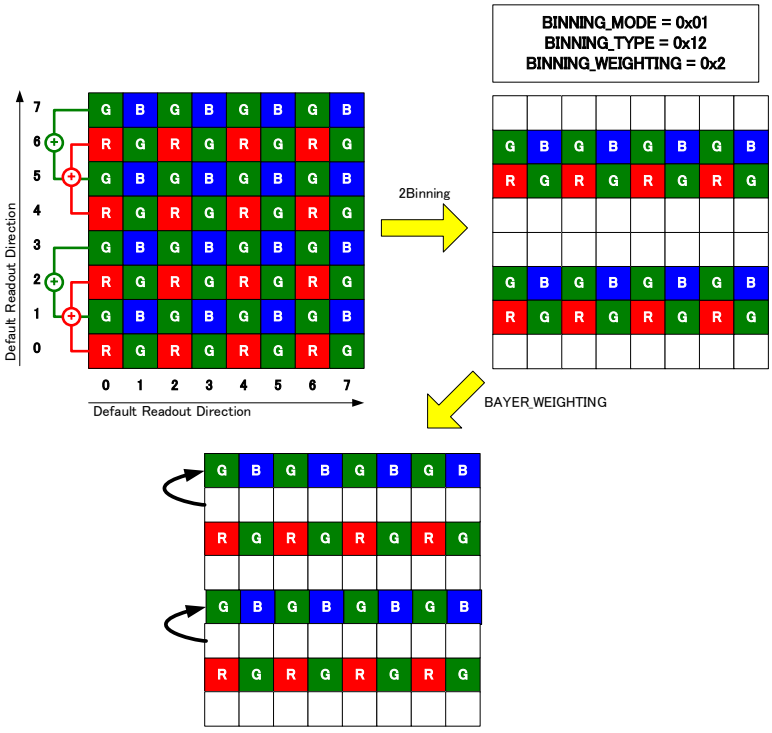

Figure 5-12 Bayer weighting methodology

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5.6. Optical black level clamp

5.6.1. Default setting (normal usage)

This sensor has the optical black level clamping function to make the black level stable against changes in operating conditions. The average value of the black level is adjusted to the pedestal level (0x40).

In the case where RAW8 (non-compression) format is selected, the clamping level becomes 1/4 following the output format internally.

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5.6.2. Test mode setting

Set the registers shown in the table below to control output black level for test purpose.

Table 5-35 Optical black level clamp related registers and descriptions

	Address	Bit	Name	Description
I²C register	0x3092	[1:0]	MANUAL_DATA_PEDESTAL_VALUE [9:8]	Manual setting value for Data Pedestal Default setting value : 0x40
	0x3093	[7:0]	MANUAL_DATA_PEDESTAL_VALUE [7:0]	
	0x3090	[0]	MANUAL_DATA_PEDESTAL_ENABLE	Output black level is controlled with MANUAL_DATA_PEDESTAL_VALUE register value 0x0 : pedestal = 0x40 (fixed value) 0x1 : pedestal = MANUAL_DATA_PEDESTAL_VALUE else : inhibited value

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5.7. Image compensation function setting

There are some other functions in the sensor image pipeline. Use-case may be chosen in terms of trade-off for power consumption and image quality, for example.

5.7.1. Shield Pixel

PDAF capable sensor is equipped with half metal-shielded pixels called "shielded pixel" which is embedded uniformly within regular pixels at a certain ratio. Metal-shielded pixels have two types; a right shielded and left shielded, and are located in green pixels. Phase information from these left and right shields enables Phase Detection Auto Focus (PDAF) for high-speed auto focus by outside ISP.

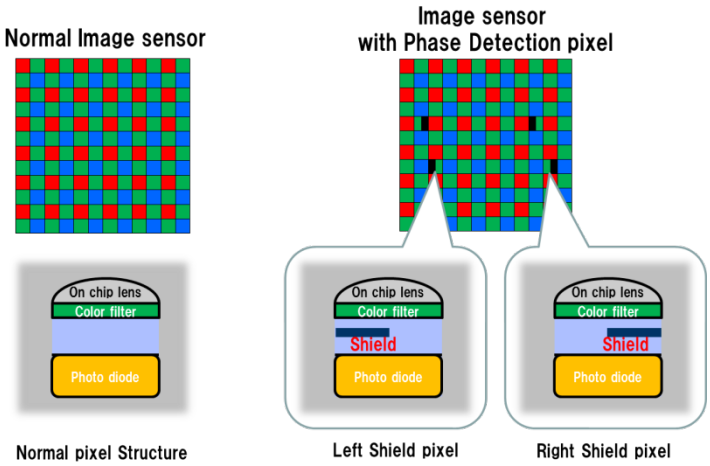

Figure 5-13 Structure of sensor

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5.7.2. Shield Pixel Correction (SPC)

In this paragraph, abstracts of Shield Pixel Correction and an additional defect correction which are both unique function for PDAF capable sensors.

Shield pixel correction

Shield pixels have smaller signal values than normal green pixels because a part of the light is blocked with the metal shield. A shield pixel requires to have some gain such that the signal level of each shield pixel will be equivalent to a normal pixel. This is called “Shield Pixel Correction” (SPC).

For more details, refer to the PDAF Module Calibration Manual.

Note that, when using SPC, writing 9 x 7 knot point Gain table to OTP is required.

This SPC gain map value is written by the module vendor as the module calibration process.

SPC is controlled by register. It's possible to set effective pixel area and shield pixel area separately. (Please refer to 4.6 Output image format about effective pixel area and shield pixel area.)

Table 5-36 SPC control register

	Address	Bit	Name	Description
I²C register	0x7BC8	[0]	EFFECTIVE_SPC_GAIN_EN	Shield Pixel (include Effective pixel area) Gained Correction Enable 0 : Disable 1 : Enable Default setting value : 0x1
	0x7BC9	[0]	SHIELD_SPC_GAIN_EN	Shield Pixel (include Shield pixel area) Gained Correction Enable 0 : Disable 1 : Enable(only available EFFECTIVE_SPC_GAIN_EN =1) Default setting value : 0x1

Additional defect correction

After completion of the above correction, the shielded pixels are additionally and automatically corrected to be as equivalent with normal pixel as possible. So there is no need of special correction setting by module vendor or set vendor.

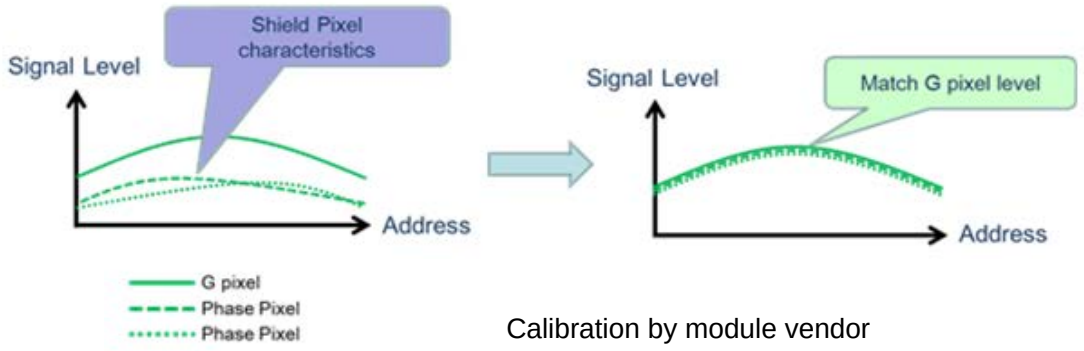

Figure 5-14 Shield Pixel Correction

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5.7.3. Defect Pixel Correction (DPC)

5.7.3.1. Static Defect Correction

This function correct the pixel defects up to 12 defects by matching the physical address information of defect pixels stored in the OTP in advance and the read address to access when you actually read. It does defect correction processing of the pixel data corresponding to the address that matches. The address matching between the physical address and the read address is automatically done within the sensor.

"Single Defect pixel" and "Continuous Defect Pixels" (including Same Color Continuous Defect Pixels) can be corrected.

See "IMX258 OTP manual " for how to use the function.

5.7.3.2. Dynamic Defect Correction

This is a function to detect and correct single pixel defects. It performs defect compensation with using pixels surrounding a defect pixel.

* If an adjacent pixel of the same color is defective, this function cannot correct the defect.

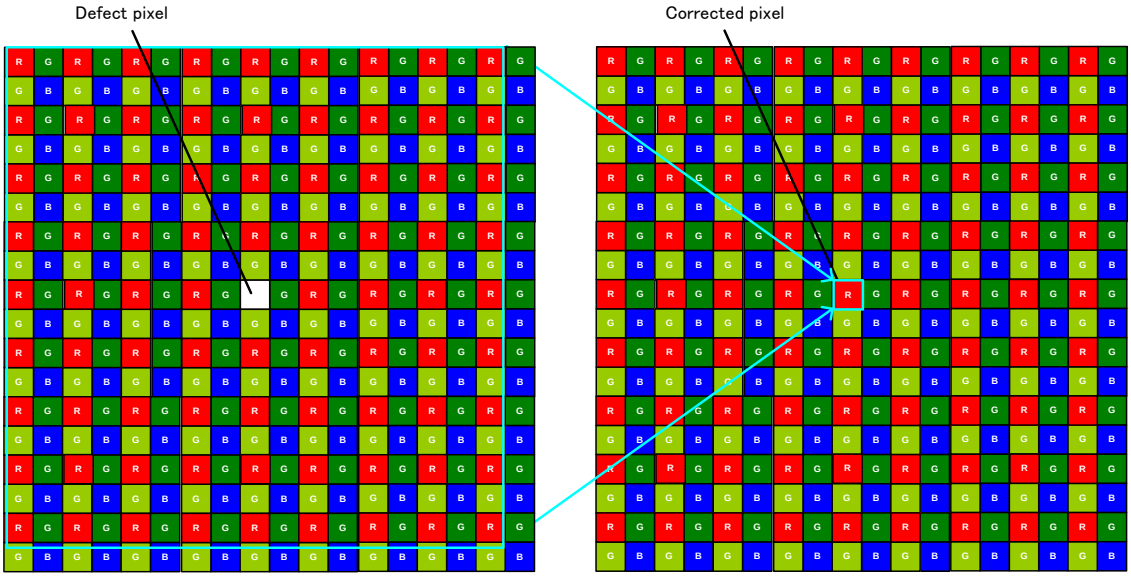

Figure 5-15　Dynamic Defect Correction model figure

Whether to turn each Defect Correction ON or OFF can be set with the following registers.

Table 5-37 Defect correction register

	Address	Bit	Name	Description
I²C register	0x0b05	[0]	MAP_COUP_CORR_EN	Mapped couplet correction control 0 : disable 1 : enable
	0x0b06	[0]	SING_DEF_CORR_EN	dynamic singlet correction control 0 : disable 1 : enable

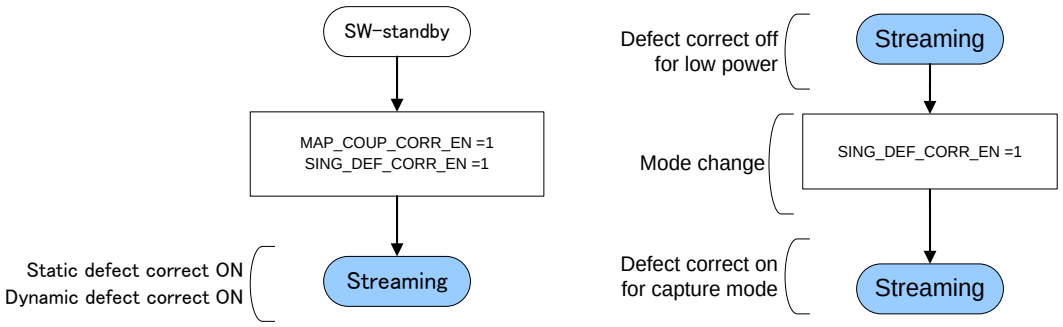

Figure 5-16 Defect correction flow chart

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6. Power ON/OFF Sequence

6.1. Power ON sequence

6.1.1. Power ON reset

This sensor doesn't have a built-in "Power ON Reset" function.

The XCLR pin is set to "LOW" and the power supplies are brought up. Then the XCLR pin should be set to "High" after INCK supplied.

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6.1.2. Power ON sequence

6.1.2.1. Start up sequence with 2-wire serial communication (external reset)

Follow the power supply start up sequence below.

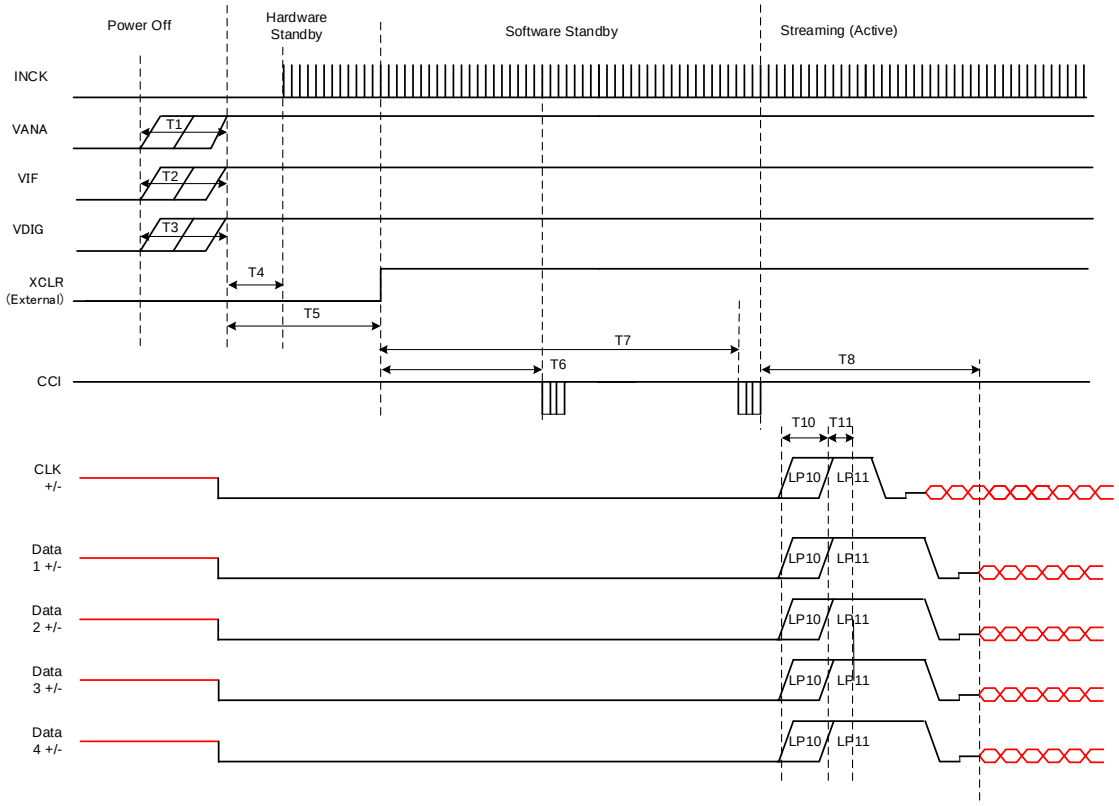

Figure 6-1 Start up sequence with 2-wire serial communication (external reset)

*Presence of INCK during Power Off is acceptable despite of above chart.

Table 6-1 Startup sequence timing constraints (2-wire serial communication mode with external reset)

Item	Label	Min.	Max.	Unit	Comment
VANA rising – VANA ON	T1	VANA and VDIG and VIF may rise in any order.		µs	Slew rate of VANA, VDIG and VIF (0%-100%): Max50 mv/us
VDIG rising – VDIG ON	T2			µs	
VIF rising – VIF ON	T3			µs	
VANA and VDIG and VIF rising - INCK start	T4	0		µs	
VANA and VDIG and VIF rising - XCLR rising	T5	0		ms	After T1,T2 and T3
INCK start and XCLR rising till CCI Read version ID register wait time	T6	0.4		ms	
INCK start and XCLR rising till Send Streaming Command wait time (To complete reading all parameters from NVM)	T7	12		ms	
Start of first streaming from Sending Streaming Command.	T8		2.0 ms + The delay of the coarse integration time value		
DPHY power up	T10	1	1.1	ms	
DPHY init	T11	100	110	µs	

* XCLR needs to be Low level until all power supplies complete power-ON.

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6.2. Power down sequence

6.2.1. Power down sequence with 2-wire serial communication

Follow the power down sequence below.

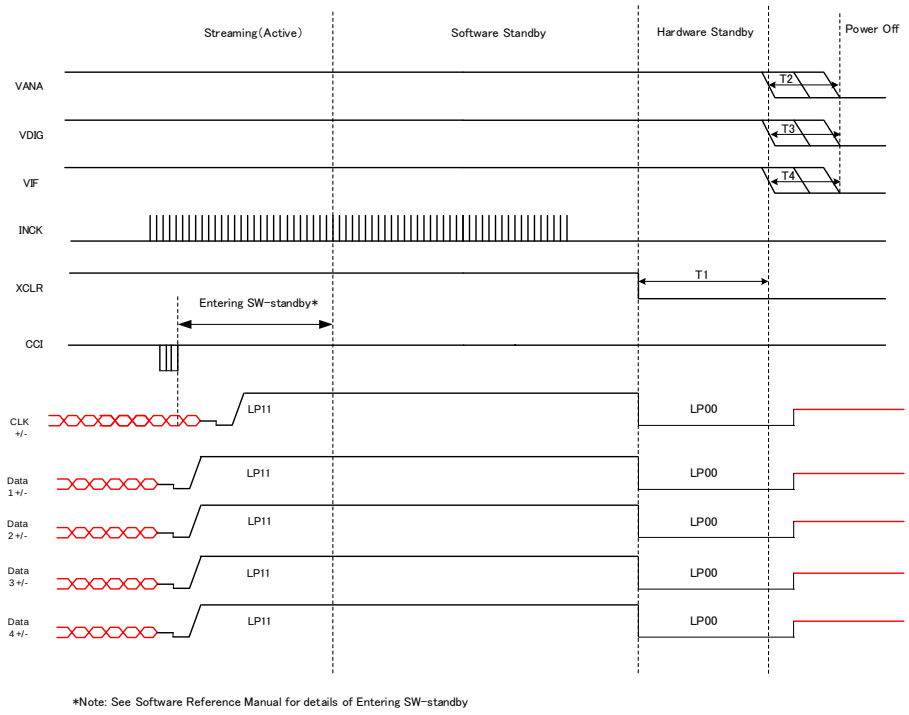

Figure 6-2 Power down sequence with 2-wire serial communication (external reset)

Table 6-2 Power down sequence timing constraints (2-wire serial communication mode with external reset)

Item	Label	Min.	Max.	Unit	Comment
XCLR Neg-edge - VANA (VDIG or VIF) fall	T1	0		µs	
Sequence free of VANA falling and VDIG falling and VIF falling	T2,T3,T4	VANA and VDIG and VIF may fall in any order.		µs	

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7. Mode Transition Sequence and Register Update Timing

7.1. Transition between SW-standby and Streaming

Sensor can make transition between SW-standby and streaming without using power ON/OFF.

7.1.1. SW-standby to Streaming

The following figure shows how to start streaming at first time after power on sequence and register setting timing restriction

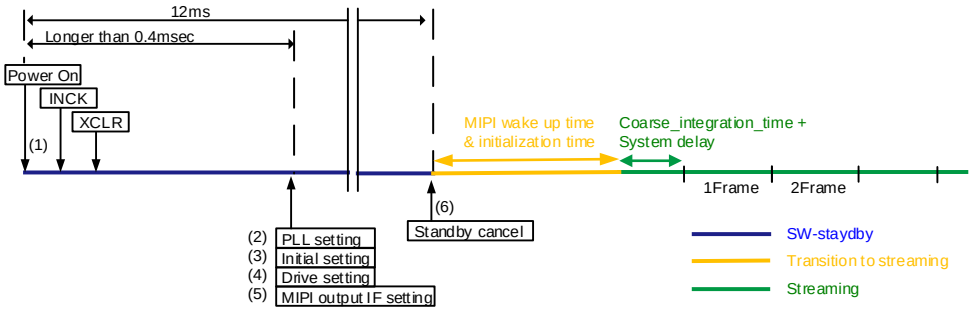

Figure 7-1 Start streaming sequence after power ON

Table 7-1 Start streaming sequence after power ON

(1)	Refer to power up sequence timing diagram	Note: Refer to Power Related sequence of Figure 7-1 for procedure of (2) - (6).
(2)	Set PLL parameters	
(3)	Basic settings (operation-critical setting)	
(4)	Set readout mode (start/end position, size, mode, integration time, and gain)	
(5)	Set MIPI interface parameters	
(6)	Start streaming with 0x0100 (MODE_SEL = 1)	
	After “MIPI Wake Up Time” + “Initialize Time”, 1st frame starts and images come out	

The following figure shows how to start a streaming after first streaming.

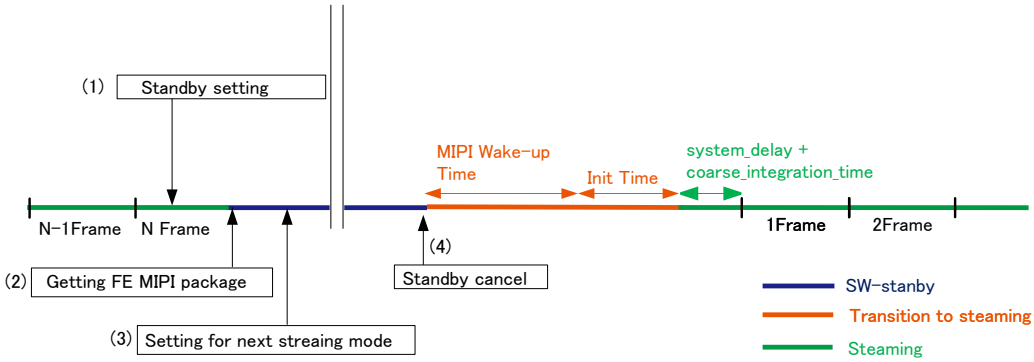

Figure 7-2 Start streaming after first streaming

Table 7-2 Start streaming after first streaming

(1)	Standby setting in streaming with 0x0100 (MODE_SEL = 0)	Note: Refer to Figure 7-2 for procedure of (1) to (4).
(2)	Waiting for MIPI FE package	
(3)	Set register for next streaming mode	
(4)	Start streaming with 0x0100 (MODE_SEL = 1)	
	After “MIPI Wake Up Time” + “Initialize Time”, 1st frame starts and images come out	

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7.1.2. Streaming to SW-standby

This section will introduce how to end streaming and exit to SW-standby.

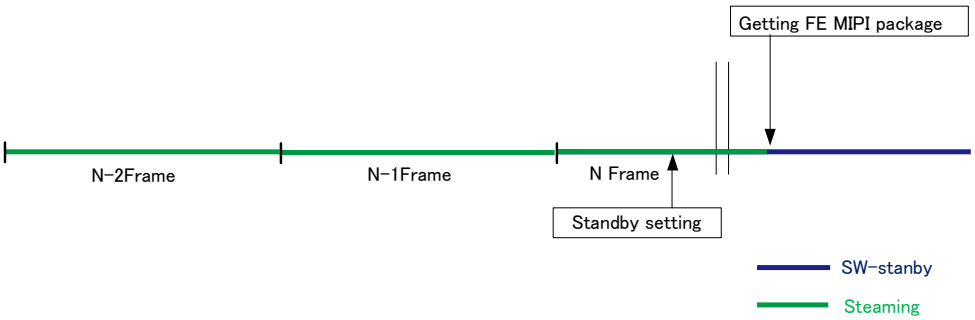

Figure 7-3 transition to SW-standby from streaming

(1) In case a SW-standby command is issued in between “FS” and “FE”, this sensor completes outputting the image data and transits to a standby state.

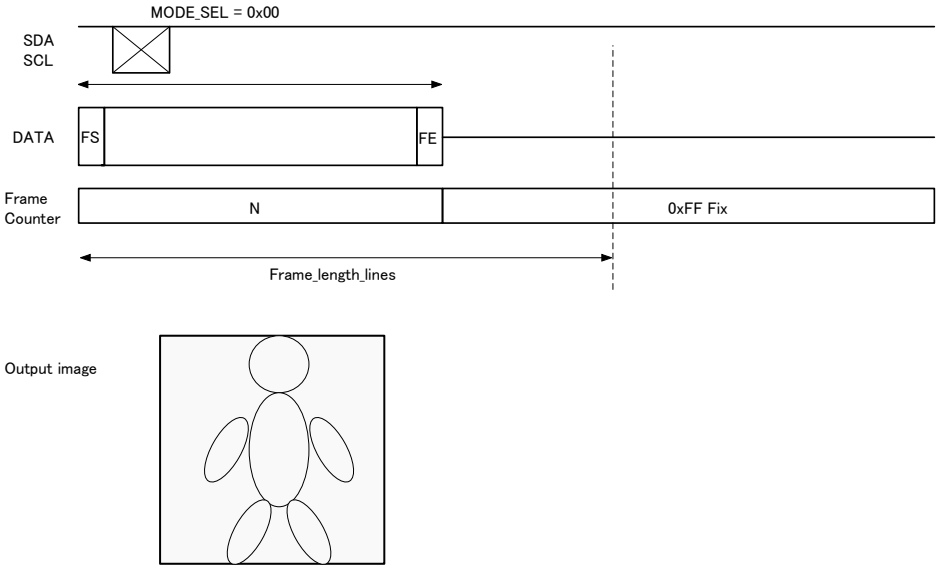

Figure 7-4　SW-standby transition pattern 1

(2) In case a SW-standby command is issued within a “Frame Blanking” period, this sensor immediately transits to a software standby state.

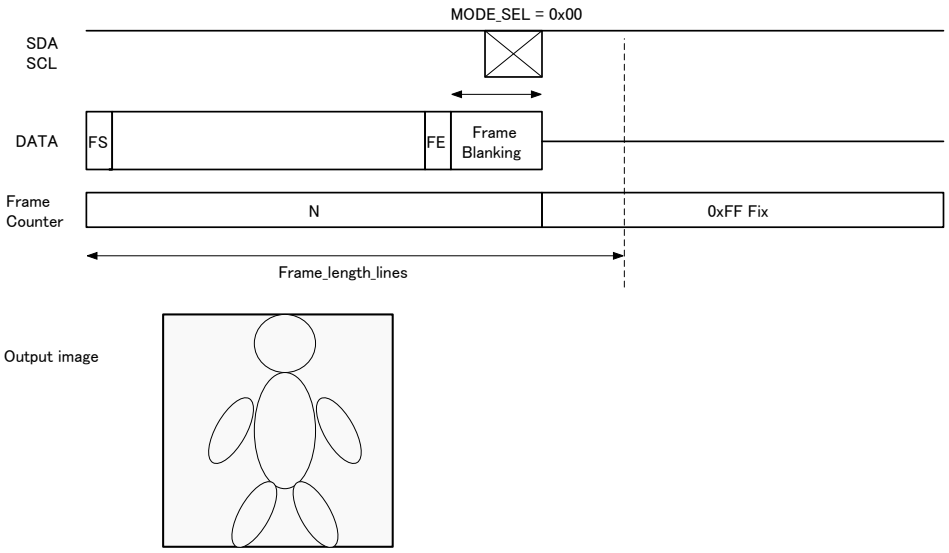

Figure 7-5　SW-standby standby transition pattern 2

(3) In case a SW-standby command is issued in between “FS” and “FE” while the sensor is working in fast SW-standby mode, this sensor completes outputting the line’s image data to where the command belongs and transit to the standby.

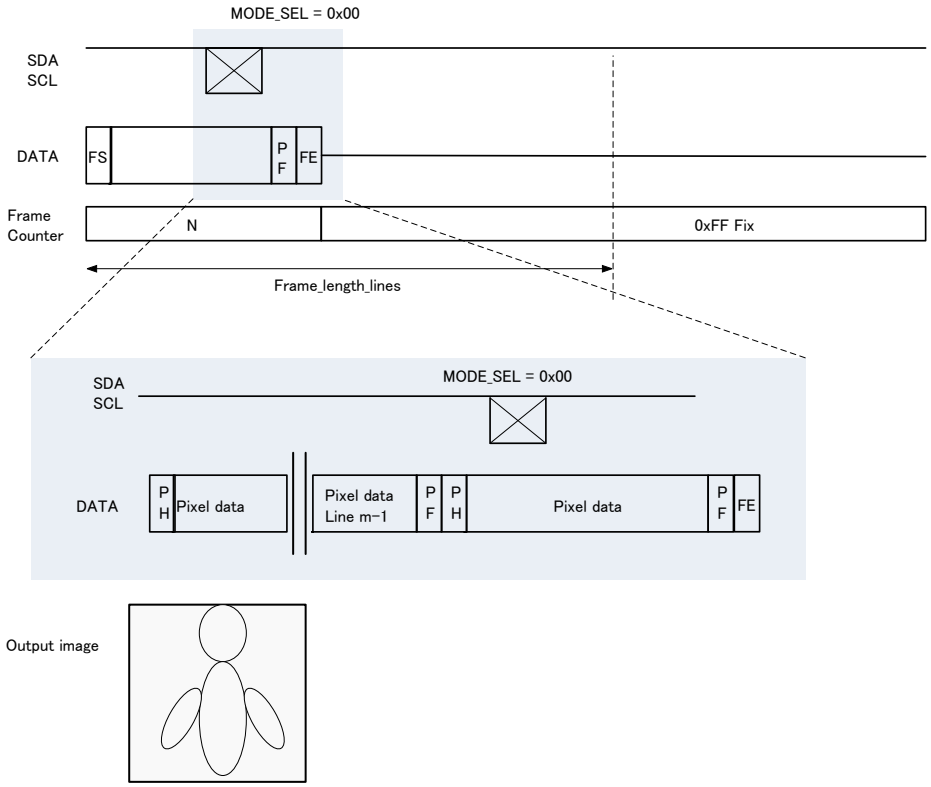

Figure 7-6 Software standby transition pattern 3 (Fast SW standby)

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7.2. Streaming mode transition

Changes between different operation modes may or may not cause a corrupted frame. In this section, under what conditions the sensor cause the corrupted frame is first explained. Then, by knowing the conditions, different kinds of mode transitions are discussed.

7.2.1. Change sequence of corrupted frame related registers

When changing the mode with Corrupted-frame-related registers (vertical direction parameters and some other registers listed in Table 7-3 photo-electron charge integration operation becomes irregular for one frame after updating of the register. This frame shall be treated as invalid frame. Invalid frame should not be output.

Table 7-3 List of corrupted frame causing registers

	Address	Bit	Name	Description
I²C register	0x0101	[1]	IMG_ORIENTATION_V	Image orientation for Vertical direction 0 : normal 1 : reverse
	0x0220	[5:0]	HDR_MODE[5:0] (*only bit[0] cause corrupted frame)	[0]: 0 HDR disable 1 HDR enable [1]: 0 combined gain used (during HDR) 1 separate gain used (during HDR) [2]: not used [3]: not used [4]: not used [5]: 0 short exposure determined by ratio (during HDR) 1 short exposure controlled by direct control (during HDR)
	0x0342	[7:0]	LINE_LENGTH_PCK[15:8]	The length of line Unit : pixels Format : 16-bit unsigned integer * Set to 5352d. Any other value change require, please confirm with SONY.
	0x0343	[7:0]	LINE_LENGTH_PCK[7:0]	
	0x0346	[3:0]	Y_ADD_STA[11:8]	Vertical direction analog cropping start position within the active pixels area Unit : pixels Format : 16-bit unsigned integer * Note that this is the cropping end position when flipping (IMG_ORIENTATION_V=1)
	0x0347	[7:0]	Y_ADD_STA[7:0]	
	0x034a	[3:0]	Y_ADD_END[11:8]	Vertical direction analog cropping end position within the active pixels area Unit : pixels Format : 16-bit unsigned integer * Note that this is the cropping start position when flipping (IMG_ORIENTATION_V=1)
	0x034b	[7:0]	Y_ADD_END[7:0]	
	0x0385	[3:0]	Y_EVN_INC[3:0]	No. of lines skipped from even number line to odd number line in Sub-sampling mode Format : 16-bit unsigned integer
	0x0387	[3:0]	Y_ODD_INC[3:0]	No. of lines skipped from odd number line to even number line in Sub-sampling mode Format : 16-bit unsigned integer
	0x0900	[0]	BINNING_MODE	Binning mode enable 0 : disable 1 : enable
	0x0901	[3:0]	BINNING_TYPE_V[3:0]	Binning type selection for Vertical 1 : no binning 2 : 2 or 3binning 4 : 4binning *Setup other than the above is forbidden.

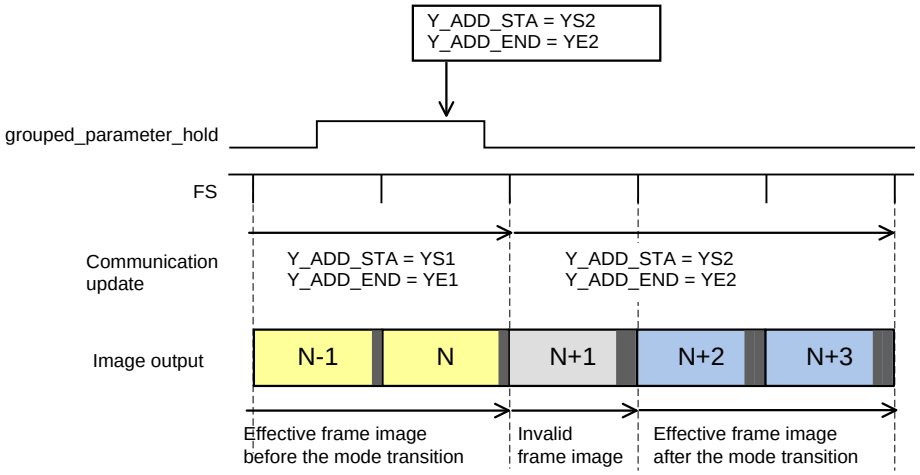

Figure 7-7 Corrupted-frame-related registers change sequence

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7.2.2. Mode transition sequence under consideration of corrupted frame

In this paragraph, four available mode transitions in this sensor are explained together with their use case. You can find conditions of using each mode transition method and causing an invalid frame on which details are already explained in previous sections.

Table 7-4 List of available mode transitions (possibility of occurrence of corrupt frames, and other precautions)

Mode transition			Availability of each transition mode	
Mode name		Features and notes/conditions for use	With changes of PLL/MIPI related settings (see Table 7-5)	Without change of PLL/MIPI related settings.
Via SW standby	SW-standby mode transition (default)	- Standard method for any kind of mode transition. - No corrupted frame.	Available	Available
	Fast SW-standby mode transition	- Versatile and fast transition method. - When MODE_SEL[0] falls, picture output stops and mode transition occurs.	Available	Available
On-the-fly	Normal mode transition (default)	- Usable only the case without clock change. - Occurrence of corrupted frame (masking available)	Not available	Available
	Fast mode transition	- Usable only the case without clock change but fast mode change. - When GRP_PARAM_HOLD falls, picture output stops and mode transition occurs.	Not available	Available.
	Loss frame less mode transition(Option)	- It is possible with loss frame less mode transition between HDR and Full Resolution(Option)	Not available	Available (only between HDR and Full Resolution)

Table 7-5 List of registers to be set only in SW-standby as mode transition.

	Address	Bit	Name	Description
I²C register	0x0105	[0]	MASK_CORR_FRM	This is register to mask corrupted frames. 0 : transmit corrupted frames 1 : mask corrupted frames
	0x0106	[0]	FAST_STANDBY_CTL	0 : after outputting all current frames, switch to software standby. Effective in Via SW-standby transition 1 : immediately after stopping outputting all current frames, switch to software standby
	0x0350	[0]	FRM_LENGTH_CTL	Frame length automatic tracking control as shutter time exceeding a current operation vertical period Select whether or not the frame length is changed automatically when FRM_LENGTH_LINES < COARSE_INTEG_TIME + α (α = type-specific adjustment parameter, and is 10(d) for this type) 0 : no automatic tracking control of frame length 1 : automatic tracking control of frame length In this case, "COARSE_INTEG_TIME + α" operates instead of FRM_LENGTH_LINES
	0x3003	[0]	SHORT_FRAME_RS	Fast mode transition. Effective in On-the-fly transition. 0: normal mode change 1: Fast mode change
	0x0114	[1:0]	CSI_LANE_MODE	Number of lanes for CSI 0 : 1-lane *not supported 1 : 2-lane 2 : 3-lane *not supported 3 : 4-lane
	0x0112	[7:0]	CSI_DT_FMT_H [7:0]	The output data format for CSI CSI_DT_FMT_H : Uncompressed Data Bit Width CSI_DT_FMT_L : compressed Data Bit Width 0x0808: RAW8 (Top 8 bits of pixel data) 0x0A0A: RAW10 Setup other than the above is forbidden.
	0x0113	[7:0]	CSI_DT_FMT_L [7:0]	
	0x0301	[4:0]	IVTPXCK_DIV	The Pixel Clock Divider for Internal Video Timing System Range : 4,5,7,8,10 Format : 16-bit unsigned integer *Setup other than the above is forbidden.
	0x0303	[2:0]	IVTSYCK_DIV	The System Clock Divider for Internal Video Timing System

			Range : 2, 4 Format : 16-bit unsigned integer *Setup other than the above is forbidden.
0x0305	[3:0]	PREPLLCK_VT_DIV	The pre-PLL Clock Divider for Internal Video Timing System Clock Range : 1 to 4 Step : 1 Format : 16-bit unsigned integer *Setup other than the above is forbidden..
0x0306	[2:0]	PLL_IVT_MPY[10:8]	The PLL multiplier for Internal Video Timing System Clock Range : 57 to 216 (Dual PLL) 51 to 216 (Single PLL) Step : 1 Format : 16-bit unsigned integer *Setup other than the above is forbidden
0x0307	[7:0]	PLL_IVT_MPY[7:0]	
0x0309	[4:0]	IOPPXCK_DIV	The Pixel Clock Divider for Internal Output Pixel System Range : 8, 10 (The setting value is decided by output bit width) Format : 16-bit unsigned integer *Setup other than the above is forbidden.
0x030b	[1:0]	IOPSYCK_DIV	The System Clock Divider for Internal Output Pixel System Range : 1, 2 Format : 16-bit unsigned integer *Setup other than the above is forbidden.
0x030d	[3:0]	PREPLLCK_OP_DIV	The pre-PLL Clock Divider for Internal Output Pixel System during "Dual PLL mode" (PLL_MULT_DRIV=1). Range : 1 to 4 Step : 1 Format : 16-bit unsigned integer *Setup other than the above is forbidden.
0x030e	[2:0]	PLL_IOP_MPY[10:8]	The PLL multiplier for Internal Output Pixel System "Dual PLL mode" (PLL_MULT_DRIV=1). Range : 51 to 216 Step : 1 Format : 16-bit unsigned integer *Setup other than the above is forbidden.
0x030f	[7:0]	PLL_IOP_MPY[7:0]	
0x0310	[0]	PLL_MULT_DRIV	PLL mode select 0 : Single PLL mode 1 : Dual PLL mode

	0x0820	[7:0]	REQ_LINK_BIT_RATE_MBPS[31:24]	Output Data Rate [Mbps] Bit[32:16] integer Bit[15:0] decimal
	0x0821	[7:0]	REQ_LINK_BIT_RATE_MBPS[23:16]	
	0x0822	[7:0]	REQ_LINK_BIT_RATE_MBPS[15:8]	
	0x0823	[7:0]	REQ_LINK_BIT_RATE_MBPS[7:0]	

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7.2.3. SW-standby mode transition

A diagram below illustrates mode transition sequence when clock setting change is required (see Table 7-5). Let the sensor go into SW-standby mode by setting MODE_SEL = 0 before mode change. After setting parameters for the next streaming, set MODE_SEL=1. This mode transition method can also be used for cases which do not require clock change. This mode does not cause any invalid frame both before and after the transition.

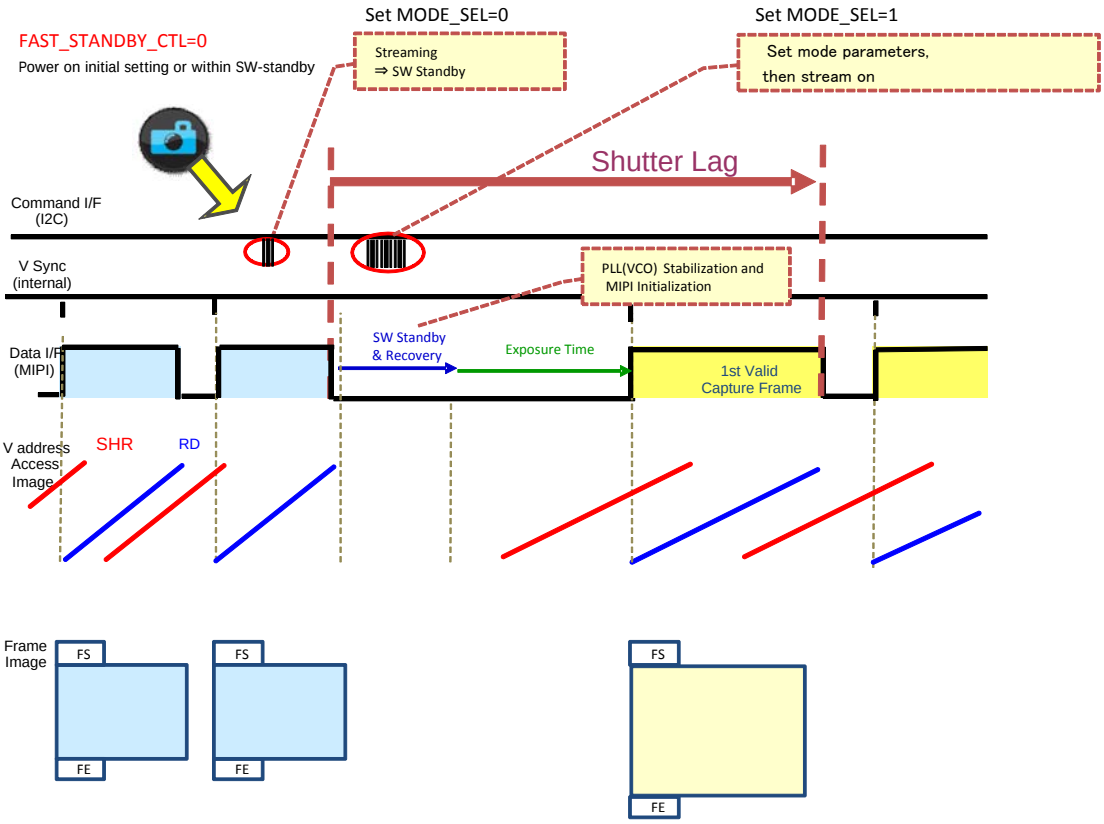

Figure 7-8 SW-standby mode transition (available for with/without clock change)

Table 7-6 SW-standby related register

	Address	Bit	Name	Description
I²C register	0x0100	[4:0]	MODE_SEL[4:0]	Mode Select 0 : Software Standby 1 : Streaming *Setup other than the above is forbidden.

7.2.4. Fast SW-standby mode transition

A diagram below illustrates mode transition sequence when clock setting change is required. This method of mode transition is shortest shutter lag and is versatile. This mode also go into the SW-standby (MODE_SEL=0) mode once for setting mode parameters for next streaming, then get out by MODE_SEL=1. However differently from the SW-standby mode transition, the last frame before mode transition is stopped during streaming (corrupted frame) by setting MODE_SEL=1 under the condition FAST_STANDBY_CTL = 1 is set once before the mode transition, e.g. in power on sequence or during SW-standby. This mode transition method can be also used for the mode transition without clock change.

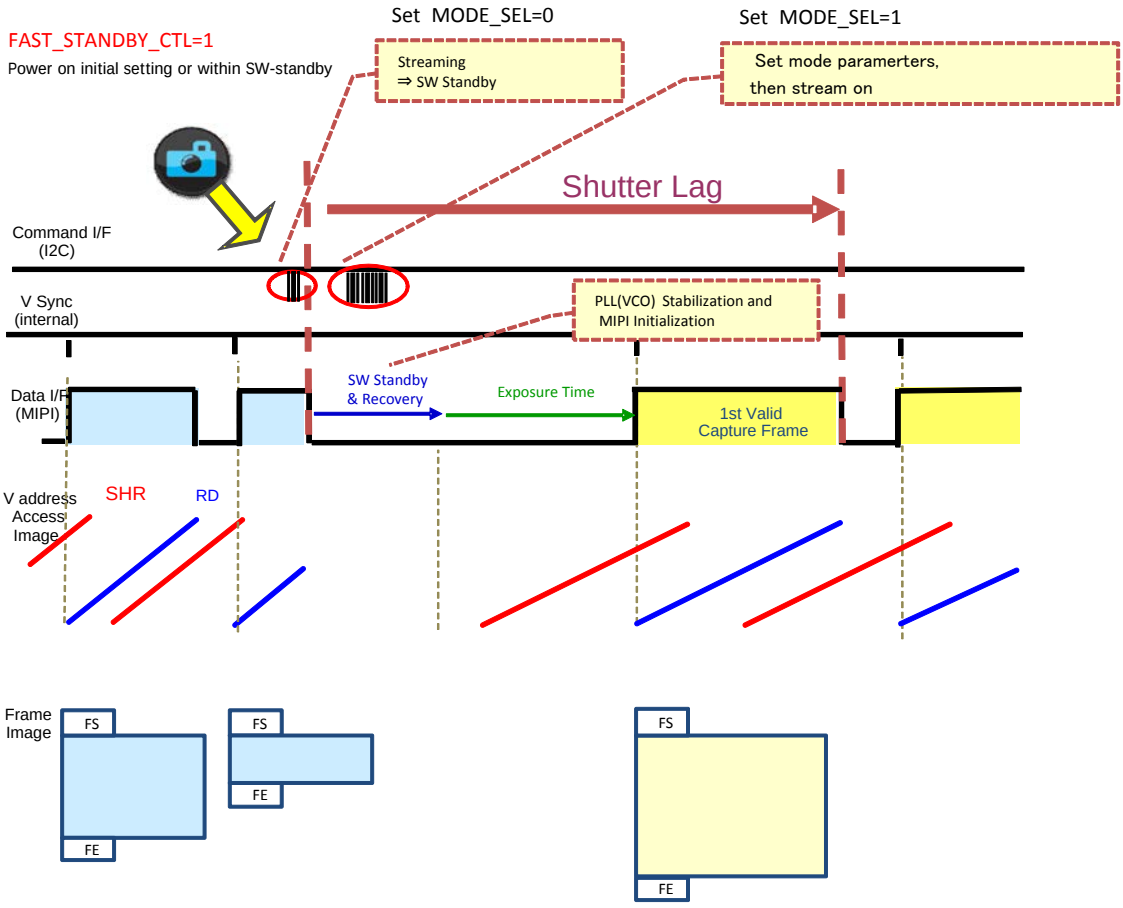

Figure 7-9 Fast SW-standby mode transition

Table 7-7 Fast SW-standby related registers

	Address	Bit	Name	Description
I²C register	0x0100	[4:0]	MODE_SEL[4:0]	Mode Select 0 : Software Standby 1 : Streaming *Setup other than the above is forbidden.
	0x0106	[0]	FAST_STANDBY_CTL	0 : after outputting all current frames, switch to software standby 1 : immediately after stopping outputting all current frames, switch to software standby

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7.2.5. Normal mode transition

A diagram below illustrates mode transition sequence when clock setting remain the same.

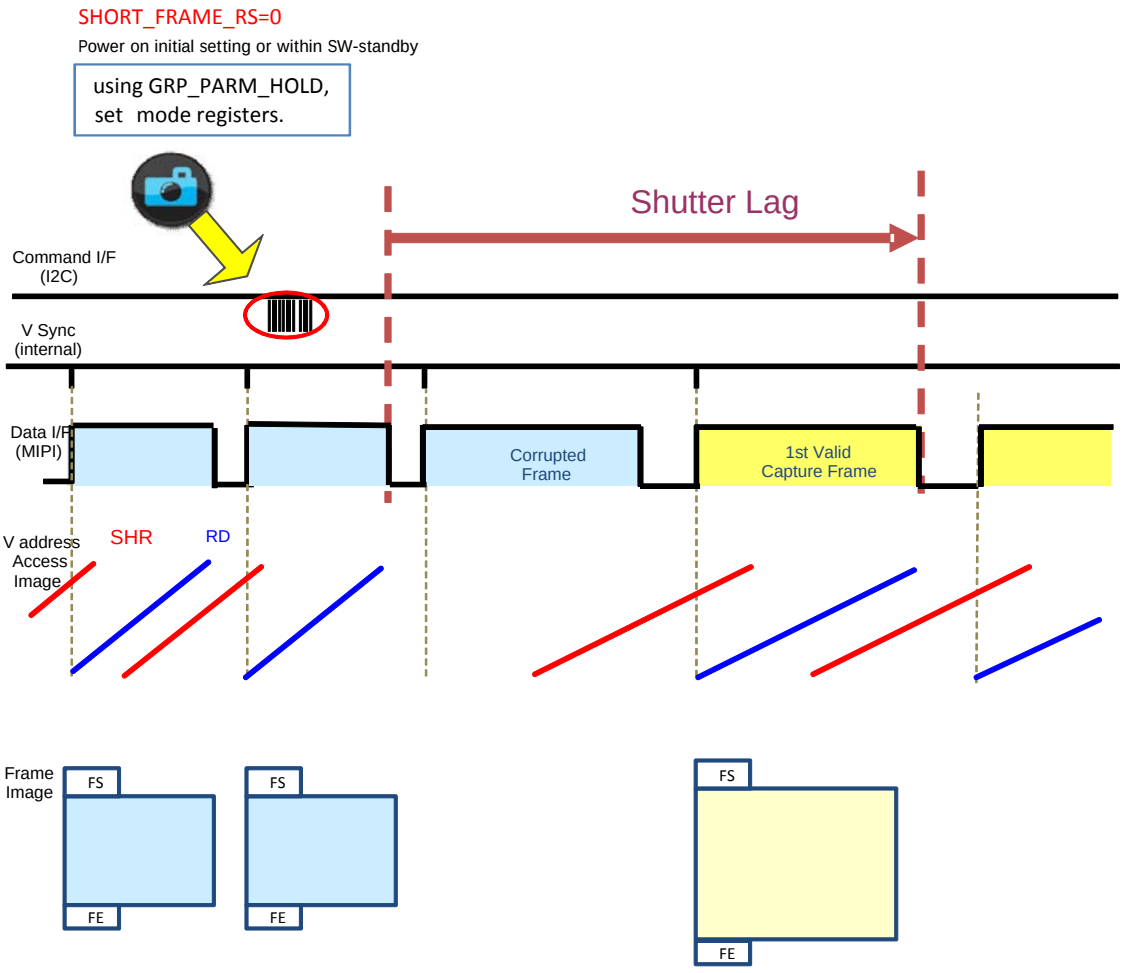

Figure 7-10 Normal mode transition (without clock change)

The corrupted frame can be masked not to be output by setting MASK_CORR_FRM = 1.

Table 7-8 Normal mode transition related register

	Address	Bit	Name	Description
I²C register	0x0105	[0]	MASK_CORR_FRM	This is register to mask corrupted frames. 0 : transmit corrupted frames 1 : mask corrupted frames

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7.2.6. Fast mode transition

A diagram below illustrates mode transition sequence for the sensor when clock setting remain the same (when corrupted frame related registers (see Table 7-3) and CIT target register are changed at the same time).

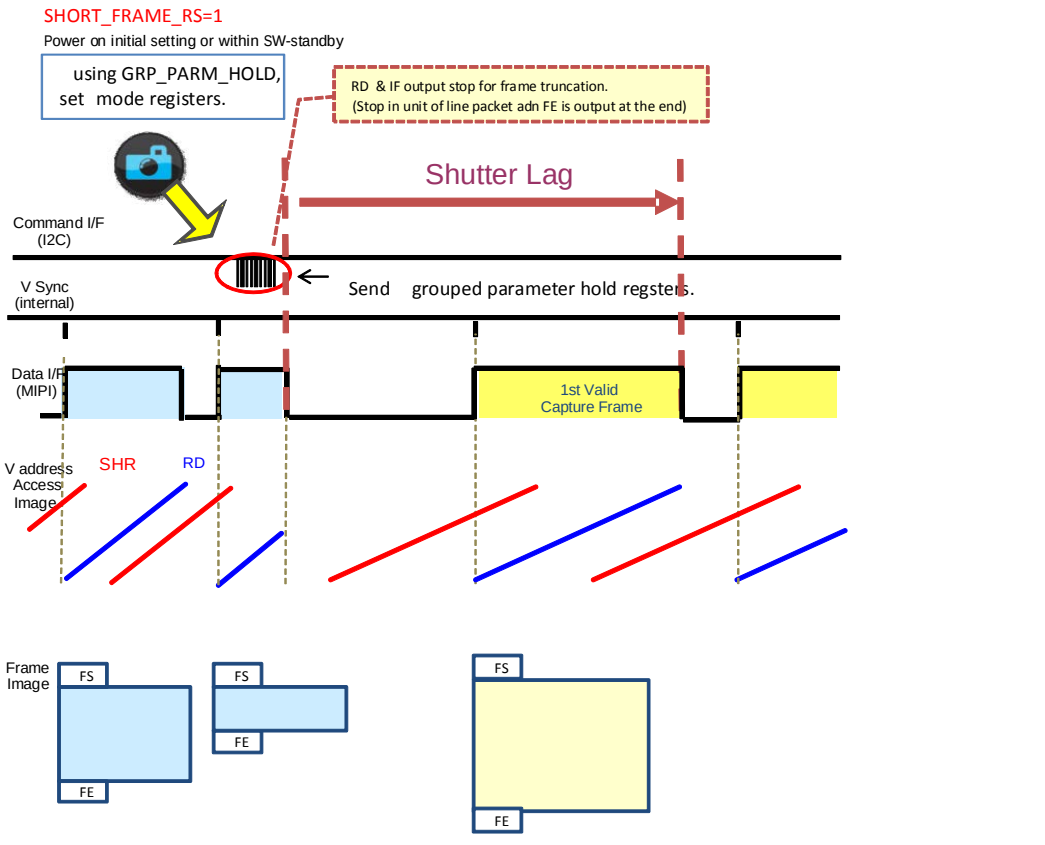

Figure 7-11 Fast mode transition

Table 7-9 Fast mode transition related register

	Address	Bit	Name	Description
I²C register	0x3003	[0]	SHORT_FRAME_RS	Fast mode transition 0: normal mode change 1: Fast mode change
	0x0104	[0]	GRP_PARAM_HOLD	This register is a hold register for updating multiple parameters in the same frame. 0 : consume as normal 1 : hold

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7.2.7. Loss frame less transition between HDR and Full Resolution

A diagram below loss frame less mode transition between HDR and Full Resolution sequence when clock setting remain the same. The Full Resolution when doing this mode transition is different from usual setting.

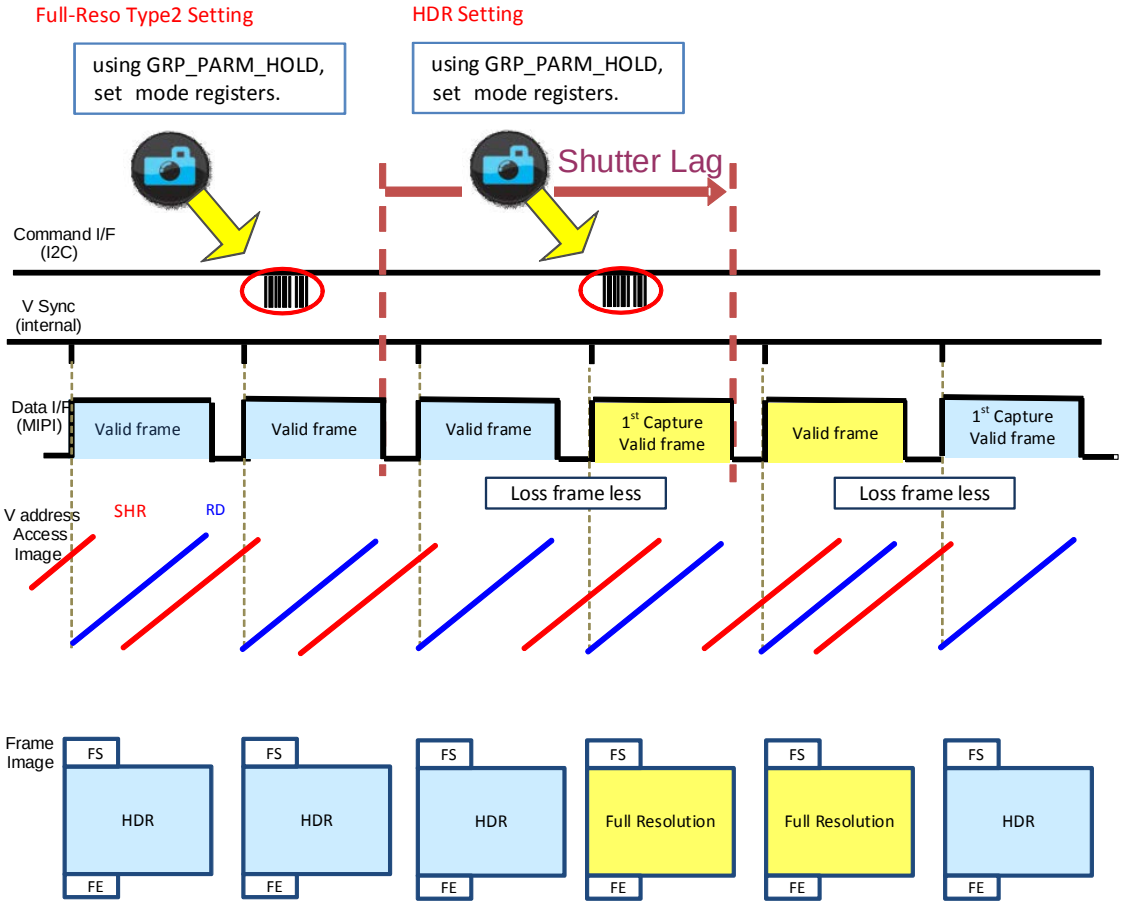

Figure 7-12 Loss frame less transition

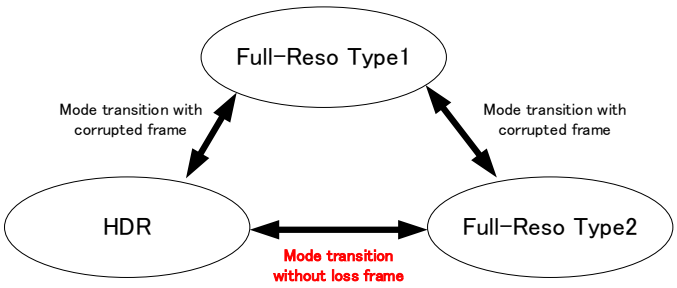

Figure 7-13 Full-Resolution and HDR transition

Table 7-10 Loss frame less mode transition related register

	Address	Bit	Name	Description
I²C register	0x0220	[5:0]	HDR_MODE[5:0]	Setting value: 0x01 or 0x03 or 0x23 Bit[0] HDR mode enable 0 : HDR disable 1 : HDR enable Bit[1] Gain mode select during HDR 0 : combined gain used 1 : separate gain used Bit[4:2] Reserved Bit[5] exposure mode select during HDR 0 : short exposure determined by ratio (controlled by EXPO_RATIO(0x0222)) 1 : short exposure controlled by direct control
	0x0222	[4:0]	EXPO_RATIO	Exposure_ratio [4:0] Defines exposure ratio between short and long exposure. Short exposure value = coarse_integration_time / Exposure_ratio 1,2,4,8,16(unsigned integer) can be set.

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7.3. Exposure and gain change sequence and AE bracketing

This section describes about the timing to update changes in integration time related registers, and changes in gain system registers. In addition, it describes the method to update registers at every vertical period using AE bracketing feature.

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7.3.1. Integration time change sequence

Basically, GPH must be used in changing exposure time or shutter time. Set the value “1” to GRP_PARAM_HOLD register and set the integration duration value to COARSE_INTEG_TIME (CIT) register. Then set GRP_PARAM_HOLD back to “0”. The integration time is changed from the next frame and the image shot with the new integration time is output from the second frame after resetting GRP_PARAM_HOLD register.

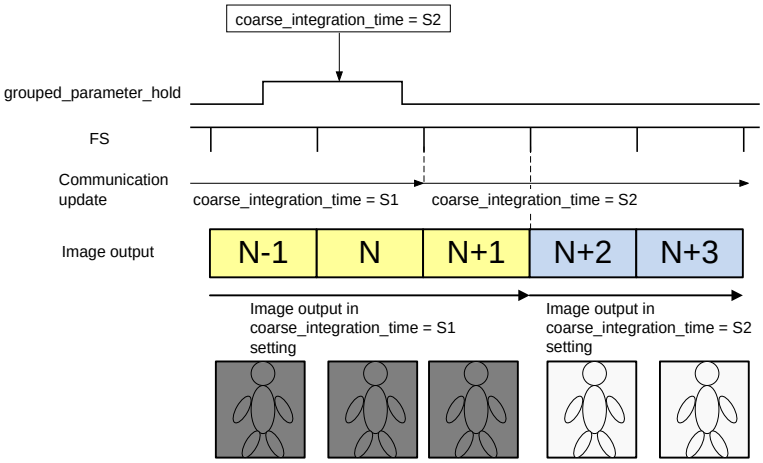

Figure 7-14 Integration time change sequence

Table 7-11 Integration time setting register

	Address	Bit	Name	Description
I²C register	0x0202	[7:0]	COARSE_INTEG_TIME[15:8]	Coarse storage time Unit : lines Format : 16-bit unsigned integer
	0x0203	[7:0]	COARSE_INTEG_TIME[7:0]	
	0x0104	[0]	GRP_PARAM_HOLD	This register is a hold register for updating multiple parameters in the same frame. 0 : consume as normal 1 : hold

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7.3.2. Gain change sequence

With this sensor, register settings for Gain are updated 2 frames after those set with GPH. In the case of IMX214, this update timing is different because it depends on the settings of summing, however there are always 2 frames delays for the update timing with this sensor. Gain change sequence also requires a usage of GPH together with integration time settings.

Basic gain change sequence

Set the values to ANA_GAIN_GLOBAL / DIG_GAIN_GR/DIG_GAIN_R / DIG_GAIN_B/DIG_GAIN_GR/ DIG_GAIN_B/DIG_GAIN_GB registers. Then set GRP_PARAM_HOLD back to “0”. The gain values are changed from the 2nd next frame and the image shot with the new gains is output from the 2nd frame after resetting “GRP_PARAM_HOLD” register. Hence, if the new gain and integration time is changed within the same GPH slot, a capture with both setting in synchronous is output.

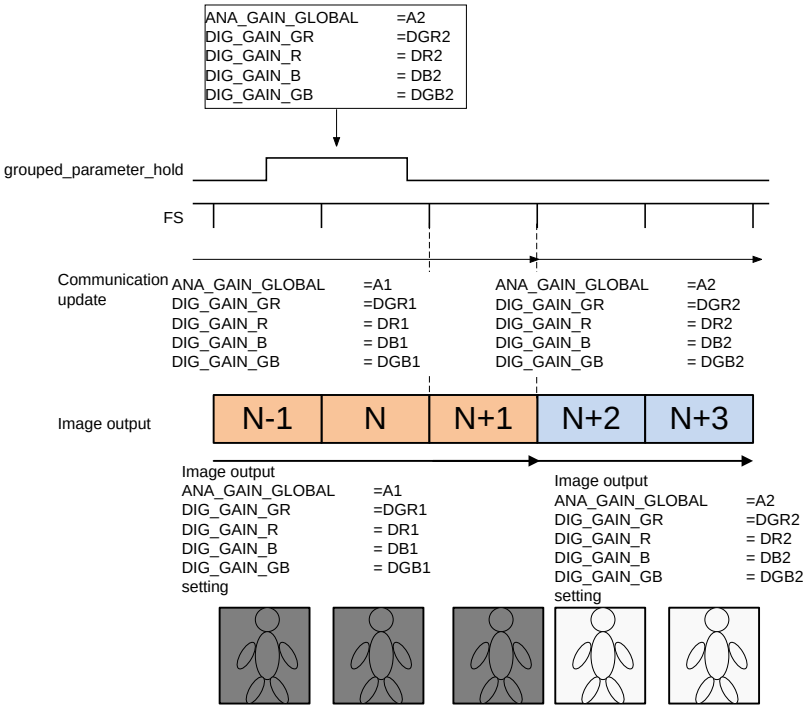

Figure 7-15 Gain change sequence

Table 7-12 Gain setting register

	Address	Bit	Name	Description
I²C register	0x0204	[0]	ANA_GAIN_GLOBAL[8]	Analog gain control code for ALL color Format : 16-bit unsigned integer Range : 0 to 480 *Setup other than the above is forbidden. Gain = ANA_GAIN_C0 / (ANA_GAIN_C1 - ANA_GAIN_GLOBAL)
	0x0205	[7:0]	ANA_GAIN_GLOBAL[7:0]	
	0x020e	[7:0]	DIG_GAIN_GR[15:8]	Digital gain control code for GR Format : 16-bit unsigned iReal
	0x020f	[7:0]	DIG_GAIN_GR[7:0]	
	0x0210	[7:0]	DIG_GAIN_R[15:8]	Digital gain control code for R Format : 16-bit unsigned iReal
	0x0211	[7:0]	DIG_GAIN_R[7:0]	
	0x0212	[7:0]	DIG_GAIN_B[15:8]	Digital gain control code for B Format : 16-bit unsigned iReal
	0x0213	[7:0]	DIG_GAIN_B[7:0]	
	0x0214	[7:0]	DIG_GAIN_GB[15:8]	Digital gain control code for GB Format : 16-bit unsigned iReal
	0x0215	[7:0]	DIG_GAIN_GB[7:0]	
	0x0104	[0]	GRP_PARAM_HOLD	This register is a hold register for updating multiple parameters in the same frame. 0 : consume as normal 1 : hold

With this sensor, Changing gain and CIT can be updated in every frame from HOST by using GPH.

Note that the Gain update timing differs to the IMX214. It is recommended that GPH is used for this setting.

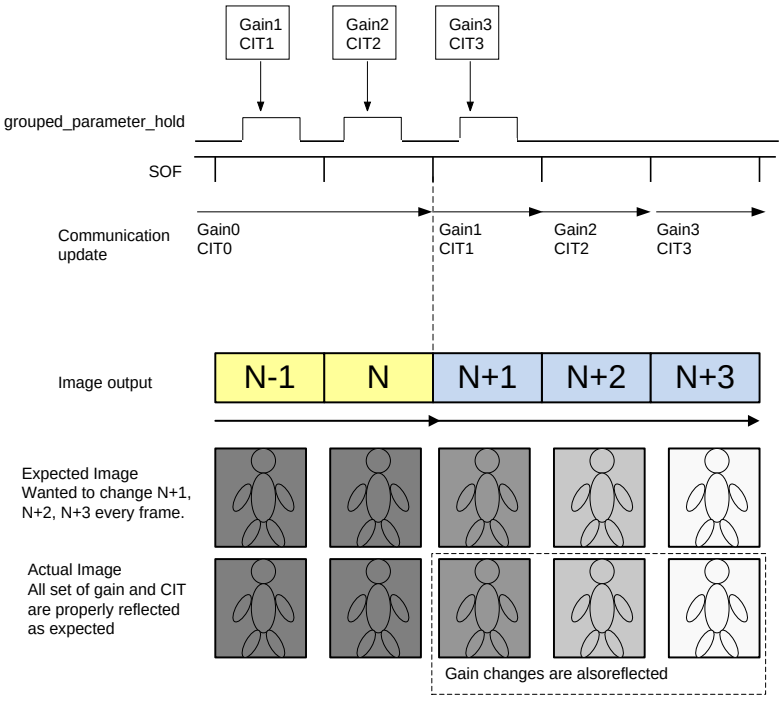

Figure 7-16 Gain change sequence (With CIT change)

Constraints:

1) Register change shall be only CIT, analog gain and digital gain.
2) Host should complete settings by I2C within 1 frame (see "communication period" shown in Figure 2-15).

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7.3.3. AE bracketing

This function could be used to output the picture for up to five frames continuously, without transmitting coarse integration time, analog/digital gain, and flash settings every frame and setting by setting LUT in advance. This sensor is designed to repeat pre assigned LUT for multiple times.

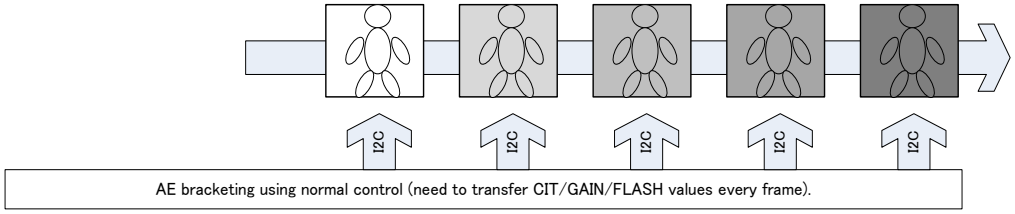

Figure 7-17 AE bracketing - without use of LUT

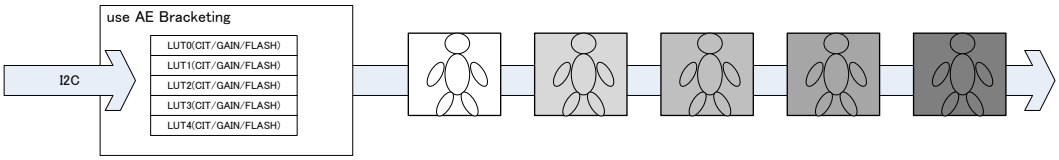

Figure 7-18 AE bracketing - with use of LUT

Table 7-13 AE bracketing related registers

	Address	Bit	Name	Description
I²C register	0x0e00	[7:0]	BRACKETING_LUT_CTL	Bracketing Look Up Table control 0 : disabled 1 to n : bracketing over n frame. (n = type-specific parameter, and is 5(d) for this type)
	0x0e01	[7:0]	BRACKETING_LUT_MODE	Bit[0] Bracketing sequence control 0 : return to SW standby after bracketing 1 : continue in streaming after bracketing Bit[1] Loop control 0 : single bracketing 1 : loop mode Bit[2] Output mask control 0 : no output mask 1 : output mask Bit[7:3] Reserved

	0x0104	[0]	GRP_PARAM_HOLD	This register is a hold register for updating multiple parameters in the same frame. 0 : consume as normal 1 : hold
	0x0e10	[7:0]	COARSE_INTEG_TIME_00[15:8]	Coarse integration time for bracketing_LUT_frame_A
	0x0e11	[7:0]	COARSE_INTEG_TIME_00[7:0]	
	0x0e12	[0]	ANA_GAIN_GLOBAL_10[8]	Global analogue gain code for bracketing_LUT_frame_A
	0x0e13	[7:0]	ANA_GAIN_GLOBAL_10[7:0]	
	0x0e14	[7:0]	DIG_GAIN_GR_20[15:8]	Green (red row) channel digital gain value for bracketing_LUT_frame_A
	0x0e15	[7:0]	DIG_GAIN_GR_20[7:0]	
	0x0e16	[7:0]	DIG_GAIN_R_20[15:8]	Red channel digital gain value for bracketing_LUT_frame_A
	0x0e17	[7:0]	DIG_GAIN_R_20[7:0]	
	0x0e18	[7:0]	DIG_GAIN_B_20[15:8]	Blue channel digital gain for bracketing_LUT_frame_A
	0x0e19	[7:0]	DIG_GAIN_B_20[7:0]	
	0x0e1a	[7:0]	DIG_GAIN_GB_20[15:8]	Green (blue row) channel digital gain value for bracketing_LUT_frame_A
	0x0e1b	[7:0]	DIG_GAIN_GB_20[7:0]	
	0x0e1d	[4]	FLASH_TRIG_RS_30	Bit[3:0] Reserved Bit[4] Flash strobe trigger for bracketing_LUT_frame_A 0 : disable 1 : flash strobe is retimed to this frame Bit[7:5] Reserved
	:	:	:	:
	0x0e48	[7:0]	COARSE_INTEG_TIME_04[15:8]	Coarse integration time for bracketing_LUT_frame_E
	0x0e49	[7:0]	COARSE_INTEG_TIME_04[7:0]	
	:	:	:	:
	0x0e55	[4]	FLASH_TRIG_RS_34	Bit[3:0] Reserved Bit[4] Flash strobe trigger for bracketing_LUT_frame_E 0 : disable 1 : flash strobe is retimed to this frame Bit[7:5] Reserved

See this sensor Register Map for complete set of registers for five look-up tables.

How to control AE bracketing features

AE bracketing sequence always starts during SW-standby, but there are two possible ways to exit; 1) back to SW-standby and 2) move to streaming mode. Additionally, single mode bracketing and loop mode bracketing is available. AE bracketing function continues to repeat until setting BRACKETING_LUT_CTL = 0, See below for details.

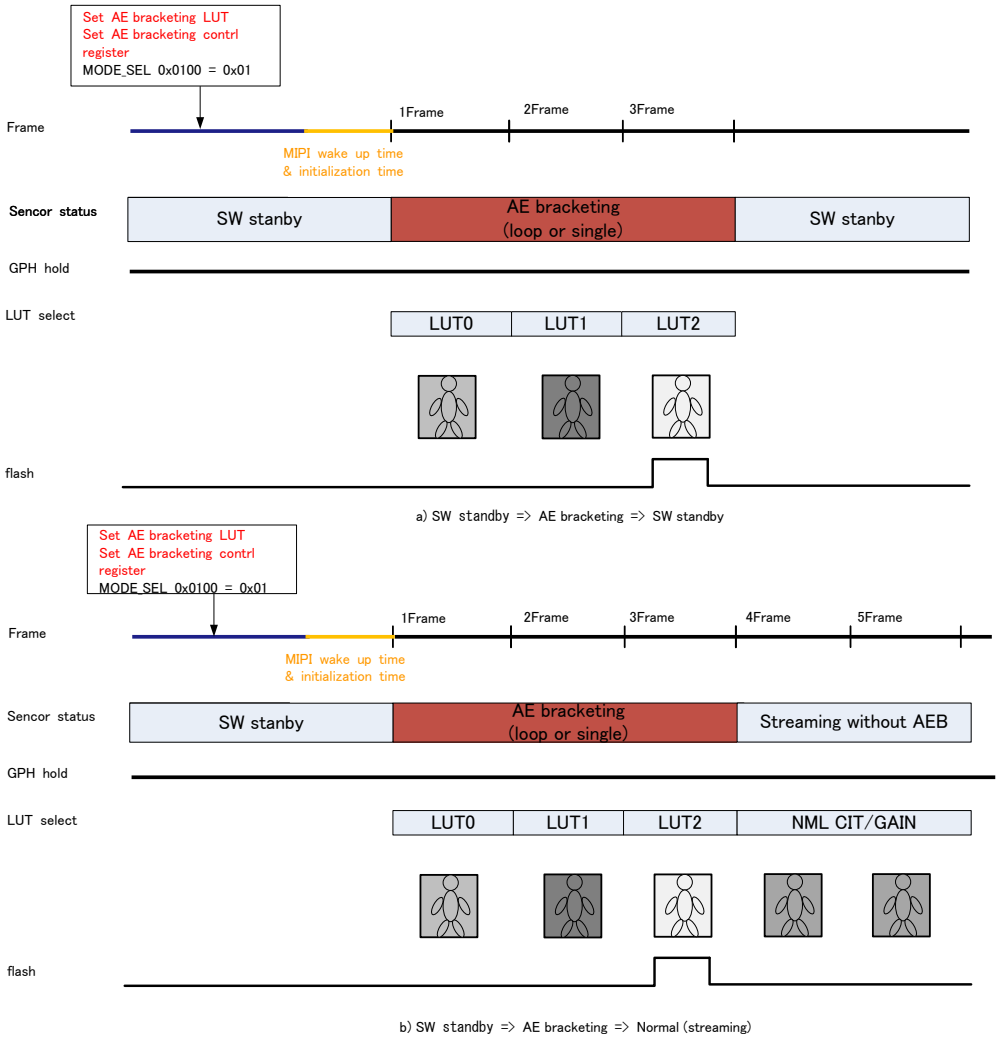

Figure 7-19 AE bracketing sequence timing chart (example of single mode)

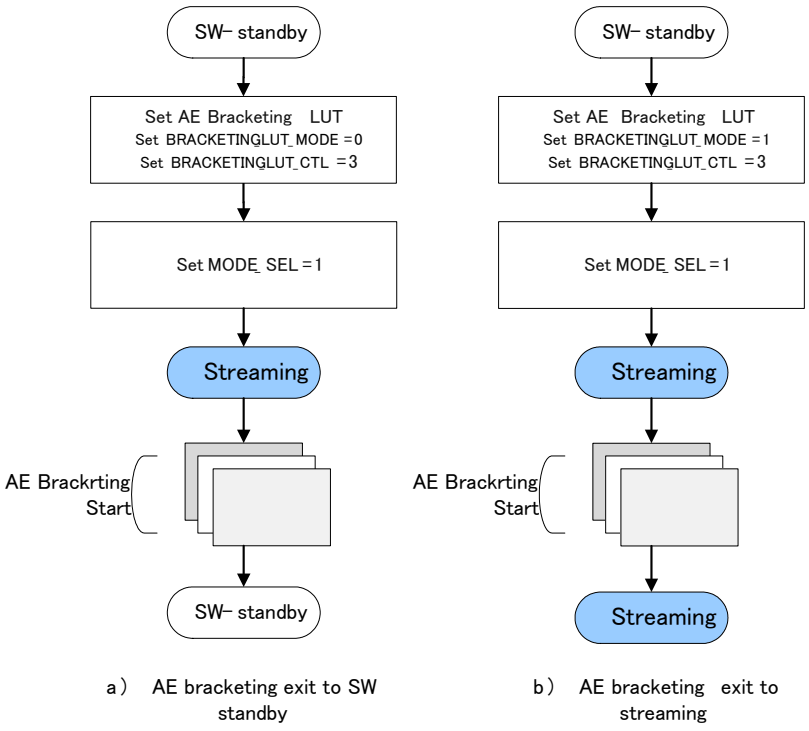

Figure 7-20 Auto bracketing sequence flow chart

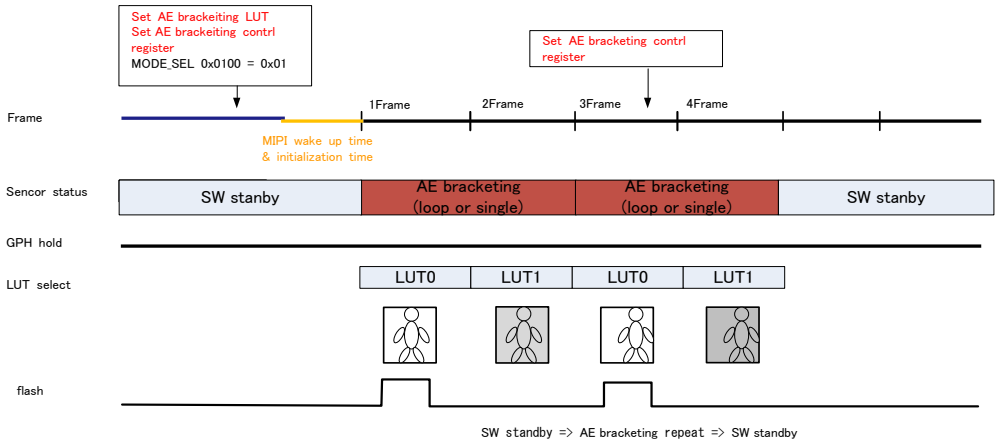

Figure 7-21 AE bracketing sequence (example of 2-repeat mode)

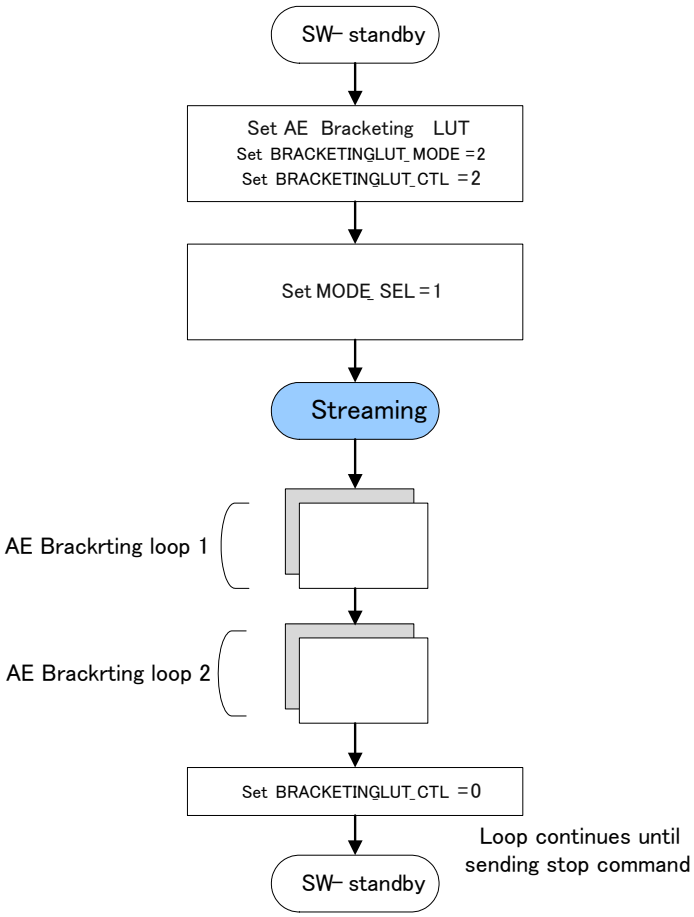

Figure 7-22 AE bracketing sequence (example of 2-repeat mode)

Above example show the limited combination of possible function for AE bracketing. Other combinations of repeat or single mode and either of exit modes are possible with those registers introduced in this paragraph.

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8. Settings related to HDR capture mode picture quality

This sensor built-in HDR function consists of the blocks shown in the following block diagram. In sensor, most of control functions are handled by built-in firmware. In this chapter, user accessible control registers of each block are explained.

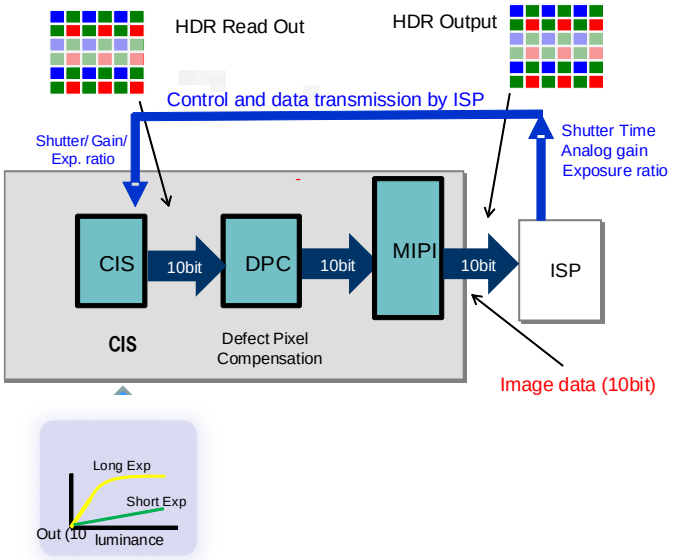

Figure 8-1 HDR mode data flow

HDR system of the sensor requires following signal input from the sensor and feedback from ISP:

- Input from the sensor: Image data (HDR Raw).
- Output to the sensor: Settings of shutter time, analog gain, exposure ratio.

See details in the following sections.

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8.1. Integration time and gain setting

In HDR Full-resolution mode, you can set different integration time* and gain settings for long exposure pixels and short exposure pixels.

Gain setting and integration time setting for the long integration pixels should follow those for Normal capture mode settings. Refer to the “5.4 Electronic shutter and integration time setting” for the integration time setting. In HDR capture mode, the digital gain setting shall be set to 0dB (In HDR capture mode, only the analog gain is usable). For gain setting, refer to “5.5 Gain setting”.

You can select either one of the following to set the integration time for short integration.

- Automatically calculate from the long integration time – Auto mode
- Set directly using a register – Direct mode

To set gain for short integration, you can set arbitrary values despite that of long integration pixels in full pixel mode.

Table 8-1 Integration time control and analogue gain control for HDR capture mode

	Address	Bit	Name	Description
I2C register	0x0220	[5:0]	HDR_MODE	[0]: 0 HDR disable1 HDR enable [1]: 0 combined gain used (during HDR) 1 separate gain used (during HDR) [2]: Not used [3]: Not used [4]: Not used [5]: 0 short exposure determined by ratio (during HDR) 1 short exposure controlled by direct control (during HDR)
	0x0221	[7:4]	HDR_RESO_REDU_H	HDR_RESO_REDU_H: Horizontal scaling factor during HDR HDR_RESO_REDU_V: Vertical scaling factor during HDR 0x11=Through (for Full-resolution) Other values are prohibited.
	0x0221	[3:0]	HDR_RESO_REDU_V	
	0x0222	[4:0]	EXPO_RATIO	Ratio settings for calculating the ratio of short integration exposure time when in HDR mode Range : 1, 2, 4, 8, 16 *Setup other than the above is forbidden. *When HDR_MODE[5]=0, it is valid. Short exposure time = COARSE_INTEG_TIME / EXPO_RATIO
	0x0224	[7:0]	ST_COARSE_INTEG_TIME[15:8]	Settings for the exposure time when directly setting the short integration exposure time when in HDR mode Unit : lines Format : unsigned integer *When HDR_MODE[5]=1, it is valid.
	0x0225	[7:0]	ST_COARSE_INTEG_TIME[7:0]	
	0x0204	[0]	ANA_GAIN_GLOBAL[8]	Analog gain setting value Range: 0 to 480 Same format as in ANA_GAIN_GLOBAL See "Method to set short integration gain" section for details of setting.
	0x0205	[7:0]	ANA_GAIN_GLOBAL[7:0]	
	0x0216	[0]	ST_ANA_GAIN_GLOBAL[8]	
	0x0217	[7:0]	ST_ANA_GAIN_GLOBAL[7:0]	

Method to set integration time for short integration

When set as HDR_MODE [5] = 0, the exposure time for the short exposure setting is calculated from the setting value of the long exposure. – Auto mode

Short Exposure integration time = COARSE_INTEG_TIME [15:0] / EXPO_RATIO [4:0]

In this case, COARSE_INTEG_TIME[15:0] has to be set up in multiple of EXPO_RATIO setting.

When set as HDR_MODE [5] = 1, any value can be set directly to the short exposure setting. –Direct mode

Short Exposure integration time = ST_COARSE_INTEG_TIME [15:0]

Note) In ”Direct mode”, EXPO_RATIO setting is ignored.

Method to set short integration gain

When set as HDR_MODE [1] = 1, the register value for short exposure pixels give the gain for short exposure pixels.

Short Exposure Gain = ST_ANA_GAIN_GLOBAL [8:0]

Table 8-2 Analogue gain control

Long exposure	Short exposure
ANA_GAIN_GLOBAL [8:0]	ST_ANA_GAIN_GLOBAL[8:0]

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9. Miscellaneous Function

9.1. Thermal meter

This function reads the thermal data from an internal sensor and averages it, it can be read as I2C or EBD data (See A-1)

Thermal meter function only works under the condition with calibration data. The calibration data is optimized by individual sensor and is measured / stored in factory area of OTP.

Also, due to moving average principle, the temperature data is only valid after completion of 8 frame moving average every time after mode transition and power on sequence.

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9.1.1. Thermal meter related registers

The following table shows thermal meter related control registers.

Table 9-1 Thermal meter register setting

Name	Address	Bit	Description
TEMP_SEN_CTL	0x0138	[0]	Temperature control enable 0 : disable 1 : enable
TEMP_SEN_OUT	0x013a	[7:0]	Temperature data output 0x81 to 0xec : -20 [degrees C] 0xed : -19 [degrees C] ~ 0x00 : 0 [degrees C] ~ 0x4f : 79 [degrees C] 0x50 to 0x7f : 80 [degrees C]

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9.1.2. Thermal meter operation sequence

Thermal meter works both during Standby and streaming. While the thermal meter is ON, transition from Standby to Streaming or Streaming to Standby is possible.

Temperature measurement during SW-standby

The sequence for operating the thermal gauge while in Standby is shown as follows.

Valid thermal data is output from the 2nd frame.

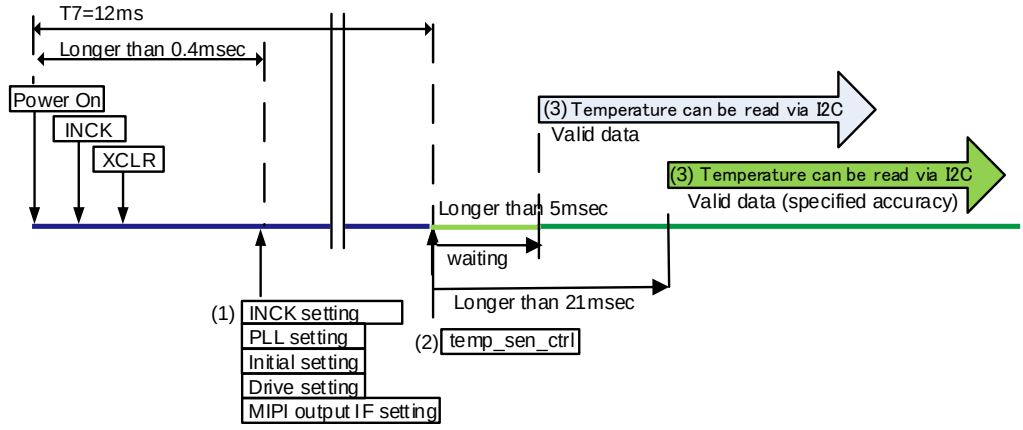

Figure 9-1 Thermal meter working in standby

Table 9-2 Thermal meter working in standby

(1)	Set the INCK frequency (0x0136,0x0137)
(2)	Set the TEMP_SEN_CTL (0x0138)
(3)	Read TEMP_SEN_OUT to get the temperature (0x013a)

Temperature measurement in streaming mode (1)

The following diagram and table shows about a thermal meter operation sequence working in streaming with TEMP_SEN_CTL being set before MODE_SEL=1 (streaming-1)

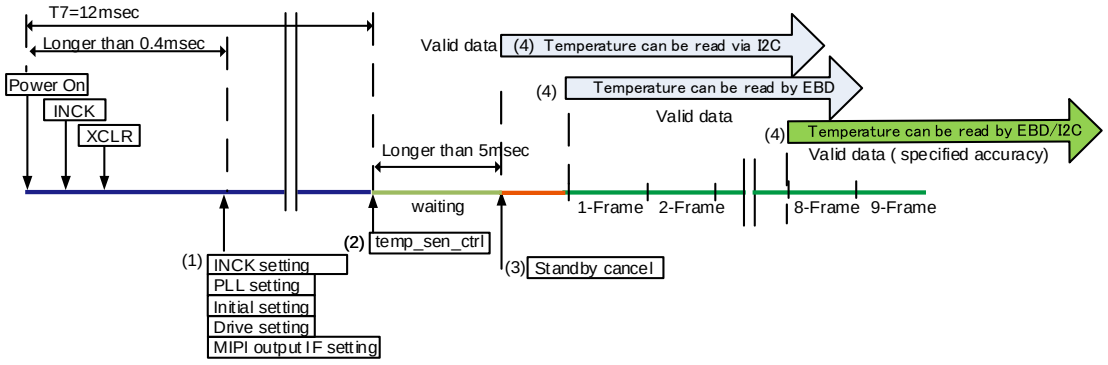

Figure 9-2 Thermal meter working in streaming (1)

Table 9-3 Thermal meter working in streaming (1)

(1)	Set the INCK frequency (0x0136,0x0137)
(2)	Set the TEMP_SEN_CTL (0x0138)
(3)	Set the MODE_SEL (0x0100)
(4)	Read TEMP_SEN_OUT to get the temperature (0x013a)

Temperature measurement in streaming mode (2)

The following diagram and table shows about a thermal meter operation sequence working in streaming with TEMP_SEN_CTL being set after MODE_SEL=1. (streaming-2)

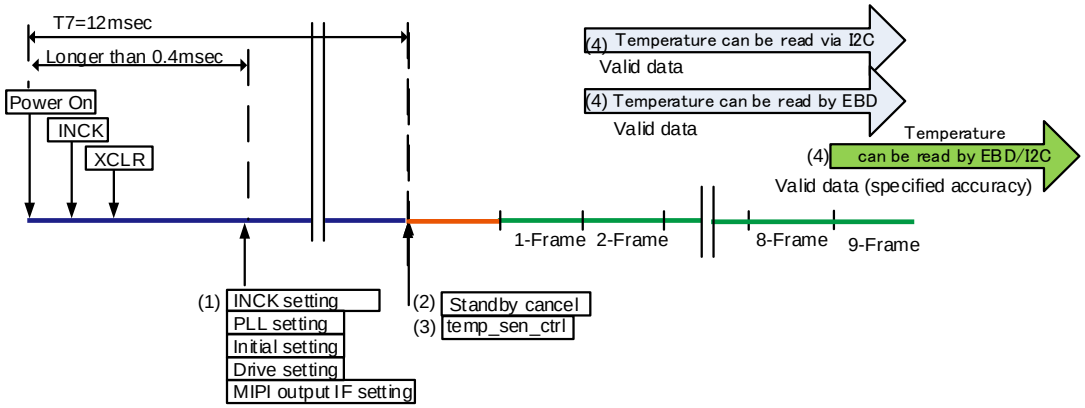

Figure 9-3 Thermal meter working in streaming (2)

Table 9-4 Thermal meter working in streaming (2)

(1)	Set the INCK frequency (0x0136,0x0137)
(2)	Set the MODE_SEL (0x0100)
(3)	Set the TEMP_SEN_CTL (0x0138)
(4)	Read TEMP_SEN_OUT to get the temperature (0x013a)

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9.1.3. Accuracy of temperature measurements

This sensor internally performs 8 frames moving average to output higher accuracy temperature. When it operates in thermal mode during Standby and when it measures temperature during Streaming more than 8 frames after TEMP_SEN_CTL =1, 8 frames averaged temperature data can be obtained after 9 frames.

*** Sensor output is guaranteed for -20-80deg ±5deg.**

This specification may be changed without prior notice. And in that case, we will announce the change to customers each time.

*** Thermal mode offers extremely low power consumption.**

*** Sensor shipped with no calibration data in OTP does not operate normally.**

*** If calibration data is not written in OTP, TEMP_SEN_OUT is 0x6c (or other fixed values) regardless of temperature.**

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9.2. Test pattern output (types of test patterns)

This sensor can output test patterns by using a built-in pattern generator.

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9.2.1. Types of test patterns

This sensor has a function to output fixed video signals from a built-in test pattern generator by setting related registers.

While related register must be set to output a test pattern, there is no restriction on the sequence for setting the registers. The required test pattern can be output by setting the related registers during image capturing.

Table 9-5 Test pattern related registers and description

	Address	Bit	Name	Description
I²C register	0x0600	[0]	TP_MODE [8]	Test Pattern selection 0 : No pattern 1 : Solid color 2 : 100% color bars 3 : Fade to grey color bars 4 : PN9 *Setup other than the above is forbidden.
	0x0601	[7:0]	TP_MODE [7:0]	
	0x0602	[1:0]	TD_R [9:8]	Test data for replacing R pixels when using test patterns
	0x0603	[7:0]	TD_R [7:0]	
	0x0604	[1:0]	TD_GR [9:8]	Test data for replacing GR pixels when using test patterns
	0x0605	[7:0]	TD_GR[7:0]	
	0x0606	[1:0]	TD_B [9:8]	Test data for replacing B pixels when using test patterns
	0x0607	[7:0]	TD_B[7:0]	
	0x0608	[1:0]	TD_GB [9:8]	Test data for replacing GB pixels when using test patterns
	0x0609	[7:0]	TD_GB[7:0]	

Black level is automatically set as 0.

Registers other than those listed above are setup as the hardware initial value.

9.3. Long exposure

Long exposure mode is a function to extend exposure up to approx. 128 times of longer than FRM_LENGTH_LINES (0x0340, 0x0341) which is allowed in normal setting. This function enables long exposure by extending only V-bank without changing the operating any other setting such as FRM_LENGTH_LINE and the setting of LINE_LENGTH_PCK(0x0342,0x0343), while offering low power consumption.

Table 9-6 Long exposure mode related registers

	Address	Name	Bit	Description
I2C register	0x3002	CIT_LSHIFT	[2:0]	Long exposure mode setting. 0 : Long exposure mode OFF Exposure time = COARSE_INTEG_TIME Other : Long exposure mode ON Exposure time = COARSE_INTEG_TIME << LSHIFT Ex. 1=2times 2=4times 3=8times | 7=128times (max setting)
	0x0202 0x0203	COARSE_INTEG_TIME	[15:0]	Coarse storage time Unit : lines Format : 16-bit unsigned integer
	0x0340 0x0341	FRM_LENGTH_LINES	[15:0]	The length of frame Unit : lines Format : 16-bit unsigned integer
	0x0342 0x0343	LINE_LENGTH_PCK	[15:0]	The length of line Unit : pixels Format : 16-bit unsigned integer * Set to 5352d. Any other value change require, please confirm with SONY.

Long exposure mode setting

Table 9-7 Set for long exposure

(1)	Set CIT_LSHIFT as you want
	Set COARSE_INTEG_TIME as you want
	Set FRM_LENGTH_LINES as you want
	Set LINE_LENGTH_PCK as you want

The frame rate during long exposure mode is as follows:

Frame Rate [frame/s] = *Pixel_rate* [pixels/s] / (*Total number of pixels* [pixels/frame] x2^{CIT_LSHIFT})

Pixel rate [pixels/s] = *VTPXCK* [MHz] * 4 (*Total number of VTPX channel)*

Total number of pixels [pixels/frame]

= FRM_LENGTH_LINES [lines/frame] * LINE_LENGTH_PCK [pixels/line]

The setting range of exposure time during long exposure mode is as follows:

1 ≦ COARSE_INTEG_TIME ≦ FRM_LENGTH_LINES -10

Setting example

Table 9-8 Long exposure time related registers(example)

4:3 full resolution output mode VTPXCLK=130MHz	CIT_LSHIFT	3d (x8)
	COARSE_INTEG_TIME	60725d
	LINE_LENGTH_PCK	5352d (initial value)
	FRM_LENGTH_LINES	65535d

Exposure time

Exposure time = (60725 * 8 * 5352) / (130[MHz] *4) = 5 [sec]

* When this long exposure mode is used, mode transition of SW-standby mode transition or Fast SW-standby mode transition (see 7.2.3 or 7.2.4) is recommended.
* When this long exposure mode is used, FLASH function is not available.
* When this long exposure mode is used, picture quality is not guaranteed because S/N will deteriorate depending on the exposure time.

9.4. Flash light control sequence

This sensor can internally generate the control pulse assuming to trigger the flash light emission and output from the external pins. The flash light trigger pulse width and output timing can be controlled by registers shown in Table9-9. Flash control pulse is output from FSTROBE pins. The setting of strobe pulse is determined by reference point, delay and trigger mode. Details of setting are explained by following sections.

Table 9-9 Flash light control setting registers

	Address	Bit	Name	Description	Notes
I²C register	0x0c12	[7:0]	FLASH_STRB_ADJ [7:0]	Register to control counter for flash pulse width in rolling shutter mode. Flash pulse width (high) = (TFLASH_STRB_WIDT_H_RS_CTL / INCK frequency) * FLASH_STRB_ADJ Flash pulse width (low) = (TFLASH_STRB_WIDT_L_RS_CTL / INCK frequency) * FLASH_STRB_ADJ Range : 1 to 255	
	0x0c14	[7:0]	FLASH_STRB_START_POINT [15:8]	Register to select reference point for flash pulse in rolling shutter mode. Adjustable in one line steps. Range : 0 to last line	
	0x0c15	[7:0]	FLASH_STRB_START_POINT [7:0]		
	0x0c16	[7:0]	TFLASH_STRB_DLY_RS_CTL [15:8]	Register to control the rising edge point of Flash pulse from FLASH_STRB_START_POINT in rolling shutter mode. Step : 1H Range : 0 to 65535	
	0x0c17	[7:0]	TFLASH_STRB_DLY_RS_CTL [7:0]		
	0x0c18	[7:0]	TFLASH_STRB_WIDT_H_RS_CTL [15:8]	Register to control the high level width of flash pulse in rolling shutter mode. Flash pulse width (high) = (TFLASH_STRB_WIDT_H_RS_CTL / INCK frequency) * FLASH_STRB_ADJ	
	0x0c19	[7:0]	TFLASH_STRB_WIDT_H_RS_CTL [7:0]		
	0x0c1a	[7:0]	FLASH_MD_RS [7:0]	Bit[0] flash pulse mode control 0 : single trigger mode. 1 : continuous mode. Bit[1] flash pulse complete or truncated select 0 : complete pulse mode in rolling shutter mode 1 : truncated pulse mode in rolling shutter mode Bit[2] reference start point select 0 : exposure 1 : readout (in rolling shutter mode) Bit[3] flash pulse sync or async select 0 : synchronous 1 : asynchronous Bit[4] Reserved Bit[5] flash pulse single or multi select 0 : single	

				1 : multiple Bit[7:6] Reserved	
	0x0c1b	[7:0]	FLASH_TRIG_RS [7:0]	Flash trigger 0 : disable 1 : enable *Return to 0 in single mode, automatically *Setup other than the above is forbidden.	
	0x0c1c	[7:0]	FLASH_STAT [7:0]	Bit[0] flash pulse status 0 : Not retimed to this frame 1 : Retimed to this frame Bit[1] flash status for global reset mode *not supported 0 : Not active in global reset mode 1 : Active in global reset mode Bit[7:2] Reserved	read only
	0x0c26	[7:0]	TFLASH_STRB_WIDT2_H_RS_CTL [15:8]	Register to control the high level width of 2nd flash pulse in rolling shutter mode when TFLASH_STRB_CNT_RS_CTL=2. Range : 1 to 65535 2nd Flash pulse width (high) = (TFLASH_STRB_WIDT2_H_RS_CTL / INCK frequency) * FLASH_STRB_ADJ	
	0x0c27	[7:0]	TFLASH_STRB_WIDT2_H_RS_CTL [7:0]		
	0x0c28	[7:0]	TFLASH_STRB_WIDT_L_RS_CTL [15:8]	Register to control the low level width of flash pulse in rolling shutter mode. Range : 1 to 65535 Flash pulse width (low) = (TFLASH_STRB_WIDT_L_RS_CTL / INCK frequency) * FLASH_STRB_ADJ	
	0x0c29	[7:0]	TFLASH_STRB_WIDT_L_RS_CTL [7:0]		
	0x0c2a	[7:0]	TFLASH_STRB_CNT_RS_CTL [7:0]	Register to control flash pulse count in rolling shutter mode. Range : 1 to 255	

9.4.1. Reference point

Reference point is the base point of delay settings for flash control pulse and can be determined by FLASH_MD_RS[2]. As example, following charts shows single trigger mode. It is also same for other trigger modes. In case of HDR capture mode, start of long exposure should be the reference point with “start of exposure” setting. On the other hand, “start of readout” is not change.

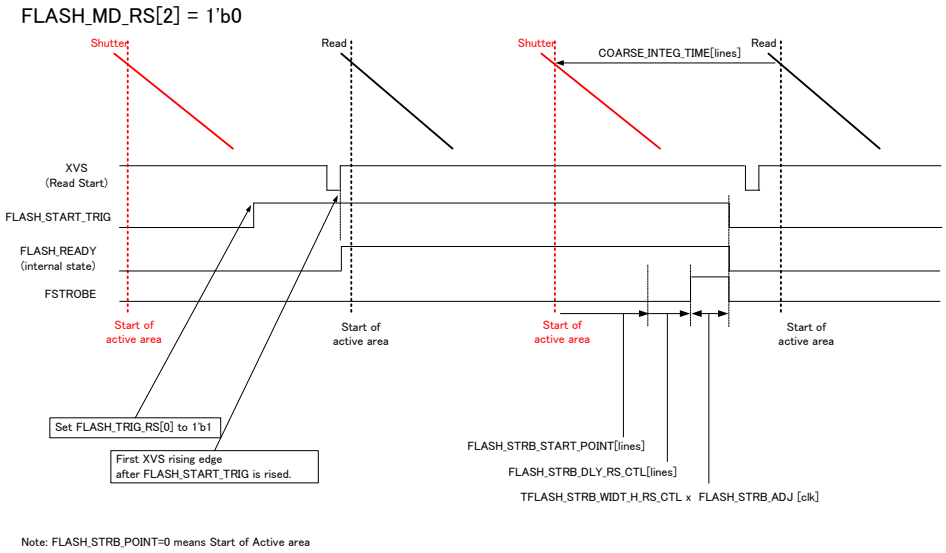

Figure 9-4 Reference point (Start of exposure)

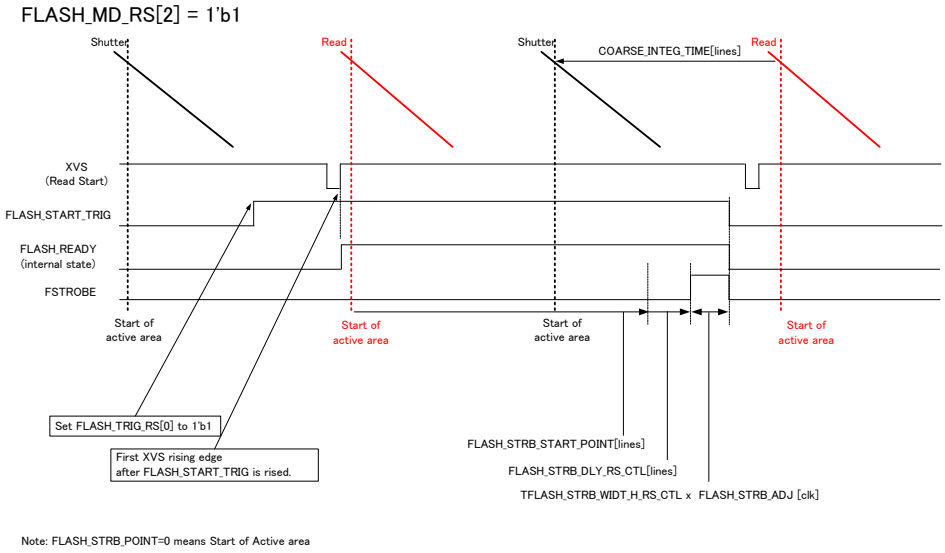

Figure 9-5 Reference point (Start of readout)

9.4.2. Single trigger mode / Continuous mode

This sensor supports both single trigger strobe mode and continuous mode.

Single trigger mode is enabled by setting FLASH_MD_RS[0] to 1'b0.

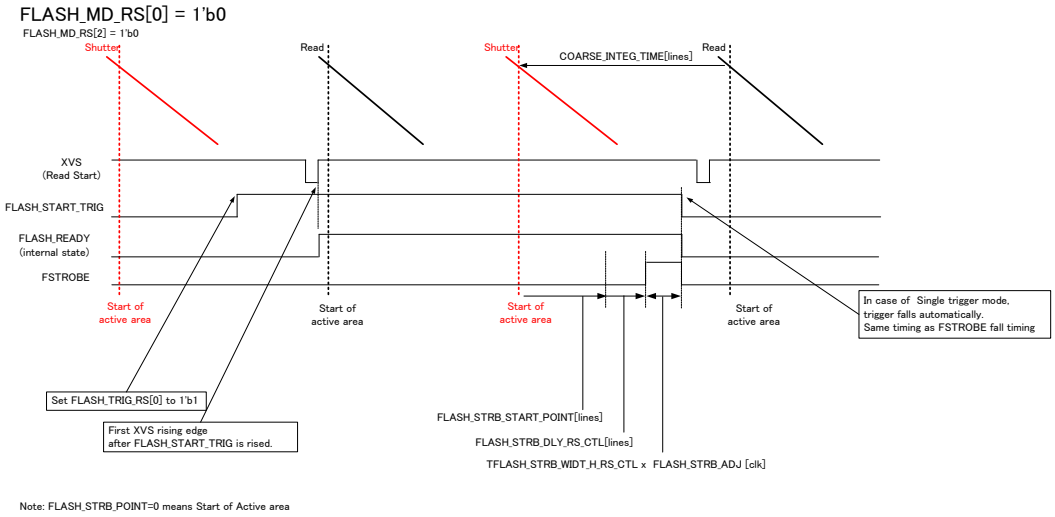

Figure 9-6 Single Trigger mode

Continuous mode is enabled by setting FLASH_MD_RS[0] to 1'b1. In this mode, flash control pulse can be output both continuously and periodically.

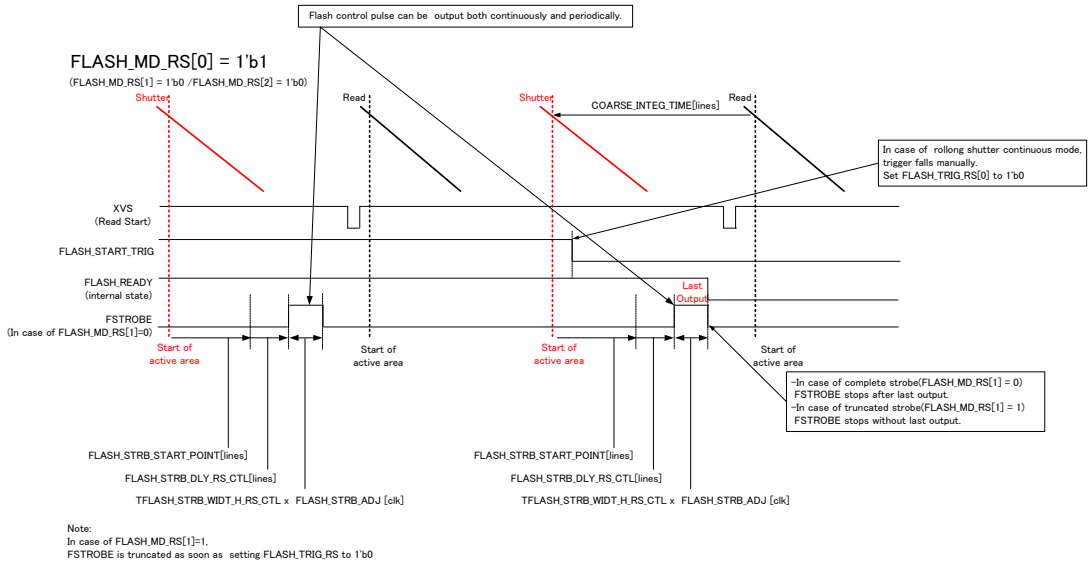

Figure 9-7 Continuous mode

9.4.3. Multiple strobe

This sensor supports both single flash strobe mode and multiple flash modes. Multiple flash strobe mode is enabled by setting FLASH_MD_RS[5] to 1'b1. In this mode, more than one output of flash control pulse can be controlled. Multiple strobes can set not only in single trigger mode but also in continuous mode. Following chart shows single trigger mode and reference point of shutter as an example. Number of flash control pulse is determined by TFRASH_STRB_CNT_RS_CTL. In case more than 3 strobes are output in 1 frame, width of strobe pulse can't be set separately. On the other hand, dual flash strobe can control the pulse width separately. Following Table shows duty and width period that you can set.

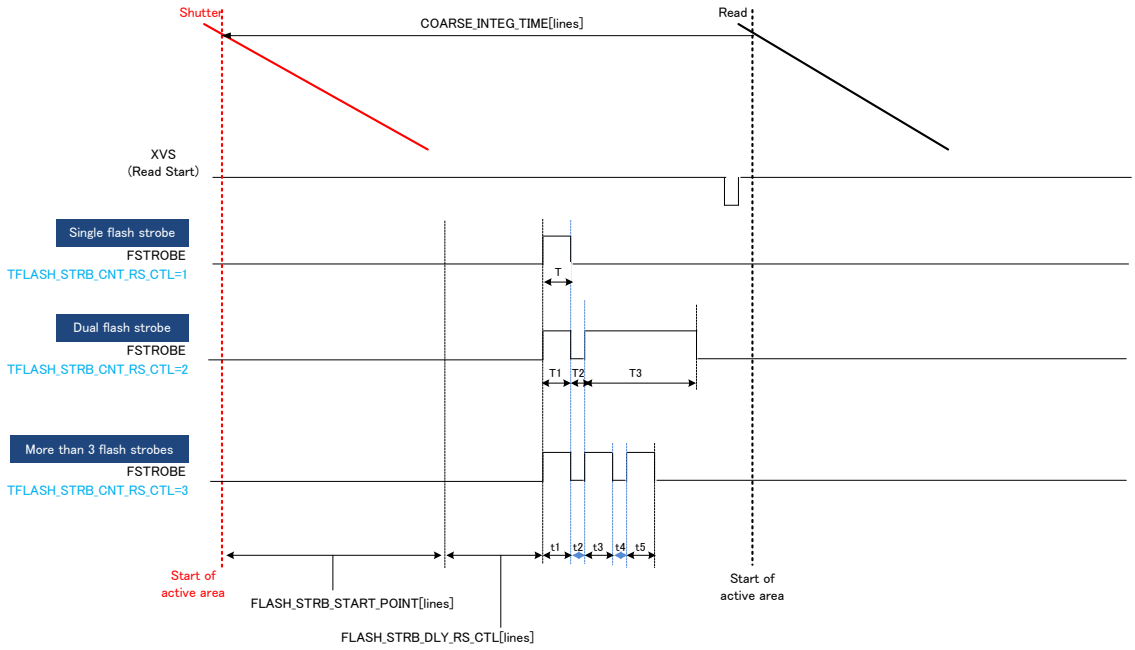

Figure 9-8 Single flash strobe / Multiple flash strobe

Table 9-10 Single Flash strobe duty control register

Time	Register
T	TFLASH_STRB_WIDT_H_RS_CTL × FLASH_STRB_ADJ[clk]

Table 9-11 Dual Flash strobe duty control register

Time	Register
T1	TFLASH_STRB_WIDT_H_RS_CTL × FLASH_STRB_ADJ[clk]
T2	TFLASH_STRB_WIDT_L_RS_CTL × FLASH_STRB_ADJ[clk]
T3	TFLASH_STRB_WIDT2_H_RS_CTL × FLASH_STRB_ADJ[clk]

Table 9-12 More than 3 Flash strobe duty control register

Time	Register
t1	TFLASH_STRB_WIDT_H_RS_CTL × FLASH_STRB_ADJ[clk]
t2	TFLASH_STRB_WIDT_L_RS_CTL × FLASH_STRB_ADJ[clk]
t3	TFLASH_STRB_WIDT_H_RS_CTL × FLASH_STRB_ADJ[clk]
t4	TFLASH_STRB_WIDT_L_RS_CTL × FLASH_STRB_ADJ[clk]
t5	TFLASH_STRB_WIDT_H_RS_CTL × FLASH_STRB_ADJ[clk]

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9.5. One time programmable (OTP) memory

See “IMX258 OTP Manual”

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9.6. Pulse for OIS driver

This sensor can output the pulse for OIS driver. This pulse is generated from VTPXCK.

High period and Low period can be set by registers. The pulse can be reset by H sync.

Refer to “9.7 Monitor terminal settings” for outputting OIS Pulse from the monitor terminal.

Table 9-13 Pulse output setting registers for OIS driver

	Address	Bit	Name	Description
I2C register	0x5ac4	[7:0]	OIS_H_WIDTH	High frequency pulse output for OIS driver is set with IVTPXCK cycle number [1-255] (def:8)
	0x5ac5	[7:0]	OIS_L_WIDTH	Low frequency pulse output for OIS driver is set with IVTPXCK cycle number [1-255] (def:8)
	0x5ac6	[0]	OIS_HRESET_EN	Enable H sync reset for pulse output for OIS driver. (def:0) 0: Do not reset 1: Reset with H sync

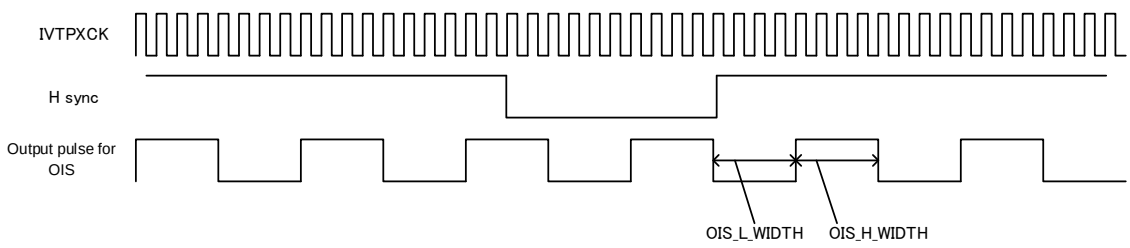

Figure 9-9 OIS_HRESET_EN=0 operation

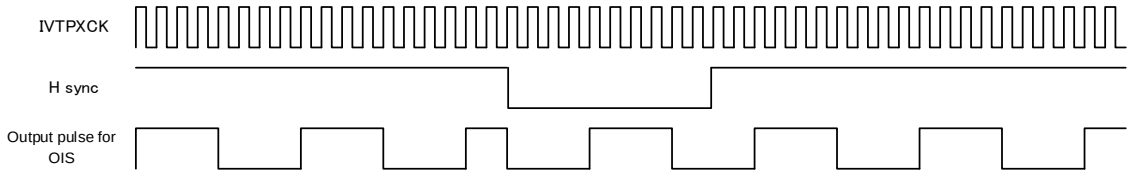

Figure 9-10 OIS_HRESET_EN=1 operation

9.7. Monitor terminal settings

This sensor can output 3 internal signals (XVS/Flash strobe/OIS pulse) via monitor terminals.

The monitor terminals mean the following three(3) terminals, such as FSTROBE (41 pin), XVS (48 pin) and GPO (42 pin), See the following table for register settings.

Table 9-14 Monitor terminal setting

	Address	Bit	Name	Setting value
I2C register	0x4635	[1:0]	OUTIF1	XVS IO Control 0d : Output
	0x4636	[1:0]	OUTIF2	GPO IO Control 0d : Output
	0x5A5A	[7:0]	TEST_SDO[7:0]	1d: OIS Pulse is selected. 15d: H sync is selected.
	0x5A5B	[7:0]	TEST_FSTRB[7:0]	15d: V sync is selected. 115d: H sync is selected.
	0x463A	[7:0]	TESTMNT2[7:0]	FFh: GPO(42pin)'s signal is selected by TEST_FSTRB[7:0] FEh: GPO (42pin)'s signal is selected by TEST_SDO [8:0]
	0x463B	[7:0]	TESTMNT3[7:0]	FFh: XVS(48pin)'s signal is selected by TEST_FSTRB[7:0] FEh: XVS(48pin)'s signal is selected by TEST_SDO [8:0]
	0x4643	[7:0]	GPIOSEL	00h

FSTROBE (41 pin)

Flash Strobe can be output via FSTROBE pin.

See "9.4 Flash light control sequence" for the detail of Flash Strobe control.

XVS (48 pin)

XVS can be output via XVS pin. On the other hand, V sync / H sync / OIS Pulse can be selected and output via XVS pin.

Signal is selected by TEST_FSTRB [7:0] (TESTMNT3 [7:0] = FFh) or . TEST_SDO [8:0] (TESTMNT3 [7:0] = FEh)

GPO (42 pin)

V sync / H sync / OIS Pulse can be selected and output via GPO pin.

Signal is selected by TEST_FSTRB [7:0] (TESTMNT2 [7:0] = FFh) or . TEST_SDO [8:0] (TESTMNT2 [7:0] = FEh)

Setting examples:

Case1: simultaneous output of H sync, V sync and Flash Strobe.

Table 9-15 Monitor Setting example case 1

Pin name	Selected Signal	Setting value
FSTROBE (41 pin)	Flash strobe	TEST_SDO:15d、TEST_FSTRB :15d、TESTMNT2: FEh、TESTMNT3:FFh、GPIOSEL:00h
XVS (48 pin)	V sync	
GPO (42pin)	H sync	

Case2: simultaneous output of OIS Pulse, Flash Strobe and H sync.

Table 9-16 Monitor Setting example case 2

Pin name	Selected Signal	Setting value
FSTROBE (41 pin)	Flash strobe	TEST_SDO:1d、TEST_FSTRB :115d、TESTMNT2: FFh、TESTMNT3:FEh、GPIOSEL:00h
XVS (48 pin)	OIS Pulse	
GPO (42pin)	H sync	

Case3: simultaneous output of OIS Pulse, Flash Strobe and V sync.

Table 9-17 Monitor Setting example case 3

Pin name	Selected Signal	Setting value
FSTROBE (41 pin)	Flash strobe	TEST_SDO:1d、TEST_FSTRB :15d、TESTMNT2: FFh、TESTMNT3:FEh、GPIOSEL:00h
XVS (48 pin)	OIS Pulse	
GPO (42pin)	V sync	

9.7.1. V sync / H sync

V sync and H sync are the internal timing of image sensor.

V sync is the timing of the frame unit, and H sync is the line unit ones. Polarity and Pulse width of V sync / H sync can be set.

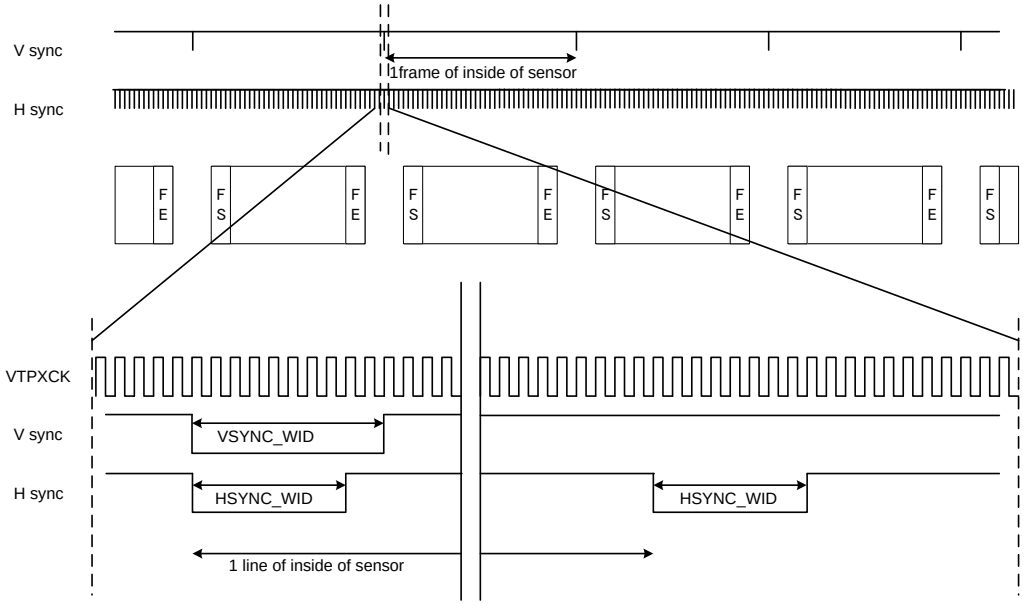

Figure 9-11 Image of V sync / H sync

Table 9-18 V sync / H sync settings

	Address	Bit	Name	comment
I2C register	0x5C0C	[0]	VSYNC_POL	Polarity of V sync Pulse (def:0) 0:Lo-Active, 1:Hi-Active
	0x5C0D	[2:0]	VSYNC_WID	Pulse width of V sync Pulse (Unit: IVTPXCK cycle) (def:0) 0d: x10 1d: x20 2d: x50 3d: x100 4d: x200 5d: x500 6d: x1000 7d: x2000
	0x5C0E	[0]	HSYNC_POL	Polarity of H sync Pulse (def:0) 0:Lo-Active, 1:Hi-Active
	0x5C0F	[2:0]	HSYNC_WID	Pulse width of H sync Pulse (Unit: IVTPXCK cycle) (def:0) 0d: x10 1d: x20 2d: x50 3d: x100 4d: x200 5d: x500 6d: x1000 7d: x2000

9.8. Dual Camera

9.8.1. Dual camera operation

This section describes about a method of getting a pair of synchronous image from two sensors controlled by one host ISP device. This sensor can set either of Master mode or Slave mode, and each sensor is possible to change gain settings individually while keeping synchronous relation between sensors.

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9.8.1.1. Block diagram of Dual camera application

The following figure shows the block diagram of the Dual camera system.

Dual camera operation using combination of this sensor is realized by connecting VSYNC signal between two sensors. This sensor can be output VSYNC for synchronization when it is using as a Master mode, and this sensor can also receive VSYNC signal when it is using as a Slave mode.

Synchronization of two sensors is achieved with shared CCI bus by having two different 1st CCI addresses and two common 2nd CCI addresses between two sensors.

- Any settings using 1st CCI addresses are independently applied for each sensor.
- Settings with 2nd CCI address are commonly applied for both sensors.

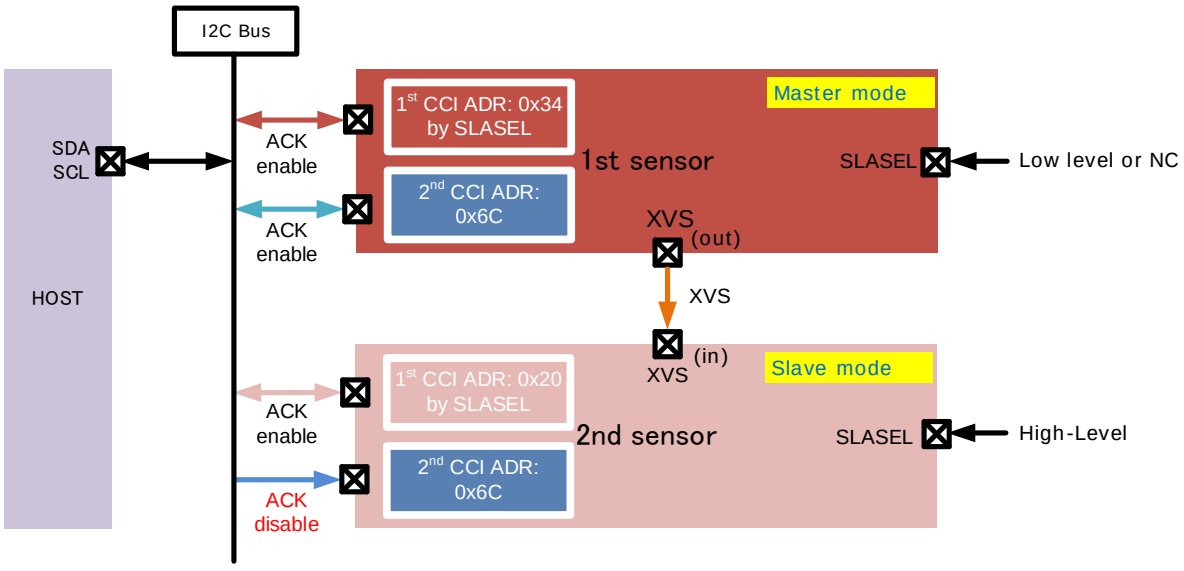

Figure 9-12 Dual camera system block diagram with shared CCI bus

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9.8.2. CCI communication setting

This sensor has a built-in 2nd CCI address of 0x6c which is common for all sensors. When the 2nd CCI address is activated and with different 1st CCI address which is controlled by SLASEL setting, each sensor has each CCI addresses. (For example, Master sensor has CCI address with 0x34 and 0x6c, Slave sensor has CCI address with 0x20 and 0x6c. See the section “2.3 Default CCI slave address configuration”.)

The above configuration enables to set different settings on each sensor and to set common settings on both sensors. Consequently each sensor can synchronously capture a same scene with individual gain setting.

In Dual cam system with shared CCI bus connection, The 2nd CCI address shall be activated and the either Master or Slave sensor should be set as ACK responder based on the following table.

Table 9-19 Control Register of 2nd address

	Address	Bit	Name	Description	initial value(HEX)
I^2C register	0x3006	[0]	SLAVE_ADD_EN_2ND	2nd Slave Address Enable 0: disable, 1: enable	1'h0
	0x3007	[0]	SLAVE_ADD_ACKEN_2ND	Enable ACK for 2nd CCI interface 0: disable,1: enable	1'h0

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9.8.3. Master and Slave sensor settings

The setting registers for each Master and Slave sensor are shown below and these setting should be issued during SW standby.

Table 9-20 Control Register for Master and Slave mode

	Address	Bit	Name	Description	Master Mode Setting (HEX)	Slave Mode Setting (HEX)
I2C register	0x3004	[0]	MASTER_SLAVE_SEL	Master or Slave mode setting 0 : Slave mode 1 : Master mode (default)	1'h1 (default)	1'h0
	0x5A5D	[0]	EXTOUT_EN	Master or Slave mode setting 0 : Slave mode (default) 1 : Master mode	1'h1	1'h0 (default)
	0x4635	[1:0]	OUTIF1	XVS In/Out setting 0,1,2: Master mode(Output) 3 : Slave mode(Input) (default)	2'h0	2'h3 (default)
	0x5a90	[3:0]	VDMY1_STA	Master or Slave sensor settings Master or Slave sensor should be switch these values	4'h4 (default)	4'h0
	0x5a92	[3:0]	VDMY1_WID		4'h4 (default)	4'h8
	0x5a93	[7:4]	VDMY2_WID		4'h4 (default)	4'h0

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9.8.4. Control sequence of Dual camera application with shared CCI bus (recommended)

In shared CCI bus connection, CCI address setting should be set as follows,

- Any settings using 1st CCI addresses are independently applied for each sensor.
- Settings with 2nd CCI address are commonly applied for both sensors.

The following figure shows the control sequence of Dual camera application with shared CCI bus. Before streaming starts, it is necessary to set "MODE_SEL" to the slave sensor first. Then "MODE_SEL" for master sensor should be set.

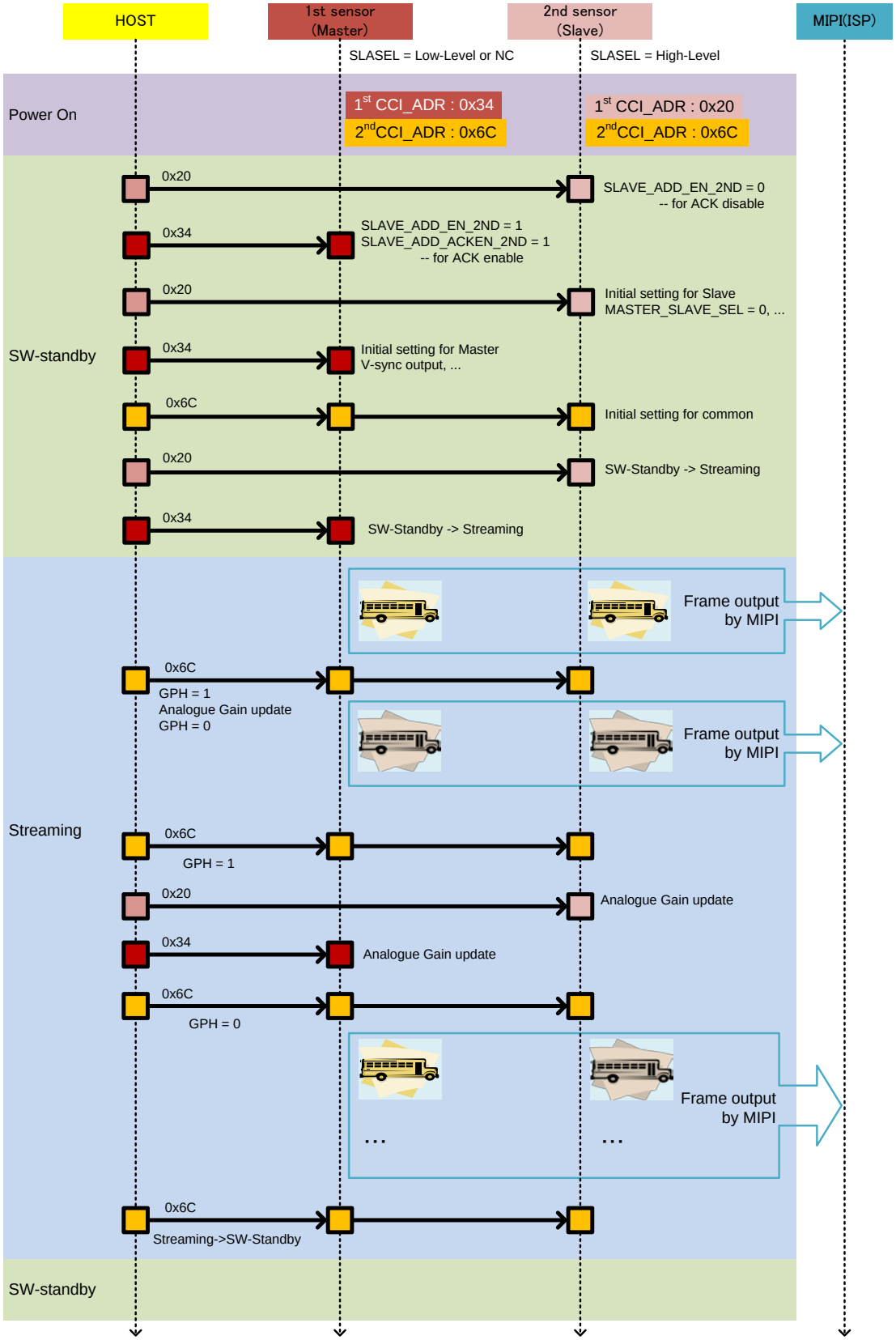

Figure 9-13 Communication control and timing with shared CCI Bus

9.8.5. Restriction of Dual camera usage with shared CCI bus

The restrictions of Dual camera usage for this sensor are shown as below.

- Master and Slave sensor must be operated with the same operation mode.
- FRM_LENGTH_LINES, LINE_LENGTH_PCK must be the same value.
- COARSE_INTEG_TIME must be the same value at the 1st frame.
- The embedded thermal meter of Slave sensor in standby mode is not supported. If you want to use embedded thermal meter at standby mode, it is only available of Master sensor.
- AEB (AE bracketing) mode is not supported.
- GPH (grouped parameter hold) must be used for updating gain during streaming.
- Fast mode transition is not supported
- Between two sensors, there exists a worst case time difference in MIPI outputs calculated with the following equation.

$$\Delta t_{max} = 130 * t_{INCK} = 130 / f_{INCK} \text{（Worst case)}$$

Where: t_{INCK} is external clock period and f_{INCK} is external clock frequency to the sensor.

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9.8.6. Dual camera system with Separated CCI bus (optional)

The following figure shows the block diagram of the Dual camera system using with separated CCI bus. In this use case, one sensor is connected to I2C Bus (A) and the other sensor is connected to I2C Bus (B). When the Dual camera system with Separated CCI Bus is operated, both of 1st CCI addresses do not require the different CCI address. It means that the same 1st CCI address is acceptable in this connection. On the other hand, there is no need to setting for 2nd Slave address.

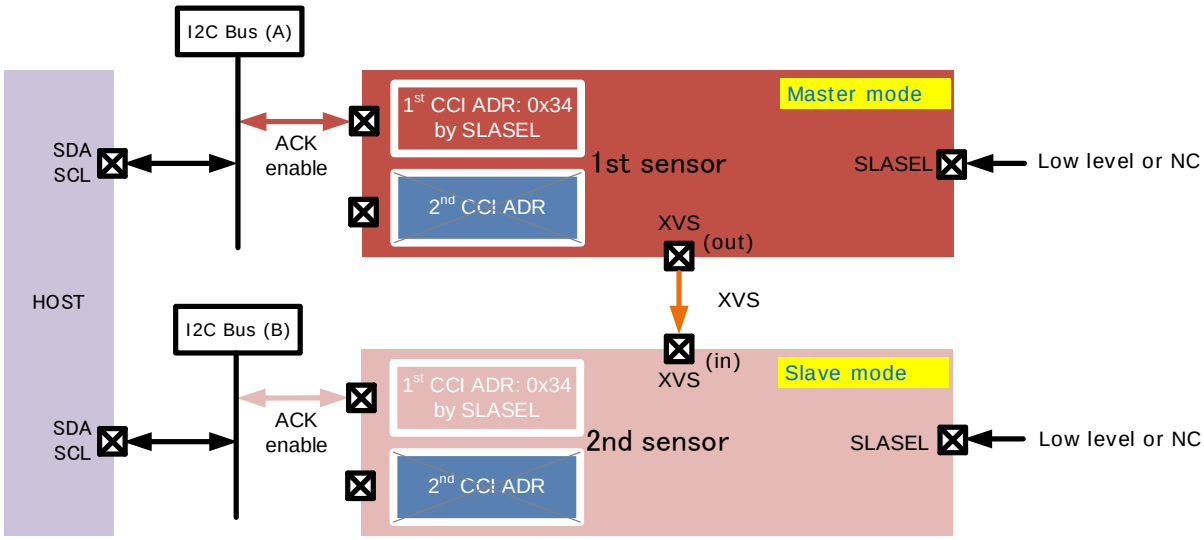

Figure 9-14 Dual camera system block diagram with separated CCI bus

The following figure shows the system control sequence of the Dual camera system using with separated CCI Bus.

First of all, it is necessary to set "MODE_SEL" to the Slave mode sensor before streaming starts. Then, “MODE_SEL” for Master mode sensor should be set.

If you need to change the both sensors setting at same time, it is necessary to pay attention about setting delay time between separated CCI Bus. If there is a large delay time, it will be happen that there is not a synchronized case between Master and slave sensors.

The other restrictions are same as Dual camera system with shared CCI Bus.

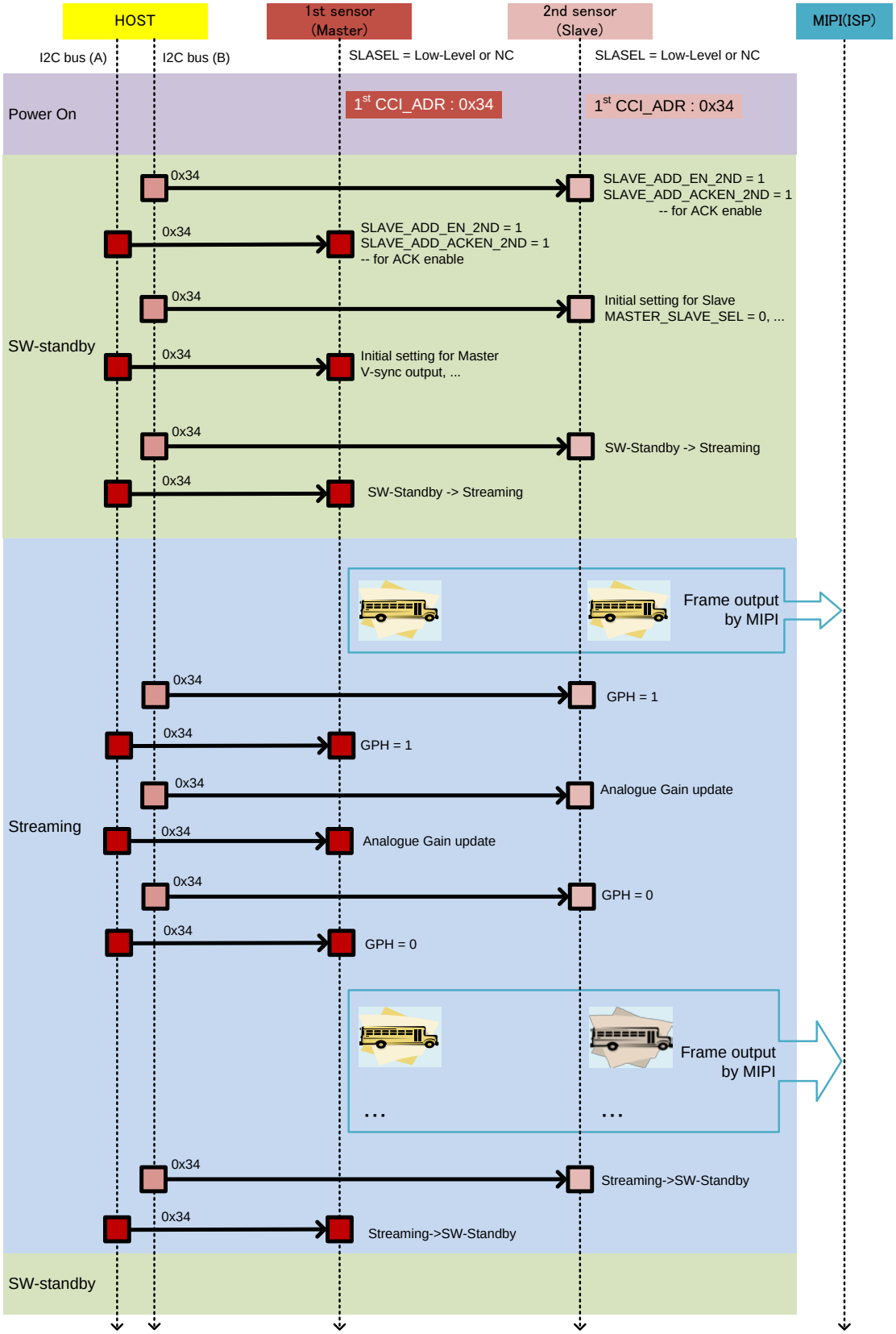

Figure 9-15 Communication control and timing with separated CCI Bus

9.8.7. Restriction of dual/multi camera usage

The restrictions of dual(or multi) camera usage for this sensor are shown as below.

NO.	Restriction Item	Addition
1	Synchronous input signal restrictions for slave sensor	To keep the slave sensor first image normal since streaming starts, it is required to keep the both sensors' shutter time as equal as possible at least for first frame just after streaming ON. From the second frame, each shutter time can be set distinctively. Refer to each sensor's software reference manual for shutter time calculation. Tsh = Tline * (CORSE_INTEG_TIME+FINE_INTEG_TIME / LINE_LENGTH_PCK [pixels/line])
2	The frame rate	The frame rate of master and slave sensor should be set as close as possible.. Although to make two sensors' frame rate completely the same may be difficult, especially if the sensor type and/or operation mode is different, it is recommended to make the frame rate as close as possible by tuning V-blanking or H-period between two sensors.
3	Sensor output latency	The two sensors operate synchronously with master XVS. However slight difference in video output phase may exist due to an asynchronous command capture and data transfer from internal logic domain to MIPI output domain. It should be in maximum of several cycles of VTPXCK cycle.
4	Mode transition	For avoiding the uncertainty of mode operation, SW-standby or Fast SW-standby in mode transition is recommended.
5	Thermal meter	The embedded thermal meter of slave sensor in standby mode is not supported. Because the slave sensor does not receive external XVS signal in SW standby state, which is necessary for operation of thermal meter.
6	Manufacture of two sensors	Dual sensor operation described in this document is only applicable for Sony CIS censors for cellular products.

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10. Lens Shading Correction (LSC)

This sensor has a built-in lens shading correction (LSC) function for each color (R/Gr/B/Gb) separately. The LSC can be usable only in Normal capture mode.

A purpose of the LSC function in this sensor is primarily for module level calibration of four colors. However, it can be also usable as a substitute function of LSC function as usually done in ISP if matches your functional and/or image quality requirements.

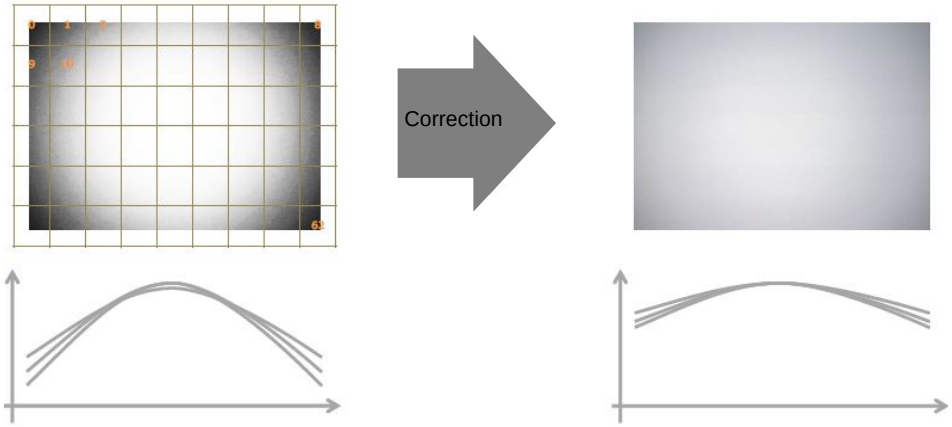

Figure 10-1 Lens Shading Correction

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10.1. Abstract of LSC system

LSC system consist of two RAMs(Table1 and Table2) for enabling back ground writing of high volume knot point data over CCI communication.

Table1 initial parameters are automatically loaded from OTP after power on (This sensor can store the LSC related data in OTP).

Table2 is blank after power on sequence. Please write by CCI communication if using.

Actual gain to be applied to each pixel is interpolated vertically and horizontally with Spline method as shown in below figure.

In case of only once setting during startup (global setting), either of the two RAM table is used.

In case of switching between both sides, it is required of writing and enabling knot point settings.

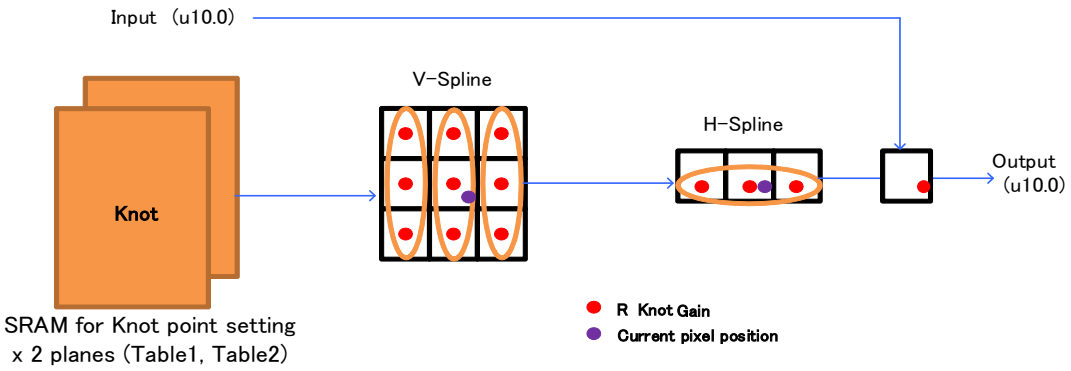

Figure 10-2 LSC schematic block diagram

Above diagram shows knots versus its location in a full-pixel output (example of R pixel).

The same correction is applied in the same way with other resolutions and colors.

Number of knot point is 9(H) x 7(V) and location of each knot point is as shown in the following figure.

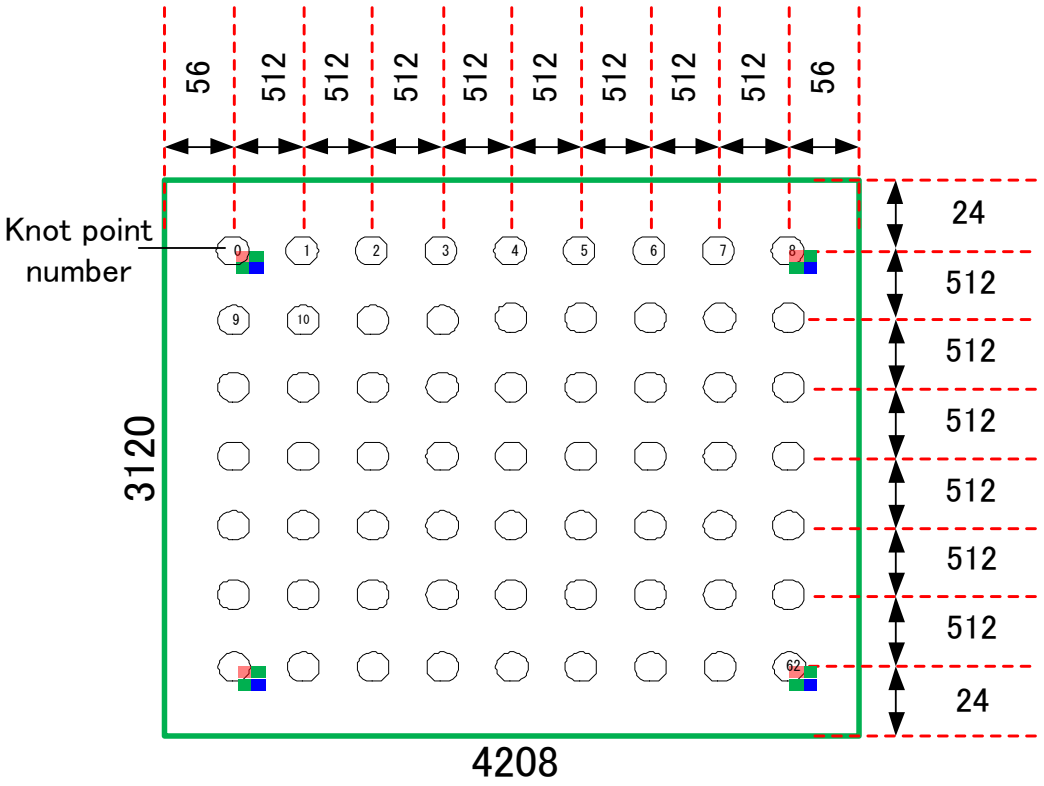

Figure 10-3 Location of knot points 9x7

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10.2. LSC control registers

The following table shows control registers of LSC and knot point tables. Regarding complete information on the knot point setting table, see IMX258 Register Map.

Table 10-1 LSC setting register

	Address	Bit	Name	Description
I²C register	0x0220	[5:0]	HDR_MODE	[0] HDR select 0 : HDR disable 1 : HDR enable [1] Gain select during HDR 0 : combined gain used (during HDR) 1 : separate gain used (during HDR) [5] short exposure controlled during HDR 0 : short exposure determined by ratio (during HDR) 1 : short exposure controlled by direct control (during HDR)
	0x0222	[4:0]	EXPO_RATIO	Defines exposure ratio between short and long exposure. Short exposure value = coarse_integration_time / Exposure_ratio 1,2,4,8,16(unsigned integer) can be set.
	0x0b00	[0]	SHD_CORR_EN*1	0: LSC disable 1: LSC enable
	0x3021	[0]	LSC_MANUAL_TABLE_SEL	Knot point table switching register 0:Table1 1:Table2
	0x3025	[0]	LSC_TABLE_STATUS	Knot point table using status(Read Only) 0:Table1 1:Table2
	0x7b8c	[1:0]	KNOT_FMT_R	Define knot point(R pixel) *2 0= u2.8, 1= u3.7, 2= u1.9, 3= u4.6
	0x7b8d	[1:0]	KNOT_FMT_GR	Define knot point(R pixel) *2 0= u2.8, 1= u3.7, 2= u1.9, 3= u4.6
	0x7b8e	[1:0]	KNOT_FMT_GB	Define knot point(R pixel) *2 0= u2.8, 1= u3.7, 2= u1.9, 3= u4.6
	0x7b8f	[1:0]	KNOT_FMT_B	Define knot point(R pixel) *2 0= u2.8, 1= u3.7, 2= u1.9, 3= u4.6
	0xA100	[1:0]	LSC_TABLE1_R_00 [9:8]	Table1 LSC Knot point R00 *3
	0xA101	[7:0]	LSC_TABLE1_R_00 [7:0]	
	0xA102	[1:0]	LSC_TABLE1_R_01 [9:8]	Table1 LSC Knot point R01 *3

	0xA103	[7:0]	LSC_TABLE1_R_01 [7:0]	
	...	...	...	...
	0xA17A	[1:0]	LSC_TABLE1_R_61 [9:8]	Table1 LSC Knot point R61 *3
	0xA17B	[7:0]	LSC_TABLE1_R_61 [7:0]	
	0xA17C	[1:0]	LSC_TABLE1_R_62 [9:8]	Table1 LSC Knot point R62 *3
	0xA17D	[7:0]	LSC_TABLE1_R_62 [7:0]	
	0xA17E	[1:0]	LSC_TABLE1_GR_00 [9:8]	Table1 LSC Knot point GR00 *3
	0xA17F	[7:0]	LSC_TABLE1_GR_00 [7:0]	
	0xA180	[1:0]	LSC_TABLE1_GR_01 [9:8]	Table1 LSC Knot point GR01 *3
	0xA181	[7:0]	LSC_TABLE1_GR_01 [7:0]	
	...	...	...	...
	0xA1F8	[1:0]	LSC_TABLE1_GR_61 [9:8]	Table1 LSC Knot point GR61 *3
	0xA1F9	[7:0]	LSC_TABLE1_GR_61 [7:0]	
	0xA1FA	[1:0]	LSC_TABLE1_GR_62 [9:8]	Table1 LSC Knot point GR62 *3
	0xA1FB	[7:0]	LSC_TABLE1_GR_62 [7:0]	
	0xA1FC	[1:0]	LSC_TABLE1_GB_00 [9:8]	Table1 LSC Knot point GB00 *3
	0xA1FD	[7:0]	LSC_TABLE1_GB_00 [7:0]	
	0xA1FE	[1:0]	LSC_TABLE1_GB_01 [9:8]	Table1 LSC Knot point GB01 *3
	0xA1FF	[7:0]	LSC_TABLE1_GB_01 [7:0]	
	...	...	...	...
	0xA276	[1:0]	LSC_TABLE1_GB_61 [9:8]	Table1 LSC Knot point GB61 *3
	0xA277	[7:0]	LSC_TABLE1_GB_61 [7:0]	
	0xA278	[1:0]	LSC_TABLE1_GB_62 [9:8]	Table1 LSC Knot point GB62 *3
	0xA279	[7:0]	LSC_TABLE1_GB_62 [7:0]	
	0xA27A	[1:0]	LSC_TABLE1_B_00 [9:8]	Table1 LSC Knot point B00 *3
	0xA27B	[7:0]	LSC_TABLE1_B_00 [7:0]	
	0xA27C	[1:0]	LSC_TABLE1_B_01 [9:8]	Table1 LSC Knot point B01 *3
	0xA27D	[7:0]	LSC_TABLE1_B_01 [7:0]	
	...	...	...	...
	0xA2F4	[1:0]	LSC_TABLE1_B_61 [9:8]	Table1 LSC Knot point B61 *3
	0xA2F5	[7:0]	LSC_TABLE1_B_61 [7:0]	
	0xA2F6	[1:0]	LSC_TABLE1_B_62 [9:8]	Table1 LSC Knot point B62 *3
	0xA2F7	[7:0]	LSC_TABLE1_B_62 [7:0]	
	0xA300	[1:0]	LSC_TABLE2_R_00 [9:8]	Table2 LSC Knot point R00
	0xA301	[7:0]	LSC_TABLE2_R_00 [7:0]	

	0xA302	[1:0]	LSC_TABLE2_R_01 [9:8]	Table2 LSC Knot point R01
	0xA303	[7:0]	LSC_TABLE2_R_01 [7:0]	
	...	...	...	...
	0xA37A	[1:0]	LSC_TABLE2_R_61 [9:8]	Table2 LSC Knot point R61
	0xA37B	[7:0]	LSC_TABLE2_R_61 [7:0]	
	0xA37C	[1:0]	LSC_TABLE2_R_62 [9:8]	Table2 LSC Knot point R62
	0xA37D	[7:0]	LSC_TABLE2_R_62 [7:0]	
	0xA37E	[1:0]	LSC_TABLE2_GR_00 [9:8]	Table2 LSC Knot point GR00
	0xA37F	[7:0]	LSC_TABLE2_GR_00 [7:0]	
	0xA380	[1:0]	LSC_TABLE2_GR_01 [9:8]	Table2 LSC Knot point GR01
	0xA381	[7:0]	LSC_TABLE2_GR_01 [7:0]	
	...	...	...	...
	0xA3F8	[1:0]	LSC_TABLE2_GR_61 [9:8]	Table2 LSC Knot point GR61
	0xA3F9	[7:0]	LSC_TABLE2_GR_61 [7:0]	
	0xA3FA	[1:0]	LSC_TABLE2_GR_62 [9:8]	Table2 LSC Knot point GR62
	0xA3FB	[7:0]	LSC_TABLE2_GR_62 [7:0]	
	0xA3FC	[1:0]	LSC_TABLE2_GB_00 [9:8]	Table2 LSC Knot point GB00
	0xA3FD	[7:0]	LSC_TABLE2_GB_00 [7:0]	
	0xA3FE	[1:0]	LSC_TABLE2_GB_01 [9:8]	Table2 LSC Knot point GB01
	0xA3FF	[7:0]	LSC_TABLE2_GB_01 [7:0]	
	...	...	...	...
	0xA476	[1:0]	LSC_TABLE2_GB_61 [9:8]	Table2 LSC Knot point GB61
	0xA477	[7:0]	LSC_TABLE2_GB_61 [7:0]	
	0xA478	[1:0]	LSC_TABLE2_GB_62 [9:8]	Table2 LSC Knot point GB62
	0xA479	[7:0]	LSC_TABLE2_GB_62 [7:0]	
	0xA47A	[1:0]	LSC_TABLE2_B_00 [9:8]	Table2 LSC Knot point B00
	0xA47B	[7:0]	LSC_TABLE2_B_00 [7:0]	
	0xA47C	[1:0]	LSC_TABLE2_B_01 [9:8]	Table2 LSC Knot point B01
	0xA47D	[7:0]	LSC_TABLE2_B_01 [7:0]	
	...	...	...	...
	0xA4F4	[1:0]	LSC_TABLE2_B_61 [9:8]	Table2 LSC Knot point B61
	0xA4F5	[7:0]	LSC_TABLE2_B_61 [7:0]	
	0xA4F6	[1:0]	LSC_TABLE2_B_62 [9:8]	Table2 LSC Knot point B62
	0xA4F7	[7:0]	LSC_TABLE2_B_62 [7:0]	

Note1: The LSC can be usable only in Normal capture mode. When Normal capture mode LSC is controlled by SHD_CORR_EN register. (Please see 10.3 Operation sequence of LSC)

Note2: These register value are copied from OTP and it should be set as common value

Note3: These register value are copied from OTP

10.3. Operation sequence of LSC

The LSC can be usable only in Normal capture mode. When Normal capture mode LSC is controlled by SHD_CORR_EN register.

Selected of HDR Capture mode or Normal Capture mode is controlled by HDR_MODE and EXPO_RATIO registers

Table 10-2 Capture mode decode table

Capture mode	HDR_MODE			EXPO_RATIO[4:0]	LSC
	[0]	[1]	[5]		
Normal	0	x	x	X	Controlled by SHD_CORR_EN
	1	0	0	1	
HDR	1	other			OFF

This sensor has two RAM tables as shown in “” as knot point tables. Either of tables for use in correction is selected with LSC_MANUAL_TABLE_SEL by ISP during streaming and then updated internally in synchronous with V-sync. Note that the flipping between two tables is only done with V-sync timing (see” Figure 10-5 Knot point information setting and reflection timing (global setting)”).

Note that setting data into the both of tables during standby (power on initial setting or SW standby between mode transitions) is not feasible.

Knot point data is set to the RAM table via CCI communication either during global setting (Figure 10-5… read/write relation of tables are fixed to the default setting) as power on procedure, SW-standby between modes or dynamically during streaming Figure 10-6 read/write tables can be flipped) depending on system requirement.

Writing, updating or changing knot point data

- During global setting(Power on initial setting):

This sensor can store the LSC related data in OTP. These LSC data and control parameters are automatically loaded to LSC Table 1 during power on initial setting.

Writing knot point data during global setting (SW-standby):

See Figure 10-6

- During other SW-standby state (between streaming modes):

Updating knot point data during SW-standby between streaming modes.

Both Knot Table can be changed freely

- During streaming (on the fly):

Changing knot point data during streaming.

Check LSC_TABLE_STATUS in order to know current table, and set writing knot point data to Knot Table (inverse table of LSC_TABLE_STATUS).

. See Figure 10-7

Despite of the above explained capability in this sensor, considering of data volume to be transferred, it is recommended to set the knot point data only during global setting based on the LSC method explained in “LSC data structure10.4 ”

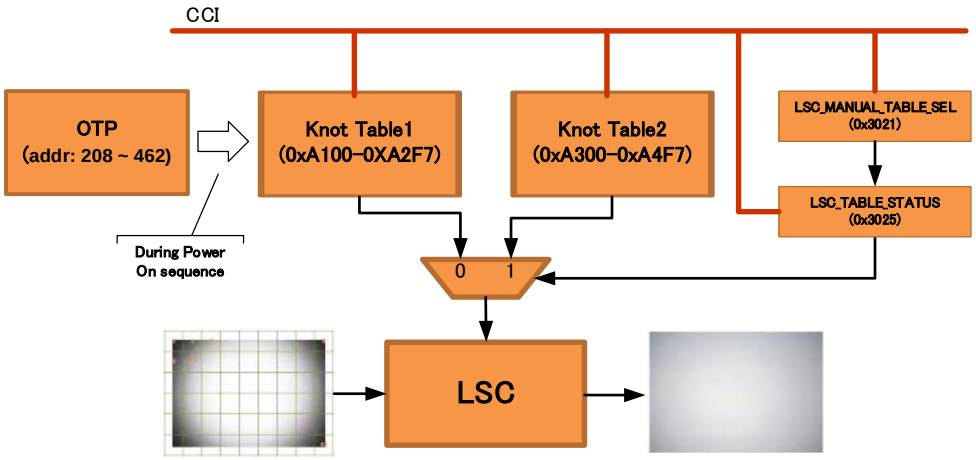

Figure 10-4 LSC system block diagram

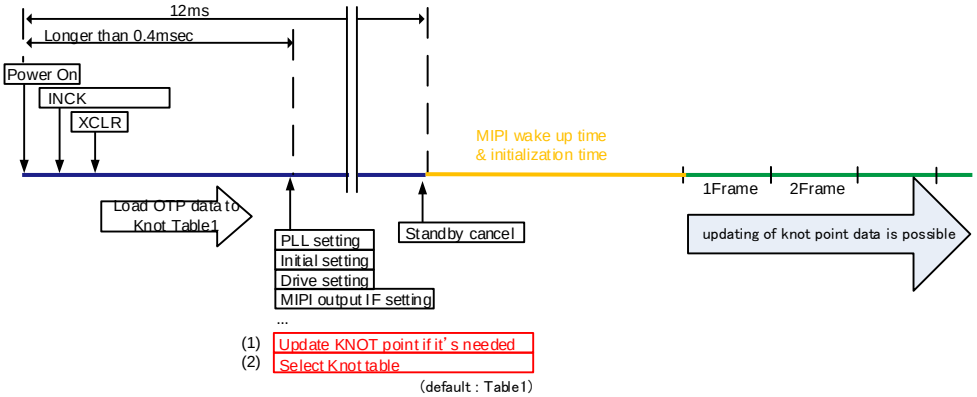

Figure 10-5 Knot point information setting and reflection timing (global setting)

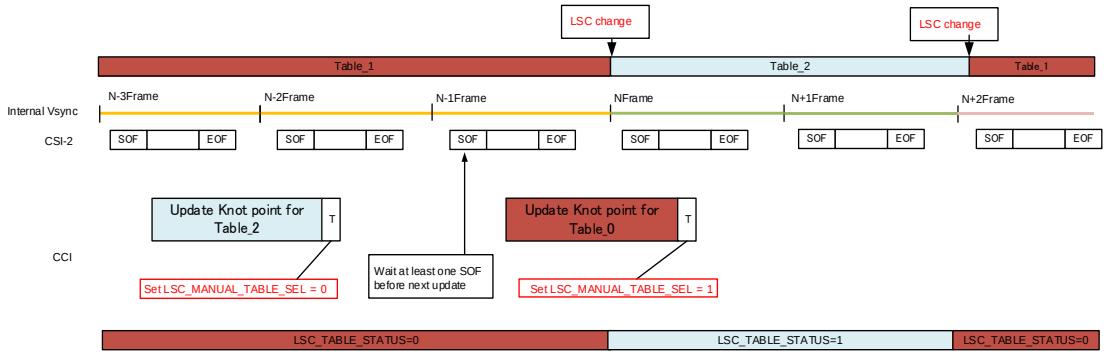

Figure 10-6 Knot point information update setting during streaming

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10.4. LSC data structure

There are two areas to store the LSC related data in OTP. One is for LSC compressed data storage area which is consist of three tables and the other is for LSC control parameters storage area. These LSC data and control parameters are automatically loaded to the sensor after power on.

Each LSC Knot Point data stored in OTP is transformed as follows and common setting value of Global_OFFSET is used to the each color(R/Gr/Gb/B) and each table.

Knot_xx[9:0] = GLOBAL_OFFSET [9:0] + LSC_TABLEx_y_zz[7:0]

Note; GLOBAL_OFFSET[9:0] (addr : 460, 461),

LSC_TABLE1_x_yy[7:0] (addr : 208 to 459)

KNOT_FMT_Global (addr: 462) specify the floating-point position of Knot point data.

KNOT_FMT Global: floating-point position of Knot point data

0x0= u2.8

0x1= u3.7

0x2= u1.9

0x3= u4.6

For example: KNOT_FMT Global = 0x0

Knot point is an u2.8 number. E.g. 1101111111b means 3+127/ 256 in decimal.

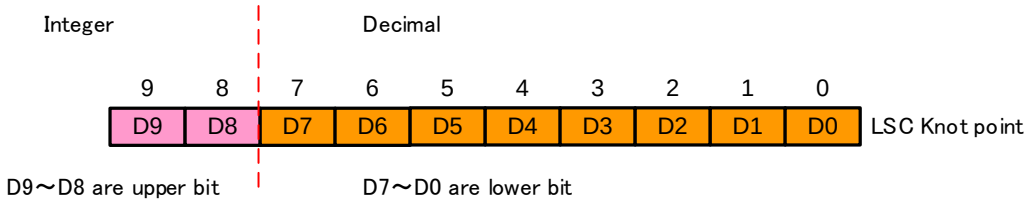

Figure 10-7 Knot point DATA structure (u2.8)

KNOT_ FMT Global [1:0] is used as common setting below,

KNOT_FMT_B[1:0] = KNOT_FMT Global [1:0]

KNOT_FMT_GB[1:0] = KNOT_FMT Global [1:0]

KNOT_FMT_GR[1:0] = KNOT_FMT Global [1:0]

KNOT_FMT_R[1:0] = KNOT_FMT Global [1:0]

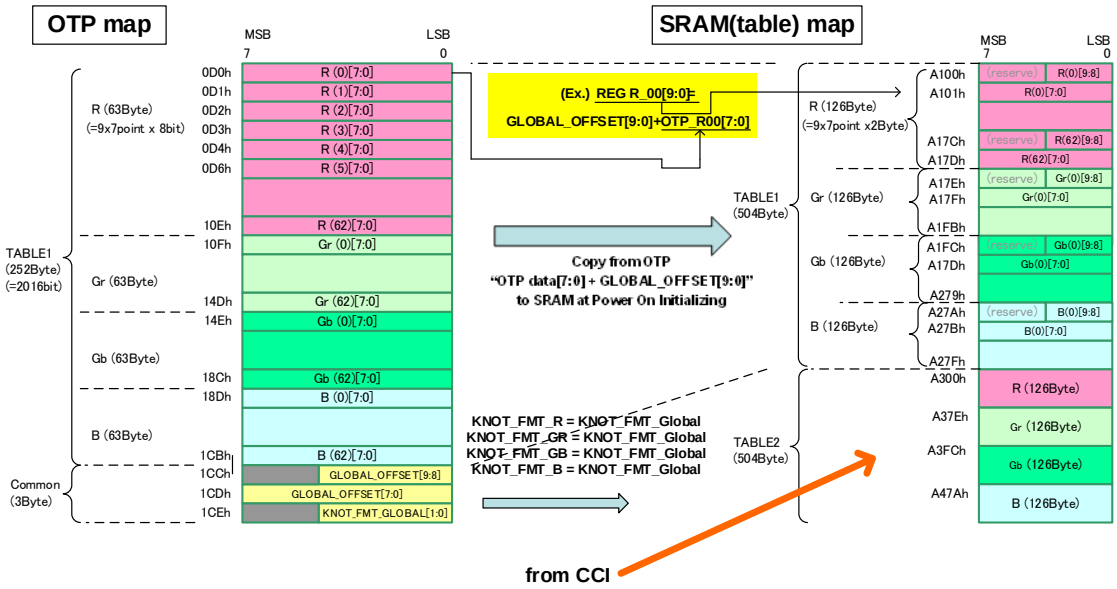

Figure 10-8 Knot table data loaded to sensor SRAM

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11. Register Map

See “IMX258 Register Map”.

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Appendix

A-1. Register update grouping

In 7.1 and 7.2, operation and setting method of each register is mainly discussed. In this Appendix chapter, on the other hand, registers are discussed as groups classified by update timing, setting reason, behavior of each register depending on various mode transition, Practical method of combing and updating various types of registers are main theme of this section.

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A-1.1 Procedure for mode transition setting

In this sensor, most of registers are grouped as follows from register update aspect.

Group A (Global setting only in Power On)

A-1: INCK and PLL setting

A-2: Global settings (basic configuration, Analog parameters and IQ parameters)

Group B (Operation mode settings for every mode change)

B-1: must be set in SW-standby (see Table 7-5)

B-2: corrupted frame related registers (see Table 7-3)

B-3: other most registers in address # of 0x0xxx and 0x3xx (except Group A/B-1/B-2/C)

Group C (special purpose registers)

C-2: must be set every time before change in streaming as work around (defined as needed).

C-3: Temperature sensor related registers (for detail see 9.1)

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A-1.2 Things to be considered for mode transitions

The following table shows various issues around mode transitions that have to be kept in mind.

As you can see in the following table, there are two methods in the capture mode transitions as

follows:

Via SW-standby transition

In this method, all mode change related registers are set during software standby state and is universal method of mode transition. The SW-standby is controlled by MODE_SEL.

On-the-fly transition

This mode transition is to instantly change the streaming without using SW-standby. This mode does not insert black out of image during mode transition if the condition of usage is matched. On-the-fly transition method usually has some constraints for usage, and so the usable case is limited. On-the-fly transition is controlled by GPH (Grouped parameter hold).

Table A-1 Summary of mode transition related issues

Capture mode transition method (Normal <-> Normal, Normal <-> HDR, HDR <-> HDR)		Use of GPH	Shutter lag	Corrupted frame output	Applicable register update Group	Register example *1
Via SW-standby	SW-standby mode transition	No	Long	No	All of A, B, C	IOP_SYS_DIV REQ_LINK_BIT_RATE_MBPS
	Fast SW-standby mode transition	No	Short	Yes	All of A, B, C	
On the fly	Normal mode transition	Yes	Long	Yes (depend on setting)	B-2, B-3	HDR_MODE Y_ADD_STA BINNING_TYPE
	Fast mode transition	Yes	Short	Yes	B-2, B-3, C-1	
	(No frame loss)	Yes	N/A	No	B-3	SING_DEF_CORR_EN DIG_CROP_X_OFFSET FLASH AE Full-Reso Type2 <-> HDR

Note *1: To know more about group classification of each register, see IMX258 Register Map or IMX258 Register Setting Table.

A-1.3 Mode transition procedure

In this paragraph, practical method of mode transition sequence and register settings are explained. From mode transition view point, sensor's states are divided into the following four stats; (1) Power ON, (2) Initial SW-standby, (3) Streaming and (4) SW-standby.

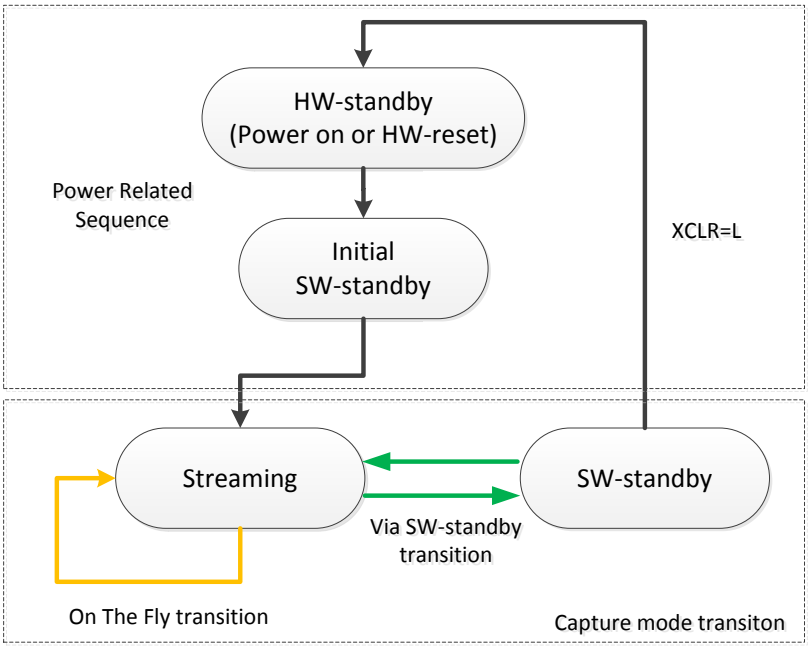

Figure A-1 Mode transitions

Purpose of the above figure is to simply describe the mode transitions from power on to streaming (Power related sequence) and between streaming (Capture mode transitions).

Table A-2 Mode transition procedures

Mode transition	Transition procedures
Power related sequence	Group A-1 → Group A-2, Group B(all) → MODE_SEL=1 Minimum setting*1: Difference from registers' default value of Group B
On The Fly transition	GPH=1 → Group B-2, B-3, Group C-1 → GPH=0 Example: From HDR capture mode of full resolution to Normal capture mode of full resolution. Minimum setting*1: Difference of register value between the transition modes.
Via SW-standby	MODE_SEL=0 → Group B-1, B-2, B-3, Group C-1 → MODE_SEL=1 Example: From Normal capture mode of full resolution to Normal capture mode of 2-binning with MIPI low data rate Minimum setting*1: Difference of register value between the transition modes.

Note *1 : Minimum setting can reduce CCI transfer time.

A-2. Embedded data lines

Contents and output sequence of Embedded Data Lines are shown as below.

Table A-3 Embedded line 0

Pixel #	Index	Register Name	EBD Byte	Meaning of EBD Byte
1			0x0A	EBD Format Code (0x0A = Simplified 2byte Tagged Data Format)
2			0xAA	Tag
3			0x00	Register Address MSB[15:8]
4			0xA5	Tag
5			0x05	Register Address LSB[7:0]
6			0x5A	Tag
7	0x0000	FRAME_COUNT	value	Valid data
8			0x5A	Tag
9	0x0001	PIXEL_ORDER	value	Valid data
10			0x55	Tag
11			0x07	Dummy data
12			0x5A	Tag
13	0x0002	DATA_PEDESTAL	value	Valid data
14			0x5A	Tag
15	0x0003	DATA_PEDESTAL	value	Valid data
16			0xAA	Tag
17			0x01	Register Address MSB[15:8]
18			0xA5	Tag
19			0x01	Register Address LSB[7:0]
20			0x5A	Tag
21	0x0004	IMAGE_ORIENTATION	value	Valid data
22			0xA5	Tag
23			0x10	Register Address LSB[7:0]
24			0x5A	Tag
25	0x0005	CSI_CHANNEL_IDENTIFIER	value	Valid data
26			0xA5	Tag
27			0x3A	Register Address LSB[7:0]
28			0x5A	Tag
29	0x0006	TEMP_SENSOR_OUTPUT	value	Valid data
30			0xAA	Tag
31			0x02	Register Address MSB[15:8]
32			0xA5	Tag
33			0x00	Register Address LSB[7:0]
34			0x5A	Tag
35	0x0007	FINE_INTEGRATION_TIME	value	Valid data
36			0x5A	Tag
37	0x0008	FINE_INTEGRATION_TIME	value	Valid data
38			0x5A	Tag
39	0x0009	COARSE_INTEGRATION_TIME	value	Valid data
40			0x5A	Tag
41	0x000A	COARSE_INTEGRATION_TIME	value	Valid data
42			0x5A	Tag
43	0x000B	ANALOGUE_GAIN_CODE_GLOBAL	value	Valid data
44			0x5A	Tag
45	0x000C	ANALOGUE_GAIN_CODE_GLOBAL	value	Valid data

46			0xA5	Tag
47			0x0E	Register Address LSB[7:0]
48			0x5A	Tag
49	0x000D	DIGITAL_GAIN_GREENR	value	Valid data
50			0x5A	Tag
51	0x000E	DIGITAL_GAIN_GREENR	value	Valid data
52			0x5A	Tag
53	0x000F	DIGITAL_GAIN_RED	value	Valid data
54			0x5A	Tag
55	0x0010	DIGITAL_GAIN_RED	value	Valid data
56			0x5A	Tag
57	0x0011	DIGITAL_GAIN_BLUE	value	Valid data
58			0x5A	Tag
59	0x0012	DIGITAL_GAIN_BLUE	value	Valid data
60			0x5A	Tag
61	0x0013	DIGITAL_GAIN_GREENB	value	Valid data
62			0x5A	Tag
63	0x0014	DIGITAL_GAIN_GREENB	value	Valid data
64			0x5A	Tag
65	0x0015	SHORT_ANALOGUE_GAIN_GLOBAL	value	Valid data
66			0x5A	Tag
67	0x0016	SHORT_ANALOGUE_GAIN_GLOBAL	value	Valid data
68			0xA5	Tag
69			0x20	Register Address LSB[7:0]
70			0x5A	Tag
71	0x0017	HDR_MODE	value	Valid data
72			0x5A	Tag
73	0x0018	HDR_RESOLUTION_REDUCTION	value	Valid data
74			0x5A	Tag
75	0x0019	EXPOSURE_RATIO	value	Valid data
76			0x55	Tag
77			0x07	Dummy data
78			0x5A	Tag
79	0x001A	DIRECT_SHORT_INTEGRATION_TIME	value	Valid data
80			0x5A	Tag
81	0x001B	DIRECT_SHORT_INTEGRATION_TIME	value	Valid data
82			0xAA	Tag
83			0x03	Register Address MSB[15:8]
84			0xA5	Tag
85			0x00	Register Address LSB[7:0]
86			0x5A	Tag
87	0x001C	IVT_PIX_CLK_DIV	value	Valid data
88			0x5A	Tag
89	0x001D	IVT_PIX_CLK_DIV	value	Valid data
90			0x5A	Tag
91	0x001E	IVT_SYS_CLK_DIV	value	Valid data
92			0x5A	Tag
93	0x001F	IVT_SYS_CLK_DIV	value	Valid data
94			0x5A	Tag
95	0x0020	IVT_PRE_PLL_CLK_DIV	value	Valid data
96			0x5A	Tag
97	0x0021	IVT_PRE_PLL_CLK_DIV	value	Valid data
98			0x5A	Tag
99	0x0022	IVT_PLL_MULTIPLIER	value	Valid data
100			0x5A	Tag

101	0x0023	IVT_PLL_MULTIPLIER	value	Valid data
102			0x5A	Tag
103	0x0024	IOP_PIX_CLK_DIV	value	Valid data
104			0x5A	Tag
105	0x0025	IOP_PIX_CLK_DIV	value	Valid data
106			0x5A	Tag
107	0x0026	IOP_SYS_CLK_DIV	value	Valid data
108			0x5A	Tag
109	0x0027	IOP_SYS_CLK_DIV	value	Valid data
110			0x5A	Tag
111	0x0028	IOP_PRE_PLL_CLK_DIV	value	Valid data
112			0x5A	Tag
113	0x0029	IOP_PRE_PLL_CLK_DIV	value	Valid data
114			0x5A	Tag
115	0x002A	IOP_PLL_MULTIPLIER	value	Valid data
116			0x5A	Tag
117	0x002B	IOP_PLL_MULTIPLIER	value	Valid data
118			0x5A	Tag
119	0x002C	PLL_MULTI_DRIVE	value	Valid data
120			0xA5	Tag
121			0x40	Register Address LSB[7:0]
122			0x5A	Tag
123	0x002D	FRAME_LENGTH_LINES	value	Valid data
124			0x5A	Tag
125	0x002E	FRAME_LENGTH_LINES	value	Valid data
126			0x5A	Tag
127	0x002F	LINE_LENGTH_PCK	value	Valid data
128			0x5A	Tag
129	0x0030	LINE_LENGTH_PCK	value	Valid data
130			0x5A	Tag
131	0x0031	X_ADDR_START	value	Valid data
132			0x5A	Tag
133	0x0032	X_ADDR_START	value	Valid data
134			0x5A	Tag
135	0x0033	Y_ADDR_START	value	Valid data
136			0x5A	Tag
137	0x0034	Y_ADDR_START	value	Valid data
138			0x5A	Tag
139	0x0035	X_ADDR_END	value	Valid data
140			0x5A	Tag
141	0x0036	X_ADDR_END	value	Valid data
142			0x5A	Tag
143	0x0037	Y_ADDR_END	value	Valid data
144			0x5A	Tag
145	0x0038	Y_ADDR_END	value	Valid data
146			0x5A	Tag
147	0x0039	X_OUTPUT_SIZE	value	Valid data
148			0x5A	Tag
149	0x003A	X_OUTPUT_SIZE	value	Valid data
150			0x5A	Tag
151	0x003B	Y_OUTPUT_SIZE	value	Valid data
152			0x5A	Tag
153	0x003C	Y_OUTPUT_SIZE	value	Valid data
154			0xA5	Tag
155			0x80	Register Address LSB[7:0]

156			0x5A	Tag
157	0x003D	X_EVEN_INC	value	Valid data
158			0x5A	Tag
159	0x003E	X_EVEN_INC	value	Valid data
160			0x5A	Tag
161	0x003F	X_ODD_INC	value	Valid data
162			0x5A	Tag
163	0x0040	X_ODD_INC	value	Valid data
164			0x5A	Tag
165	0x0041	Y_EVEN_INC	value	Valid data
166			0x5A	Tag
167	0x0042	Y_EVEN_INC	value	Valid data
168			0x5A	Tag
169	0x0043	Y_ODD_INC	value	Valid data
170			0x5A	Tag
170	0x0044	Y_ODD_INC	value	Valid data
171			0x07	End of Data

Table A-4 Embedded line 1

Pixel #	Index	Register Name	EBD Byte	Meaning of EBD Byte
0			0x0A	EBD Format Code (0x0A = Simplified 2byte Tagged Data Format)
1			0xAA	Tag
2			0x04	Register Address MSB[15:8]
3			0xA5	Tag
4			0x00	Register Address LSB[7:0]
5			0x5A	Tag
6	0x0001	SCALE_MODE	value	Valid data
7			0x5A	Tag
8	0x0002	SCALE_MODE	value	Valid data
9			0xA5	Tag
10			0x04	Register Address LSB[7:0]
11			0x5A	Tag
12	0x0003	SCALE_M	value	Valid data
13			0x5A	Tag
14	0x0004	SCALE_M	value	Valid data
15			0xA5	Tag
16			0x08	Register Address LSB[7:0]
17			0x5A	Tag
18	0x0005	DIGITAL_CROP_X_OFFSET	value	Valid data
19			0x5A	Tag
20	0x0006	DIGITAL_CROP_X_OFFSET	value	Valid data
21			0x5A	Tag
22	0x0007	DIGITAL_CROP_Y_OFFSET	value	Valid data
23			0x5A	Tag
24	0x0008	DIGITAL_CROP_Y_OFFSET	value	Valid data
25			0x5A	Tag
26	0x0009	DIGITAL_CROP_IMAGE_WIDTH	value	Valid data
27			0x5A	Tag
28	0x000A	DIGITAL_CROP_IMAGE_WIDTH	value	Valid data
29			0x5A	Tag
30	0x000B	DIGITAL_CROP_IMAGE_HEIGHT	value	Valid data
31			0x5A	Tag
32	0x000C	DIGITAL_CROP_IMAGE_HEIGHT	value	Valid data
33			0xAA	Tag
34			0x09	Register Address MSB[15:8]
35			0xA5	Tag
36			0x00	Register Address LSB[7:0]
37			0x5A	Tag
38	0x000D	BINNING_MODE	value	Valid data
39			0x5A	Tag
40	0x000E	BINNING_TYPE	value	Valid data
41			0x5A	Tag
42	0x000F	BINNING_WEIGHTING	value	Valid data
43			0xAA	Tag
44			0x0B	Register Address MSB[15:8]
45			0xA5	Tag
46			0x00	Register Address LSB[7:0]
47			0x5A	Tag
48	0x0010	SHADING_CORRECTION_ENABLE	value	Valid data

49			0x55	Tag
50			0x07	Dummy data
51			0x5A	Tag
52	0x0011	GREEN_IMBALANCE_FILTER_ENABLE	value	Valid data
53			0x5A	Tag
54	0x0012	GREEN_IMBALANCE_FILTER_WEIGHT	value	Valid data
55			0x5A	Tag
56	0x0013	BLACK_LEVEL_CORRECTION_ENABLE	value	Valid data
57			0x5A	Tag
58	0x0014	MAPPED_COUPLET_CORRECT_ENABLE	value	Valid data
59			0x5A	Tag
60	0x0015	SINGLE_DEFECT_CORRECT_ENABLE	value	Valid data
61			0xA5	Tag
62			0x0A	Register Address LSB[7:0]
63			0x55	Tag
64			0x07	Dummy data
65			0xA5	Tag
66			0x8E	Register Address LSB[7:0]
67			0x5A	Tag
68	0x0016	ABSOLUTE_GAIN_GREENR	value	Valid data
69			0x5A	Tag
70	0x0017	ABSOLUTE_GAIN_GREENR	value	Valid data
71			0x5A	Tag
72	0x0018	ABSOLUTE_GAIN_RED	value	Valid data
73			0x5A	Tag
74	0x0019	ABSOLUTE_GAIN_RED	value	Valid data
75			0x5A	Tag
76	0x001A	ABSOLUTE_GAIN_BLUE	value	Valid data
77			0x5A	Tag
78	0x001B	ABSOLUTE_GAIN_BLUE	value	Valid data
79			0x5A	Tag
80	0x001C	ABSOLUTE_GAIN_GREENB	value	Valid data
81			0x5A	Tag
82	0x001D	ABSOLUTE_GAIN_GREENB	value	Valid data
83			0xAA	Tag
84			0x0C	Register Address MSB[15:8]
85			0xA5	Tag
86			0x18	Register Address LSB[7:0]
87			0x5A	Tag
88	0x001E	TFLASH_STROBE_WIDTH_HIGH_RS_CTRL	value	Valid data
89			0x5A	Tag
90	0x001F	TFLASH_STROBE_WIDTH_HIGH_RS_CTRL	value	Valid data
91			0x55	Tag
92			0x07	Dummy data
93			0x5A	Tag
94	0x0020	FLASH_TRIGGER_RS	value	Valid data
95			0x5A	Tag
96	0x0021	FLASH_STATUS	value	Valid data
97			0xA5	Tag
98			0x24	Register Address LSB[7:0]
99			0x5A	Tag
100	0x0022	SA_STROBE_TRIGGER	value	Valid data
101			0x5A	Tag
102	0x0023	SPECIAL_ACTUATOR_STATUS	value	Valid data
103			0x5A	Tag

104	0x0024	TFLASH_STROBE_WIDTH2_HIGH_RS_CTRL	value	Valid data
105			0x5A	Tag
106	0x0025	TFLASH_STROBE_WIDTH2_HIGH_RS_CTRL	value	Valid data
107			0x5A	Tag
108	0x0026	TFLASH_STROBE_WIDTH_LOW_RS_CTRL	value	Valid data
109			0x5A	Tag
110	0x0027	TFLASH_STROBE_WIDTH_LOW_RS_CTRL	value	Valid data
111			0x5A	Tag
112	0x0028	TFLASH_STROBE_COUNT_RS_CTRL	value	Valid data
113			0xAA	Tag
114			0x30	Register Address MSB[15:8]
115			0xA5	Tag
116			0x25	Register Address LSB[7:0]
117			0x5A	Tag
118			value	Dummy data
119			0x5A	Tag
120	0x0029	LSC BLEND COEF STATUS	value	Valid data
121			0xA5	Tag
122			0x38	Register Address LSB[7:0]
123			0x5A	Tag
124	0x002A	SCALE_MODE_EXT	value	Valid data
125			0x55	Tag
126			0x07	Dummy data
127			0x5A	Tag
128	0x002B	SCALE_M_EXT	value	Valid data
129			0x5A	Tag
130	0x002C	SCALE_M_EXT	value	Valid data
131			0x07	End of Data