

Guest Editorial

IEEE International Integrated Reliability Workshop (IIRW) 2019

THE IEEE International Integrated Reliability Workshop (IIRW) is a unique event that takes place every year at the beautiful Fallen Leaf Lake, in Tahoe, California. This workshop brings together reliability engineers and researchers from around the world, to exchange ideas over four days in a relaxed, friendly, and informal atmosphere. The workshop focuses on the recent advances in research concerning semiconductor device reliability and its different challenges. Topics include front-end-of-line reliability issues (bias temperature instability, hot-carrier degradation, time dependent dielectric breakdown), back-end-of-line/middle-of-line degradation effects (electromigration, stress migration, time dependent dielectric breakdown) as well as memory reliability, chip to package interaction, degradation effects in wide-bandgap-materials and high-voltage devices, and many others.

In 2019, IIRW hosted the second Reliability Experts Forum where distinguished reliability experts around the world gathered in a day-long discussion to exchange knowledge and ideas in the field of memory reliability. This event included three panels which covered (*i*) conventional memory reliability, (*ii*) reliability of emerging memory, and (*iii*) emerging memory reliability and neuromorphic application. The first panel was moderated by Baozhen Li from IBM and the discussion was initiated by Dr. Barry O’Sullivan (*imec*), who presented a summary about DRAM peripheral device reliability, and then continued by a discussion focused on reliability of 3D NAND conducted by Cristian Zambelli (Univ. Ferrara). The second panel was headed by Dr. Andrew Kim from Intel: Prof. Luca Larcher (Advanced Materials) opened the discussion with a summary on modeling of degradation issues in RRAM; the discussion was continued by a presentation of characterization techniques for RRAM reliability given by Prof. Kin Leong Pey (SUTD). The next field covered by this panel was MRAM reliability, where Dr. Richard Southwick (IBM) conducted the debates, followed by a presentation by Dr. Kin P. Cheung (NIST) devoted to polymer-based glassy electret RAM. Moderated by Dr. Andreas Kerber, the third panel was opened with a summary of emerging memory reliability challenges presented by Dr. Chandra Mouli (Micron) and then Dr. Eduard Cartier (IBM) conducted a discussion devoted to reliability requirements for artificial intelligence which was followed by Dr. Gennadi Bersuker (Aerospace Corporation),

who shared his knowledge and ideas in the field of RRAM in neuromorphic applications. Finally, this panel was ended by Prof. Subramaniam Iyer (UCLA) summarizing issues and possible solutions related to charge-trap memory in advanced nodes and neuromorphic applications. All three panels stimulated very fruitful discussions with the audience and brought up the points of consensus and differences in every topic, which helped provide many clarifications to different concepts.

The regular technical program included five tutorials, nine invited papers, and twenty-nine regular papers presented in oral and poster sessions. This special issue of IEEE TDMR includes seven most impactful papers covering different aspects of FEOL, BEOL, and memory reliability.

In the first paper, Kerber and coauthors study the impact of FEOL degradation phenomena – bias temperature instability (BTI), hot-carrier degradation (HCD), time dependent dielectric breakdown (TDDB), and self-heating – on performance of digital CMOS circuits in the GHz regime. To achieve this goal, the authors focus on reliability characterization of ring-oscillators representing a basic digital circuit. The impacts of all aforementioned degradation modes were thoroughly analyzed, and this analysis allowed the authors to correlate degradation of discrete transistors with circuit aging.

The second paper by Waltl presents a very extensive summary of how ultra-low noise can be used to characterize defect properties in scaled transistors. For this characterization, a new tool named “defect probing instrument” was developed and applied to study defects over a wide class of transistors based on Si, SiC, and 2D materials. This work discusses in great detail the experimental methodology as well as defect properties.

In the third paper Stampfer *et al.*, employ large transistor arrays to extract and stochastically analyze parameters of defects involved in BTI and random telegraph noise. Main focus is put on statistical processing of threshold voltage shifts induced by charge capture and emission events by/from discrete defects. Acquired experimental results are augmented by TCAD modeling and this strategy allows the authors to predict device lifetime in the operating regime with good accuracy.

In the fourth paper O’Sullivan *et al.* study negative bias temperature instability (NBTI) in high voltage logic for memory devices. They correlate peculiarities of NBTI aging in these devices with the parameters of the high-k/metal gate stack technology and provide feedback which should help optimize device technology to mitigate NBTI.

The fifth paper of this issue provides an analysis of the impact of the geometrical parameters of the FinFET transistor (such as the fin width and its height) on negative/positive bias instability (N/PBTI). These studies are focused on kinetics of trapping of charge carriers by border traps in the high-k gate stack. The authors report improved NBTI reliability in devices with taller fins; PBTI reveals a similar trend but its temperature dependence was shown to be much weaker than that of NBTI.

In the sixth paper Zanotti and co-author model reliability of IMPLY-based LIM circuits. To achieve this goal, they use a compact model for RRAM which is based on physical principles and covers non-idealities at both device and circuit levels. Extensive simulations conducted in this work allow one to develop strategies to optimize circuit performance using compact models.

The seventh and last paper demonstrates an accurate model which allows one to analyze the void risk in vacuum molded underfill processes of real flip-chip, package-on-package devices and large PCN strips. Thorough and comprehensive

validation of the model proves that this simulation approach is a powerful tool for studies of the potential void risk.

In conclusion, we would like to thank all the authors for their efforts expanding their original work beyond what was included in IIRW 2019 proceedings and the reviewers for their valuable reviews and feedback to the authors. I would also like to express my appreciation to Dr. Edmundo A. Gutiérrez-D, the Editor-in-Chief of IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY, for supporting this initiative as well as Ms. Rosemary Schreiber for her great help. Finally, we would like to express our gratitude for Prof. Francesco Maria Puglisi and Prof. Cristian Zambelli for their help in editing and shaping up this special section.

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Stanislav Tyaginov was born in Saint Petersburg, Russia, in 1978. He received the M.Sc. degree in 2002 and the Ph.D. degree in 2006. He led the Physics-Based Hot-Carrier Degradation Model Development Group, Technical University Vienna and currently is a Marie Curie Postdoctoral Fellow with *imec*. He has authored/coauthored more than 100 papers in peer-reviewed scientific journal as well as in conference proceedings. His current research interests include device simulation, modeling of HCD, BTI, and TDDB in transistors based on Si and SiC as well as tunneling phenomena in MOS devices. He serves as a Technical Program Committee Member with IIRW and IRPS.



Zakariae Chbili received the B.S. degree in electrical engineering from Sidi Mohamed Ben Abdellah University, Fes, Morocco, in 2007, the M.S. degree in electrical engineering from the Institut National des Sciences Appliquées, Toulouse, France, in 2008, and the Ph.D. degree in electrical and computer engineering from George Mason University. He was with the National Institute of Standard and Technology, Gaithersburg, MD, USA, as a Guest Researcher from 2010 to 2015 and with GLOBALFOUNDRIES, Inc., from 2015 to 2019, where he managed the Northeast Reliability Labs. He is currently with the Non-Volatile Memory Solutions Group, Intel Corporation, Folsom, CA, USA, as a Quality Reliability Research and Development Engineer. His research interests include the reliability of emerging memory devices, reliability of advanced nodes, physics of degradation and breakdown in ultrathin gate oxides, and FinFET self-heating. He served as the General Chairman of IIRW 2019.