LEADING AT THE EDGE

TECHNOLOGY AND MANUFACTURING DAY

14 NM TECHNOLOGY LEADERSHIP

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DISCLOSURES

Intel Technology and Manufacturing Day 2017 occurs during Intel's "Quiet Period," before Intel announces its 2017 first quarter financial and operating results. Therefore, presenters will not be addressing first quarter information during this year's program.

Statements in this presentation that refer to forecasts, future plans and expectations are forward-looking statements that involve a number of risks and uncertainties. Words such as "anticipates," "expects," "intends," "goals," "plans," "believes," "seeks," "estimates," "continues," "may," "will," "would," "should," "could," and variations of such words and similar expressions are intended to identify such forward-looking statements. Statements that refer to or are based on projections, uncertain events or assumptions also identify forward-looking statements. Such statements are based on management's expectations as of March 28, 2017, and involve many risks and uncertainties that could cause actual results to differ materially from those expressed or implied in these forward-looking statements. Important factors that could cause actual results to differ materially from the company's expectations are set forth in Intel's earnings release dated January 26, 2017, which is included as an exhibit to Intel's Form 8-K furnished to the SEC on such date. Additional information regarding these and other factors that could affect Intel's results is included in Intel's SEC filings, including the company's most recent reports on Forms 10-K, 10-Q and 8-K reports may be obtained by visiting our Investor Relations website at www.intc.com or the SEC's website at www.sec.gov.

KEY MESSAGES

- Intel’s 14 nm technology is ~1.3x denser than others’ available “20 nm” and “16/14 nm” technologies.
- Intel’s 14 nm technology is expected to be similar density to others’ “10 nm” technology but ~3 years ahead.
- Intel’s 14 nm transistors have >20% performance leadership compared to others’ available technology.
- At the 14 nm technology node, Intel has developed all of the key enablers to hyper scale features and deliver significant CPT benefits.

Source: Amalgamation of analyst data and Intel analysis, based upon current expectations and available information.

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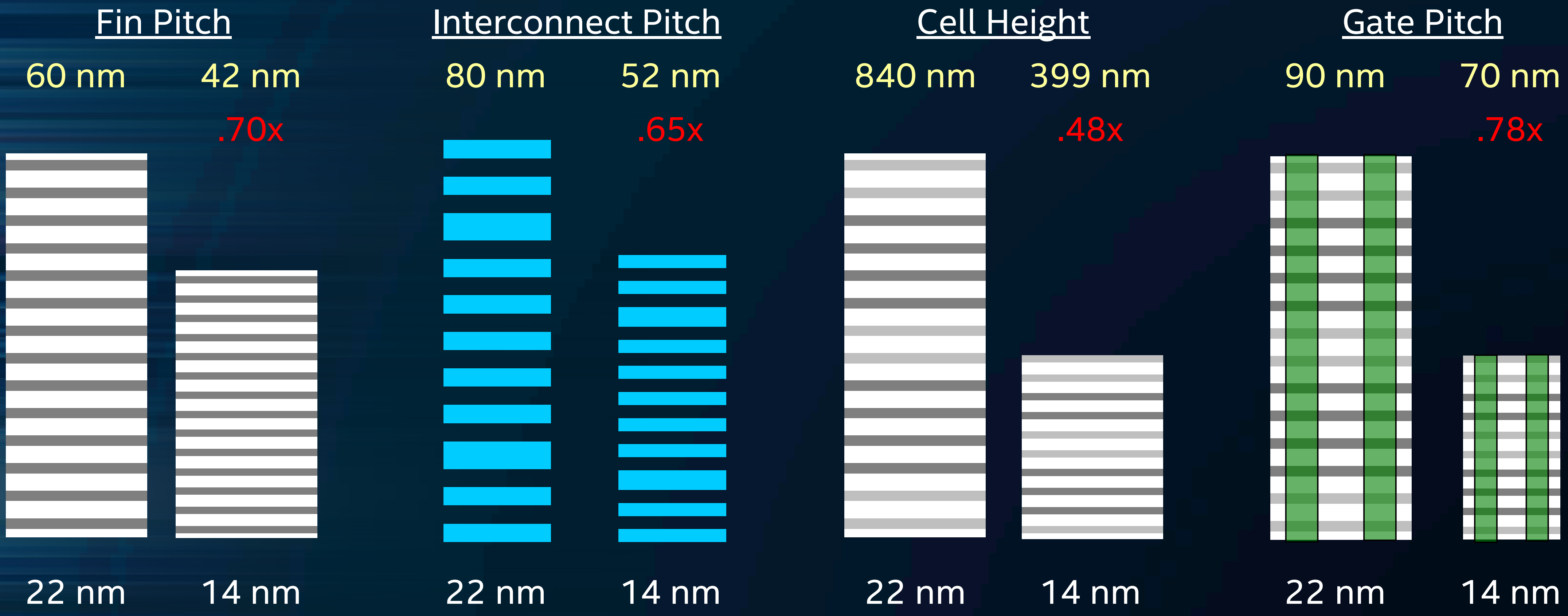
14 NM HYPER SCALING FEATURES

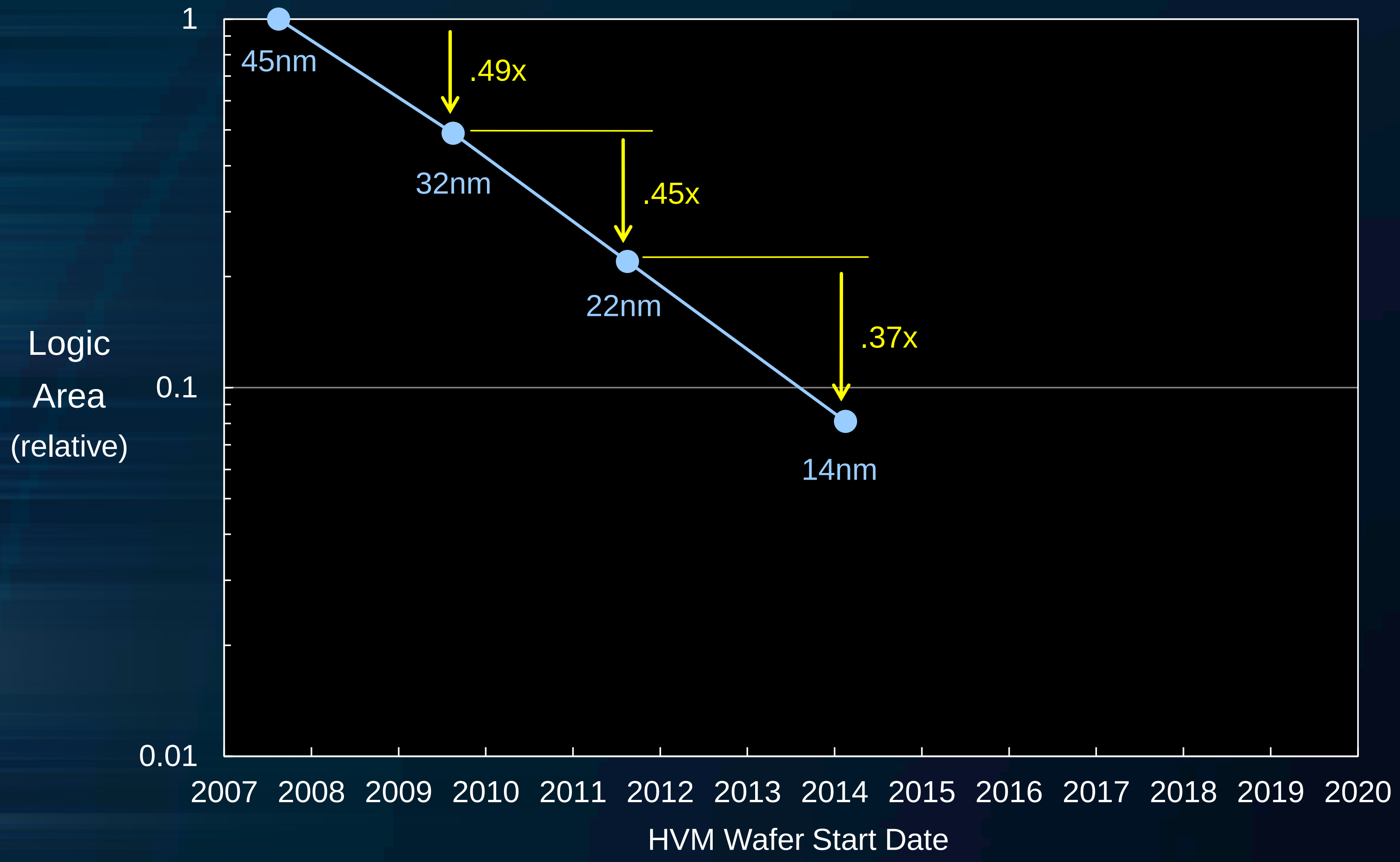


	Fin Pitch		Interconnect Pitch		Cell Height		Gate Pitch	
	60 nm	42 nm	80 nm	52 nm	840 nm	399 nm	90 nm	70 nm
		.70x		.65x		.48x		.78x
	22 nm	14 nm	22 nm	14 nm	22 nm	14 nm	22 nm	14 nm

14 nm uses aggressive feature scaling to deliver unprecedented 0.37x logic cell area scaling.

Source: Amalgamation of analyst data and Intel analysis, based upon current expectations and available information.

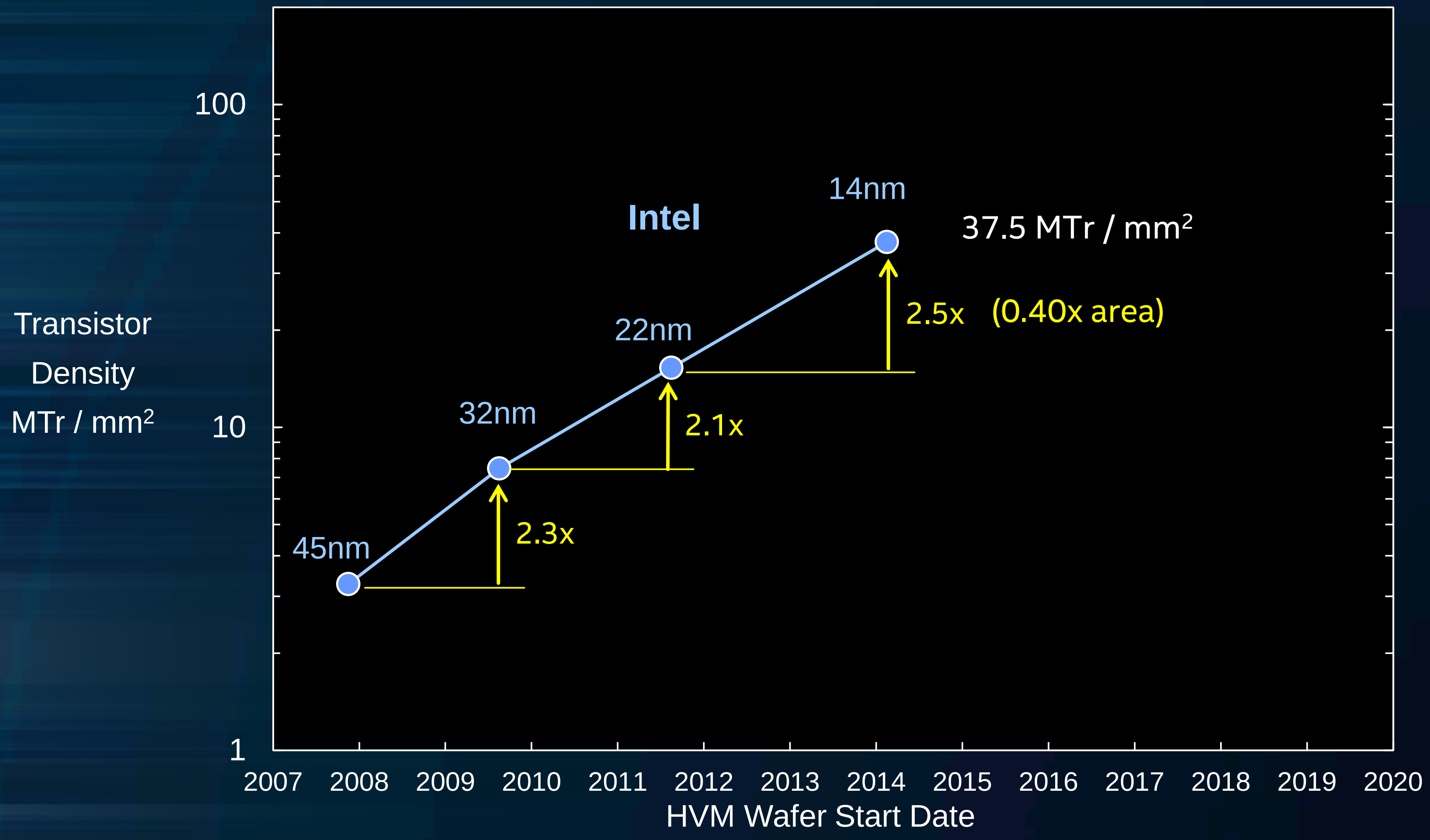
LOGIC AREA SCALING



Hyper scaling of 14 nm features provides better-than-normal 0.37x logic area scaling.

Source: Amalgamation of analyst data and Intel analysis, based upon current expectations and available information.

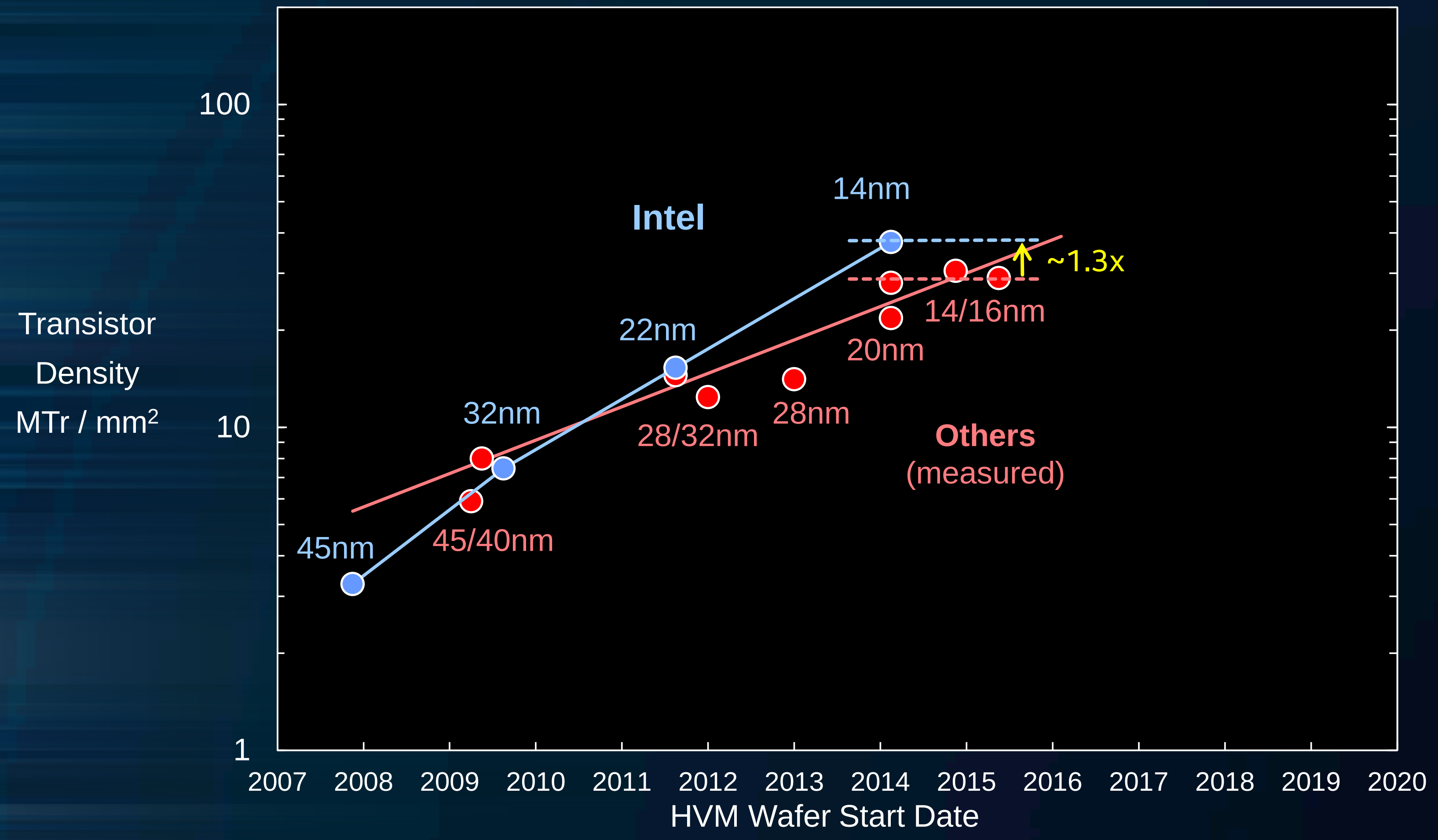
LOGIC TRANSISTOR DENSITY



Using NAND+SFF metric, 14 nm provides better-than-normal logic transistor density improvement.

Source: Amalgamation of analyst data and Intel analysis, based upon current expectations and available information.

LOGIC TRANSISTOR DENSITY



Intel's 14 nm technology is ~1.3x denser than others' "14/16/20 nm" technologies.

Source: Amalgamation of analyst data and Intel analysis, based upon current expectations and available information.

14NM TECHNOLOGY FEATURES

	Intel 14 nm	Other “20 nm”
Gate Pitch	70 nm	90 nm (1.3x)
Logic cell height	399 nm	576 nm (1.4x)
Fin Pitch	42 nm	Planar
Min Metal Pitch	52 nm	64 nm
Transistor density (MTr/mm^2)	**37.5 (1.34x)**	**28.0 (1x)**

Introduced at similar time.

Intel 14 nm is ahead of others’ “20 nm” technology on every density metric.

Source: Amalgamation of analyst data and Intel analysis, based upon current expectations and available information.

14NM TECHNOLOGY FEATURES

	Intel 14 nm	Other “20 nm”	Other “16 nm”	Other “14 nm”
Gate Pitch	70 nm	90 nm (1.3x)	90 nm (1.3x)	78 nm (1.1x)
Logic cell height	399 nm	576 nm (1.4x)	480 nm (1.2x)	576 nm (1.4x)
Fin Pitch	42 nm	Planar	48 nm (1.1x)	48 nm (1.1x)
Min Metal Pitch	52 nm	64 nm	64 nm	64 nm
Transistor density (MTr/mm²)	**37.5 (1.34x)**	**28.0 (1x)**	**29.0 (1.04x)**	**30.5 (1.09x)**

Others introduced ~1 year later.

Intel 14 nm is ahead of others’ “14/16 nm” technology on every density metric.

Source: Amalgamation of analyst data and Intel analysis, based upon current expectations and available information.

KEY MESSAGES

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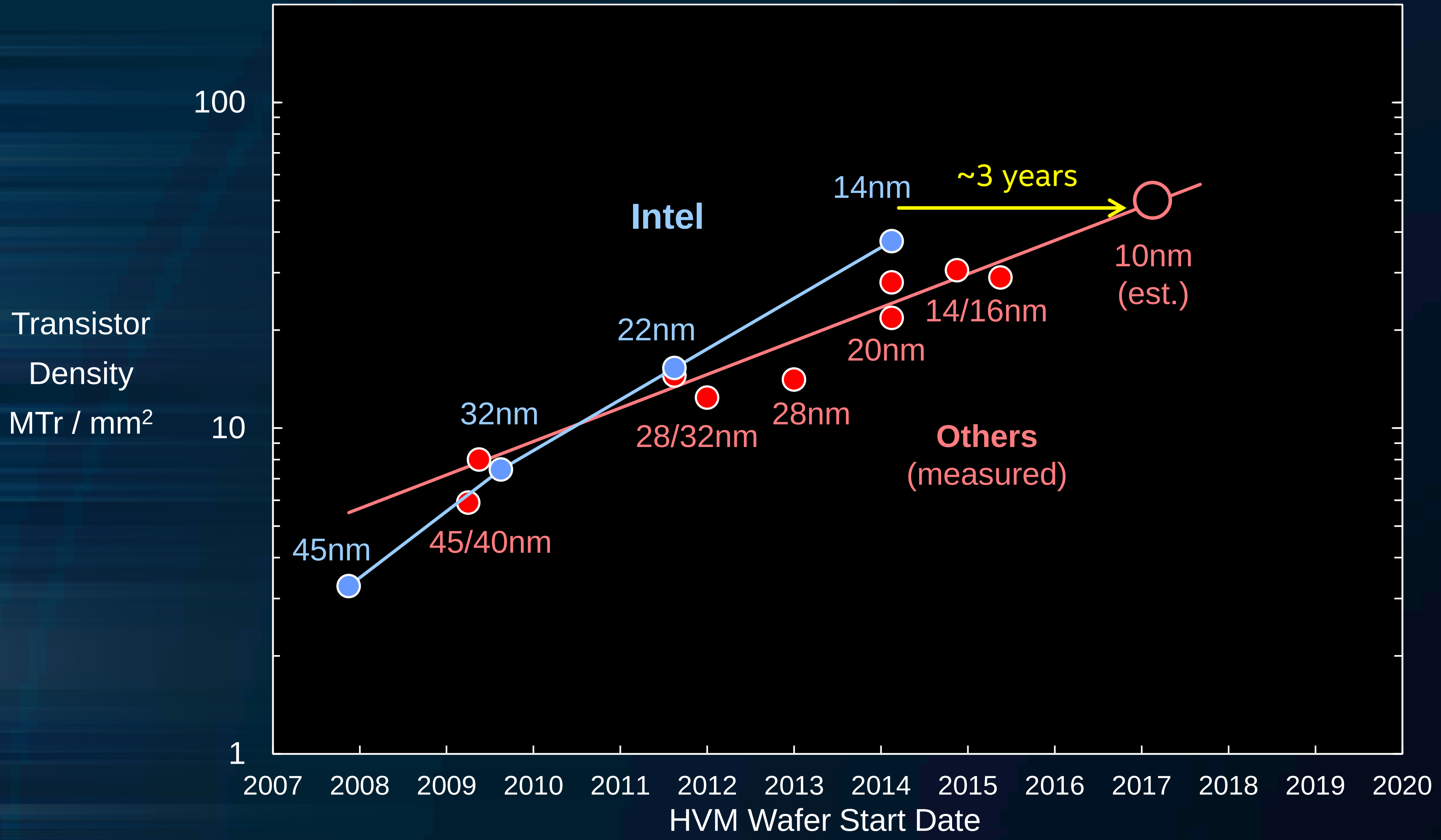
- At the 14 nm technology node, Intel has developed all of the key enablers to hyper scale features and deliver significant CPT benefits.

Source: Amalgamation of analyst data and Intel analysis, based upon current expectations and available information.

LOGIC TRANSISTOR DENSITY



Others' "10 nm" technologies expected to have similar density to Intel 14 nm, but ~3 years later.

Source: Amalgamation of analyst data and Intel analysis. 2017-2020 are estimates based upon current expectations and available information.

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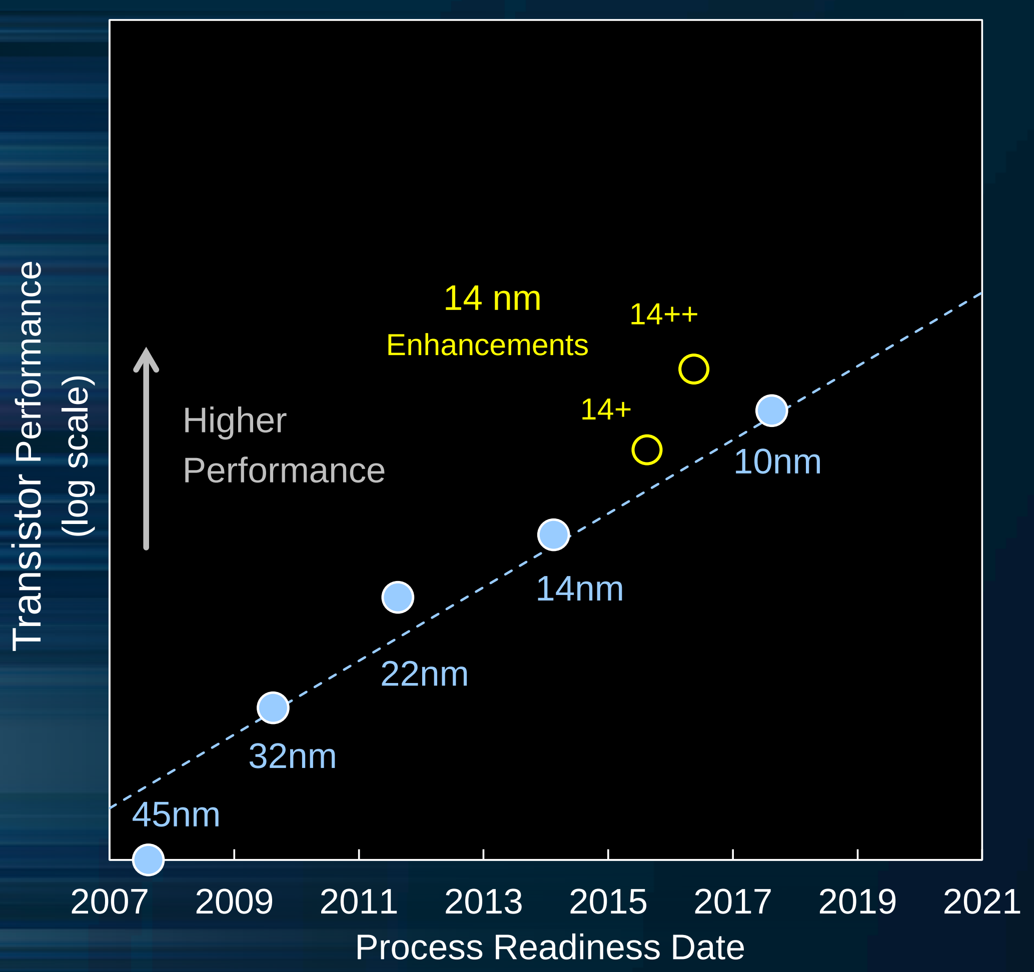
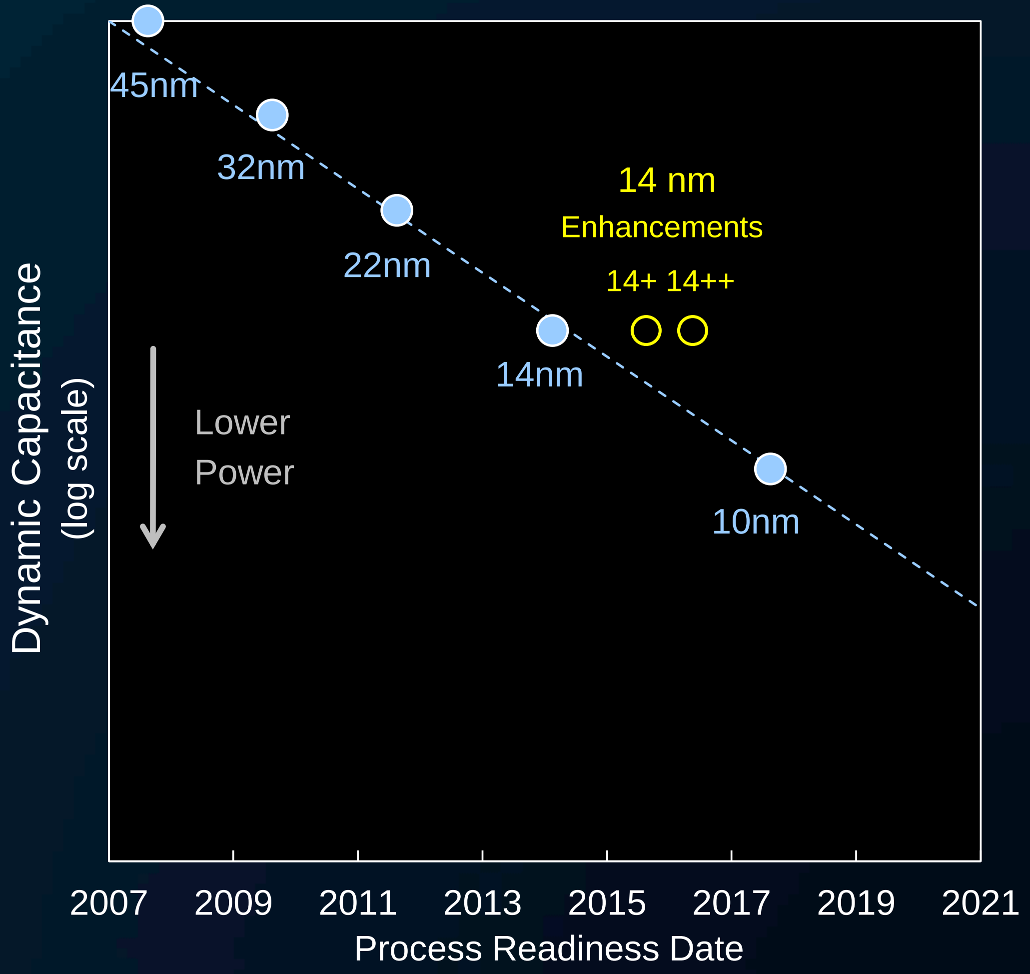
TECHNOLOGY ENHANCEMENTS

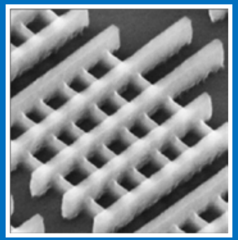




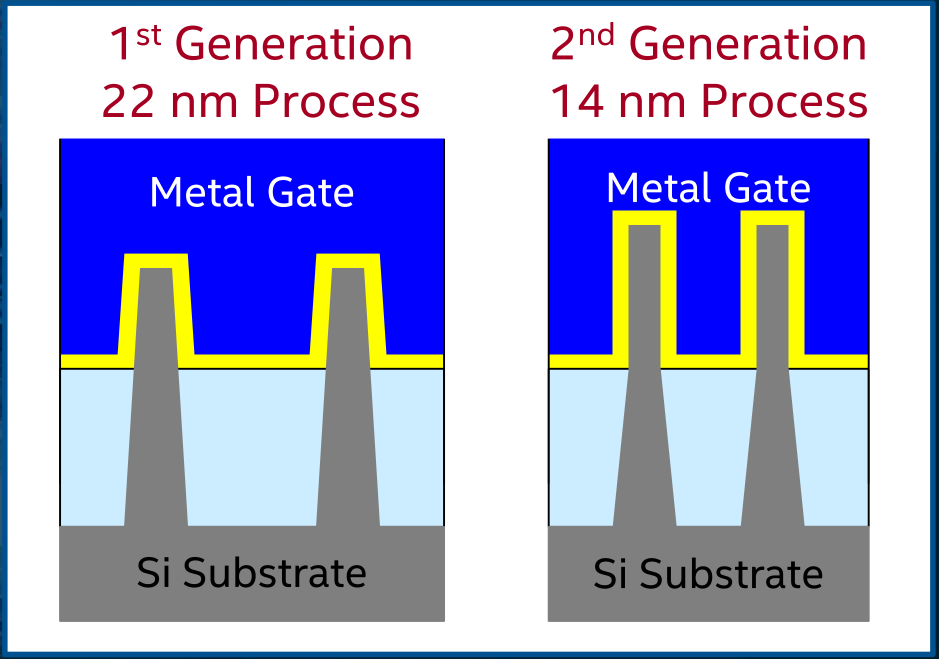
14+ and 14++ enhancements improve performance without increasing capacitance (active power).

Source: Amalgamation of analyst data and Intel analysis. 2017-2021 are estimates based upon current expectations and available information.

INTEL INNOVATION LEADERSHIP FINFETS



FINFET
TRANSISTOR

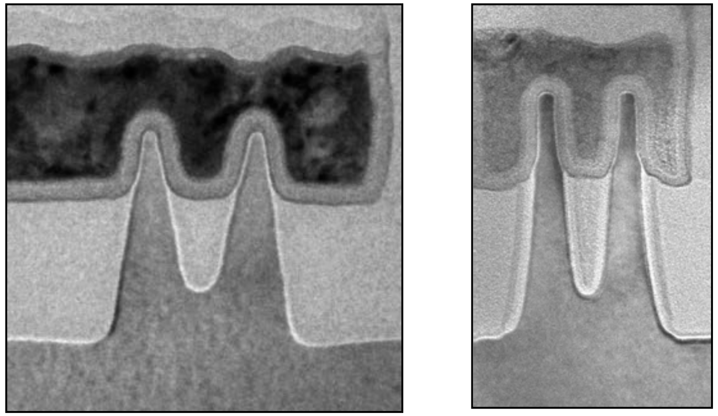


1st Generation
22 nm Process

2nd Generation
14 nm Process

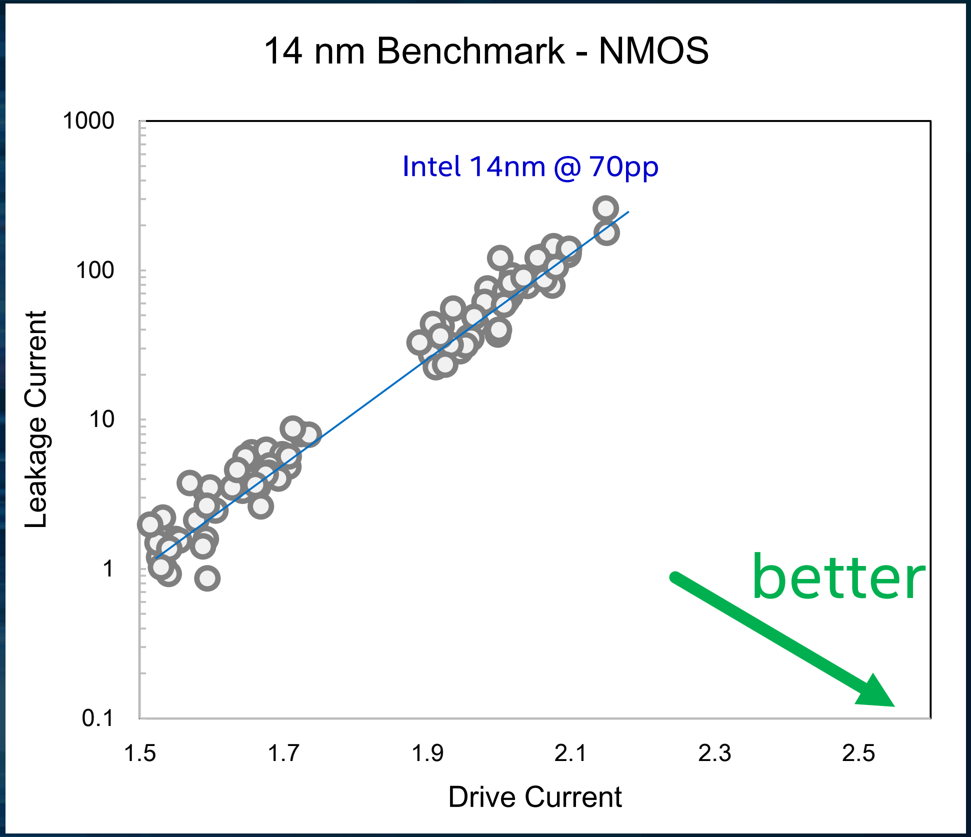
1st Generation
22 nm Process

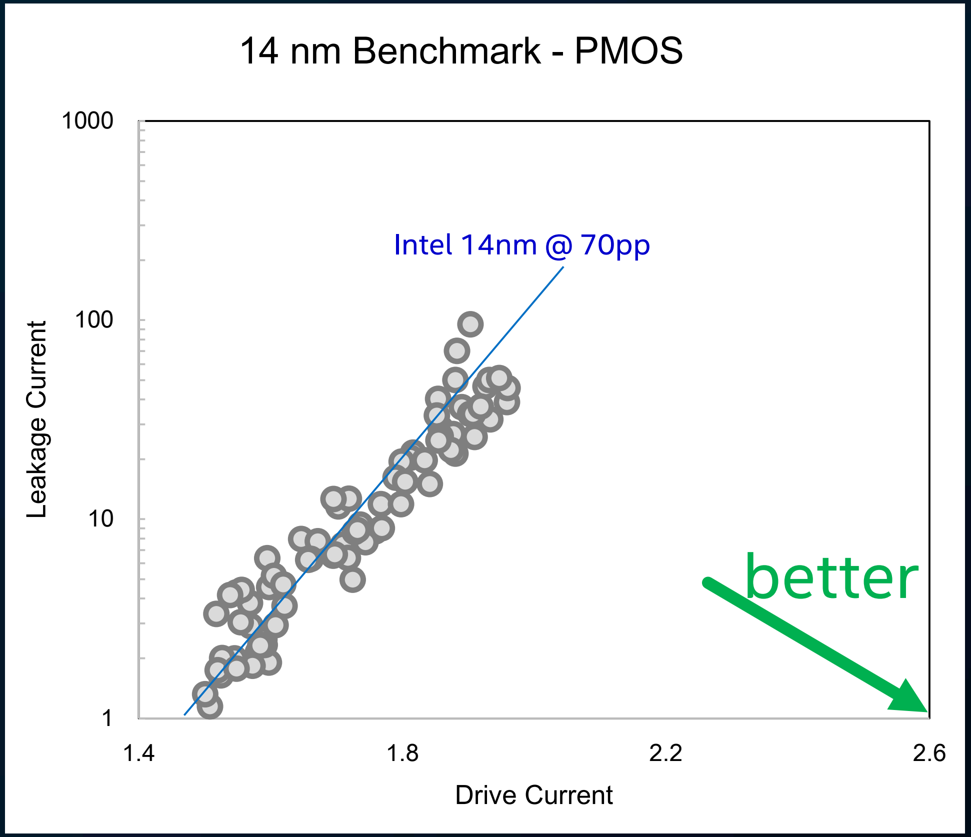
2nd Generation
14 nm Process



FinFET transistors were first introduced at 22 nm and enhanced at 14 nm.
Fin pitch and height are optimized for density and performance.

WORLD'S HIGHEST PERFORMANCE TRANSISTORS

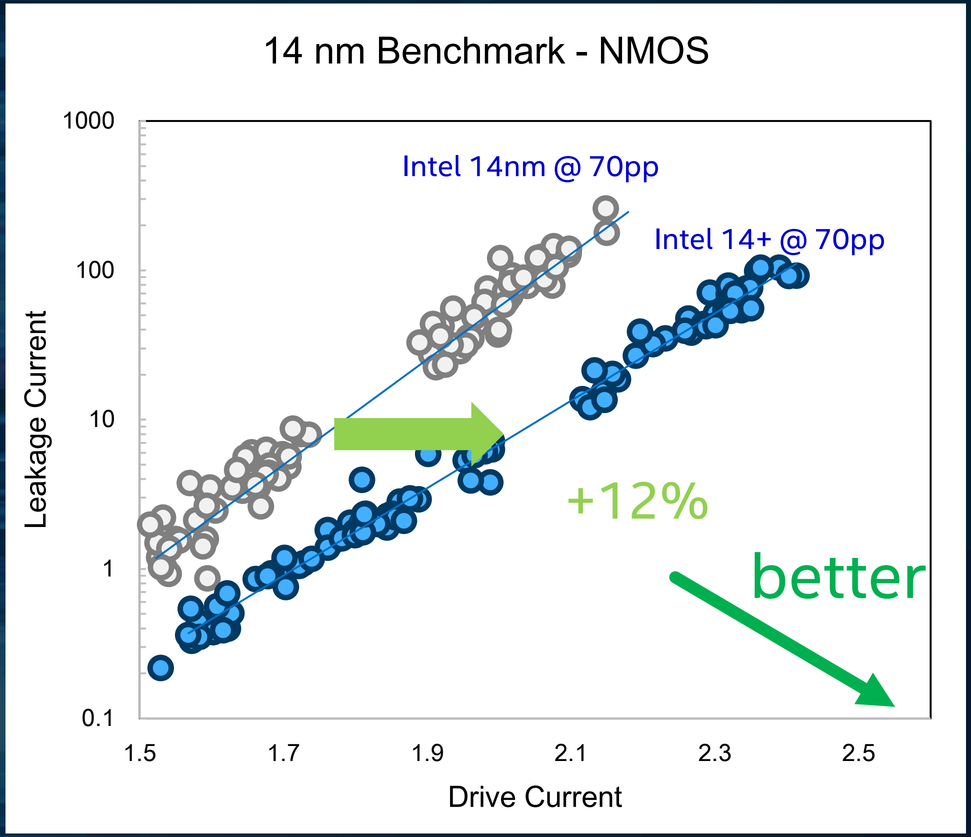


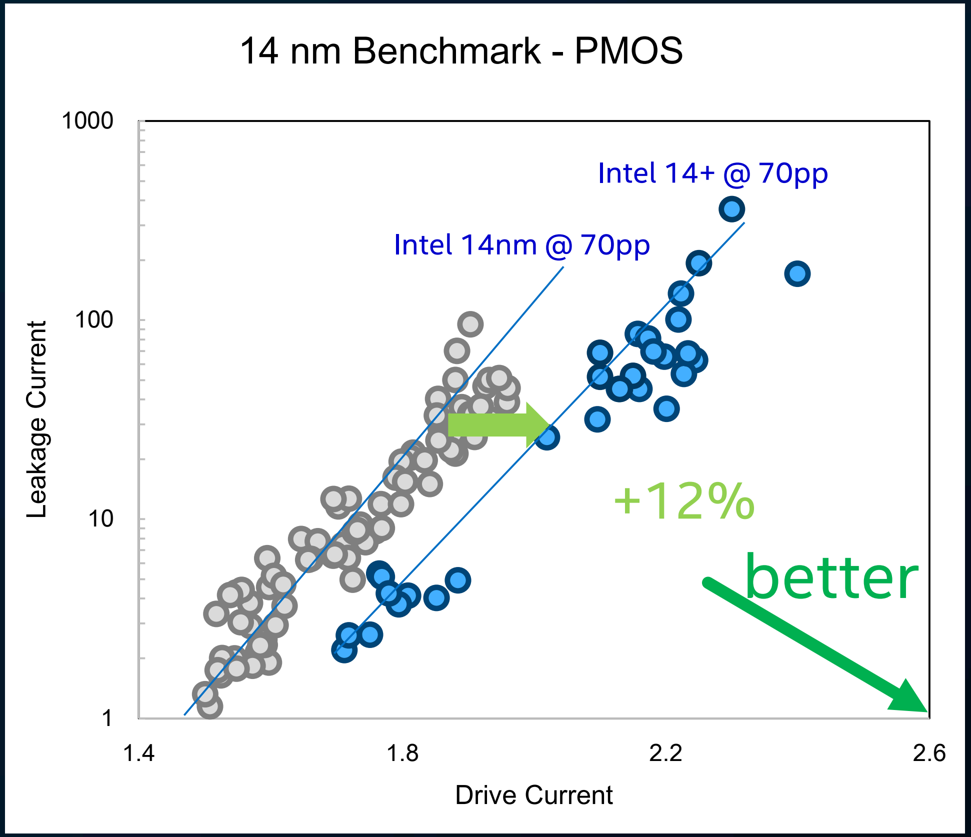


Intel demonstrated leading 14 nm performance in 2015.

Source: Intel.

WORLD'S HIGHEST PERFORMANCE TRANSISTORS

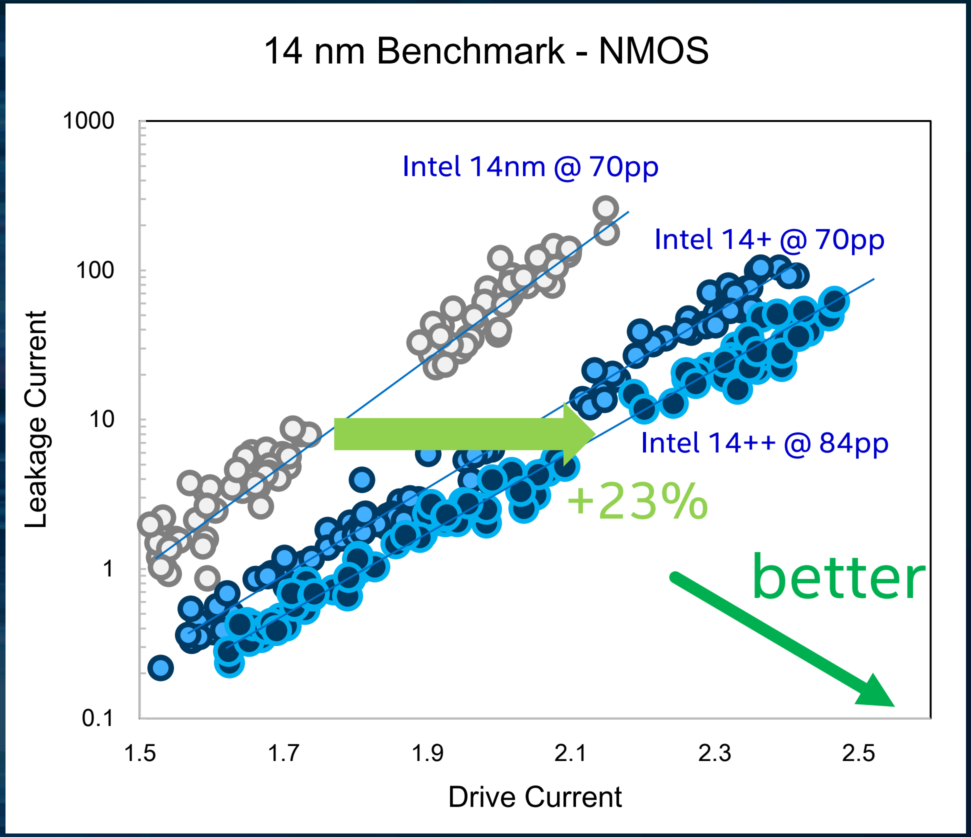


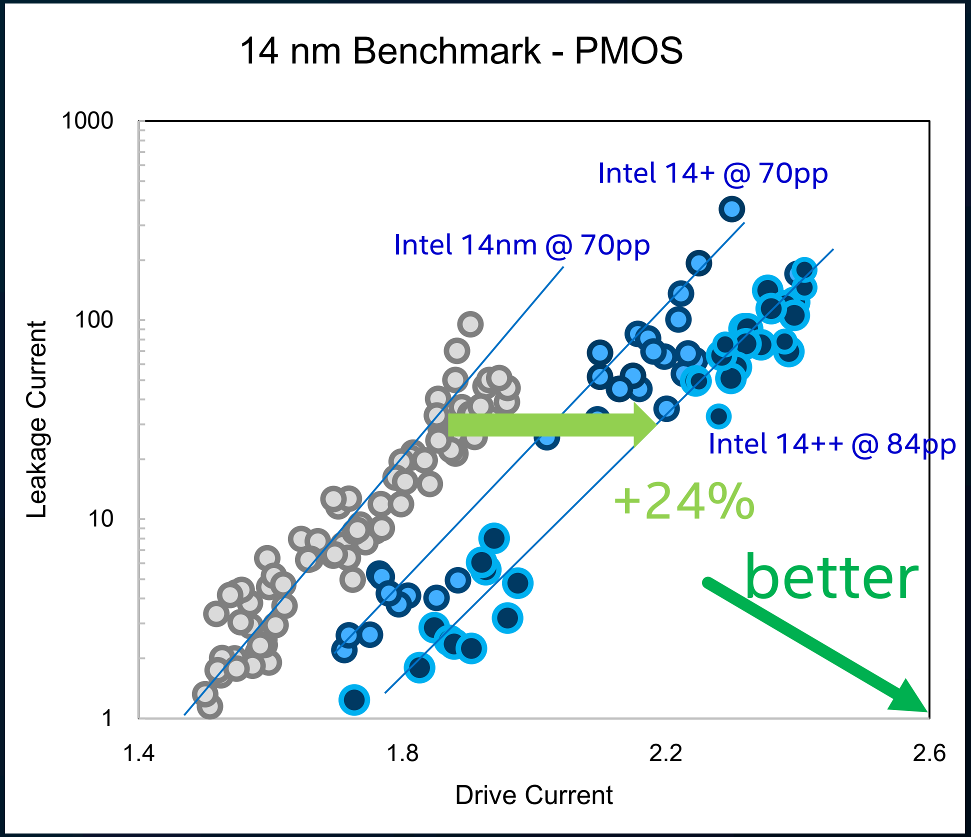


Intel's 14+ enhancement enables +12% drive current in 2016.

Source: Intel.

WORLD'S HIGHEST PERFORMANCE TRANSISTORS

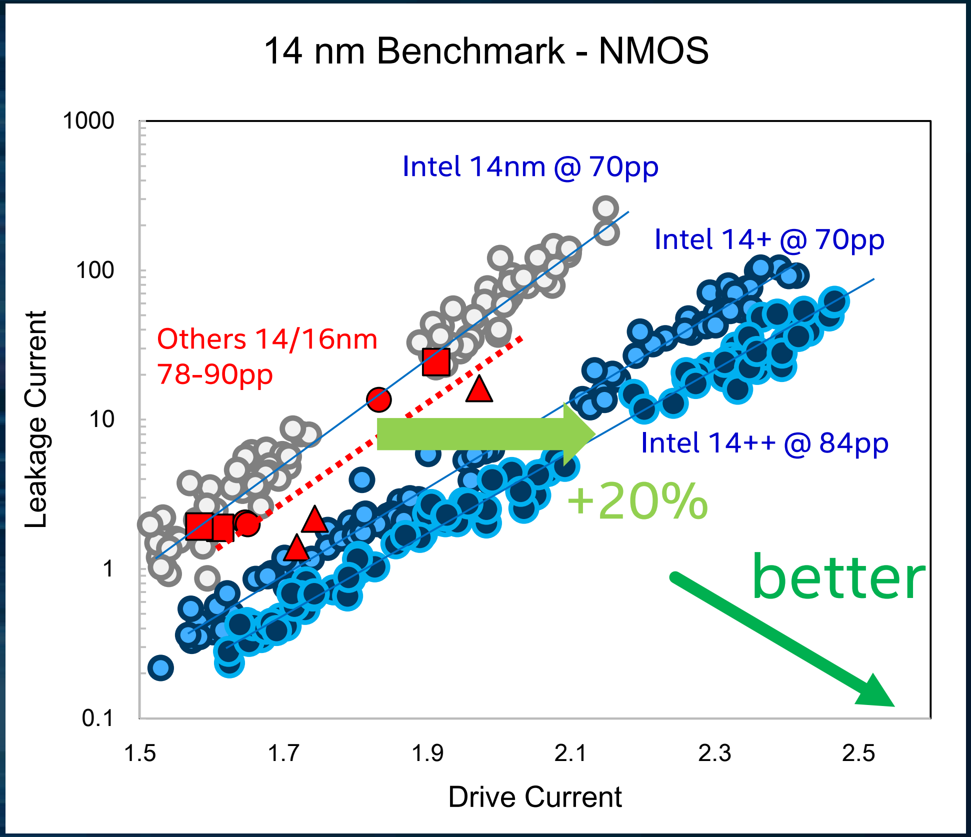


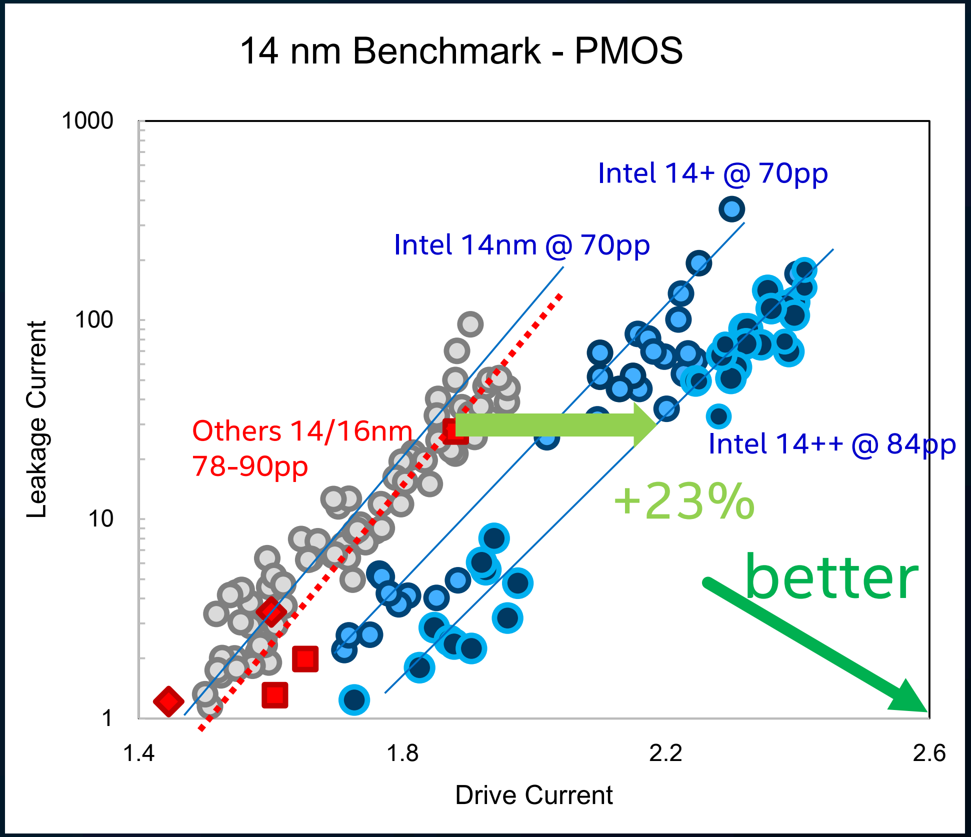


Intel's 14++ enhancement enables +23-24% higher drive current in 2017.

Source: Intel.

WORLD'S HIGHEST PERFORMANCE TRANSISTORS

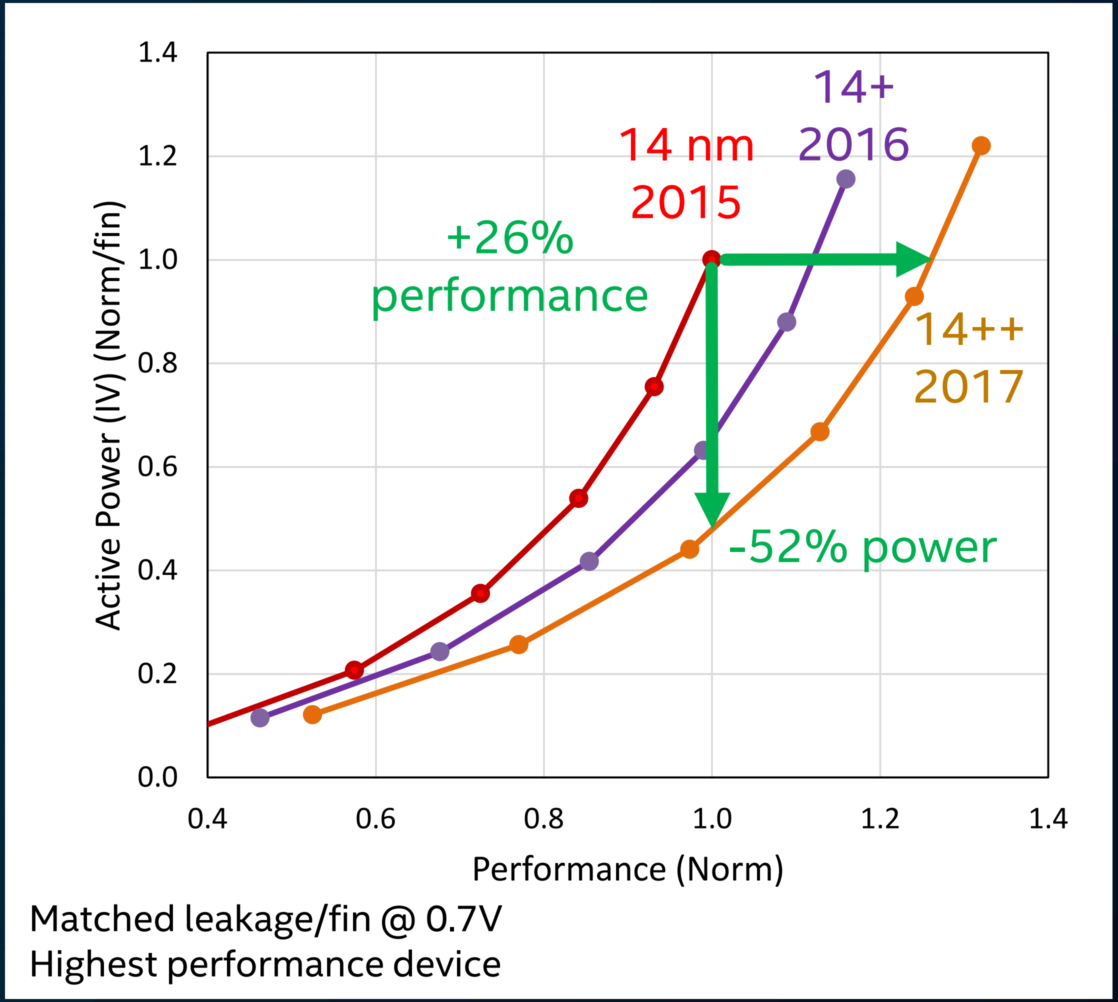




Intel's 14++ performance is >20% better than others' best "14/16 nm".

Source: Amalgamation of analyst data and Intel analysis, based upon current expectations and available information.

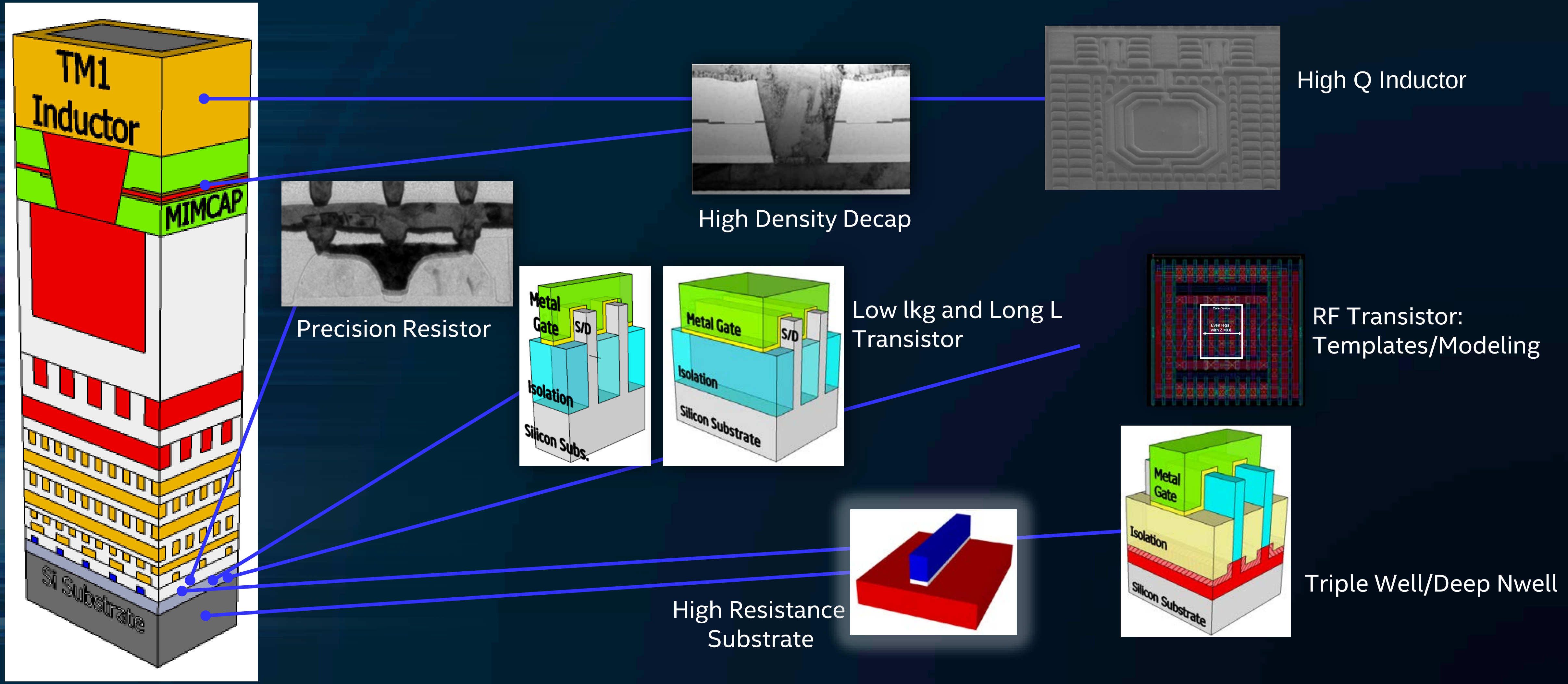
WORLD'S HIGHEST PERFORMANCE TRANSISTORS



Transistor performance enhanced on an annual cadence.

Source: Intel.

INTEL 14NM OFFERS FULL RANGE OF CAPABILITIES



High Q Inductor

High Density Decap

Precision Resistor

Low lkg and Long L Transistor

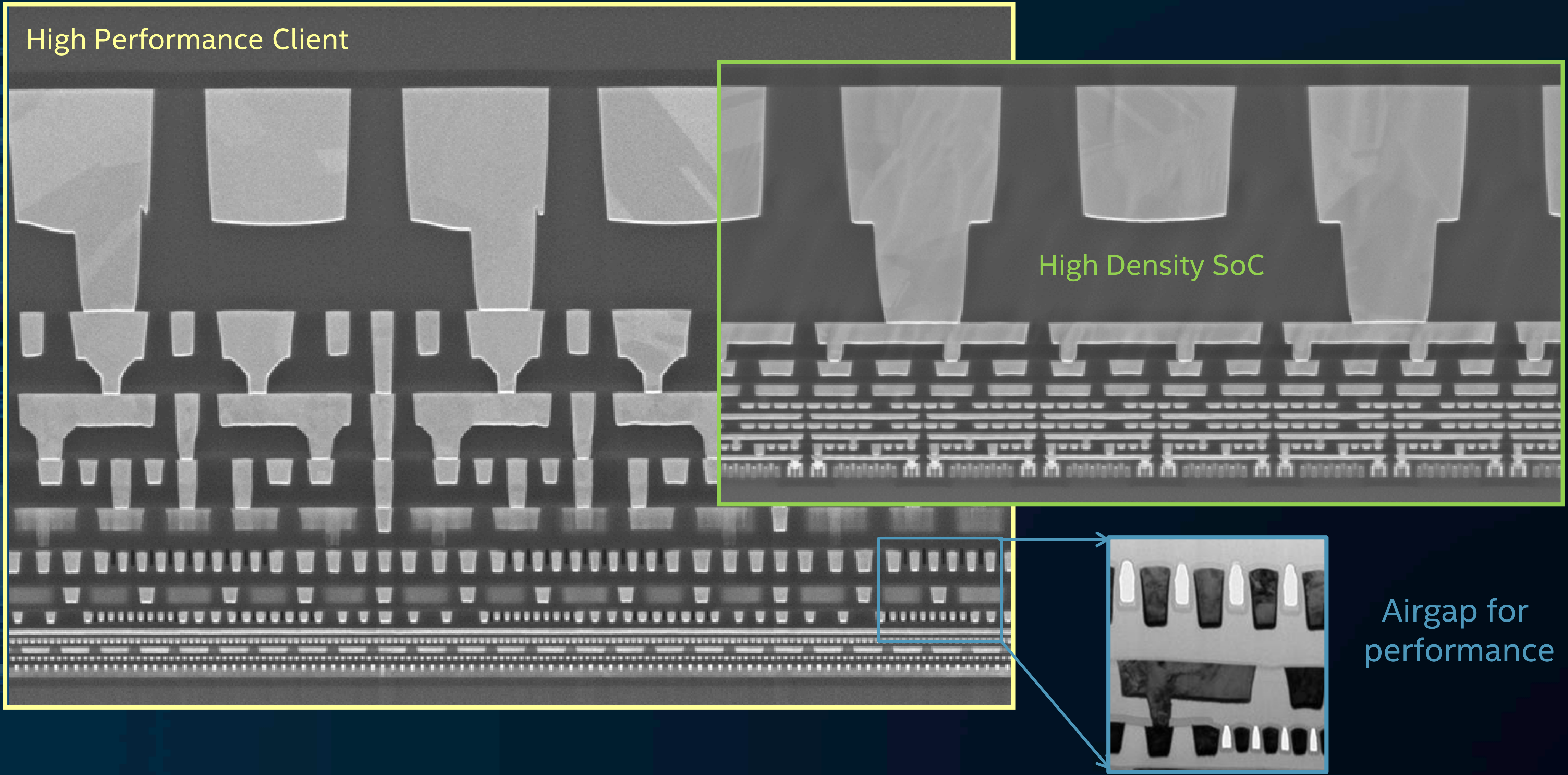
RF Transistor: Templates/Modeling

High Resistance Substrate

Triple Well/Deep Nwell

Intel's 14 nm technology offers a full suite of capabilities for product design needs.

14NM TECHNOLOGY OFFERS FULL RANGE OF INTERCONNECTS



Airgap for performance

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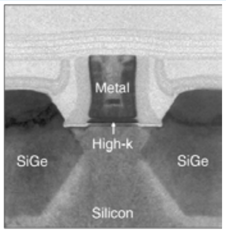
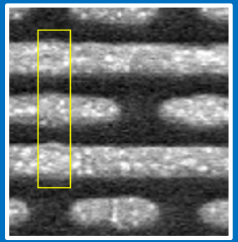
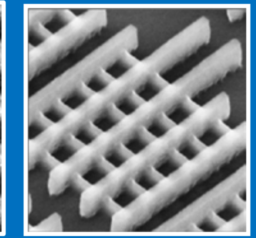
INTEL INNOVATION LEADERSHIP



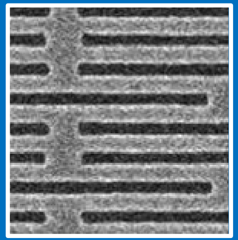
High-k Metal Gate



Self Align Via



FinFET Transistor



Hyper Scaling

45nm 32nm 22nm

14nm

Traditional scaling enablers

Hyper scaling enabler

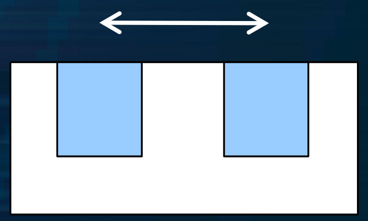
Innovations are the key to scaling. Intel drives the development of key breakthroughs.
At 14 nm, we have several generations of learning on traditional enablers.

INTEL INNOVATION LEADERSHIP BY HYPER-SCALING

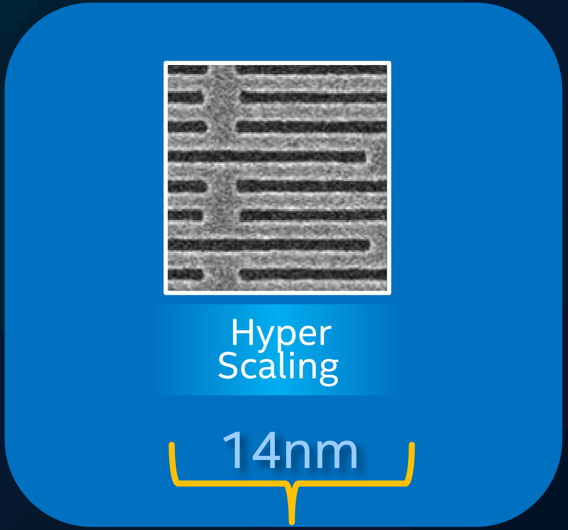
Interconnects

14 nm Technology

52 nm Pitch



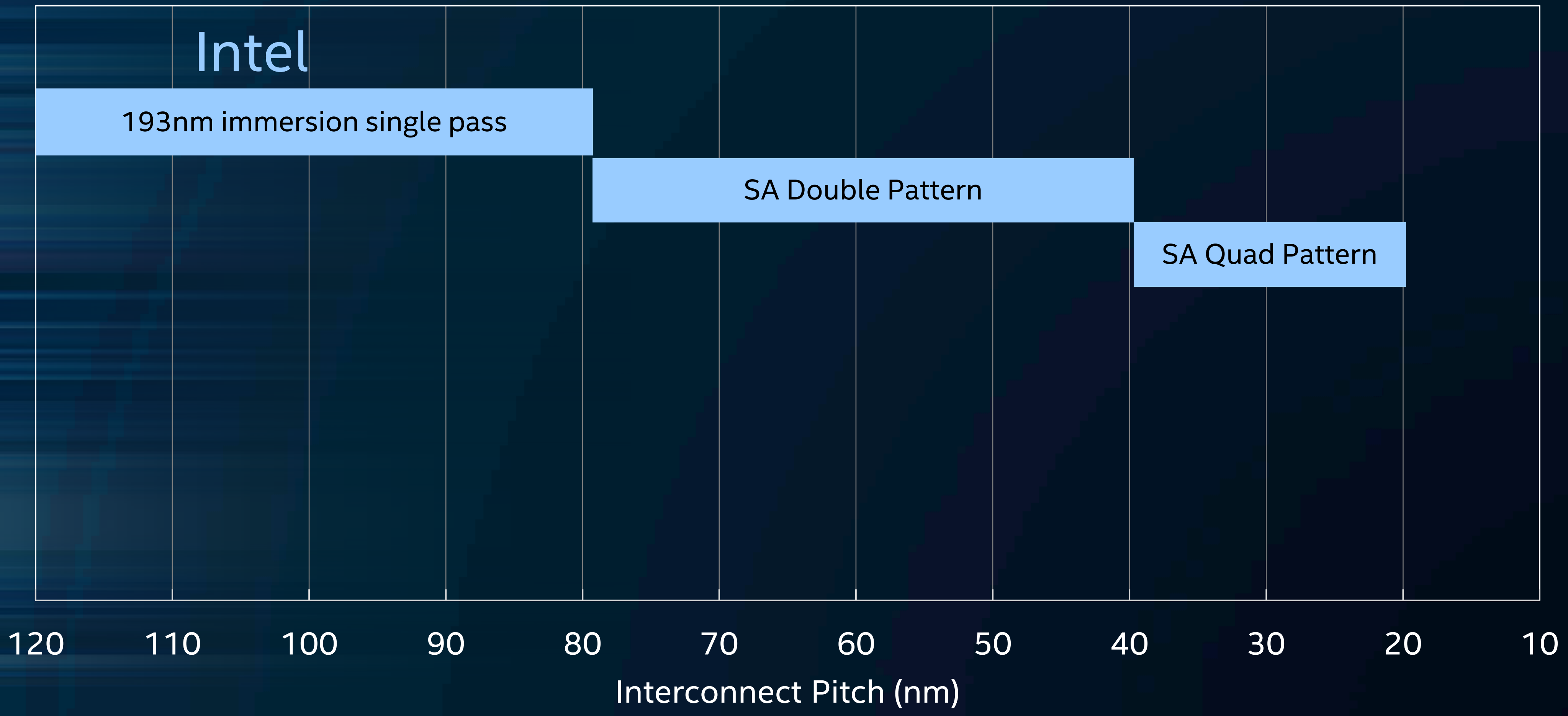
Self-Aligned
Double Patterning



Hyper scaling
enabler

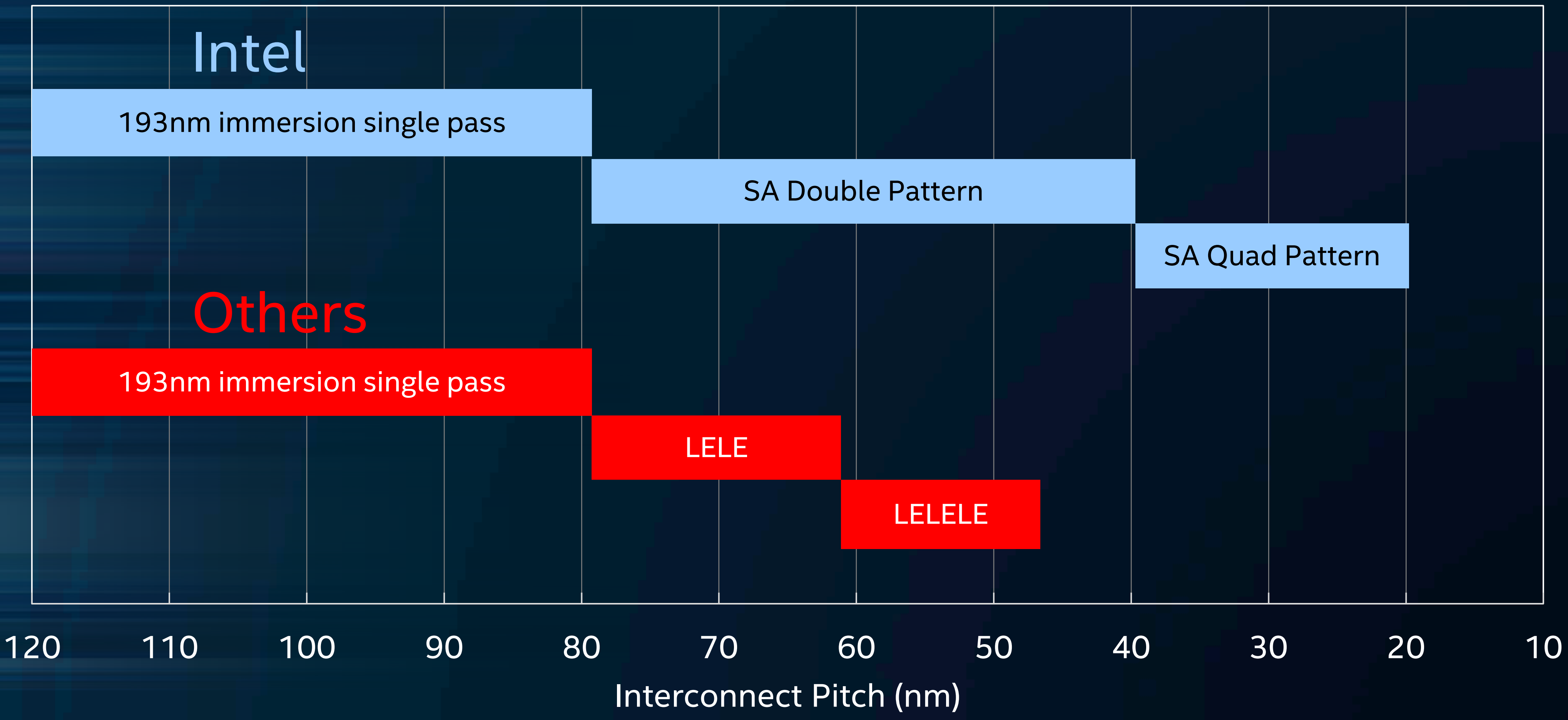
Self-Aligned Double Pattern interconnects first introduced into logic manufacturing by Intel.
Key advantage for density and yield.

INTERCONNECT PATTERNING OPTIONS



Self-Aligned patterning allows Intel to use the full range of interconnect pitches.

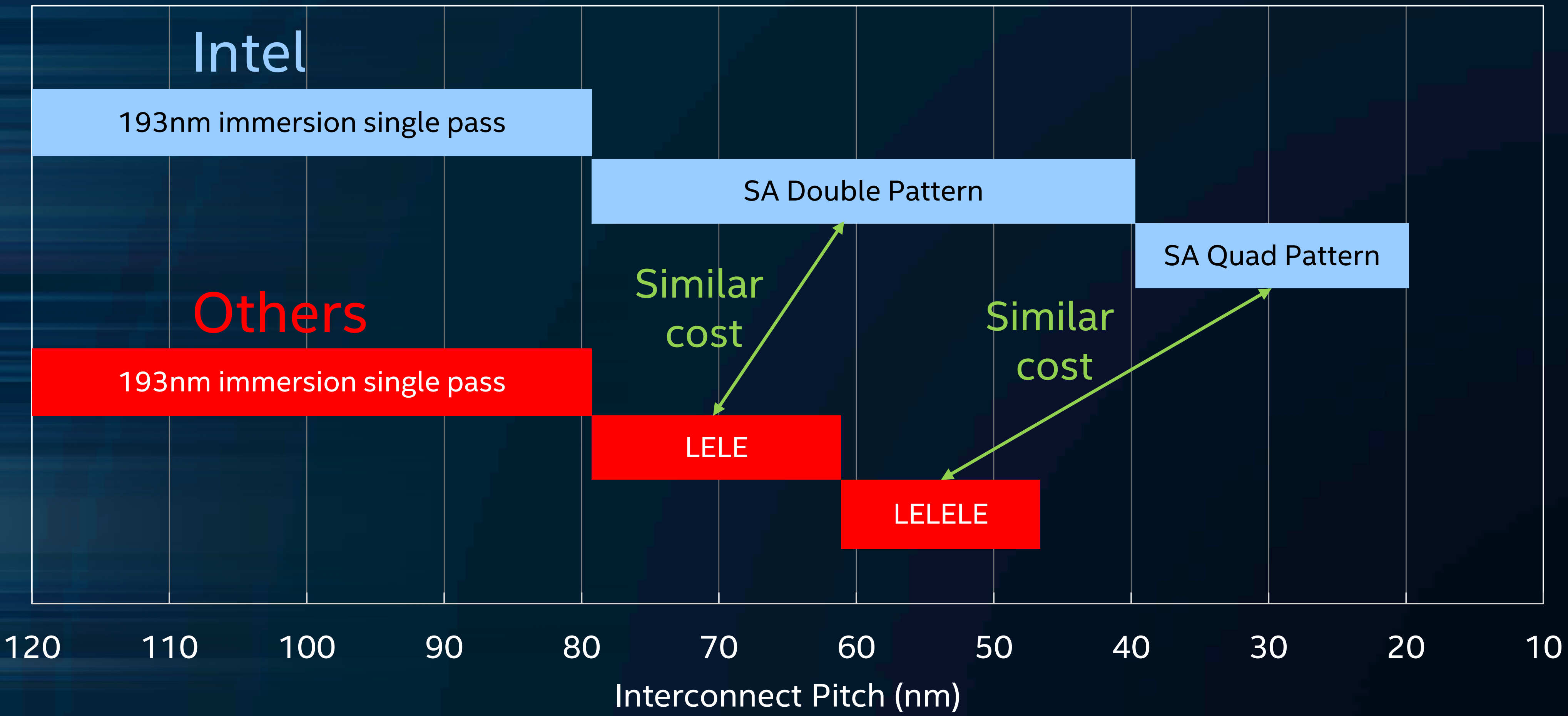
INTERCONNECT PATTERNING OPTIONS



Other’s patterning choices limit interconnect pitch options.

Source: Amalgamation of analyst data and Intel analysis, based upon current expectations and available information.

INTERCONNECT PATTERNING OPTIONS

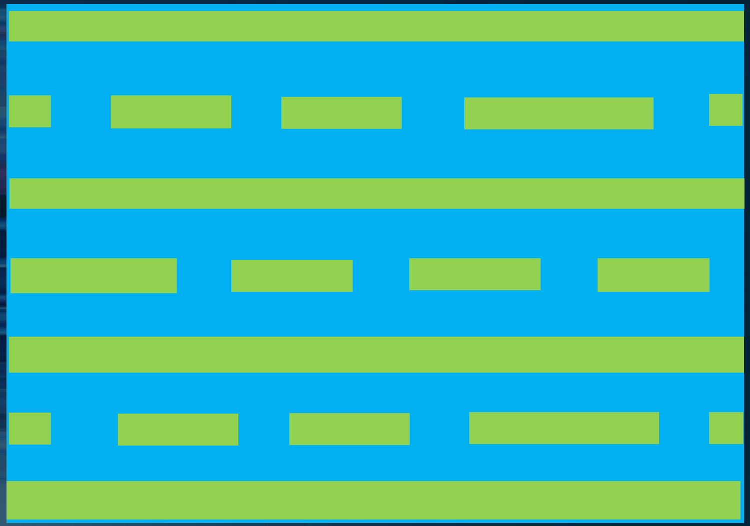


Self-Aligned Patterning allows Intel to have dense interconnects at lower cost.

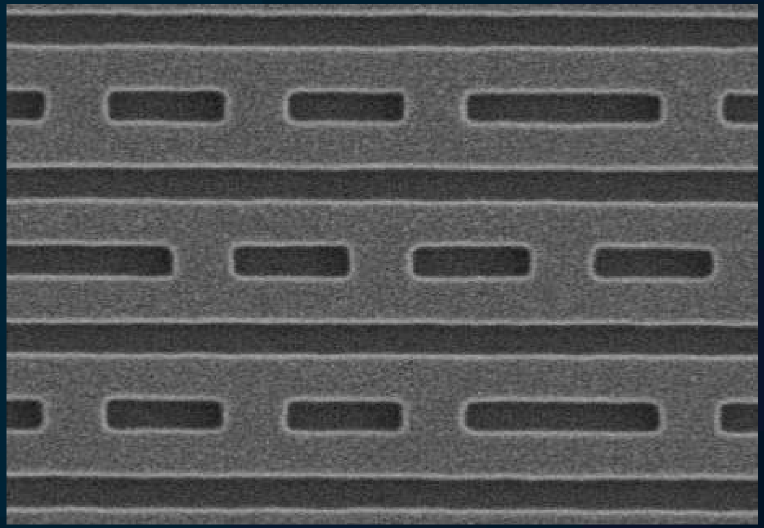
Source: Amalgamation of analyst data and Intel analysis, based upon current expectations and available information.

DOUBLE-PATTERNING LEADS TO MANUFACTURING BENEFITS

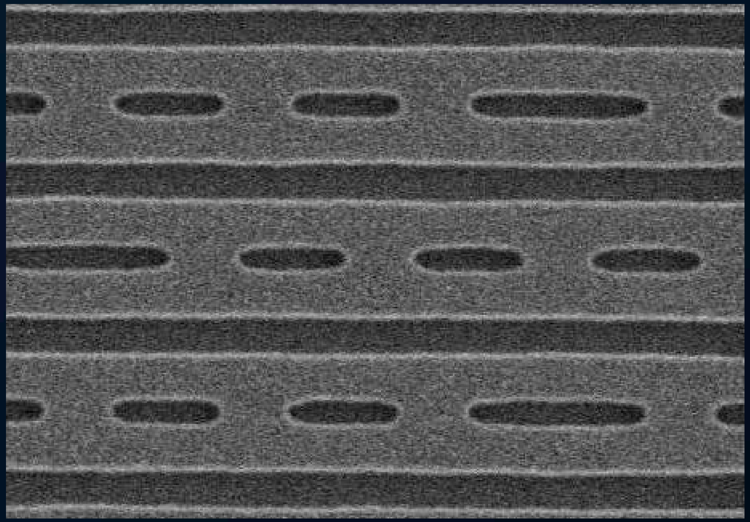
Desired Pattern



Double Patterning



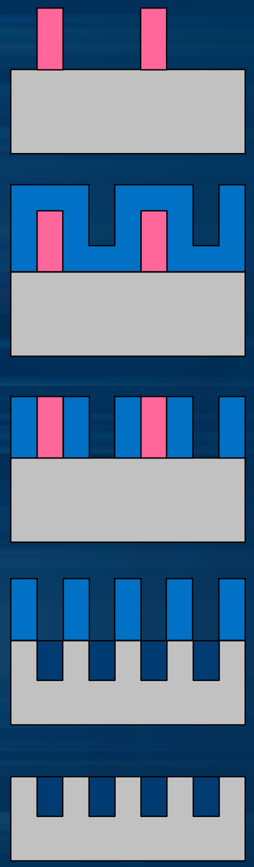
Litho / Etch



Double Patterning leads to clear benefits in process control.

SELF-ALIGNED PATTERNING LEADS TO PROCESS CONTROL

Self-Aligned Double Patterning



Litho

Spacer deposition
Thickness control ~1 nm

Etch spacer

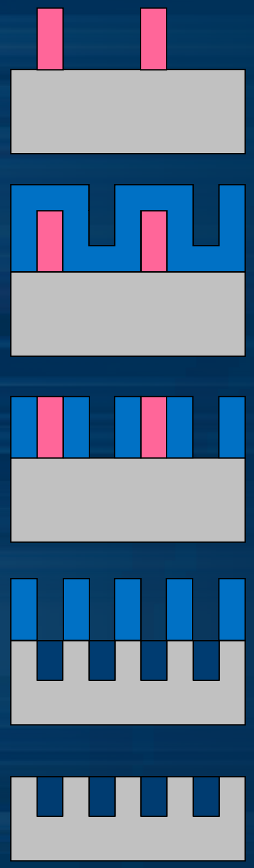
Clean and Etch

Pitch Division

Self-Aligned Patterning has placement control required for high yield.

SELF-ALIGNED PATTERNING LEADS TO PROCESS CONTROL

Self-Aligned Double Patterning



Litho

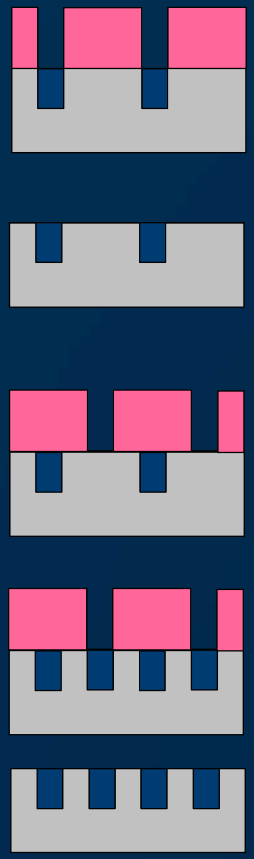
Spacer deposition
Thickness control ~1 nm

Etch spacer

Clean and Etch

Pitch Division

Litho-Etch-Litho-Etch



Litho #1

Etch #1

Litho #2
Good placement

Etch #2

Pitch division

Litho-Etch-Litho-Etch can yield same pattern.

SELF-ALIGNED PATTERNING LEADS TO PROCESS CONTROL

Self-Aligned Double Patterning

Litho

Spacer deposition
Thickness control ~1 nm

Etch spacer

Clean and Etch

Pitch Division

Litho-Etch-Litho-Etch

Litho #1

Etch #1

Litho #2
Good placement

Etch #2

Pitch division

Or Litho #2
~10 nm error

Etch #2

Pitch division

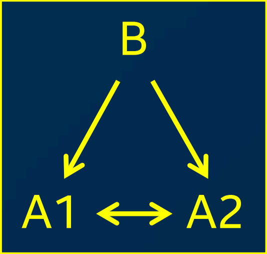
LELE process has yield and performance risk with mis-alignment between patterns.

SELF-ALIGNED PATTERNING LEADS TO PROCESS CONTROL

Self-Aligned Double Patterning

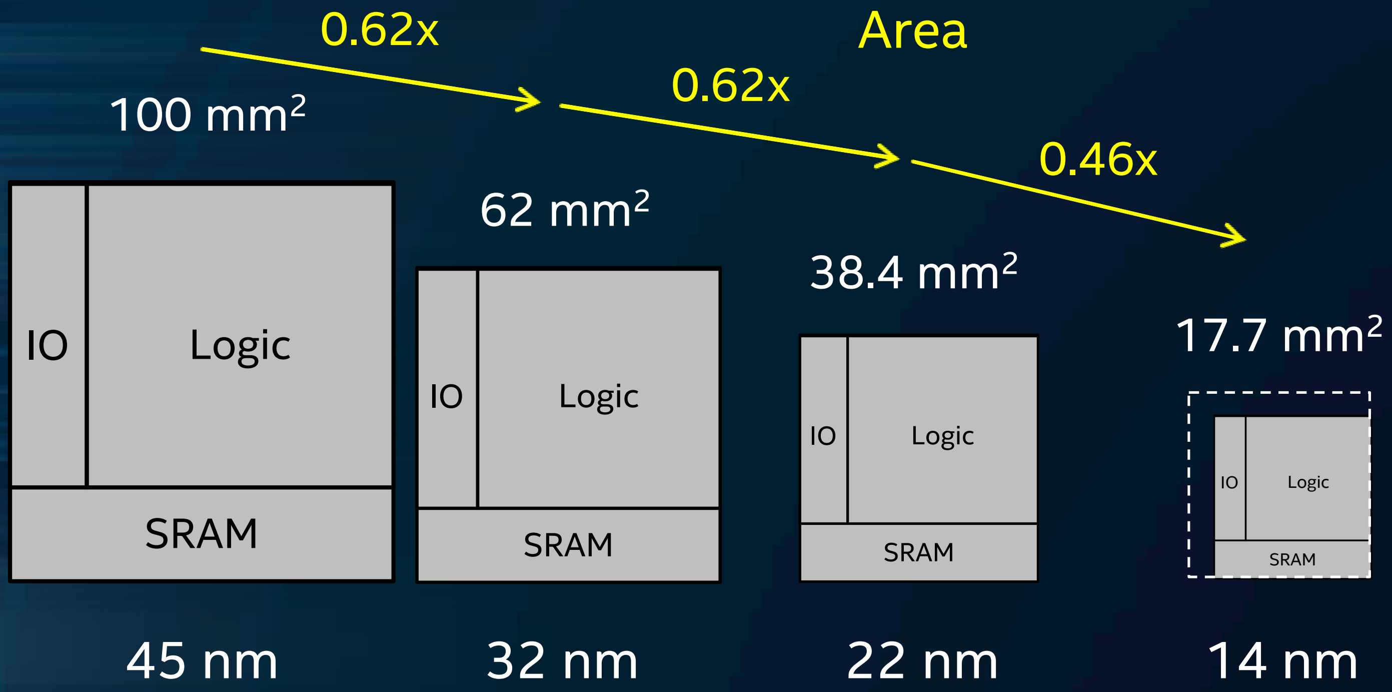
Single mask to single mask.
Alignment can be tightly controlled.

Litho-Etch-Litho-Etch



Single mask to multiple masks.
Difficult to control.

14 NM TECHNOLOGY DELIVERS SIGNIFICANT DIE SCALING



Area

0.62x

0.62x

0.46x

100 mm^2

IO Logic SRAM

45 nm

62 mm^2

IO Logic SRAM

32 nm

38.4 mm^2

IO Logic SRAM

22 nm

17.7 mm^2

IO Logic SRAM

14 nm

Circuit	Scale	Weight	Area
Logic	.39x	.60	.234x
SRAM	.54x	.25	.162x
IO	.60x	.15	.060x
Total			**.459x**

Hyper scaling delivers <0.50x die area scaling on 14 nm.

Source: Intel

BENEFITS OF INTEL'S 14 NM TECHNOLOGY

14 nm hyper scaling ⇒ ~1.4x more units per $ than traditional scaling

450 mm wafer size conversion ⇒ ~1.4x more units per $ than traditional scaling

1.6X WAFER COST

2.25X DIE INCREASE

1.4X DIE / $

300 mm

450mm

14 nm hyper scaling delivers the equivalent economic benefit as a wafer size transition.

Source: Amalgamation of analyst data and Intel analysis, based upon current expectations and available information.

SUMMARY

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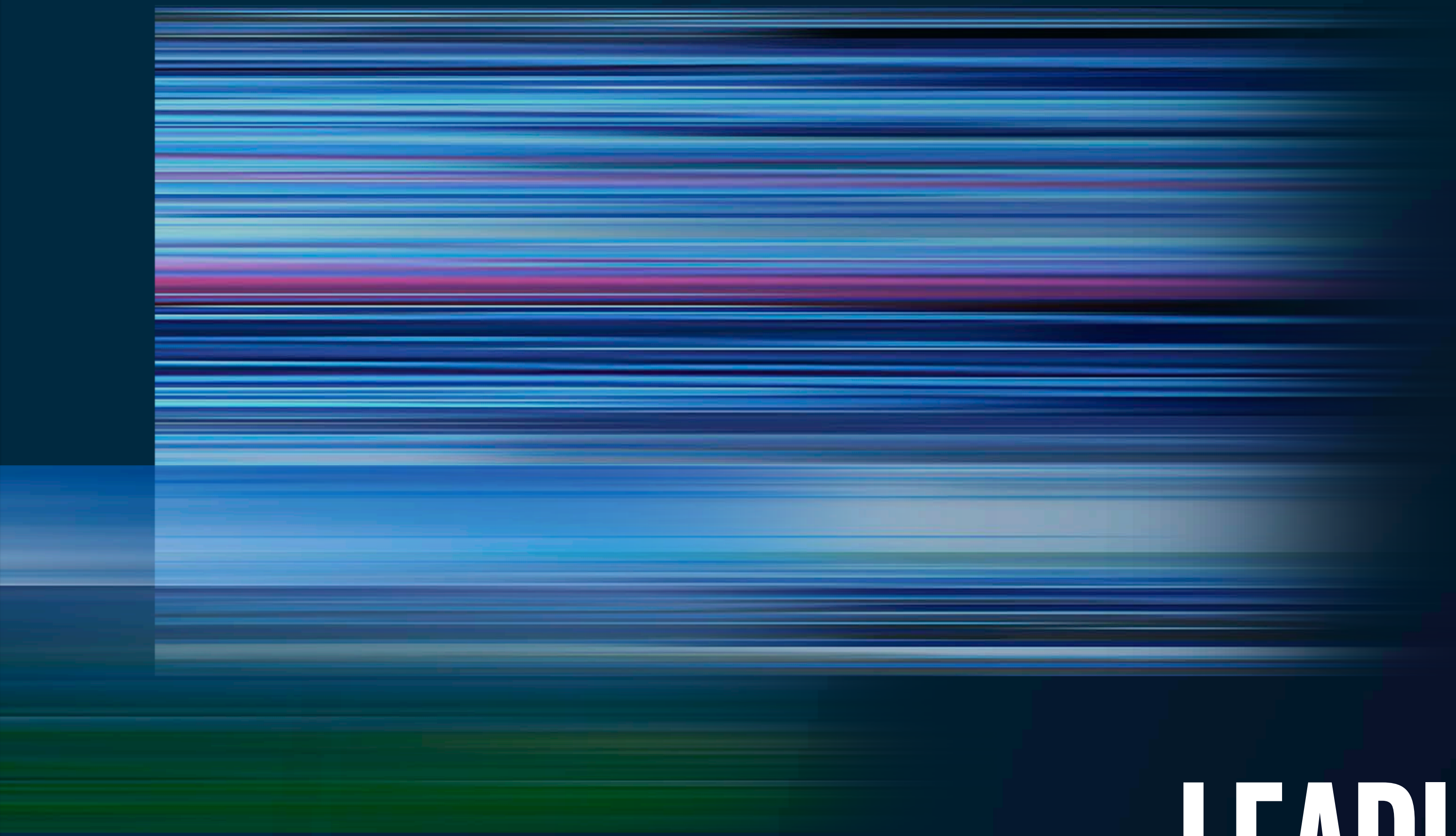

LEADING AT THE EDGE

TECHNOLOGY AND MANUFACTURING DAY