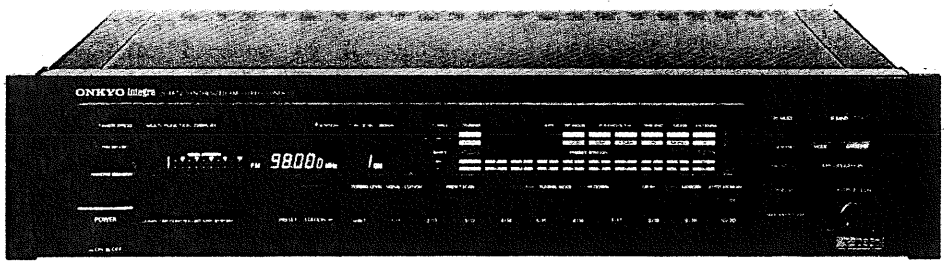
SERIAL No. 3275

ONKYO SERVICE MANUAL

SYNTHESIZED
FM STEREO TUNER

MODEL T-9090 II



UD, UDN, UDC	120V AC, 60Hz
UG	220V AC, 50Hz
UW, UWXD, UWXG	120/220V AC, 50/60Hz
UQA, UQB	240V AC, 50Hz

SAFETY-RELATED COMPONENT WARNING!!

COMPONENTS IDENTIFIED BY MARK ⚠ ON THE SCHEMATIC DIAGRAM AND IN THE PARTS LIST ARE CRITICAL FOR RISK OF FIRE AND ELECTRIC SHOCK. REPLACE THESE COMPONENTS WITH ONKYO PARTS WHOSE PARTS NUMBERS APPEAR AS SHOWN IN THIS MANUAL.

MAKE LEAKAGE-CURRENT OR RESISTANCE MEASUREMENTS TO DETERMINE THAT EXPOSED PARTS ARE ACCEPTABLY INSULATED FROM THE SUPPLY CIRCUIT BEFORE RETURNING THE APPLIANCE TO THE CUSTOMER.

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ONKYO
AUDIO COMPONENTS

SPECIFICATIONS

Tuning Range:	87.5 – 108.0MHz (AUTO MODE 50kHz steps, MANUAL MODE 25kHz steps)	
Usable Sensitivity:	Mono:	0.8μV (S/N 26dB, 40kHz Dev.) DIN
	Stereo:	20.0μV, (S/N 46dB, 40kHz Dev.) DIN
50dB Quieting Sensitivity:	Mono:	15.8dBf, 1.7μV
	Stereo:	37.2dBf, 20μV
Capture Ratio:	1.0dB	
Image Rejection Ratio:	100dB	
IF Rejection Ratio:	100dB	
Signal-to-Noise Ratio:	Mono:	95dB (IHF)
	Stereo:	85dB (IHF)
Selectivity:	80dB (±300kHz, IF: super narrow)	

AM Suppression Ratio:	60dB	
Total Harmonic Distortion:	Mono:	0.009% (IF: wide)
	Stereo:	0.02% (IF: wide)
Frequency Response:	30 – 15,000Hz (+0.5dB, –1.0dB)	
Stereo Separation:	55dB at 1kHz (IF: wide)	
	33dB at 70 – 10,000Hz (IF: wide)	
Output Voltage:	0 – 1.5V	
Dimensions (W × H × D):	465 × 103 × 387mm	
	18-5/16" × 4-1/16" × 15-1/4"	
Weight:	8.5kg, 18.7lbs.	

Specifications and features are subject to change without notice.

SERVICE PROCEDURES

1. Replacing the lamp

This unit uses the lamp listed below.

Circuit no.	Parts no.	Desciption
Q754	210064A	PL 6.3V, 250mA, Dial plate illumination

2. Safety-check out (D model)

After correcting the original service problem, perform the following safety check before releasing the set to the customer:

Connect the insulating-resistance tester between the plug of power supply cable and tapping screw holding the back panel and top cover.

Specification: 3.3MΩ ±10% at 500V

3. Change of De-emphasis

W models are equipped with a 50μsec-75μsec selector switch. This switch is located on the back panel. This switch is set to 50μsec at the factory, but may have to be reset to 75μsec depending on the area where the unit is used.

Europe: 50μsec

U.S.A.: 75μsec

4. Change of voltage

W models are equipped with a voltage selector to conform with local power supplies. This switch is located on the back panel. Be sure to set this switch to match the voltage of the power supply in your area before turning the power switch on.

This switch is set to 220V at the factory. Voltage is changed by sliding the groove in the switch with the screwdriver to the right or left. Confirm that the switch has been moved all the way to the right or left before turning the power switch on.

5. Memory Preservation

This unit does not require memory preservation batteries. A built-in memory power back-up system preserves contents of the memory during power failures and even when the unit is unplugged. The unit must be plugged in and the power switch turned on and off once in order to charge the back-up system. Note that since this is not a permanent memory, the power switch must be turned on and off a few times each month to keep the back-up system operable. The period of time during which memory contents are preserved after power has last been turned off varies depending on climate and the location and placement of the unit. On the average, memory contents are protected over a period of 3 to 4 weeks (a minimum of 2 weeks) after the last time power has been turned off. This period is shorter when the unit is exposed to very high humidity or used in an area with an extremely humid climate.

6. Procedures for replacement of flat packaged ICs

1. **Tools to be used:**

(1) **Soldering iron** .... Grounded soldering iron or soldering iron with leak resistance of 10 Mohms or more.

Form of soldering iron's tip:

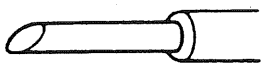


Fig. 1

(2) **Magnifying glass** ... for checking of finished works

(3) **Tweezers** ..... for handling of IC and forming of leads

(4) **Grounding ring** .... Countermeasure for electrostatic breakdown

(5) **Nipper** ..... for removing defective IC

(6) **Small brush** ..... for application of flux

2. Work Procedures:

(1) **Remove the defective IC**

Cut all leads of the defective IC one by one using a nipper and remove the IC.

(2) **Clean the pattern surface of the PC board.**

Get rid of the remaining leads and solder.

(3) Check and from the leads of the new flat packaged IC to be installed.

From every lead on the new IC using a pair of tweezers, so that all of them are aligned neatly without being risen, twisted or inclined toward one side. Especially the rising portion of every lead must be formed with greatest care.

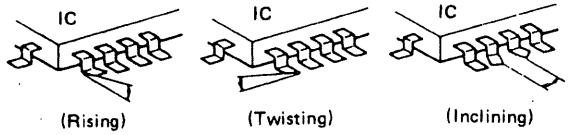


Fig. 2

(4) **Apply flux to the PC board.**

Apply flux to the pattern surface of the PC board which has been cleaned, as shown in the illustration. The area to be applied with flux is the portion of about 2.5mm in width where the IC's leads are to be soldered.

Be careful to apply minimum amount of flux required so as not to smear it on unwanted areas.

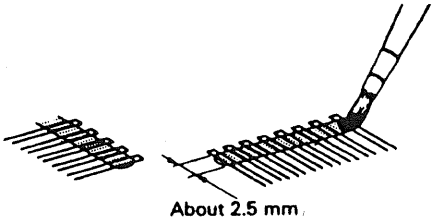


Fig. 3

(5) **Temporarily tighten the IC**

Carefully align the pattern and IC's leads, so that the IC will be temporarily tightened to the pattern on the four leads at the corners. At this time, soldering is required, but no need to apply soldering material.

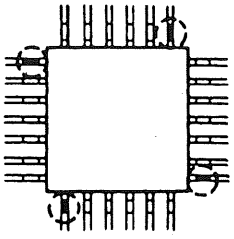


Fig. 4

(6) **Apply flux to IC's leads**

Apply flux to the areas of IC's leads where soldering is to be performed. Be careful not to smear flux on the root portion of any lead or the body of IC.

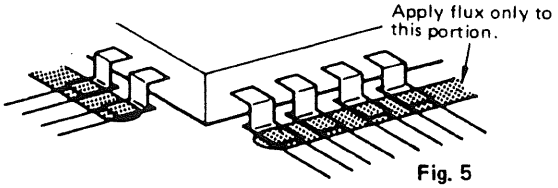


Fig. 5

(7) **Soldering**

While attaching the tip of the soldering iron to the soldering point as shown in the illustration, feed 2 –5mm of soldering wire. Then, slowly move the iron in the direction indicated by the arrow in the illustration, so that the leads will be soldered to the pattern. Move the iron in the rate of approximately 1cm in 5sec. Proceed with your work while confirming a clean fillet of solder is formed on each lead, subsequent to the melting of flux.

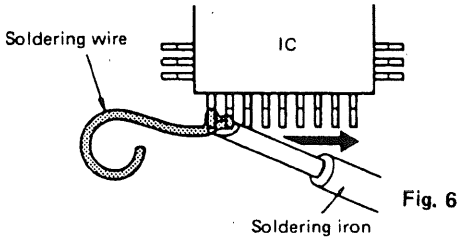


Fig. 6

CAUTION

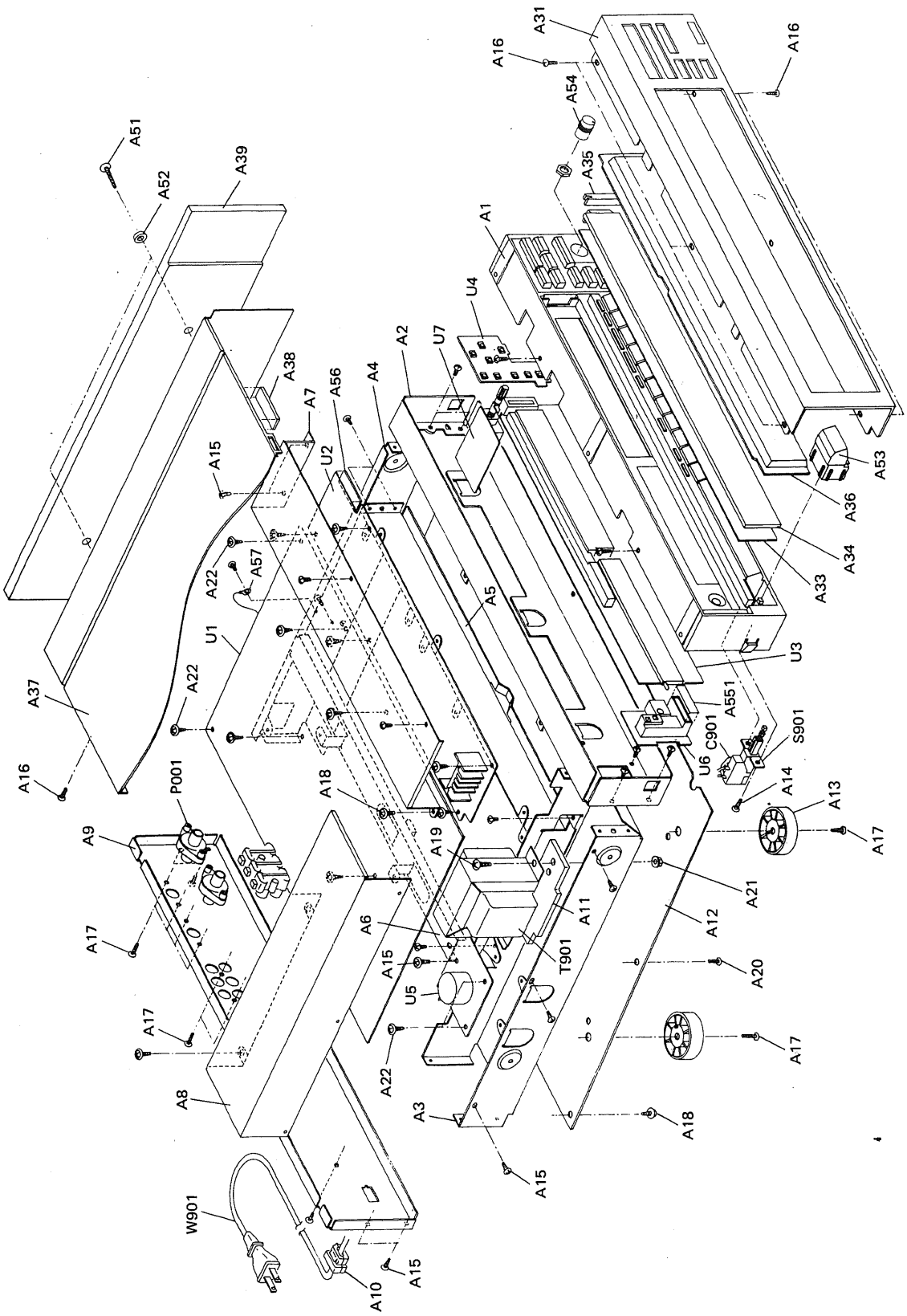
1) If you move the iron too quickly, loose soldering is likely to result.

2) Be especially careful when soldering the first lead where loose soldering is most liable to be formed.

(8) **Check the results**

When soldering of all leads is finished, check the soldered portion on every lead with a magnifying glass. A tester must not be used or checking of any soldered position

EXPLODED VIEW



PARTS LIST

REF. NO.	PART NO.	DESCRIPTION
A1	27110375B	Front bracket ass'y
A2	27110377A	Front bracket RE
A3	27115228A	Side bracket L
A4	27115229A	Side bracket R
A5	27130498	Bracket FR
A6	27130499	Bracket RE
A7	27225085A	Shield cover FR
A8	27225086-1	Shield cover PT
A9	27121042	Back panel (D)
	27121043	Back panel (G)
	27121045	Back panel (W)
	27121053	Back panel (PX)
	27121058	Back panel (Q)
A10	27300750	⚠ Strainrelief
A11	27270214A	Spacer
A12	27170242B	Bottom board
A13	27175152	Leg
A14	833430080	3TTP +8P(BC), Tapping screw
A15	834430068	3TTS+6B(BC), Tapping screw
A16	838430088	3TTS+8B(BC), Tapping screw
A17	834430108	3TTS+10B(BC), Tapping screw
A18	831430088	3TTW+8B(BC), Tapping screw
A19	838440129	4TTB+12C(BC), Tapping screw
A20	801230	3STS+8BQ(BC), Tapping screw
A21	86414010	FWN4 × 10FN, Flange nut
A22	831130088	3TTW+8B, Tapping screw
A31	1A069121	Front panel ass'y
	28135144	Badge
A33	28133188B	Back plate
A34	28130247A	Dial plate
A35	27267513	Guide, dial plate
A36	28191436A	Clear plate
A37	28184318A	Top cover
A38	28140020	Cushion
A39	28185255	Side panel L
	28185256	Side panel R

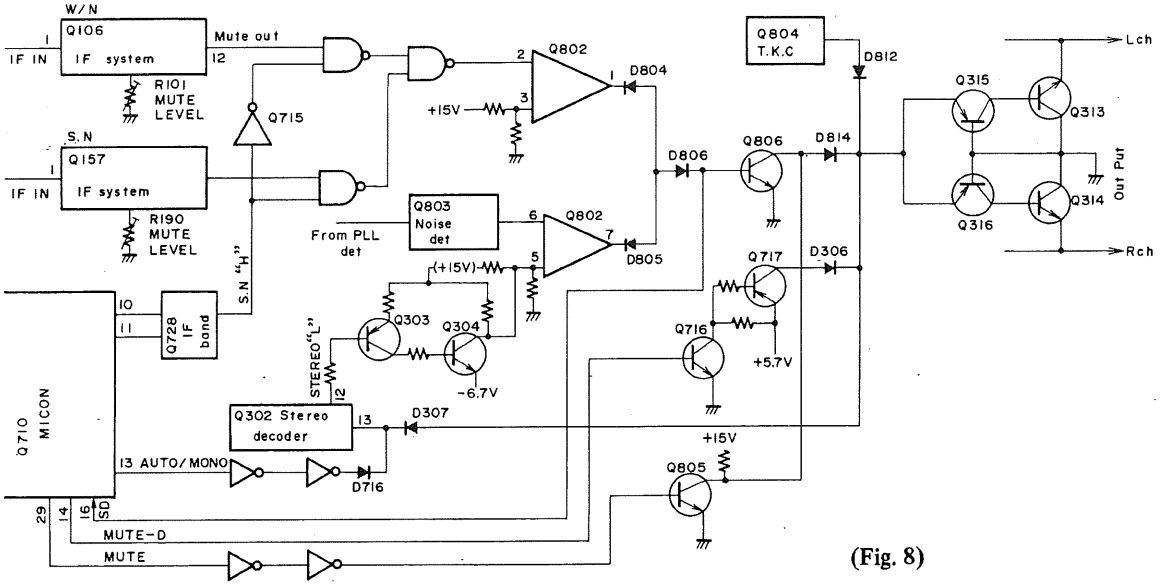
NOTE: (D) : Only 120V model
(G) : Only 220V model
(Q) : Only 240V model
(W) : Only Worldwide model
(PX) : Only PX model

REF. NO.	PART NO.	DESCRIPTION
A51	836440303	4STV+30CQ(BC), Special screw
A52	870086	Special washer
A53	28323145A	Knob POWER
A54	28323031-1	Knob TONE
A55	28199172	Film
A56	28175144	Insulated plate
A57	223004-1	Terminal
C901	3500065A	⚠ 0.01μF, AC400V/125V, Capacitor IS
C901a	27300601	⚠ SB-1925, Cover for C901
P001	25060112	NTM-1PDMR046, Antenna terminal
P904	25065123	⚠ NPS-1258P, Voltage selector switch (W/PX)
S901	25035571	⚠ NPS-111-L533P, Power switch
T901	2300260	⚠ NPT-973D, Power transformer (D)
	2300261	⚠ NPT-973G, Power transformer (G)
	2300262	⚠ NPT-973DG, Power transformer (W/PX)
	2300275	⚠ NPT-973Q, Power transformer (Q)
U1	1A069590-1	NARF-3090-1, Main circuit pc board ass'y (D)
	1A069590-1A	NARF-3090-1a, Main circuit pc board ass'y (G/Q)
	1A069590-1B	NARF-3090-1b, Main circuit pc board ass'y (W/PX)
U2	1A069591-1	NADG-3091-1, Digital circuit pc board ass'y
U3	1A069592-1	NADIS-3092-1, Display circuit pc board ass'y
U4	1A069593-1	NASW-3093-1, Operation switch pc board ass'y
U5	1A069594-1	NASW-3094-1, Power supply circuit pc board ass'y (D)
	1A069594-1A	NASW-3094-1a, Power supply circuit pc board ass'y (G/W/Q/PX)
	1A069595-1	NASW-3095-1, De-emphasis switch pc board ass'y (W/PX)
U6	1A069596-1	NAETC-3096-1, Remote control circuit pc board ass'y
U7	1A069597-1	NAETC-3097-1, Output volume pc board ass'y
W901	253123, 253136, 253140 or 253146	⚠ AS-UC-6#18, Power supply cord (D/PX)
	253127B or 253129A	⚠ AS-CEE, Power supply cord (G/W)
	253118	⚠ AS-SAA, Power supply cord (Q)

NOTE: THE COMPONENTS IDENTIFIED BY MARK ⚠ ARE CRITICAL FOR RISK OF FIRE AND ELECTRIC SHOCK. REPLACE ONLY WITH PART NUMBER SPECIFIED.

CIRCUIT DESCRIPTIONS

1. Muting circuit

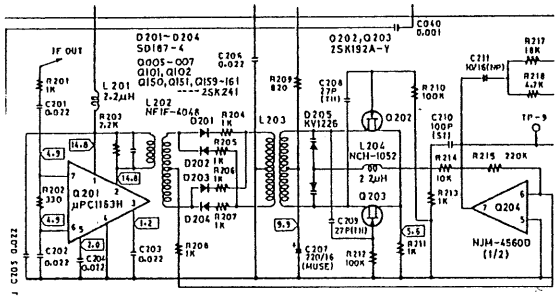


(Fig. 8)

In Q106 and Q157 FM IF system IC, the muting IF level (determined by pin 15 semi-fixed resistor) detector circuit and zero cross detector circuit are built in. At the time of tuning, this output at pin 12 becomes 0V. The Q715 NAND gate is the selector gate circuit for SUPER NARROW and WIDE/NARROW muting.

At the time of AUTO TUNING if a broadcast station is picked up, pin 12 of Q106 goes to low level and Pin 2 of Q802 goes low. Also, at the same time, when noise is not included in the detected signal, pin 6 of Q802 goes low. Because of that, output pins 1 and 7 of Q802 have +12V, the anode side of D806 has +5V, pin 16 SD terminal of the Q710 microcomputer goes high, and the automatic tuning is completed. In addition, at the same time Q806 goes ON, Q313~Q316 are in cutoff state, and the signal is output. When the Q805 transistor muting switch is OFF (when the FM MUTE indicator is extinguished), the muting is forced to the open condition.

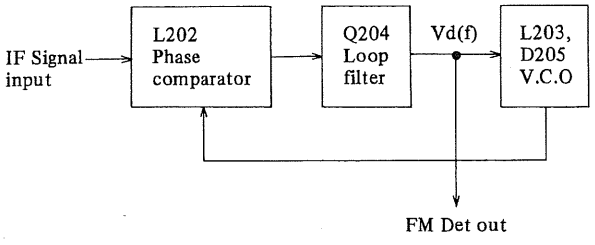
2. PLL detector circuit



(Fig. 9)

In this device, in order to have a high S/N and low percentage of distortion, a PLL (phase locked loop) detector is used. Because the PLL detector is a closed loop detector, noise generated within the loop is suppressed, and it is an extremely good S/N detector.

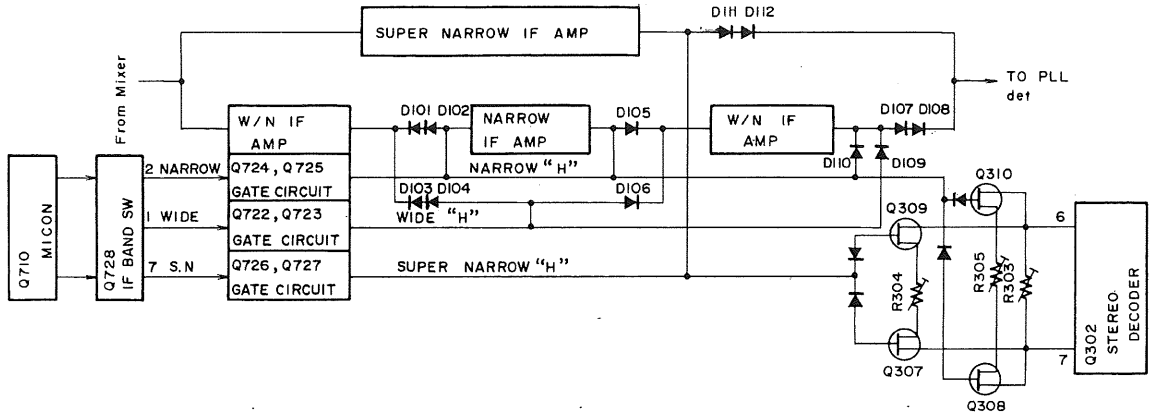
With L203 and D205 as a 10.7MHz voltage controlled oscillator, and with L202, and D201~D204 as a single phase comparator, the single phase error portion of the



(Fig. 10)

FM IF waveform and 10.7MHz voltage controlled oscillator signal are output at the center point of the secondary side of L202, passed through the loop filter, and the composite signal is then taken out. Also, when the 10.7MHz intermediate frequency is transferred, the amount of variation is compensated by the D205 variable capacitor diode, and the output error of the single phase comparator is always set to a zero level.

3. IF band selection circuit



(Fig. 11)

At the A/D input signal pin 63 of Q710, when the SD terminal goes low, automatically the IF band is determined. At the time of NARROW selection, the output of pin 10 goes H, and at the time of SUPER NARROW, pin 11 goes H. In Q728, at the band selection switch, pins 1, 2, and 7 respectively go high for WIDE, NARROW, and SUPER NARROW.

– Wide operation –

Q722 and Q723 go ON, the collector voltage of Q723 becomes essentially +B2, D103, D104, and D106 go ON, and the IF signal passes through D103, D104, and D106.

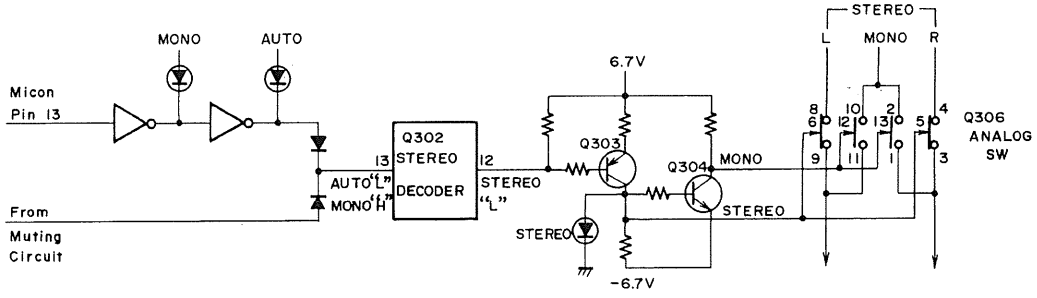
– Narrow operation –

Q724 and Q725 go ON, D102, D101, and D105 go ON, and the IF signal passes through NARROW amplifier Q104. Also, at the time of WIDE, in order to change to maximum operation, Q308 and Q310 are turned ON, and with R305, compensation of operation is carried out.

– Super Narrow operation –

Q726 and Q727 turn ON, D111 and D112 diodes go ON, and the signal passed through the super narrow IF amplifier is output in the PLL detector circuit. Also, for the alignment of narrow, Q307 and Q309 go ON, and separation is compensated by R304.

4. Stereo switch circuit



(Fig. 12)

When a stereo broadcast is received, pin 12 of Q302 goes "L", Q303 goes ON, the collector voltage becomes H, and the stereo indicator lights. Also, pins 5 ans 6 of the Q306 analog switch go H, conduction occurs between 3~4 pins and 8~9 pins, and at the Q302 stereo decoder, the L and R divided signal is output. In addition, at the time of monaural broadcast reception, and when the MODE switch is in the MONO position, pin 12 goes H, and because Q303 and Q304 are in the cutoff condition, pins 12 and 13 of Q306 go to high level, conduction takes place between pins 10~11 and 1~2, and the detected signal passes through the AF amplifier to be output.

5. Explanation of PLL synthesizer and controller IC

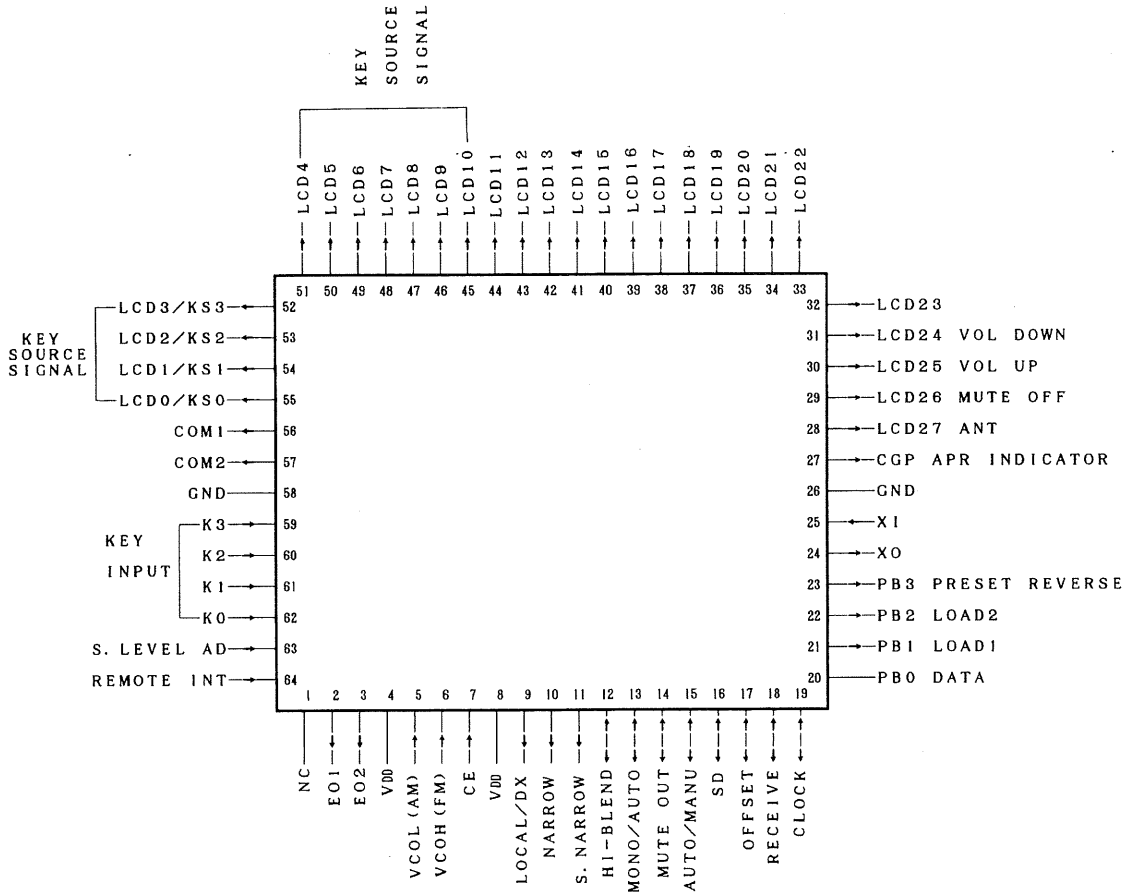
5-1. APR function (Automatic Precision Reception)

On the FM band, if there is a high level input at the SD terminal, depending upon the station signal level, there will be optimum reception function, and the output (Refer table 1) will automatically be changed.

ANT	RF	IF	AUTO/MONO	HI-BLEND
A	LOCAL	WIDE NARROW	AUTO	OFF
B	DX	SUPER NARROW	MONO	ON

Table 1 Changeover key means of APR execution.

5-2. Terminal connection



Pin No.	Symbol	Description
1	NC	No connection.
2	E01	Charge pump output of the phase detector which constitutes the PLL. High level is output when the divided oscillation frequency is higher than the reference frequency. In the opposite case, Low level is output. Floating occurs when the frequencies match. The output is applied to the variable capacitor diode in the local oscillation circuit of FM through the low pass filter Q701, Q702 and Q703. The output from both terminals is the same, but only E01 is used.
3	E02	Same as above.
4	VDD	This is the device power source terminal. At the time of operation, the supply is 5V. The internal data memory (RAM) is maintained by means of the C712 super capacitor.
5	VCOL (AM)	AM local oscillation signal input terminal. Not used.

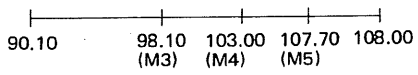
Pin No.	Symbol	Description
6	VCOL (FM)	At the FM local oscillation signal input terminal, there is direct input passage through the buffer.
7	CE	Chip enable input terminal. Device selection signal terminal. Normal operation at the high level and Memory preservation at the low level.
8	VDD	Device power source terminal.
9	LOCAL/DX	This is the output terminal for RF, either Local or DX. It is "H" for DX.
10	NARROW	This is the output terminal for IF, either Narrow or Wide. It is "H" for Narrow.
11	SUPER NARROW	This is the output terminal for IF, either Super Narrow or Wide. It is "H" for Super Narrow.
12	HI-BLEND	This terminal is for Hi-blend output ON or OFF. ON is "H".
13	MONO/AUTO	In the reception mode, the output terminal is either Auto or Mono. It is "H" for Mono.
14	MUTE OUT	The muting output terminal operates with the following modes. Power source ON, MANUAL/AUTO UP/DOWN, PRESET MEMORY call out, ANTENNA, RF, IF, AUTO/MONO, at time of MUTING selection, when the PROGRAM DISPLAY key is pushed, AUTO MEMORY time.
15	AUTO/MONO	This is the output terminal for Auto or Manual in the tuning mode. It is "H" for Auto.
16	SD	Station detection signal input terminal. "H" when active.
17	OFFSET	Offset output terminal when the signal input level is large. "H" when active.
18	RECEIVE	Indication output terminal when be received the code from remote control.
19	CLOCK	Clock signal output terminal to μPD6320GC.
20	DATA	Data signal output terminal to μPD6320GC.
21	LOAD1	Load signal output terminal to μPD6320GC.
22	LOAD2	Load signal output terminal to μPD6320GC.
23	PRESET	This is the output terminal for Shift indicator, either 1-10 or 11-20. 11-20 is "H".
24	XO	Connect to the 4.5MHz crystal osillator.
25	XI	
26	GND	Ground terminal.
27	APR	APR indication terminal.
28	ANT	This is the output terminal for ANT, either A or B. It is "H" for B.
29	LCD26/PL2	This is the out terminal for Muting of weak input, either ON or OFF. It is "H" for OFF.
30	VOL UP	Volume UP signal output terminal from remote control. Active high.
31	VOL DOWN	Volume DOWN signal output terminal from remote control. Active high.
32-44	LCD23-11	No connection.
45-55	LCD10/KS10 LCD0/KS0	These are the output terminals for key return signal source. "H" when active.
56, 57	COM1, COM2	Not used.
58	GND	Ground terminal.
59	K3	These are the input terminal for key return signal source and diode matrix.
60	K2	
61	K1	
62	K0	
63	SLEVEL	Station signal level input terminal.
64	REMOTE	System code input terminal from remote control. Active at the leading edge.

5-3. Explanation of momentary key

Output \ Input		59	60	61	62
		K3	K2	K1	K0
55	LCD0		PRESET SCAN	AUTO MEMORY	AUTO/MENU
54	LCD1	HI-BLEND	AUTO/MONO	IF	RF
53	LCD2	ANT	SIGNAL DISPLAY	TUNING LEVEL	MEMORY
52	LCD3	M4/M14	M3/M13	M2/M12	M1/M11
51	LCD4	M8/M18	M7/M17	M6/M16	M5/M15
50	LCD5		PRESET REVERSE	M10/M20	M9/M19
49	LCD6	AM	FM	UP	DOWN
48	LCD7		PROGRAM DISPLAY	APR	PROGRAM
47	LCD8	REM10	DISPLAY	AM1	AM0
46	LCD9	PRESET16	FM ONLY	FM1	FM0
45	LCD10	SYSTEM	ANTA	ANTAPRD	ANTMEMO

AUTO/MANUAL
Selector key for AUTO TUNING/MANUAL TUNING Causes reversal of AUTO/MANU.
"H" when AUTO.

AUTO MEMORY
When the AUTO MEMORY key is pushed, "MEMORY" is displayed for 5 seconds, and during this, if the PRESET STATION key is pushed, AUTO SCANNING begins. The SD signal is above the tuning level preset from memory for that station.
At this time the APR data is also stored in memory. If the station key is pushed within 5 seconds, the memory display is cleared, and the condition for memory possibility is cancelled.
Example: A 90.10MHz signal is being received. The AUTO MEMORY key is pushed, and if within 5 seconds key M3 is pushed, continuous UP feed is carried out, and if a station is received, the M3 preset channel display is executed. If there is a 1 second stop, the UP operation starts again. In the manner shown below, the data is stored in memory for M4 and successive positions in sequence up to 108.00MHz, and when scanning is completed, at the final memory station call out, the automatic memory operation is completed.



At frequencies above 90.10MHz, when there are no broadcast stations, if the data of M2 is called out, the automatic memory operation stops. In the case of starting from M1, the lower limit frequency of 87.50MHz is called out and the operation stops.

PRESET SCAN
Every 5 seconds the preset memory data is received with a sawtooth mode in the up direction. At this time, the preset station display (FL tube and LED) blinks at 1Hz. If at that time there is preset reception, after the next preset, if there is no preset reception, scanning occurs from M1.

If, during the above operation, any key is pushed, the scan stops, and that key's operation is carried out. When the PRESET SCAN key is pushed, the operation is cancelled.

RF
With the RF selector key, the LOCAL/DX output can be reversed.
The level is "H" when in DX.

TUNING LEVEL – Tuning level selector key
When this key is pushed, after the display of about 1.5 seconds, the present tuning level (when RF=LOCAL, a value of 10dB) the display returns to the original value.

During the tuning level display, if the TUNING LEVEL key is pushed, the display will appear for about another 1.5 seconds. Also, during this display, the TUNING output goes "H". During this interval, when another key is pushed, the display returns, and that key's operation is carried out.

UP/DOWN – Receiving channel UP/DOWN key
(I) Manual tuning mode
Each time the UP(DOWN) key is pushed, the frequency is raised (lowred) one step.
Also, if the key is pushed continuously for more

than 0.5 second, up to the time the key is released, continuous stepping will be carried out at about 80msec/step (in the FM band with 25kHz step, at about 50msec/step).

(II) Auto tuning mode
When the UP(DOWN) key is pushed, continuous feeding is carried out. At that time, APR functions, and the conditions required for AUTO TUNING steps are carried out.
The scanning sped is about 100msec/step.

During scanning, if the same direction UP/DOWN key is pushed, the scanning continues, and when any other key is pushed, the scanning stops, and that key's operation is carried out.

PROGRAM – Program mode setting key
When the program mode is ON, at the time of power being turned ON, the preset memory (M1-M5) is called out in sequence. (After M5, the sequence is repeated starting again with M1.)

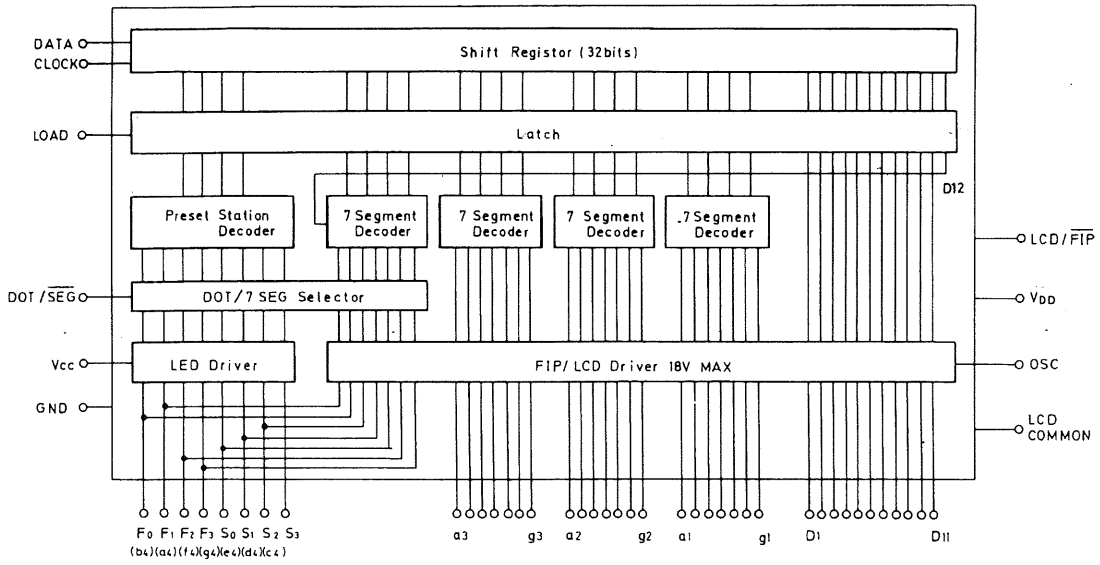
APR – APR execution key
Each time this key is pushed, the APR is executed one time.

PROGRAM DISPLAY
In the program mode, this key is used in order to confirm the next preset memory to be called out. Accordingly, this used only in the program mode.

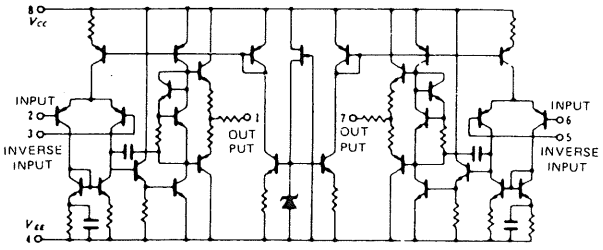
If this key is pushed while in the program mode, the preset memory to be called will be called when CE next goes from "L" to "H".

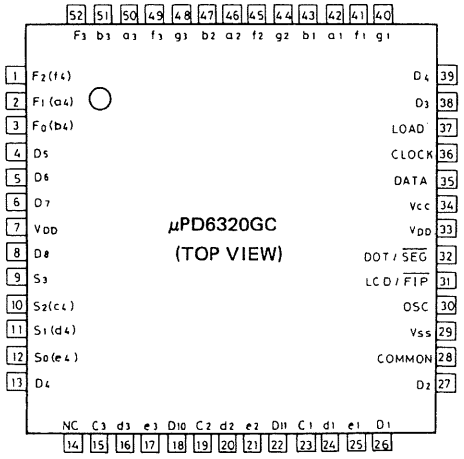
IC BLOCK DIAGRAM

μPD6320GC (Indicator drive)

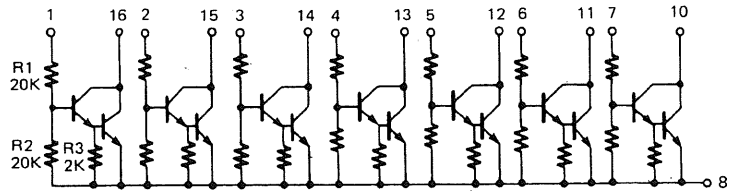


NJM4560D (Operation amplifier)

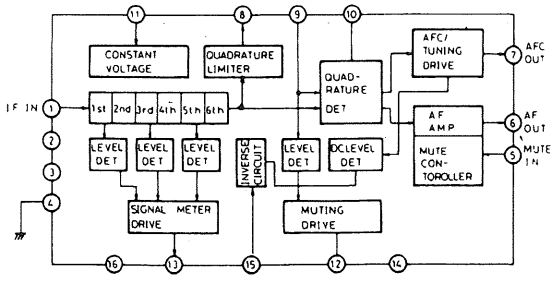




μPA81C (Buffer/Inverter)

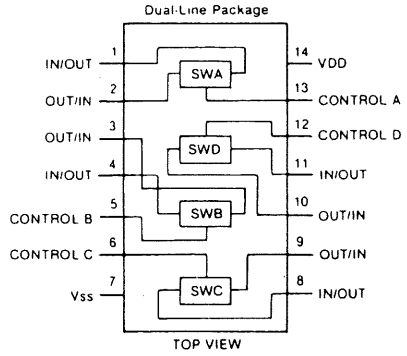


LA1235 (FM IF system)

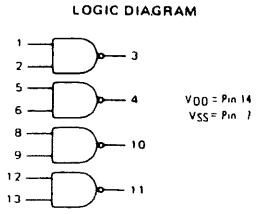


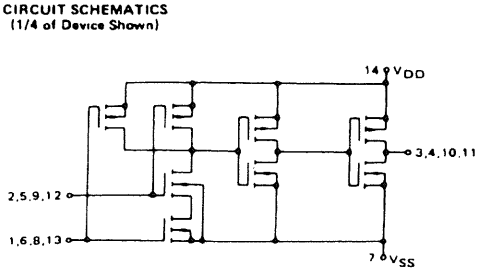
1. IF signal input
2. IF amplifier switch input
   H level: Off
5. Muting switch input
6. Composite signal output
7. AFC output
8. IF amplifier output
9. 10.7MHz input
10. Reference voltage
11. Power supply
12. Muting output
    Tuned: L level
13. Signal strength output
15. Muting level

4066B (Analog switch)

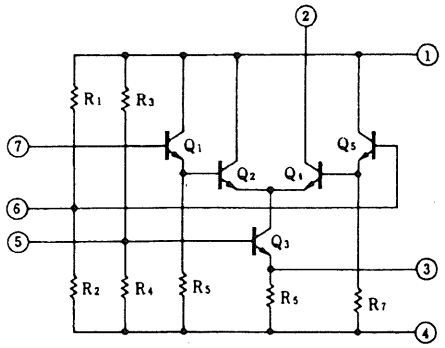


4011B (NAND gate)





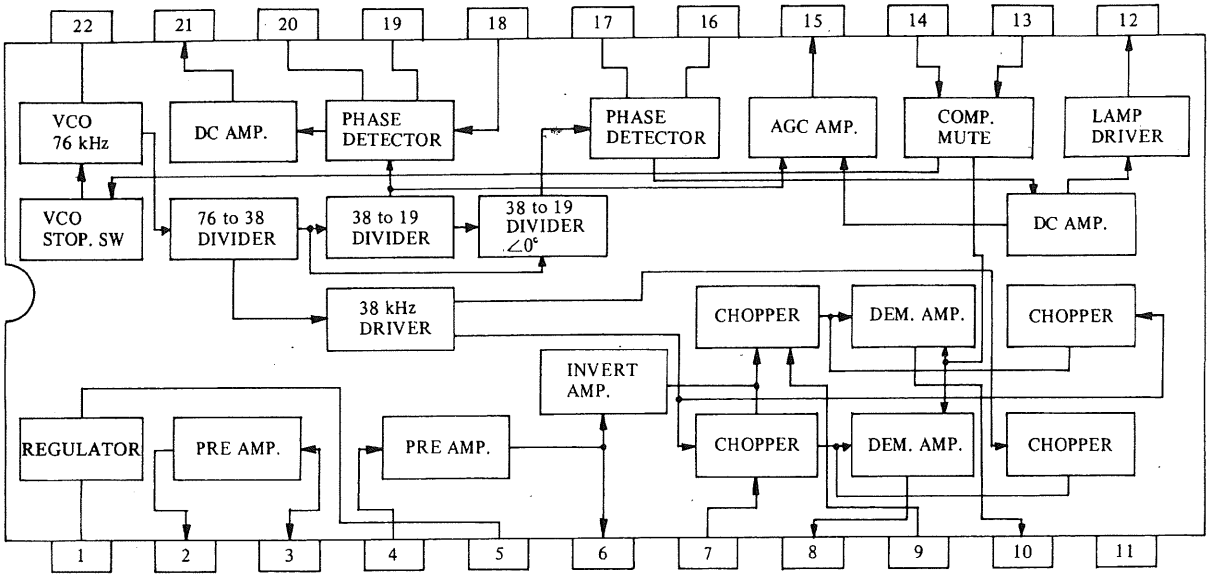
μPC1163H (RF amplifier)



Terminal No.	Operation
1	Vcc
2	OUTPUT
3	BYPASS
4	GND
5	BYPASS
6	INPUT BIAS
7	INPUT

μPC1223C (Stereo decoder)

Block diagram



Terminal No.	Connection	Terminal No.	Connection
1	Vcc	12	ST. LAMP INDICATOR
2	PRE AMP. OUTPUT 1	13	ST–MONO SW & VCO STOP
3	PRE AMP. INPUT 1	14	MUTING SWS
4	PRE AMP. INPUT 2	15	19kHz CANCEL
5	BYPASS	16	LPF
6	PRE AMP. OUTPUT 2	17	LPF
7	POST AMP. INPUT	18	FILTER INPUT
8	L–ch OUTPUT	19	LPF
9	POST AMP. INPUT	20	LPF
10	R–ch OUTPUT	21	LPF
11	GND	22	OSC RC NETWORK