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mmWave communications for 5G: implementation challenges and advances

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Abstract The requirement of the fifth generation (5G) wireless communication for high throughput motivates the wireless industry to use the mmWave (millimeter wave) communications for its wide bandwidth advantage. To compensate the heavy path loss and increase the communications capacity, phased array beamforming and massive multiple-input multiple-output (MIMO) techniques are employed at both the user equipment (UE) and base stations (BS). Considering the commercial requirements, 5G mmWave large array systems should be implemented in an energy- and cost-efficient way with a small form factor. To address above issues and realize a reliable communications link, taking into account the particular characteristics of 5G mmWave systems, this paper firstly examines the design challenges and trade-offs in system implementations, then some of the design strategies are summarized. At last, recent advance in RF front-end circuits and receiver sub-systems is then highlighted.

Keywords millimeter wave, massive MIMO, beamforming, hybrid precoding, channel estimation, phased array, power amplifier, voltage controlled oscillator (VCO)

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1 Introduction

Driven by surging wireless data traffic, mmWave communications have become a key enabler for 5G systems. Different from the crowded sub-6GHz band [1], mmWave spectrum has a massive amount of raw bandwidth [2], and high data rate can be achieved with low order modulation. Recently, several licensed and unlicensed 5G mmWave candidate spectra (from 24 to 86 GHz) have been selected by world radiocommunication conference 2015 (WRC-15) and federal communications commission (FCC), pushing forward the 5G mmWave commercial deployment progress [3, 4][1)].

Today, 5G mmWave communications are at the turning point from concept to implementation. The major associated technical challenges we are facing now are much less favorable channel propagation property and radio frequency (RF) front-end performance. Due to the high operating frequencies, there is a heavy propagation path loss, and the air interface performance is typically limited by that of RF front-end circuits and antenna. On the other hand, there still exist some implementation opportunities. As the

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1) FCC website. http://wireless.fcc.gov/.

wavelength becomes smaller, a large antenna array can be realized in a compact size. Accordingly, a directive communication can be realized with electronically-steered beamforming operation, compensating the propagation loss and increasing the coverage. With the beamforming techniques, on one hand, the performance requirements on each antenna and RF circuit can be relaxed, while on the other hand, the in-band interference can be greatly suppressed [5,6]. With above attributes, MIMO and beamforming can be employed at both the user equipment (UE) and base station (BS) to increase the link budget robustness [7], serving several users simultaneously and achieving high energy and spectral efficiency [3,6,8–10]. To fully exploit the antenna array performance and achieve commercial success, it is important to realize the 5G mmWave system in an energy- and cost-efficient way with a small form factor. This implies that the mmWave RF transceiver should be implemented as compact as possible .

The above issues call for innovation in system architecture and circuit design. This paper firstly summarizes the design challenges, trade-offs and strategies in the 5G mmWave system implementation, including technology choice, phased array architecture. In Section 3, the hybrid precoding and channel estimation for mmWave systems will be discussed. In Section 4, recent advances in the RF front-end circuits and sub-system are highlighted.

2 System implementation

In terms of link budget, the 5G mmWave air interface performance is dominated by that of RF front-end circuits, such as transmitter output power, receiver noise figure and phase locked loop (PLL) phase noise [11]. Normally, these performance limits and requirements are determined by the implementation technology and system architecture, respectively. Due to the performance limitations, during the design process both bottom-up and top-down iterative optimization methods should be used to balance the RF circuits performance. From the system point of view, the precoding and channel estimation are also essential. During the channel estimation, the phase and weight of each channel are worked out, leading to a large antenna array gain and establishing the communication link.

2.1 Implementation technology

With the advantages in electron velocity and electron mobility, III-V materials, like GaAs, are typically used to realize the mmWave circuit and system. However, due to the penalty of low integration level, high power consumption and high cost, it is not suitable to realize 5G systems using the GaAs process. In contrast, the consistent Moores law scaling of silicon has improved the transistor speed and integration level substantially, and the silicon process has now nudged into the traditional mmWave territory occupied by GaAs process.

Today, by leveraging recent advances in silicon process, several fully integrated mmWave systems have been reported. Broadcom reported a 60 GHz phased array system implemented in a 40 nm CMOS, achieving a data rate of 4.6 Gb/s over 10 meters' distance [12]. Together with Ericsson, using silicon process, IBM realized a 28 GHz four-chip phased array transceiver system, in which each chip contains a 32-element (dual-polar: H and V). As a result, the system can support eight concurrent 16-element beams [13]. It should be noted that the most important characteristic of those systems is that all the RF front-end and analog building blocks are integrated with digital control functions. In this way, the functionality and performance of the phased array and MIMO system can be preserved, which can relax the implementation space constraint and save the power consumption. Moreover, the matching among the channels can be improved to increase the system reliability.

In general, the transistor supply voltage and intrinsic gain will reduce with CMOS scaling [14]. This will affect the RF front-end circuit performance. For example, it is difficult to use stacked-device based topologies with limited voltage swing. At the meantime, the transistor output power becomes lower. Accordingly, various power combing techniques, e.g. parallel- and series-power combing, are needed to improve the power amplifier (PA) output power [15]. Moreover, different from sub-6GHz system, the 5G mmWave system is dominated by passive elements. In addition to active devices, special attention

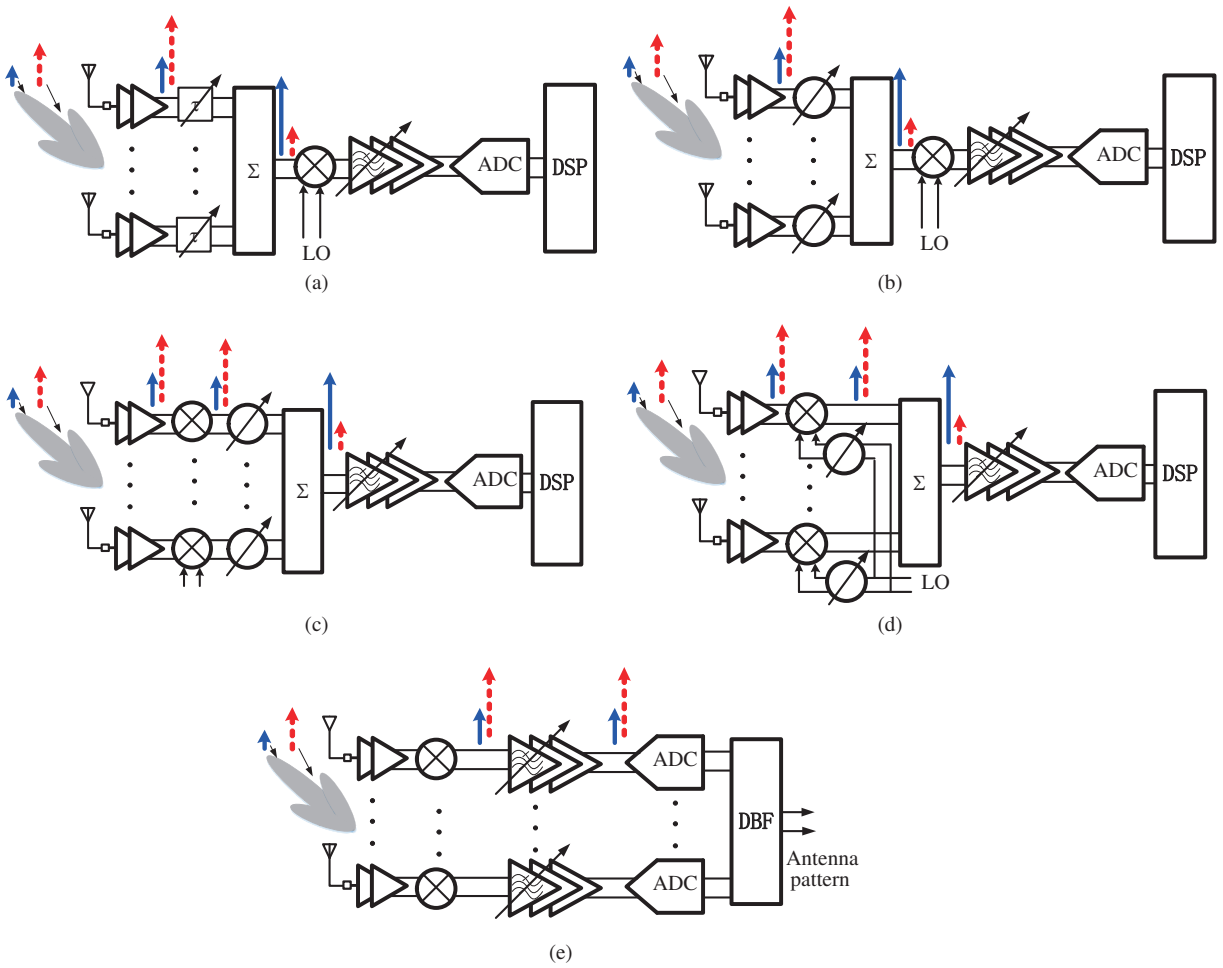

Figure 1 (Color online) The phased array system (the transmitter part is not shown for simplicity; the blue line represents desired signal while the red dashed line interference; note the arrow height represents the signal strength). (a) True time delay based; (b) RF-path; (c) IF-path; (d) LO-path; (e) digital beamforming.

should be paid to the silicon back end of line (BEOL) performance. As will be shown in Section 4, design strategies to improve the passive elements performance and matching networks become crucial, which highly depend on specific circuit topologies.

2.2 Phased array system architecture

In principle, beamforming can be realized with wideband true time delay element, assigning a dedicated delay time to each specific antenna array element. As shown in Figure 1(a), coherent functionality of the antenna array is realized with a time delay and sum function, leading to an antenna pattern with a specific gain, sidelobe and nulling performance. Clearly, the desired signal (in blue) and interference signal (in red dashed) can be enhanced and suppressed, respectively. As a result, the system coverage is increased and the in-band interference relaxed.

If the ratio of modulation bandwidth to the carrier frequency is small, the delay time in each antenna element can be replaced by a phase shift, leading to phase shifter based beamforming techniques, as shown in Figure 1(b)–(e). As the phase shifter is inherent narrow band, compared with a wideband time delay element, it is easier to be implemented, and accordingly widely accepted in the present phased-array systems [16]. To make the phased array system work properly, it is very important to have an orthogonal control of the phase and amplitude response in each channel [13]. In other words, the beam direction should remain the same if the beam shape is changed by channel weighting. On the contrary, the beam shape should remain the same if the beam direction is changed by the phase shifter.

As shown in Figure 1(b)–(e), depending on the phase shifter position, the phased array system can be categorized into four types: RF-path, intermediate frequency (IF)-path, local oscillator (LO)-path and digital beamforming [16, 17]. As discussed below, in terms of system performance and implementation complexity, they have all their own particular advantages and disadvantages.

2.2.1 *RF-path beamforming*

Figure 1(b) shows the RF-path beamforming structure. With a RF phase shifter and power combiner, the spatial filtering on the incident signal is realized. To be specific, the desired RF signal is added coherently, while the in-band strong blocker is suppressed before reaching the down-conversion mixer. In other words, the mixer sees high directivity signal pattern. As the mixer is typically the bottleneck of the receiver linearity, the in-band desensitization issues can be relaxed substantially with this structure, improving the receiver dynamic range and reducing the power consumption. Moreover, as most of RF front-end components, except the low noise amplifier (LNA) and phase shifter, are shared, the RF-path beamforming structure is very compact and scalability friendly. It is suitable to realize the system with channels of 100 or even higher.

Despite above advantages, since the phase shifter and RF power combiner is in the RF signal path, their design is not trivial. Typically their bandwidth and insertion loss affect heavily the overall transceiver performance.

2.2.2 *IF-path beamforming*

Figure 1(c) shows the IF-path beamforming structure, where the phase shifter is in the IF signal domain and its working frequency is lower than its RF-path counterpart. Accordingly, the IF phase shifter can be constructed using precision analog techniques, such as the vector modulation and switch capacitor techniques. In this way, its loss and bandwidth performances are better [18]. However, albeit above advantages, the number of mixers is the same as that of the channels, while the mixer sees a low directivity pattern [17]. As a result, the power consumption and linearity performances become worse, and the LO routing complexity increases.

2.2.3 *LO-path beamforming*

As shown in Figure 1(d), the phase shifter is realized in the LO path. Similar to the IF-path beamformer, an IF power combiner is used to sum up the incident signal, creating spatial signal filtering for the following IF and baseband circuits. Similar to the IF counterpart, LO-path beamforming has many mixers, which makes the LO distribution power hungry and very complex. In general, this will increase the channels coupling, incurring signal amplitude and phase errors. As a result, it is difficult to realize the large phased array with an IF- or LO-path beamforming.

An interesting attribute of the LO-path beamforming is that the phase shifter is operating at a single tone. So its bandwidth performance is not important. Moreover, the phase shifter can work in saturation region, relaxing its linearity requirements.

2.2.4 *Digital beamforming*

First introduced by Thales Group about 25 years ago, now digital beamforming has become technically and economically feasible, with the advances of analogue electronics as well as digital signal processing [19]. Different from above structures, all the beaforming signal processing circuits are realized in the digital domain, which makes it very easy to realize flexible beam patterns. Interestingly, each signal path has its own ADC/DAC, and the system can support multiple beams and MIMO operation. However, such architecture has several disadvantages, such as low instantaneous bandwidth and large hardware overhead, increasing the area and power consumption. Moreover, as the in-band interference is not filtered until the digital domain, the requirements for the analog-to-digital converter/digital-to-analog converter (ADC/DAC) resolution and RF linearity are stringent [17].

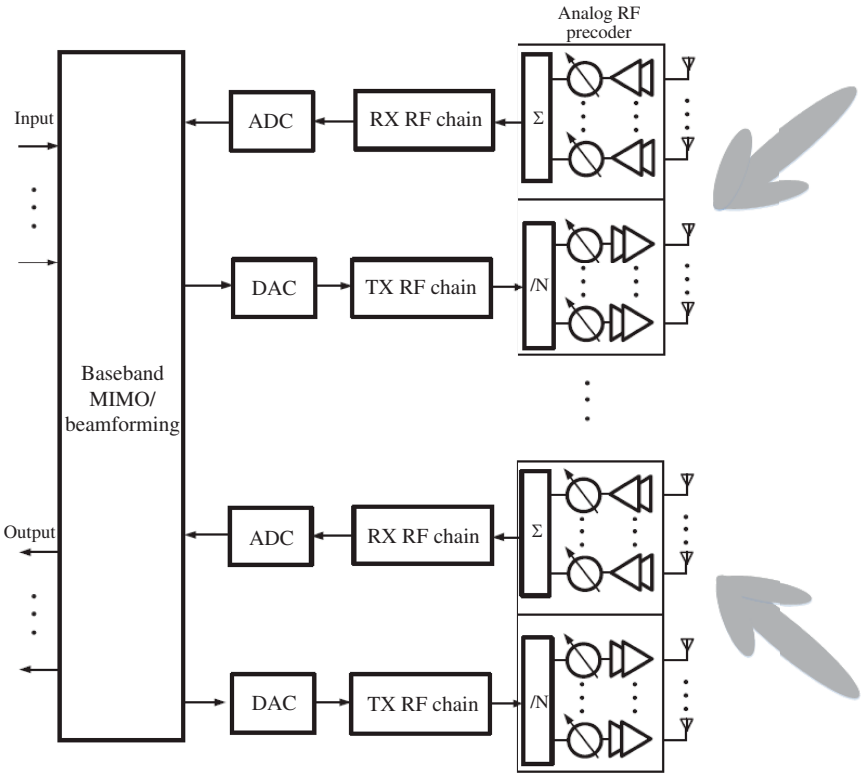

Figure 2 Hybrid RF/Baseband MIMO architecture.

2.2.5 *Direct conversion or dual conversion?*

There are two popular mmWave transceiver architectures: direct conversion and dual-conversion [14, 20, 21]. The direct conversion has the advantages of compact area and operation flexibility. However, as its modulation/demodulation circuits have very high operating frequency and are vulnerable to device imperfection, the direct conversion has severe non-idealities, such as transceiver in-phase and quadrature-phase (IQ) mismatch and LO feedthroughs. In addition, the quadrature PLL suffers from worse phase noise, large phase error, small tuning range and pulling issues. According to system simulations, these issues have a strong impact on the mmWave phased array and MIMO system design. Intensive calibration is therefore viewed as an indispensable part of the direct conversion, increasing the system complexity. As an alternative solution, the dual conversion architecture has attracted much attention. It allows in principle to remedy the device imperfection to a certain extent and enhances circuit performance by reducing the working frequency of the modulator/demodulator and PLL [14].

3 Hybrid precoding and channel estimation for mmWave MIMO

3.1 Hybrid precoding

In the 4G system, every antenna has its own RF chain, AD/DA and baseband circuits, which substantially increases the complexity, power consumption and cost of the system. In mmWave MIMO system, to address above issues, not all of the antennas have their own RF chain. Therefore, hybrid analog/digital architectures have been proposed to reduce the number of RF chains [9]. Such architecture is very suitable for making scalable array systems. As shown in Figure 2, in the transmitter part, the data streams are firstly processed by a digital precoder. Then the signal is up-converted to RF frequency and mapped via a phase shifter network to all the antennas for transmission. At the receiver side, an analogy power combiner combines the signal from the antennas. Then the signal is down-converted to the baseband and passes through a digital combiner matrix. The main challenge in the design of the

hybrid analogy/digital architecture is that even with perfect channel state information (CSI) the optimal analogy and digital beamforming matrices, which maximize the capacity, are still very difficult to obtain. To overcome these problems, researchers have studied some special hybrid beamforming schemes, either for single-user MIMO (SU-MIMO) or multi-user MIMO (MU-MIMO).

3.1.1 *SU-MIMO*

Exploiting the sparse nature of mmWave channels, low-complexity hybrid precoding algorithms were proposed in [22] to accurately approximate the spectral efficiency achieved by fully-digital precoding. With some approximations, the hybrid precoding design problem was formulated as

$$\begin{aligned} \min_{\boldsymbol{F}_{\mathrm{RF}},\boldsymbol{F}_{\mathrm{BB}}} \quad & \|\boldsymbol{F}_{\mathrm{opt}}-\boldsymbol{F}_{\mathrm{RF}}\boldsymbol{F}_{\mathrm{BB}}\|_F, \\ \text{s.t.} \quad & \boldsymbol{F}_{\mathrm{RF}}\in\mathcal{A}, \quad \|\boldsymbol{F}_{\mathrm{RF}}\boldsymbol{F}_{\mathrm{BB}}\|_F^2=N_s, \end{aligned} \tag{1}$$

where the first constraint is due to the hardware constraints on the RF precoding matrix, which limits it to a certain set of precoding matrix $\mathcal{A}$. The second constraint is a power constraint. Then the problem of mmWave precoder design was formulated as a sparsity-constrained signal recovery problem, which could be solved by orthogonal matching pursuit. Following [22], the study in [23] developed four efficient methods that provide different trade-offs between computational complexity and spectral efficiency. These methods differ in the proposed optimization techniques, which are dependent on assumptions on the number of RF chains and on the structure of the analog and digital beamforming matrices.

Unlike existing studies, which add some extra constraints on analog precoders to simplify the analog part design, it was demonstrated that the unit modulus constraints of the analog precoder simply define a Riemannian manifold [24]. Based on this Riemannian manifold, effective alternating minimization algorithms were proposed for the fully-connected and partially-connected structures, respectively. Since most hybrid precoding techniques focus on a fully connected architecture, where a large number of phase shifters consume intensive energy, a more energy-efficient hybrid precoding with a sub-connected architecture was analyzed in [25]. Furthermore, the idea of successive interference cancelation for multi-user signal detection was creatively brought into the hybrid precoding design.

3.1.2 *MU-MIMO*

The antenna arrays can also be utilized to support MU-MIMO, where users share the same time/frequency resources [26]. To enable efficient multi-user precoding processing in mmWave systems, a two-stage hybrid precoding technique was proposed in [27]. In the first stage, RF precoder at BS and RF combiners at mobile station (MS) are jointly designed to maximize the desired signal power of each user, neglecting the resulting interference among users. In the second stage, the BS digital precoder is designed to manage the multi-user interference. If both the BS and MSs have multiple RF chains, a low-complexity hybrid block diagonalization (Hy-BD) scheme was proposed to approach the capacity performance of the traditional BD processing method [28]. The advantage of the proposed Hy-BD scheme is that its heuristic RF precoder design method can achieve large array gain and the BD processing performed on the equivalent baseband channel has low complexity.

Following [29], with a hybrid structure that the number of RF chains should be twice the total number of data streams, the work in [30] extended the requirement for realizing fully digital beamforming. For cases with fewer number of RF chains, an iterative coordinate descent algorithm was devised over the elements of the RF precoder. Then zero-forcing (ZF) beamforming with power allocation was adopted as a low-dimensional digital precoder to manage the inter-user interference. Furthermore, by replacing the channel covariance matrix in the flat-fading scenario with its average over all subcarriers, the algorithm in [30] for designing the analog precoder can be also applicable to mmWave orthogonal frequency division multiplexing (OFDM) systems over frequency-selective fading channels [31].

3.1.3 *Further research directions*

The performance of the above hybrid beamforming design methods highly depends on the accuracy of channel estimation. Since the statistics of mmWave channels remain unchanged for a long time [32], the effectiveness of statistical hybrid beamforming should be further studied [23, 33]. Besides, as mentioned in Subsection 2.2, the imperfect of the RF transceiver, such as I/Q imbalance, phase noise and RF calibration error [34–36], will degrade the performance of the beamforming/combiner, and brings serious influence to CSI acquisition. To eliminate the negative influence of non-ideal hardware, robust hybrid beamforming schemes [37] should receive more attention.

3.2 Channel estimation

In mmWave MIMO systems, the CSI acquisition becomes a tough challenge due to the limited RF chains. Thus, the widely used hybrid beamforming structure makes the channel measured in the digital domain, intertwined with analog precoding and combining vectors [38]. Different from the traditional MIMO system under 6 GHz, to overcome the large path loss of mmWave channels, the access point (AP) is usually equipped with massive antennas to extract the huge array gain. As omni-direction pilot is usually not adopted subject to the link budget, the CSI acquisition is then usually divided into two steps. Before network startup, the receiver has no knowledge of the transmitter's direction, therefore beam alignment should be done first [39]. Helped by the beam alignment, the time-frequency synchronization of the system is then achieved. During the data transmission, the CSI should be estimated to obtain the optimal receiver.

3.2.1 *SU-MIMO*

To reduce the beam training overhead, a divide-and-conquer searching work was carried out across a hierarchical multi-resolution codebook [40]. Based on this hierarchical codebook, an adaptive compressed sensing (CS) method was then resorted to effectively estimate the sparse mmWave channel. The core idea of this adaptive CS based channel estimation algorithm is to divide the training process into a number of stages. Depending on the output results of previous stages, the training beam is selected at next stage. Compared to standard CS methods, the adaptive CS approach yields better performance at low SNR, which is very suitable for mmWave communication. To further reduce the number of RF chains needed for very-wide codewords, a novel hierarchical codebook was designed, taking into account the per-antenna power constraint [41]. Incorporating both the flatness of beam pattern and the maximal transmission power, a metric called generalized detection probability was then proposed to evaluate the quality of an arbitrary codeword. Compared to [40], the training overhead can be decreased by a factor of the number of RF chains, with help of the parallel transmission of multiple training sequences. Also motivated by [40], based on a set of innovative overlapped beam patterns, a fast mmWave MIMO channel estimation framework was developed to speed up the CSI acquisition process [42]. However, since the overlapped beam patterns are used to facilitate the channel estimation, the AoAs and AoDs should be on the discrete grids. This is the main drawback in [40]. Due to the low-rank property of mmWave channels, only a few eigenmodes are needed for transmission. Relying on the well-known Arnoldi iteration, the approach in [43] exploited the time division duplexing (TDD) channel reciprocity and channel sparsity to directly estimate the dominated eigenmodes rather than the whole channel.

Different from the above closed-loop beam training based methods [40–43], which is a multi-stage process that can avoid an exhaustive beam search, a CS based open-loop channel estimator was applied in the parametric channel model with quantized angle grids [44]. Since the RF beamformer prevents the use of independent and identically distributed random training vectors, efficient pilot beam patterns were designed to minimize the total coherence of the equivalent sensing matrix.

3.2.2 *MU-MIMO*

Due to a higher Doppler shift, the coherence time for the mmWave bands is much shorter than the time needed in the traditional sub-6 GHz bands [45]. Thus, it is crucial to reduce the training overhead for multi-user transmission in mmWave systems. With random beamforming, a CS based channel estimation approach was able to carry out simultaneous downlink channel sounding for multiple users [46], and the training overhead did not scale with the number of users. Through simulations, the optimal number of channel measurements to maximize the achievable rate was shown for different values of channel fading coherence. However, as each user has its own channel characteristic to the BS, adopting a fixed number of channel measurements for every user may not work well. Therefore, to adaptively determine the training duration of each user, based on the respective channel condition, [47] developed a novel simultaneous estimation with iterative fountain training framework. In this framework, the random beamforming process was optimized by matching the beam-on-graph to a code-on-graph. This solves the channel estimation problem by a generalized approximate message passing algorithm [48]. Apart from these CS-based narrow-band channel estimation schemes, the first work to investigate frequency selective fading mmWave channels was published in [49], where a distributed CS uplink channel estimation method was proposed and the pilot signals were appropriately designed.

Recently, as a powerful tool for multi-way signal processing, mutli-linear tensor algebra has been applied in uplink channel estimation for mmWave MU-MIMO systems [50]. With a proposed layered pilot transmission scheme, where the training phase consists of a number of frames and each frame is divided into a number of sub-frames, the received signal at the BS could be transformed into a third-order tensor. By means of CANDECOMP/PARAFAC (CP) decomposition, the multi-user channel acquisition was formulated as a tensor decomposition problem. Exploiting the intrinsic low-rank property of the tensor, as a result of the sparse scattering nature of mmWave channels, the uniqueness of the CP decomposition was guaranteed, and the proposed method was able to achieve a substantial training overhead reduction. Afterwards, the CP decomposition was extended to downlink multi-user channel estimation for mmWave MIMO-OFDM systems [51].

Since the channel covariance matrix keeps almost stationary over a considerable number of frames relative to the fast fading component, the channel between the k-th user and the BS in each frame can be expressed as $\boldsymbol{h}_k = \boldsymbol{R}_k^{1/2}\tilde{\boldsymbol{h}}_k$, where the entries of $\tilde{\boldsymbol{h}}_k$ are modeled as i.i.d zero mean circularly symmetric complex Gaussian random variables with unit variance. This statistical channel model can be utilized both for mmWave and microwave applications. With a novel hybrid analog/digital structure [52] in the BS, where each element of an analog precoder was equivalently expressed as a sum of two digitally controlled phase shifters, a minimum mean squared error channel estimator was developed for mmWave MU-MIMO systems by considering both perfect and imperfect channel covariance matrix cases [53].

In recent field tests, especially in the urban microcell environments, both strong line-of-sight (LOS) and non-negligible scattering components could exist in mmWave channels [54]. Inspired by signal processing in mono-pulse passive electronically scanned array radar and sonar systems, unique unmodulated frequency tones were introduced to estimate the strongest incident paths at the BS and user sides [55]. After that, to facilitate the equivalent channel estimation, all users transmit orthogonal pilot symbols to the BS along the beamforming paths of the strongest angle of arrival (AoA) directions.

3.2.3 *Further research directions*

Due to the issues of channel measurements through limited RF chains, extensive training burden and quick channel variation, it is difficult to directly apply conventional MIMO channel estimation techniques in mmWave systems with hybrid structure [38]. Further promising work may lie in following aspects. To begin with, the relatively slow variation in the angular domain is a strong motivation for considering direction of arrival (DOA) based channel estimation [56]. Apart from that, practical strategies should be presented to mitigate pilot contamination effect [57], which causes severe inter-user or inter-cell interference. In mobility scenario, the BS needs to perform beam training frequently to track time-varying channels of users, thereby spending significant training beams. Therefore, another interesting aspect for

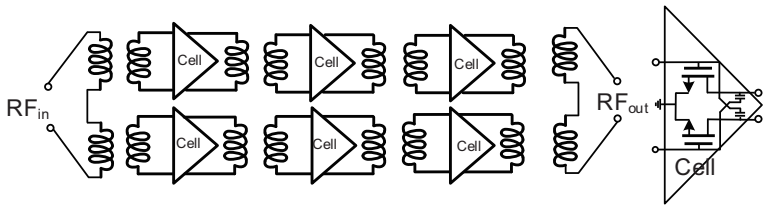

Figure 3 Schematic of the three-stage power amplifier with 4-way power-combining.

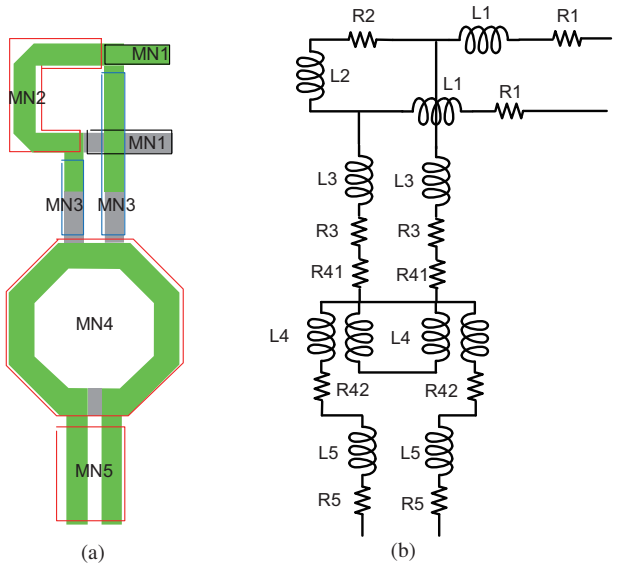

Figure 4 (Color online) (a) The proposed inter-stage matching network and (b) its equivalent circuit.

mmWave channel estimation will be fast beam tracking techniques [58, 59].

In the implementation of phased array and MIMO system, the characteristic of RF front-end circuits should be taken into account during the design of the beam precoding and channel estimation. Therefore, in Section 4, we will present the RF circuits design challenges and recent advance.

4 RF front-end circuits realization

4.1 Power amplifier

As the most power-consuming component of the RF transceiver, the PA plays an important role, particularly in terms of the system coverage and overall power efficiency [60]. With benefits of multi-antenna array, a large coverage can be achieved by using PA with moderate output power. However, as the PA working frequency is high, its output power and power efficiency performance is poor with a limited supply voltage and large parasitic. Typically, a transmission line based Wilkinson power combiner can be used to increase PA output power. But this kind of power combiner is bulky and lossy. Recently, transformer based power combing emerges as an effective solution. However, this method results in a higher insertion loss and worse bandwidth performance due to high impedance transformation ratio.

To address above issues, as shown in Figure 3, a 3-stage 60 GHz power amplifier is designed using a transformer-based 4-way power combiner [61]. To reduce the intrinsic metallization loss, the transformer is realized with top thick metal layers. As noted before, the impedance matching network is very important for the overall RF circuit performance. In this design, a shunt inductor is added in between the second stage and third stage, realizing the proposed inter-stage matching network, as indicated in Figure 4. Figure 5 shows the comparison of Smith Chart trajectories of the impedance matching networks, without and with the shunt inductor. Clearly, with the inductor, the input impedance of the third stage rotates

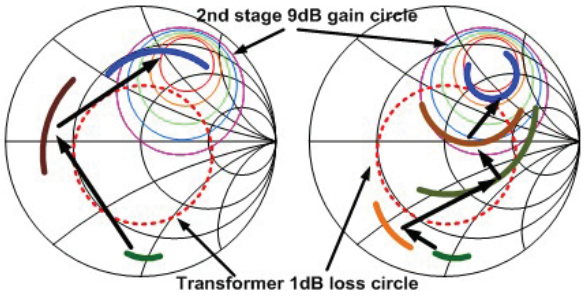

Figure 5 (Color online) Comparison of Smith Chart trajectories of the impedance matching networks, without and with the shunt inductor.

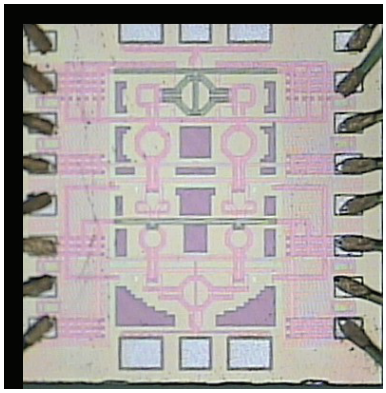

Figure 6 (Color online) Micrograph of the PA.

and falls into the 9 dB gain circle center of the second stages. Simulations prove that the insertion loss of the impedance matching network is improved by more than 1.5 dB. The PA bandwidth performance is also increased.

In the PA design, stability is an important concern. In this design, the capacitive neutralization technique is used in every PA stage, increasing the reverse isolation and GMAX. Accordingly, the PA stability and power added efficiency (PAE) performance is improved.

Figure 6 shows the chip photo. With a 65 nm CMOS process, the PA core area is only 0.68 mm $\times$ 0.88 mm. With the introduced inter-stage matching network and capacitive neutralization technique, tested results show that the PA achieves more than 20 dB S21 from 54 to 65 GHz. With a 1 V power supply, the PA achieves Psat/P1dB/PAE of 18 dBm/14.8 dBm /13.2% at 61 GHz.

At last, it should be noted for 5G high data requirements, high order modulation scheme with high PAPR, e.g. 64-QAM, will be used. This poses stringent requirements on the PA linearity and efficiency performance, which needs to be studied further.

4.2 VCO and frequency divider

As the key block of RF transceiver, the frequency synthesizer is used to provide a periodic high performance LO signal, which is capable of realizing the frequency up- and down-conversion processes. In principle, the frequency synthesizer plays a critical role in the system frequency planning and architecture [62]. To fulfill the requirement of high-order wideband modulation for 5G mmWave communication, subject to the power consumption constraint, LO signal should achieve low phase noise, low spur and wide tuning range performance. However, due to very high operating frequency, the LO performance is typically limited by the voltage controlled oscillator (VCO) and frequency divider. In this section, the design considerations of the VCO and frequency divider will be highlighted, and recent achievements will be presented.

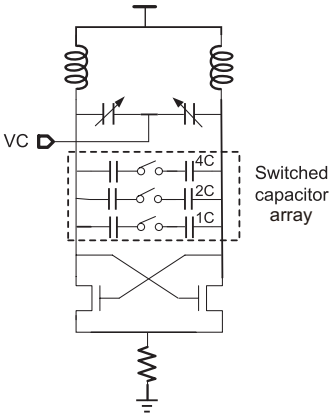

Figure 7 Switch-capacitor based VCO structure.

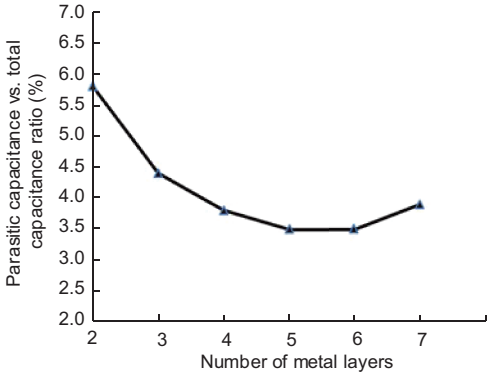

Figure 8 Parasitic capacitor ratio of the MOM capacitor vs. number of metal layers.

4.2.1 *Oscillator*

As an essential building block of a frequency synthesizer, mmWave VCO is facing several design challenges due to very high operating frequency [63].

First, as the VCO operating frequency is close to the transistor maximum oscillation frequency (f_{MAX}), the active transistor gain is low and the VCO output power is limited. Large transistor is therefore needed to satisfy the oscillation start-up condition. Secondly, the varactor has a very poor tuning ratio (i.e. $C_{\max}$ to $C_{\min}$ ratio) and a low quality factor, which will degrade the VCO tuning range and phase noise performance.

As shown in Figure 7, instead of using varactor for the LC tank coarse tuning, switch capacitor structure is utilized to address above issues [64]. Because of higher quality factor than other solutions, metal-oxide-metal (MOM) capacitor is used in this design. During the design, the switched capacitor is optimized in terms of its quality factor and parasitic capacitance ratio. Figure 8 shows the simulated ratio of the parasitic capacitance over the total MOM capacitance value. Clearly, with 5 metal layers, a compromise between the capacitor area and quality factor is achieved.

Note here to take advantage of dual-conversion transceiver structure, targeting at 60 GHz application, the VCO center frequency is set to 48 GHz. Moreover, NMOS transistors are used for their better mmWave performance, and a tail biasing resistor is chosen to suppress the flicker noise up-conversion.

With a 65 nm CMOS process, the proposed VCO achieves a tuning range from 43.9 to 49.7 GHz, consuming about 5.5 mA from a 0.9 V supply. Its phase noise is -100 dBc/Hz at 1 MHz offset from 49.7 GHz.

4.2.2 *Frequency divider*

The frequency divider operating frequency is the highest among the PLL, and it affects the PLL performance in terms of locking range, working frequency and phase noise.

In general, high speed frequency dividers can be implemented using an injection-locked frequency divider or Miller divider topology [65, 66]. However, the former one is very sensitive to process voltage and temperature (PVT) issues, while the latter is power hungry. In this design, a current-mode-logic (CML) static frequency divider for its robustness advantage is proposed.

For the typical CML frequency divider, its maximum operation frequency is limited by the parasitic capacitor. To solve this issue, a capacitive-bridged inductive shunt peaking technique is used in the frequency divider load, as shown in Figure 9 [67]. Figure 10 shows the stack inductor layout, a very compact structure by absorbing the inter-layer parasitic capacitance. The benefit of this structure is that the interconnect between the frequency divider is very short. So the frequency response of the divider load is enhanced. In this way, the frequency divider area becomes compact, and the locking range and the operating frequency performance is improved.

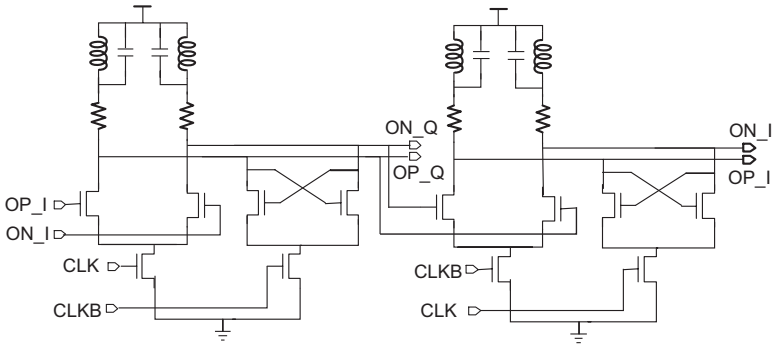

Figure 9 Static frequency divider.

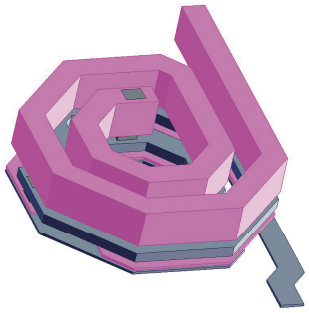

Figure 10 (Color online) The implementation of the stack inductor.

Implemented with a 65 nm CMOS process, with 0 dBm input power, the frequency divider achieved locking range of 34 – 48.5 GHz. Note the operating frequency can be enhanced further by reducing the inductor value.

4.3 Receiver

As an important part of the mmWave air interface, the receiver has several design challenges, such as large gain, wide bandwidth, high dynamic range, and sensitivity. Considering high operation frequency and wide bandwidth nature of mmWave spectrum, we will try to solve above issues from the system architecture and building block level.

Figure 11 shows the implemented 60 GHz receiver block diagram. The receiver consists of a 4-stage 60-GHz LNA, a 48 GHz RF mixer, a 12-GHz I/Q demodulator and I/Q baseband variable gain amplifiers (VGAs). As mentioned before, the sliding-IF dual conversion architecture is employed to achieve better I/Q mismatch performance and relax the requirements of the PLL tuning range and phase noise [68]. An external 48-GHz LO signal is used to drive the RF mixer and the divide-by-4 static frequency divider. With the frequency divider, the 12-GHz quadrature LO signals are generated for the demodulator operation. Note, in this design to improve the system EVM performance further, a digital calibration is realized by controlling the frequency divider phase and the VGA gain [68, 69].

Albeit the improved circuit and system design freedom offered by the sliding-IF receiver architecture, innovative circuit topologies are still needed to meet the system applications due to following reasons. As indicated in IEEE 802.15.3c standard, the 60 GHz band has 9 GHz spectrum with channel bandwidth of 2.16 GHz. It poses critical requirements on the RF chain in-band gain flatness. Additionally, the mixer is typically the system linearity bottleneck, the LNA needs a well-defined gain control step.

4.3.1 *LNA*

To address above issues, a 60 GHz LNA topology is proposed. As shown in Figure 12, the LNA consists of 4-stage differential common-source amplifiers for more than 20 dB gain. To improve the LNA gain and isolation, the capacitive neutralization technique is used. Particularly, to achieve wider bandwidth and

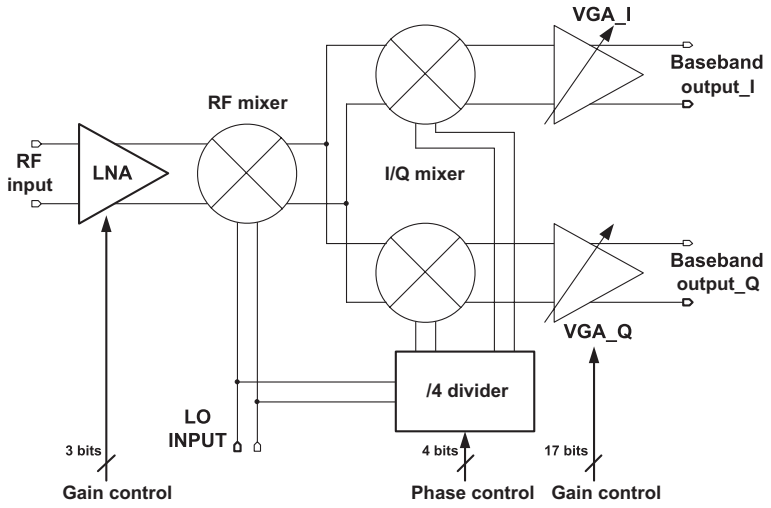

Figure 11 The block diagram of 60 GHz receiver.

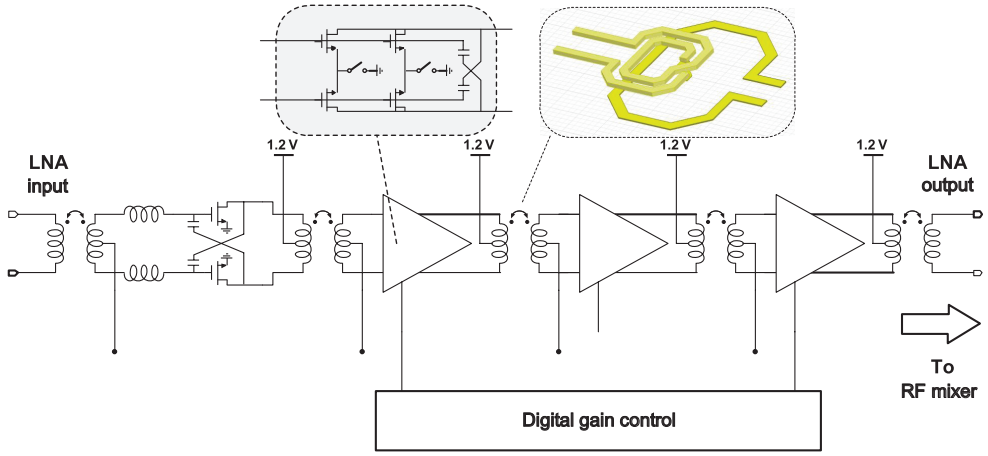

Figure 12 (Color online) Schematic of LNA.

out-of-band roll-off performance, transformer with low coupling coefficient (k) as low as about 0.3 is used to realize the inter-stage impedance matching network. Simulation and test results show that with the proposed low-k transformer based matching network, the LNA bandwidth can be larger than 15 GHz.

Typically, the LNA gain can be controlled by several ways. In [70], the LNA gain is tuned by switching on/off the common gate transistors, with a poor noise performance. In [71], the LNA gain is tuned by controlling the gate bias of the common-source amplifier. The drawback of this circuit is its poor linearity and high sensitivity to PVT corners. In this study, a tailed switch technique is used in the LNA design. By controlling the current ratio of the amplifier with tail switch, simulations indicate that well-defined gain steps can be achieved, which is not sensitive to the PVT variations. Meanwhile, the linearity performance is preserved.

4.3.2 *Mixer*

As mentioned before, a dual-conversion architecture is used in this design, which is realized by cascading a 48 GHz RF mixer and a 12 GHz demodulator, as shown in Figure 13. The 48 GHz mixer is implemented with a double-balanced Gilbert-cell mixer for its high port isolation advantage. As indicated in the schematic, a pair of series-peaking inductors is inserted between the gm stage and switching quads to eliminate the parasitic capacitor effect, which reduces the signal loss at the intermediate node and improving gain.

Same as the RF mixer, I/Q demodulators also use the active Gilbert mixer structure. Specifically, to

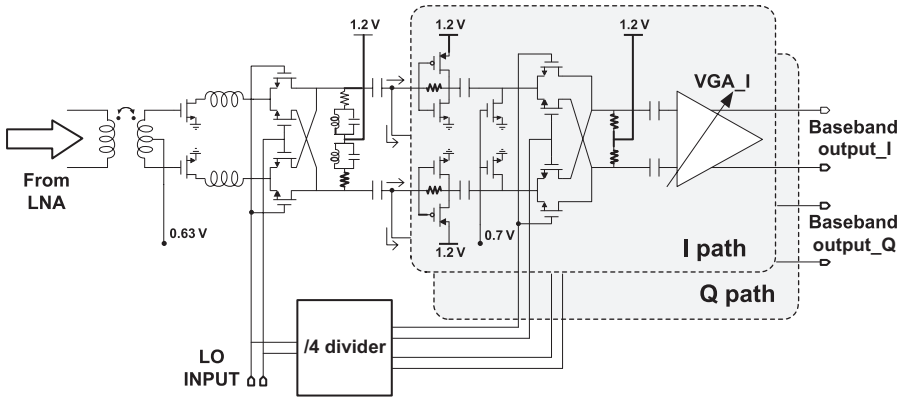

Figure 13 Schematic of the RF mixer and I/Q demodulators.

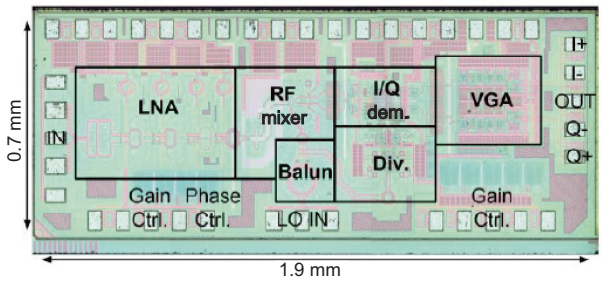

Figure 14 (Color online) The microphotograph of the 60 GHz receiver.

improve the linearity and noise performance, here the g_{m} stage and the switching quads are ac coupled. In this way, the g_{m} stage and the switching quads of the mixer can be biased independently, achieving both good linearity and low noise performance simultaneously. The g_{m} stage is realized with a self-biased inverter. Compared with NMOS or PMOS only g_{m} stage, the $g_{\mathrm{m}}/I_{\mathrm{d}}$ efficiency of the self-biased inverter is two times larger, saving the power consumption for a particular gain requirement.

In this design, two techniques are used to improve the mixer bandwidth: (1) a weak-coupling transformer is used between the LNA and mixer; (2) same as the frequency divider, two compact capacitive-bridged inductive shunt peaking loads are employed at the RF-Mixer load [72]. To improve the demodulator I/Q mismatch performance, a symmetrical layout is used. To compensate unavoidable LO signals phase mismatch and improve the I/Q mismatch performance further, a digitally controlled phase delay scheme (4 bits) is used at the output of the frequency divider.

4.3.3 *60 GHz receiver*

Based on above LNA, RF-mixer and demodulator circuits, together with a VGA circuit [73], the 60 GHz receiver is realized using a 65 nm CMOS. Figure 14 shows the microphotograph of the receiver. The area is about 1.9 mm × 0.7 mm, including all the dc and RF pads.

Figure 15 shows the measured conversion gain in 60 GHz 4 channels under high-, typical- and low-gain modes. The more than 2 GHz bandwidth of a channel proves its capability of handeling 1 GHz bandwidth in 5G system. In the low-gain mode, the LNA gain is tuned to the minimum of 15 dB. The gain flatness in each channel is better than 3 dB. The best gain flatness of less than 1.8 dB is achieved in channel 2. In the high-gain mode, both the LNA and VGA are with full gain setting. As the VGA bandwidth is slightly reduced when its gain is large, the receiver gain variation is slightly larger than its low-gain case.

To evaluate the receiver performance further, a wireless link measurement is undertaken, with the setup as shown in Figure 16. A differential I/Q QPSK signal with data rate of 3.52 Gb/s is up-converted and radiated by our designed 60-GHz transmitter and antenna. The receiver is located 1.5 m away from the transmitter, and the receiver's outputs are fed to the oscilloscope for further evaluation. Figure 17

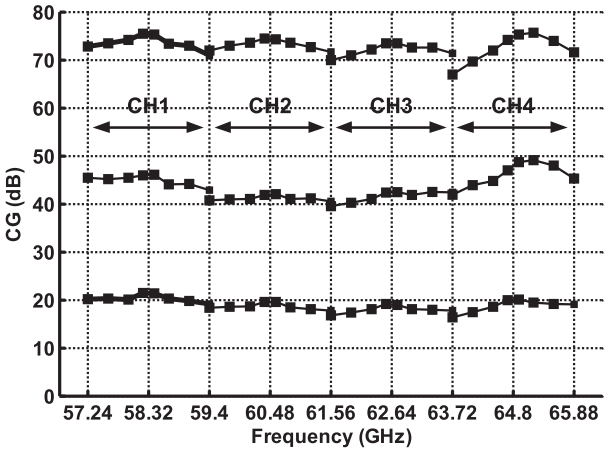

Figure 15 Measured conversion gain in high-, typical and low-gain modes.

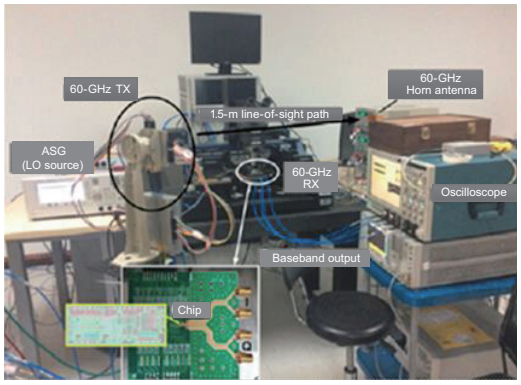

Figure 16 (Color online) A 60 GHz wireless link measurement setup.

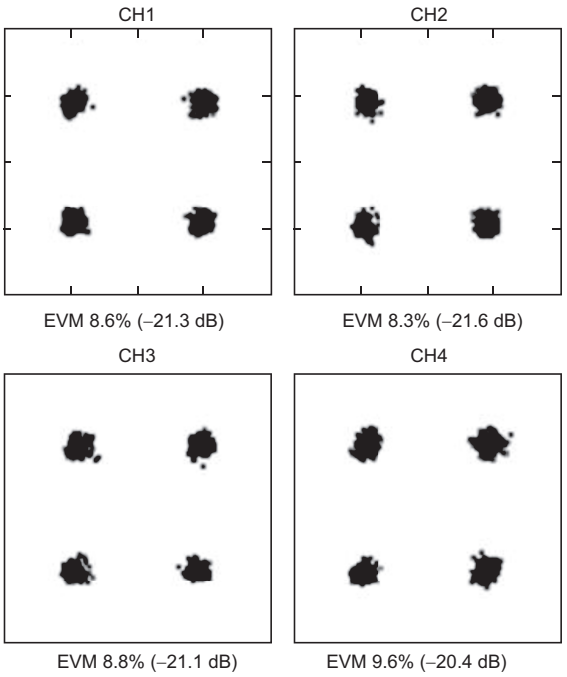

Figure 17 TX-to-RX EVM test results of four channels.

Table 1 Summary of 60 GHz receivers

Reference	[71]	[74]	[75]	[76]	This study
Process (nm)	90	65	65	65	65
Gain (dB)	0–60	9–23	35	36	20–75
Gain range (dB)	60	14	–	–	55
3-dB RF BW (GHz)	**2.16**[b)]	**2.16**[b)]	**1**[a)]	7.5	8.5
NF (dB)	7.1	< 4.9	**14**[b)]	< 11	**5**[b)]
IP1dB (dBm)	-11	N/A	-33	-18	-30
Area (mm^2)	N/A	**2**[a)]	–	**1.3**[a)]	1.33
Power (mW)	N/A	**223**[c)]	**233**[c)]	25	102.4

a) Graphically estimated.

b) Measuring one channel.

c) Including PLL and buffer.

shows the TX-to-RX EVM test results after calibration. Clearly, the EVM is better than -20 dB in each channel.

The linearity and noise measurement are also undertaken. In the high-gain mode, the receiver input P1dB is about -72 dBm, whereas in the low-gain mode the receiver input P1dB are about -30 dBm. The measured noise figure is about 5 dB when the receiver gain is 75 dB. Table 1 compares this study with the state-of-the-art receiver results. This receiver exhibits the highest conversion gain and a very large gain tuning range. In addition, its bandwidth and noise figure (NF) performance are very good.

5 Conclusion

In this paper, 5G mmWave system implementation issues are discussed in several aspects: the implementation technology choice, phased array system architecture, procoding and channel estimation. Given the 5G mmWave RF front-end system is dominated by the passive element, in view of the active device and back end of line characteristics, innovations in the impedance matching networking, circuit and system architecture are highly demanded. In this paper, to illustrate above considerations, several key 60 GHz mmWave building blocks, including PA, VCO, frequency divider, LNA and mixer, are implemented and tested. With above building blocks, a 60 GHz receiver is realized using the 65 nm CMOS process, and a TX-to-RX EVM of better than -20 dB is achieved in 60 GHz 4 channels.

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