RCA Engineer

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hybrid technology

RCA Engineer

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Our cover shows two kinds of hybrids. Electronically, we have multi-layer thick-film conductors, insulators, and resistors mounting and interconnecting beam-leaded and wire-bonded integrated circuits and chip capacitors. Agriculturally, we have the Golden Beauty version of *Zea Mays rugosa*.

Photo: Andy Whiting, MSR, Moorestown, N.J.

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- To disseminate to RCA engineers technical information of professional value
- To publish in an appropriate manner important technical developments at RCA, and the role of the engineer
- To serve as a medium of interchange of technical information between various groups at RCA
- To create a community of engineering interest within the company by stressing the interrelated nature of all technical contributions
- To help publicize engineering achievements in a manner that will promote the interests and reputation of RCA in the engineering field
- To provide a convenient means by which the RCA engineer may review his professional work before associates and engineering management
- To announce outstanding and unusual achievements of RCA engineers in a manner most likely to enhance their prestige and professional status.

There've been some changes made

We recently charted a new course for the *RCA Engineer*.

For more than 22 years, the journal has kept engineers informed and has provided a vehicle for publicizing their work. We felt we could build on that traditional value by publishing articles that would interest larger numbers of engineers and help them stay up to date in their profession.

As a result, we are now seeking out and publishing articles that review or survey fields affecting a broad cross-section of the corporation's engineers—"LSI" by Hilibrand (Jun/Jul) and "electro-optic systems" by Seeley (Apr/May) are two examples.

We are also emphasizing tutorial material: "digital electronics," a four-part series by Shapiro (Aug/Sep 1976 through Feb/Mar 1977); "color tv" by Pritchard and "electronic displays" by Johnson (Jul/Jul); and the dialog on "hybrids" by Joyce in this issue.

We have continued to seek out and publish papers that review the business environment: Jacoby on "solid state" (Jun/Jul); Winder on "microprocessors" (Feb/Mar); Bouchard on "hybrids" in this issue.

Graphically, our illustrations are now larger, more relevant to the text, and more fully explained. Editorially, we have opted to eliminate mathematical derivations, detailed supporting data, and lengthy descriptions in favor of presenting broader concepts. (The author of a paper is, generally, a phone call away for the details.)

Our experience and that of our advisors told us that these changes were desirable—so we made them. Then, through the recently completed Engineering Information Survey, which elicited opinion from more than 3000 RCA engineers, you reaffirmed our decision to move in this direction. Let me cite a few general findings to make the point. About 80% felt that the *Engineer* should publish more state-of-the-art reviews; 64% wanted more information about competitive technologies; and 52% wanted more educational material. A complete report on the survey will be published in a later issue.

The *RCA Engineer* improvements are due, in large measure, to the diligent efforts of the competent, creative staff that works with me to produce the journal. But our small staff could not do it alone. A major share of the credit belongs to the editorial representatives who work inside RCA's various engineering activities and represent the journal's primary sensory network. The *Engineer* is fundamentally what you and these representatives make it; they are your contact with the journal and our contact with you.

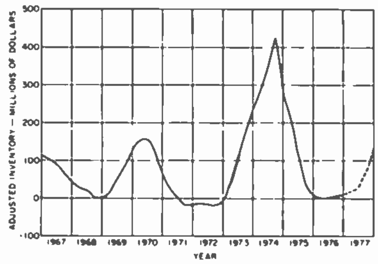
In this issue, we have dedicated two pages to the editorial representatives (pp. 42-43) in the hope you will get to know them better, and through them help to further improve the contents and policies of *your* journal—the *RCA Engineer*.

John Phillips, Editor

hybrids

After weathering a big star buildup they couldn't have lived up to, hybrids have found a role as an excellent supporting actor.

4, 8, 16, 20



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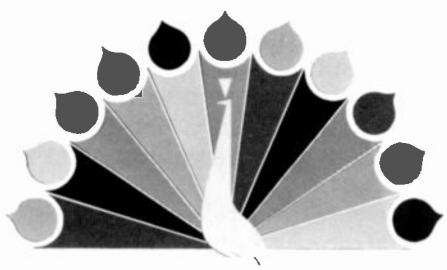

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Coming up

Our next two issues are on **advanced communications**. The Oct/Nov issue will center on **common carrier and satellite communications**, while the Dec/Jan issue will cover new developments in **broadcast communications**, such as **digital tv** and **circular polarization.**

Later issues will have **radar, software**, and **space technology** themes.

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Hybrid technology—best supporting actor

For nearly three decades, hybrid microcircuits have not quite lived up to their advanced star billings. But in the past decade, the directors of the show business called electronics have recognized the role hybrids were meant to play— to support the stars of the industry, monolithic microcircuit technology and semiconductor technology in general.

J. G. Bouchard

What is a hybrid? I'm sure you've already said "I know what a hybrid is. It's a small circuit combining active elements and deposited resistors." Most hybrid experts, however, would rather relate their definition to interconnection and packaging technology:

> *Hybrids are a class of microelectronic circuits fabricated by a complete technology that is very dynamic, constantly evolving and expanding—a technology continually being augmented by the emerging semiconductor techniques in combination with innovative thick- and thin-film technologies.*

Thus, hybrid technology is essentially an advanced method of combining, assembling, and packaging newer components into a more effective, larger part of an electronic system. With such a definition, it becomes obvious that the nature of progress in hybrid technology must be evolutionary—governed by the development of techniques considered as basic and essential to hybrids, but also tracking developments of new components to be added to the ever-growing list of hybrid ingredients, and developments and applications of more effective semiconductor assembly techniques.

Originally, hybrid microcircuits were simply the combination of deposited resistors with attached discrete packaged active elements. The very first hybrids were made using screen-printed resistors and vacuum tubes for a military fuze program in the early 1950s. When the transistor was introduced in 1955, it was a much more compatible hybrid element and greatly increased the effectiveness of hybrid technology of the late 50s and early 60s. Many hybrids were fabricated, and in fact, are still being fabricated consisting of packaged transistors in combination with deposited resistors and conductors on ceramic plates (Fig. 1). Early, uncased transistors were very fragile, very susceptible to damage during hybrid processing, and the potential size reduction by their use was realized only at extreme cost. It was not until *planar* transistors became available that the "chip-and-wire" hybrid technology became practical.

When monolithic microcircuit chips became available, they added significantly to the capacity and range of hybrid technology. Examples of hybrids incorporating ICs are illustrated in other articles of this issue.

Throughout its history, the *proper* application of hybrid technology has made available to the circuit designer the best of the microcircuit world—smaller size, better performance, higher reliability, and closer performance tolerance. The word *proper* was emphasized because too often hybrid microcircuits have been used to disadvantage.

Hybrids vs. monolithics

This controversy has been the subject of countless papers and many panel discussions at various technical meetings. Well, the battle is over, and in fact, those who always

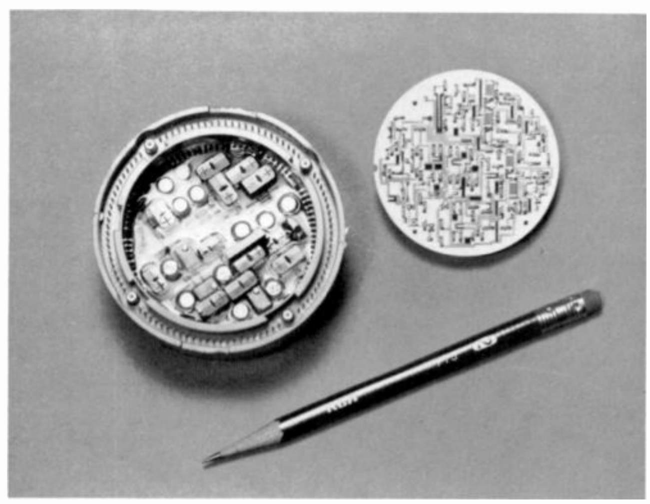

Fig. 1
Discrete device hybrid. This first form of hybrid technology is still being used in low-packing-density, low-volume applications.

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recognized hybrids as a packaging technology will claim that there never was a battle—it has always been a big fuss about a nonexisting conflict. These two technologies do not perform parallel functions, but additive ones. Hybrid and monolithic technologies do not compete; they complement each other. One might say that monolithic microcircuit and general semiconductor technologies produce the stars of the microcircuit show, and hybrid technology produces the supporting cast. The monolithic stars can perform many simple and very entertaining acts on a solo basis, but a real production usually requires several stars and the assistance of an able supporting cast. For example, a monolithic IC operational amplifier is perfectly adequate for many ordinary applications, but an instrumentation amplifier requiring high performance is better realized by a hybrid microcircuit that will typically consist of three monolithic operational amplifier chips, precision and dynamically-trimmed resistors, and compensating capacitors.

Quite often, in show business, a supporting actor entertains and keeps the audience interested, while the star is preparing for the next act. Hybrid technology occasionally performs in this capacity, achieving the necessary small size using simple IC chips until the monolithic star is ready to perform. There have been, are now, and will be, many instances where a hybrid circuit consisting of a number of IC chips is used in a socket until the monolithic equivalent is available. The monolithic equivalent may not be available initially, simply because of its long development time, or may not be practical because the volume has not yet developed to justify its higher development cost. For a while, this monolithic performs a one-man show, but then the cycle starts again. Several such monolithic chips are utilized along with an appropriate hybrid cast to create a real spectacular.

Hybrids—what volume?

Enough of show business. How about the real hybrid business. How big is it? Where does it come from? The true magnitude of the current hybrid business is not available in conventional market forecasts. For example, *Electronics* magazine, which annually publishes a forecast of electronic markets, estimated the 1977 market of *Multi-components and Hybrids* to be $281.1 million and projects a market of $403 millon for 1980. However, this is only a small fraction of the true hybrid market, since these numbers represent *only* the hybrids that get to the market as hybrids. Since the hybrid business is largely captive, the true volume of the hybrid market does not show up as hybrids but as a hidden part of the end-item market. Most hybrid microcircuits do not get sold but are produced by the end-equipment manufacturers. It is safe to say that the total value of hybrids used in such equipment as computers, automobiles, telephones, military electronics, digital watches, and mobile radios far exceeds the $281.1 million estimate.

IBM, for example, has been using thick-film hybrid technology for nearly two decades, beginning with simple RC networks. Currently, this manufacturer has the highest known level of automation,[1] producing very complex hybrid circuits. IBM's annual volume is, of course, not publicized, but is known to exceed 10 million circuits per year.

Gerry Boucharc worked for a major semiconductor manufacturer as a transistor process and desigr engineer from 1957 through 1963. In 1963, he was appointed engineering manager responsible for both monolithic and thin-film hybrid development. Since 1968, when he joined RCA, he has been responsible for Burlington's Microelectronics Facility.

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Automated Systems
Burlington, Mass.
Ext. 2387

Delco, the leading automotive electronic manufacturer, has invested over $12 million in hybrid automation[2] and currently produces upwards of 200,000 hybrids a week.

Western Electric has been using hybrid technology very extensively for many years. As part of the NIKE-X program, Western Electric developed and produced multichip wire-bonded hybrids (Fig. 2). This program led to the development of the beam-lead technology.[3] The oscillators for all Touch-Tone telephones are produced using tantalum (thin-film) hybrid circuit technology.[4]

These three companies are currently the largest producers of hybrid microcircuits, and none of them sell hybrid microcircuits.

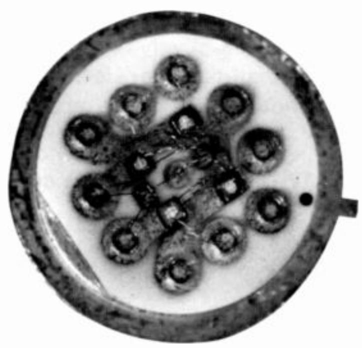

Fig. 2
Multichip wire-bonded hybrid deve.oped for the NIKE-X program. This type of hybrid was the precursor of beam-lead technology.

Why hybrids and when?

Early hybrid technology and many current applications were motivated by the need for small size. This issue contains several examples, and I'm certain you've seen many more. Thus,

Axiom I— Hybrids for small size

However, such manufacturers as IBM, Western Electric, and Delco did not adopt hybrid technology because of the available size reduction, but to take advantage of automation, which has led to *lower cost*. The major manufacturers realized early that hybrid technology lends itself very well to a high level of automation and thus greatly reduces the manufacturing labor costs. In hybrid production lines, the operators never have to move the individual pieces from station to station; they move magazines or trays containing many thousands of pieces. Within a main block of operations, the work is moved automatically by indexing-type conveyors. But the cost for this automation is very high and cannot be justified except for high-volume requirements. These companies saw the opportunity, had the volume requirements, invested in automation, and now reap the benefits. Thus,

Axiom II—Hybrids for high volume

But, hundreds of other companies are producing hybrids, none in quantities even approaching those described above. What is their motivation? In many cases, Axiom I applies: small size is important. Nevertheless, in some low volume applications, size is relatively unimportant and again, cost is the driving factor. In this issue, Brad Joyce[5] discusses the cost effectiveness of hybrids from a different perspective. Too often the hybrid-vs-discrete cost comparison is done at the component level with little or no consideration for the savings made possible at higher levels of assembly. In general, you can expect that hybrid technology can reduce system cost when a specific circuit is used many times in a system, e.g., as computer memories, test systems, multi-channel communication systems, Thus,

Axiom III—Hybrids for repetitive circuitry

It is important also to recognize the deficiencies, the drawbacks of hybrids, and where they should not be used. Too often people enamoured by the technology have insisted on applying hybrids where they were not needed, where they could not effectively compete. If your application does not need small size, there is no repetitive circuitry, and the volume is not large, hybrids most likely should *not* be used. Thus,

Axiom IV—Hybrids are not a cure-all.

Hybrids today

As we established at the the outset, "hybrid" is a *packaging* technology. Thus, the application dictates the package—it can be hermetic or not, it can be standard or custom, it can use discretes or chips—it is designed to do the job the best way possible.

Hybrid circuits currently being manufactured are the result of the proliferation of substrate-fabrication, packaging, and semiconductor-assembly technologies. The heart of all hybrids, the substrate, is produced using thick- or thin-film technology (occasionally, thick *and* thin film). Because of its lower cost, thick-film technology is used more extensively; thin-film is used when very close tolerance resistors or accurate geometries are required.

Although a large number of hybrid circuits are manufactured using pre-packaged semiconductor devices, the most universally used assembly technique is *chip-and-wire*. This technique has low-cost capability for high volume manufacture, as it is readily automated. The full range of device types is available in chip form, which allows for versatility in design and optimum size reduction with high reliability.

Even before IBM announced their Solid Logic Technology, *flip-chips* were touted as the ideal semiconductor form for hybrid manufacture. Thus far, they certainly have proven so for IBM, which has vertically integrated and now produces such chips for the millions of hybrids they manufacture. But for those hybrid manufacturers who have to buy chips, and have neither the money nor the volume to justify internal chip production, the limited availability of flip-chips, both in quantity and chip type, has principally limited their use to a very-high-volume company like IBM.

When *beam-lead* devices were first announced, many of us in the hybrid industry said, "This is it. This is the ideal form of semiconductors for hybrid manufacture." It was, and is still, the ideal form for hybrid manufacture; but it did not turn out to be a form that was cost effective for the assembly of discrete devices. Thus, the projected high volume for beam leads did not materialize, their costs continued high, only limited types were available, and their promise in the hybrid field, like the flip-chip, has for the most part, been realized in one company—in this case, Western Electric.

The future

Recently, Dr. C. Thornton, Director of the Electronics Technology and Devices Lab, USA-ECOM Fort Monmouth, New Jersey stated, "Over half the Army's (electronic) equipment to be built from here on out will use hybrid circuitry, both thin and thick-film."[6] As mentioned, hybrid technology is also firmly entrenched in computers, automotive electronics, and the telephone industry. And there is no doubt that hybrid applications will continue to proliferate.

Thick-film or screen-printed technology will continue to dominate: ceramic plates will become larger, substrate complexity will increase through more multilayers, and printing costs will be decreased by the use of multi-image printing and non-noble metal inks. The relationship of thick and thin film will continue as each meets a unique need.

Chip-and-wire will continue to dominate as the major non-captive-market assembly technology, and its effectiveness

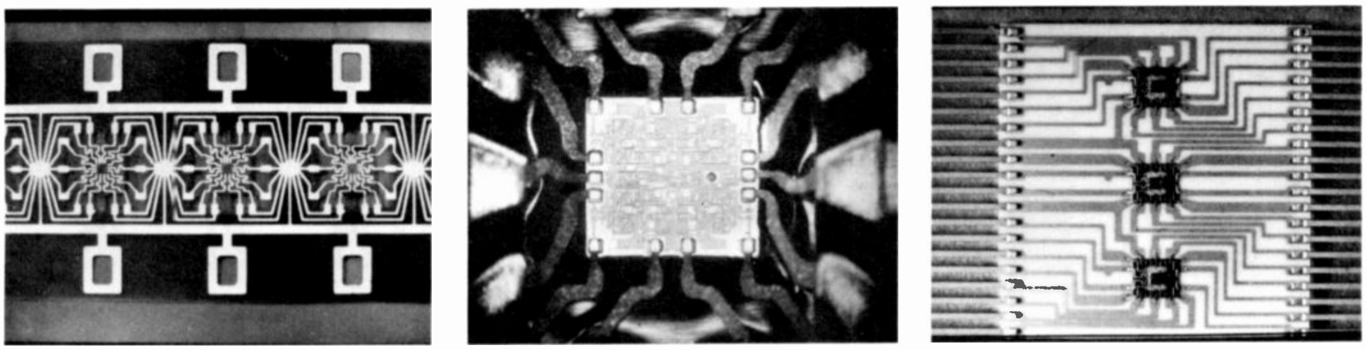

Fig. 3
Tape bonding has outstanding automation potential. Left, IC chips bonded to polyimide tape; center, close-up of chip bonding; right, tape-bonded hybrid.

will be further increased by automatic wire bonding. The discrete-device hybrid volume will decrease, but at a very slow rate. Very few new beam-lead and flip-chip hybrids will be designed.

These preceding predictions are almost obvious and should evoke few disputes, but it is much more difficult to predict the future of two new techniques: tape-bonding and leadless ceramic carriers.

Tape-bonding[7] (Fig. 3) offers some of the advantages of beam leads without some of its drawbacks—and some unique advantages. Like beam leads, it is gang-bonded, i.e., all leads are bonded in a single operation. But unlike beam-leads, tape-bonding makes practical both automated testing and burn-in after the chip is attached to the polyimide film. For very complex, high-reliability circuits, this is a most significant advantage. On the negative side, tape bonding, as currently practiced, requires specially "bumped" chips. It appears to have outstanding automation potential, and several semiconductor manufacturers are using this technique for assembling some of their packaged devices. A hybrid manufactured with tape-bonded devices could be the same size and use the same packaging techniques as a chip-and-wire hybrid. Because of gang-bonding and the higher assembly yield made possible by testing at the tape level, tape bonding offers potentially lower manufacturing cost. It is also expected that gang-bonded tape terminations would be more reliable than individual wires.

Another hybrid technology that is in its trial period utilizes leadless ceramic chip carriers,[6] which are essentially flat-packs with solder terminations instead of flat ribbon leads. The main advantage of this technology lies in the ease of testing and burn-in in the sealed package. It does not provide the size reduction of chip-and-wire or tape-bonded hybrids (2 to 4 times larger) and is only about one-fourth the size of a DIL circuit on a PC board.

The critics are still reviewing both of these technologies. The extent of their application in general hybrid production depends almost exclusively on the extent to which the semiconductor manufacturers utilize these technologies for the manufacture of their discrete families. The automatability, and thus low-cost potential, of tape-bonding may stir vertical integration and singular, high-volume, captive application somewhat similar to flip-chip at IBM and beam-leads at Western Electric. Wide-scale acceptance, however, will depend on the semiconductor manufacturers' acceptance of this bonding technology. Ceramic carriers cannot be automated as easily and thus do not offer the cost advantage that tape bonding does; furthermore, ceramic carriers must overcome the drawback of larger size. A leading semiconductor executive recently predicted that the ceramic carrier would eventually become the major hybrid component.[9] He pointed out that although tape-bonding has lower cost potential, the high volume required to realize these low costs would never materialize, as he predicts will occur for the ceramic-carrier devices. For these predictions to come true, a major portion of the DIL discrete semiconductor market must shift to ceramic carriers. In my opinion, the four-to-one size reduction is hardly enough justification for this major shift in discrete assembly packaging.

I expect that ceramic carriers will continue to be used for large hybrids requiring complex monolithic chips. But it is very doubtful that the volume of this form of active device will ever be significant.

Evolution will continue; a major revolution is unlikely. Tape-bonding has the potential of creating such a revolution—but it must first get the financial and moral support of the major semiconductor manufacturers. Otherwise it will be the beam-lead story all over again.

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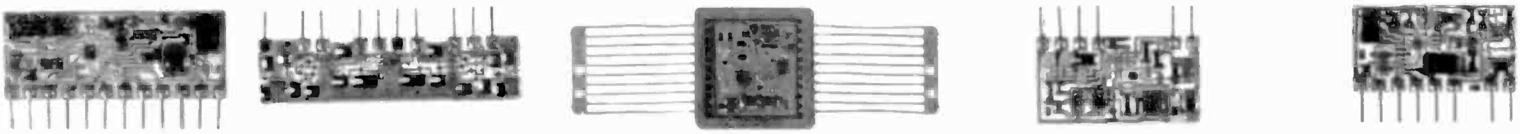
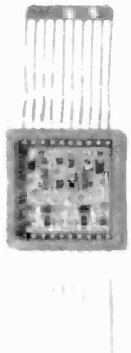
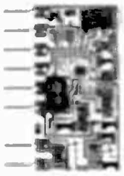


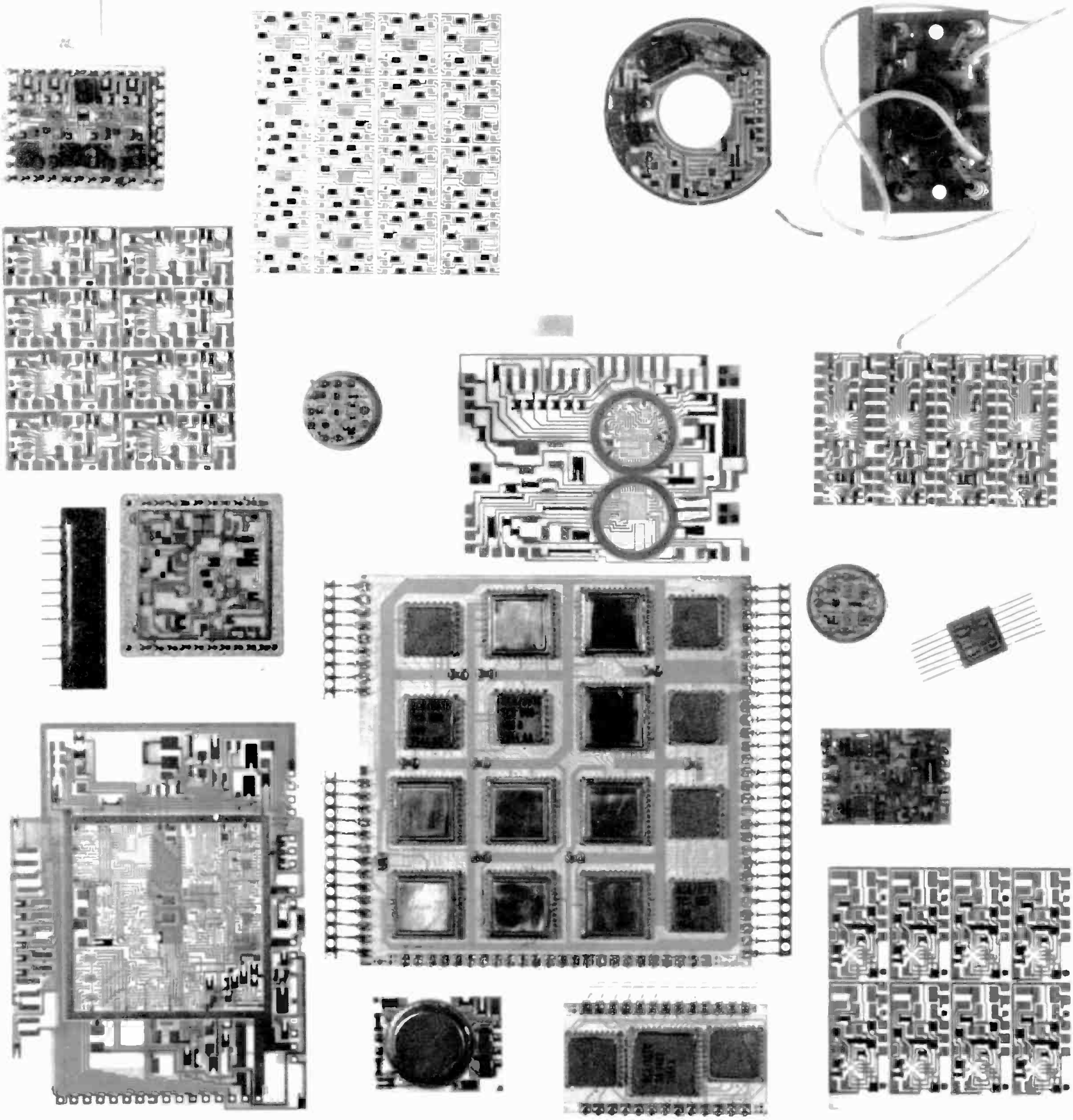
A circuit designer meets hybrid technology



B.T. Joyce



This dialog between a design engineer and a hybrid products engineer presents hybrid circuit design problems and the solutions in an informal, desk-side encounter, along with typical sketches, notes, and photographs



This paper about hybrids is directed specifically at design engineers who are held responsible for the technical integrity of the products they start on the way toward profitable production. It bypasses the technical sales pitch about the benefits of hybrids, all those good words written many times before in many different ways about many applications. Instead, we get down to the nitty-gritty technical concerns of the engineer who has an unproved circuit design and faces the prospects of committing it to unfamiliar packaging methods which (to him) seem totally unforgiving of error and frozen against change. The dialog starts in the hybrid production area.

Dsn eng: Thanks for showing me around the hybrid lab.

Hyb eng: Glad to. But we are really not a lab any more.

Dsn eng: Yes, I guess that's true. I'm impressed. Some day when I have a proven circuit design, I'd like to convert it to hybrids.

Hyb eng: You don't have to have a proven design before considering hybrid packaging.

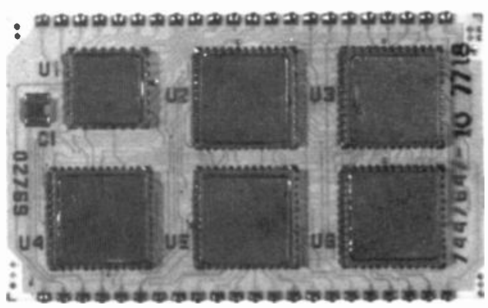
Dsn eng: Then I'd have to have a lot more time for the development—time, believe me, I never seem to get on the projects I'm always put on.

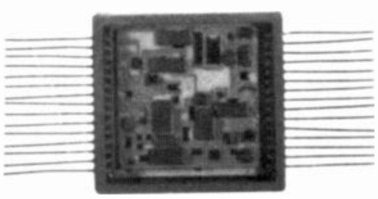
Hyb eng: Have you got a few minutes? I think you and I should sit down and get into some of the nitty-gritty details of hybrid design. No sales pitch. Honest! I'm sure you have heard about all the good things hybrids can do for you many times.

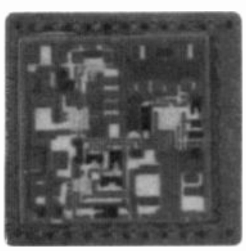
Dsn eng: True. In fact you were coming on pretty strong during the mini-tour you just gave me!

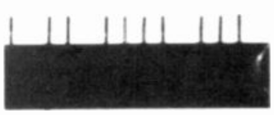
Hyb eng: Yes, I suppose I was. Instinct, I guess. But, how about it; can we chat for awhile?

Dsn eng: Sure, why not?









The two engineers settle down at a conference table in the engineering office area of the hybrid engineer. The hybrid engineer has near him drawing and photograph files and a desk loaded with what he calls "show and tell" hybrids, bits and pieces (literally "pieces," in some cases) of hybrids accumulated over years of product activity. Both have pads of paper to make notes and sketches to accompany their words.

Hyb eng: If hybrid packaging makes sense for your design, you should be considering that approach right from the beginning, designing and partitioning your circuit to take advantage of the fact.

Dsn eng: I thought I wasn't going to get a sales pitch. That sounds like motherhood. Lock—when I commit a circuit to a PC board, I've got a fighting chance, after the board is put together, to make the thing work. Let's face it, the first time through, errors *do* occur—not all the time, but often enough to make a few grey hairs. And you expect me to get locked into hybrids where the only way I can get a good look at my circuit is through a microscope? No way!

Hyb eng: What makes you think we can't do a reasonable job of fixing up problems?

Dsn eng: Can I change the value of some of the components?

Hyb eng: That depends upon what kind of components you're talking about. We actually have a lot of flexibility in the design of the hybrid, especially if we can anticipate specific areas that might change.

Dsn eng: How about resistors? Sometimes by changing a resistor value after the circuit is put together, I can improve its performance.

Hyb eng: How much of a change are you talking about? And which way?

Editor's note: For this dialog, the author draws upon his experiences as a circuit designer and a hybrid products engineer. Brad Joyce's biography and photo appear in his other article in this issue.

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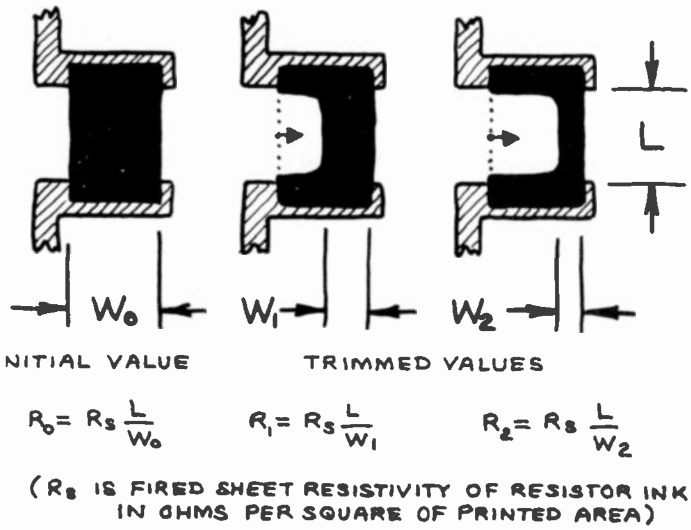
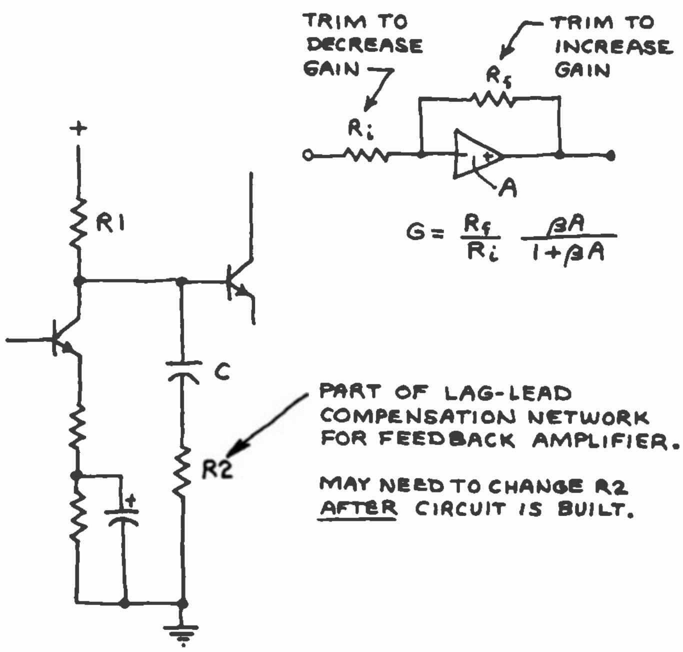
Final manuscript received June 7, 1977.

Dsn eng: Which way?

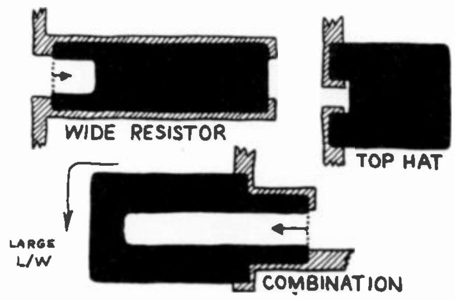
Hyb eng: Yes. Up or down? You see, we usually trim a thick-film resistor to the value you specify on the schematic, trimming before putting any chip parts down on the substrate. But, see, it's usually possible to trim the resistor more after the circuit is built by removing more resistor material. This drives the resistance up—but it's a one-way street. Without any special attention, a resistor can usually be doubled this way.



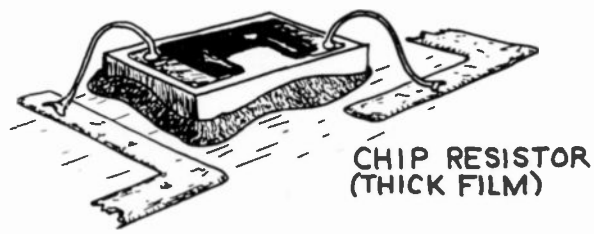
Dsn eng: Great! But what if I want to lower the resistor value? The resistor value could go either way. To improve the ac stability of a feedback amplifier, I might want to reduce or increase a resistor in a lag-lead compensation network. For that matter, I might want to change the basic gain of an op amp by altering R_i or R_f. Of course, here we might actually have a choice. If when you trim a resistor it always goes up, then we can trim one resistor to increase the gain or trim the other resistor to decrease the gain. But in general, I may have to make a resistor lower. What do you suggest?

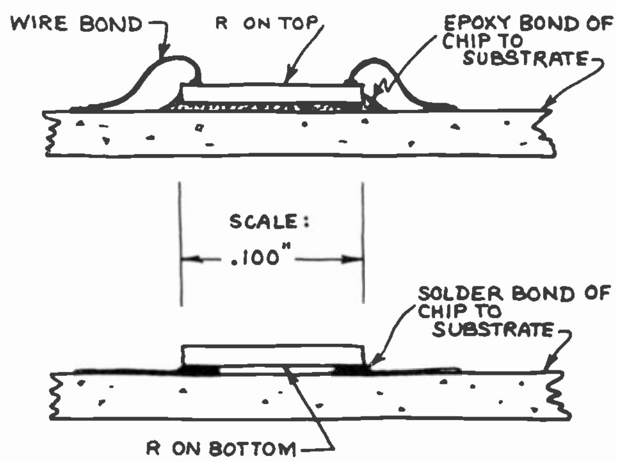


Hyb eng: Then we need to plan ahead, identify any uncertain resistor and start with a value you know is small enough, and actually plan to trim it again, say during the initial engineering sample run of hybrids. We can deliberately design such a resistor in a form that favors a wide range of final trimmed values such as by making it very wide or in a top-hat shape.



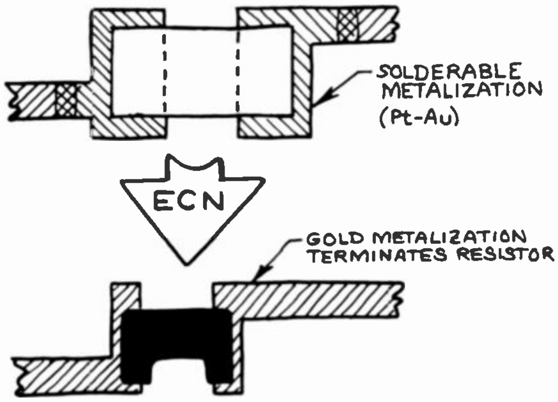
We have an alternative approach to make it easy to change resistors—somewhat more expensive to the hybrid product, though. We can use a chip resistor instead of a thick-film resistor. Chip resistors come in thick-film or thin-film types. With the thick-film type, we pay someone else to print, dry, and fire resistors. He cuts them into individual dice to sell to us. The thick-film types can be mounted face up or face down. One type is connected by wire bonds to the substrate





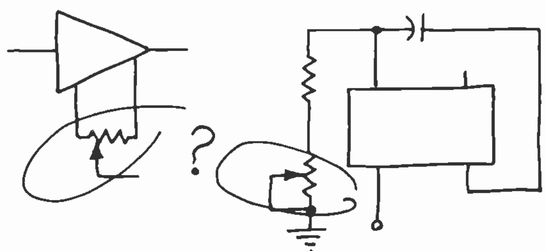
metalization; the other by solder. So we get lots of flexibility simply be leaving room for a chip resistor in the hybrid layout. A good general-purpose resistor configuration covers the resistor range of 1 ohm to 10 megohms, handles 100 mW, and comes in one size, 75 mils long by 50 mils wide.

The resistor can be changed very simply by trained operators or technicians. Downstream when the product gets into quantity production, we may decide that it is economical to get rid of the chip resistor and substitute a regular thick-film type.



TRIMMED THICK-FILM RESISTOR IS LESS EXPENSIVE THAN CHIP.

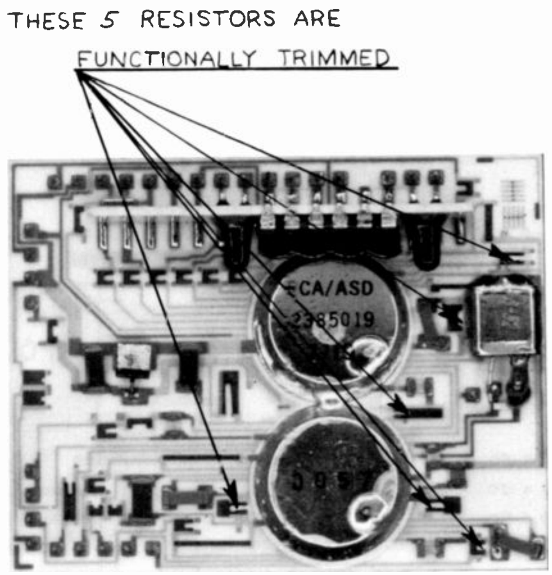
Dsn eng: What if I have to adjust a resistor after the hybrid is built? Can you give me a pot to adjust dc offset of an amplifier or one to set the frequency of a free-running multivibrator?



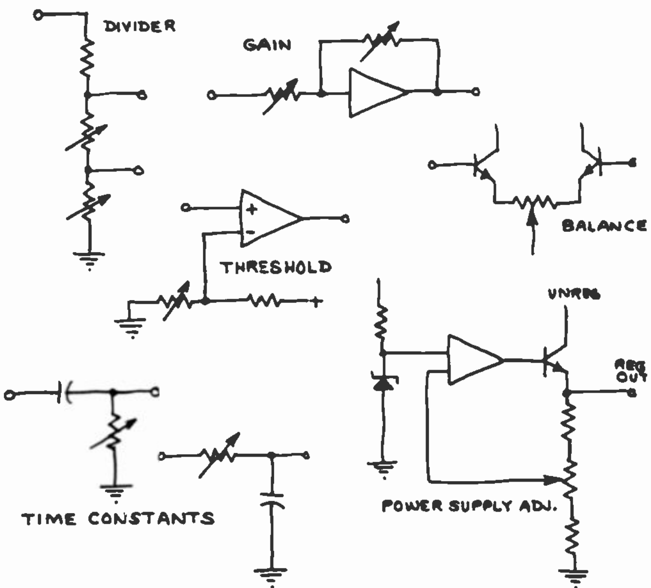
Hyb eng: Giving you a direct answer, yes! In certain complex hybrids, where we treat the ceramic substrate much like a PC board, we can mount conventional discrete parts on the ceramic "board" and thus make room for your potentiometers.

Here's a photo of the Range Counter/Display hybrid from the AN/GVS-5 Laser Rangefinder. Although it doesn't happen to have any potentiometers, it does offer space for large parts like a crystal and LED display devices. The semiconductor chips are all hermetically sealed and protected under the two round covers. Clearly, there is space for pots too. This circuit actually did have a requirement for some variable resistors, which we took care of by functional trimming.

Dsn eng: "Functional trimming." What's that?



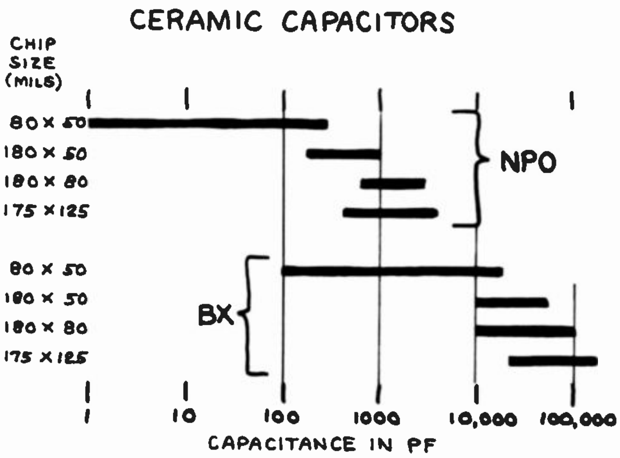
Hyb eng: "Functional trim," "active trim," dynamic trim"— these are all terms used to identify a resistor-trimming operation that takes place while the circuit is under power. We can actually trim a resistor while monitoring a specific circuit function such as your dc offset or your multivibrator frequency and then stop the trimming precisely when the correct value is reached. This range-counter hybrid actually has five functional trims on it. There are all sorts of circuit functions that can take advantage of functional trimming.



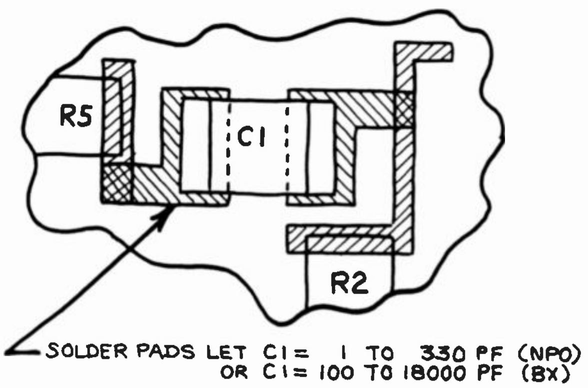
FUNCTIONAL TRIM

Dsn eng: I like that. OK, I've got a pretty good picture on how you can handle resistors. Suppose I need to change a capacitor?

Hyb eng: No problem, especially with some advanced planning. If we know, for example, that the value of a particular capacitor is a little uncertain, then we will make it a point to make sure its value falls well within a range of capacitance available for one specific size of chip capacitor. Capacitor ranges generally overlap for various chip dimensions. The hybrid can then be laid out with the metalization pattern appropriate for that size chip capacitor.



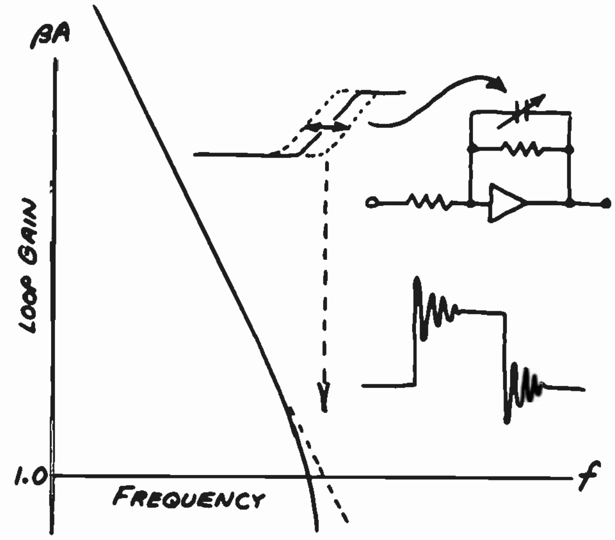
For example, one pattern is totally suitable for receiving a solder-mounted capacitor ranging from 1 pF to 330 pF if it is an NPO class-1 ceramic or from 100 pF to 18,000 pF if it is a BX class 2 ceramic.



Dsn eng: Can you give me a variable capacitor that I can adjust after the circuit is built?

Hyb eng: Depends on what you are trying to do. Just like the case of the pot, we could find room on a ceramic board for a fairly large variable capacitor, the sort of miniature component that you might have put on a PC board. But what do you have in mind? I have some options that may really intrigue you.

Dsn eng: Well, for one thing, I'm designing a video amplifier that is right on the ragged edge of not meeting spec at high frequencies, and my analysis shows that no way am I going to make it unless I either select parts or trim up the loop gain and adjust phase for each individual circuit. A little trimmer capacitor across the feedback resistor to the summing point will do the trick. It will give me some lead at the frequencies where I'm getting into trouble.



Hyb eng: What range of capacitance must you cover?

Dsn eng: Well, I know what I need on my breadboard and have a pretty good idea what I need on a PC board. But I haven't the foggiest notion about what I may need on a hybrid! In fact, that's a real problem, and one I'm not too anxious to fool around with.

Hyb eng: You're sure you can't find one value of capacitance which will do the trick for each circuit built?

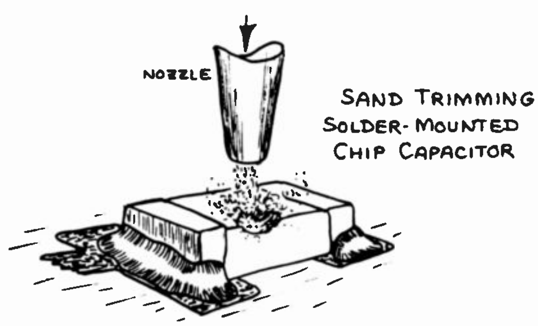
Dsn eng: Absolutely! There are some lags in the loop over which I have no control.

Hyb eng: Back to my question about the range of adjustment you need. What would you use if you put the circuit on a PC board?

Dsn eng: Oh, something between 3 and . . . 10 puffs, to play it safe.

Hyb eng: No sweat! We'll functionally trim the capacitor.

Dsn eng: Here we go again! You mean functionally trim it like the resistors?



Hyb eng: Essentially. With resistors we abrade away material to make the resistance go up; with capacitors we abrade away material to make the capacitance go down. The ceramic chip capacitors are parallel plate capacitors with a high-K ceramic dielectric between them. The trimming operation cuts away the plates and dielectric material. So, we can power up your circuit and trim a capacitor for the high-freqency performance you are looking for.

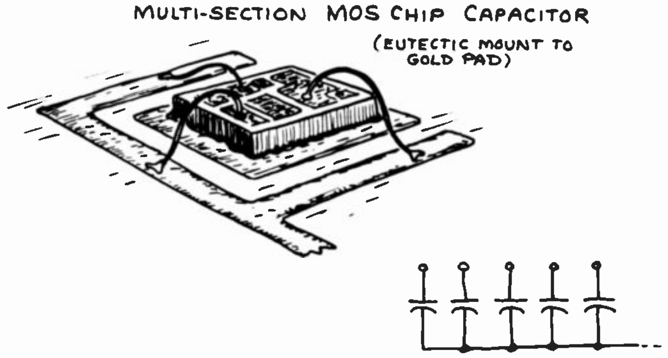
Dsn eng: Sounds good. But can you choose the right capacitor in the first place, one that can be trimmed to the value we really need in the hybridized circuit? You sort of ducked around that point.

Hyb eng: Sorry! As a matter of fact, with hybrid packaging, all conductor runs are obviously very short. Compared with your breadboard or PC board, stray capacitance and inductance are significantly reduced, making it possible to get better frequency performance from any particular paper design. Your circuit in hybrid form will probably work better than ever because some of the lags you used to get from strays will be reduced, thus pushing out the frequency response. We can make a good guess at what capacitance value to put across the feedback resistor and then try trimming . And, if we pick the wrong starting value, it is no big deal to change the capacitor to another value—just a soldering operation by one of our assembly workers.

Incidentally, for small values of capacitance, the low "puffs" or even tenths of "puffs," we can make use of monolithic chip capacitors that use silicon dioxide as the dielectric—basically an adaptation of the MOS transistor technology. One electrode is the aluminum metalization pad on top of the chip; the other electrode is the bulk silicon body of the chip. Such capacitors are quite stable, like 35 ppm/°C.

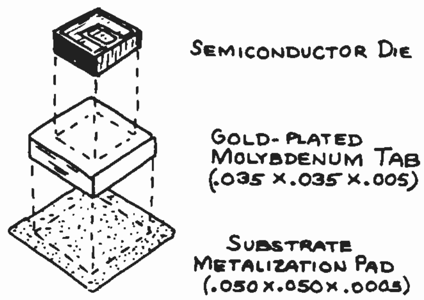
There are some single-chip, multi-capacitance MOS devices on the market which let you pick the capacitor value just by specifying which wire-bond pads you want connected up to your circuit.

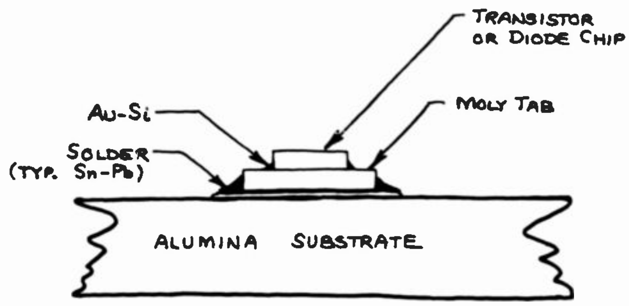
Multi-Section MOS Chip Capacitor



Dsn eng: Well, I assume from what you've been telling me about resistors and capacitors that I shouldn't be particularly worried about changing semiconductor devices if I needed to.

Hyb eng: Up to a point, you are right. Diodes and transistors of one type can usually be easily changed to another type. The main reason this is true is because we have standardized on the area allocated and on the way we attach these devices to a substrate.





First, we eutectically mount the silicon chip to a gold-plated molybdenum (or kovar) tab. Then later, we solder the chip-tab assembly to the thick-film metalization on the substrate. A 35-mil square metal tab is a standard size we have picked to take care of most transistors and diodes. Thus, a change of type is easy. (Obviously, we'd better make sure we order any alternative chips that might be candidates for use in order to avoid purchasing delays.) But really, the possibility that you may need to make such a change is small if you have done a reasonably thorough design analysis and breadboard test of your circuit. Actually, we have had cases where selected transistor parts were needed instead of the standard catalog items. In such cases, the basic hybrid design remained unchanged by the use of selected parts. Selected part drawings were generated, of course, so that the appropriate parameters could be controlled, and the parts list had to be ECN'd.

Dsn eng: Selected parts? I thought with chips you had to take what you could get; that unless you packaged the chips and properly tested them, you didn't really have any guarantee of performance.

Hyb eng: Not too many years ago, your comment would have been right on. The semiconductor manufacturers, especially the big boys, really could care less about the hybrid people. Just buying chips could be a hassle if they weren't garden-variety types. Not so nowadays! The hybrid business has really come of age, enough to represent significant chip volume to the semiconductor people. And a number of speciality houses have gone into business just to serve the hybrid manufacturers and have set themselves up to meet requirements such as providing the selected parts.

Dsn eng: But I still thought you had to package a chip before you could really tell how it was going to perform. And then, what good is the chip to you?

Hyb eng: No good! At least that chip or any other chips that the vendor may check out in a final package. His trick is to use sampling techniques. He can pull samples from a specific wafer that contains hundreds of transistors or, for that matter, pull appropriate samples from an entire wafer lot. His tests on packaged samples pretty well spell out the performance characteristics of the lot so that he can sell to us chips guaranteed to meet our spec, even where we call out something special. But let's face it, selected parts cost more money than standard parts. And just as you try to avoid selected parts when designing circuits for PC boards, you also try to avoid selected chips for circuits that will be built as hybrids. But the flexibility to select is nevertheless still there.

Dsn eng: You know something? I think I have a right to feel a bit paranoid. So far in our conversation, we've been talking about all the things that might be questionable about my circuit design and the mistakes *I* might make. But let's face it, I'm really worried about the mistakes that *you guys* make. I've heard some real horror stories! You have no monopoly on geniuses.

Hyb eng: Amen! But we can get awfully creative when we have to fix a goof and when all the bosses are trying to help us.

Dsn eng: Yup, I known what you mean! But at least on a PC board when you have an unwanted conductor shorting two signal runs together, it's not too hard to cut away copper on the outside or even drill out the etch on a buried layer. What do *you* do?

Hyb eng: Same sort of thing. Sometimes we break an unwanted conductor run with a diamond-pointed scribe; other times we sand blast it out.

Dsn eng: Sand blast? You mean like trimming resistors?

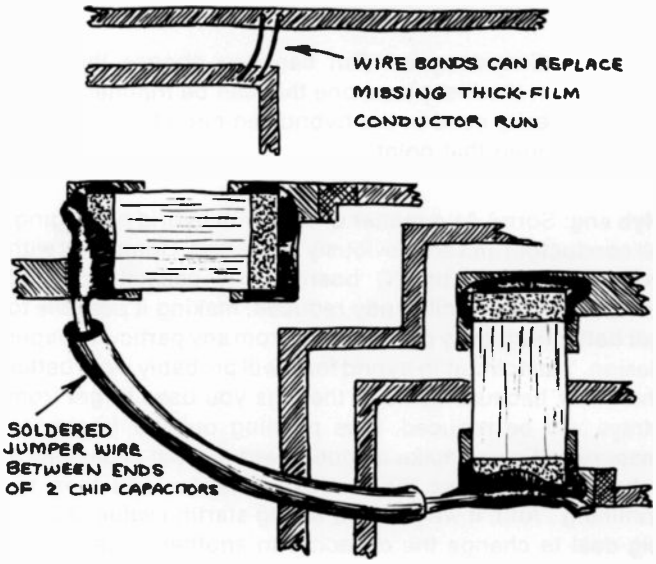
Hyb eng: Exactly. But we have to be careful not to damage anything in the local area around the line being cut. After all, if a resistor gets hit by an overspray of sand, its value may go up and go out of spec. Overspray on the face of a semiconductor can cause damage also. Let's face it, we have plenty of motivation to try to avoid having to cut away metal. We don't need that kind of problem, and we check the basic layouts very carefully for that reason.

Actually, it is usually easier to open shorts then to short opens.

Dsn eng: Come again?

Hyb eng: You know—replace a missing conductor run after the hybrid is made.

Dsn eng: On a PC board, we just solder in a jumper wire between a couple of convenient points.



Hyb eng: Sometimes we do the same sort of thing. In certain cases, we jump an open with gold wire bonds. Wherever there are soldered capacitors around, there are some good places to solder in a jumper. But the approach falls apart if the nice, solderable capacitor locations just don't happen to be associated with the missing conductor run. And unlike the PC board, where any exposed copper conductor is a good candidate for soldering, the metalized hybrid substrate has many gold conductor runs that can be soldered safely only with some of the more exotic solder alloys. Regular tin-lead solders leach away the contacted gold.

Dsn eng: Sounds hairy, but I suppose no worse than some of the fixes I've had to put on a PC board the first time through manufacturing.

Hyb eng: That's the real point I have been trying to make. Sure, everything is scaled down to a smaller size; but we have a whole bag of tricks (reasonable ones, believe me) that we use to get around problems if they occur—tricks that are no more special to us in building hybrids than the ones you are familiar with.

Dsn eng: How much of a circuit can I get into a hybrid?

Hyb eng: Hey! Great! You're ready to take a serious look at hybrid packaging?

Dsn eng: Well, let's say I'm listening. But I really don't have any feel for how much circuitry I can expect to shrink to a practical hybrid—you know, one that isn't going to cost a mint and cause a lot of grief. I could care less about "pushing the state of the art."

Hyb eng: You are asking a question that doesn't have a clean answer. Exactly how many parts you cram into a hybrid (in effect, how complex you make it) depends very much on the application and the product interests you are trying to serve. But let me throw some thoughts out—ones loaded with personal bias.

You can at least get a ball-park feel for what the hybrid can do for you. For instance, I can make one sweeping generalization: If you have a circuit function using discrete parts that are packaged tightly together on a PC board, we can package that same circuit function into one or more hybrids that will use only about one-tenth of the board area. Without qualms, we can take a digital logic circuit with twelve ICs and even a couple of capacitors and put them together in a single, hermetically-sealed one-by-one-inch package. And many hybrid houses (including ours) are doing a lot better than that!

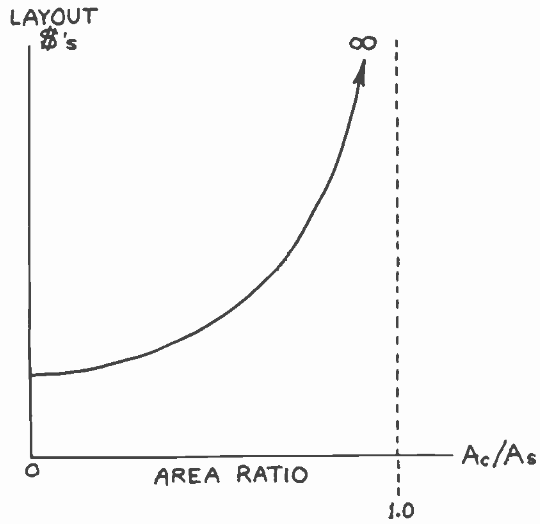
There is one thing that you really must be careful about when you start to move into hybrid packaging.

Dsn eng: What's that?

Hyb eng: That you and the hybrid engineer don't get carried away with the idea of packaging as much as possible into the hybrid package.

Dsn eng: How do I keep out of trouble?

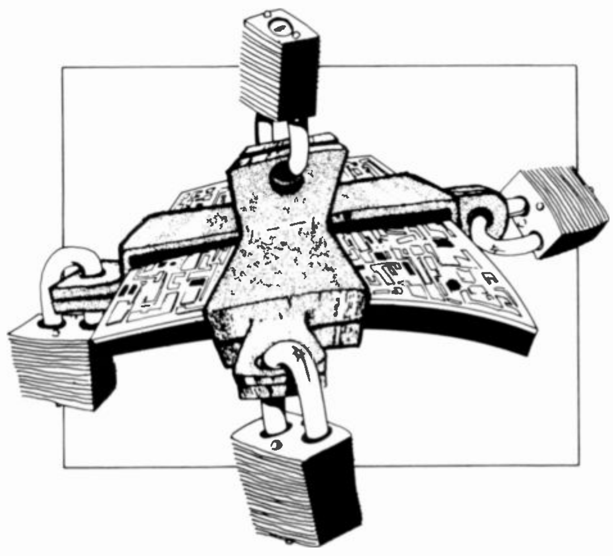
Hyb eng: Make sure some sort of decent area survey is done that makes an effective comparison of the area of the substrate with the area of all the chip parts and thick-film resistors. As a simple rule of thumb, I like to hold the area of the components to about one-half the substrate area. Let's face it, as the component area approaches the area of the substrate, the costs for just trying to lay out the circuit approach infinity.

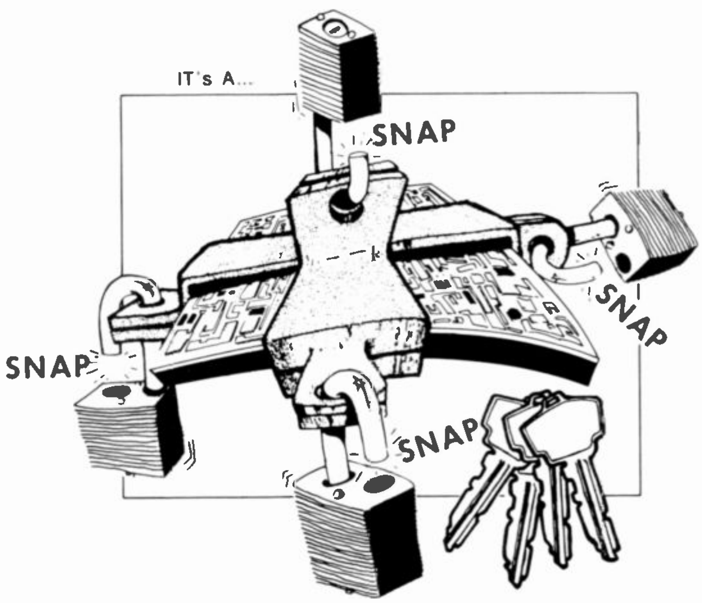


Dsn eng: A truism! But I've got the message.

Thanks for taking the time with me. I've got to get going. I have a meeting to get to in five minutes. But I'll be back later to get into details on a design I'm working on now. Say, have you ever considered writing down some of the stuff you've been telling me about?

Hyb eng: Who'd read it?





If I'm LOCKED Into Hybrids,
Are My Design Changes LOCKED OUT?

The changing role of hybrids in modern electronics systems

J.A. Bauer

Hybrid technology has improved to keep pace with the developments in monolithic ICs. Here's what one RCA facility is capable of doing in hybrid design and production.

Hybrid technology has generally replaced all other techniques of interconnecting and mounting multiple-chip components for high-density packaging. It has surpassed "cordwood" mini-mods and other techniques because the hybrid can use smaller uncased components and because direct connections to both active and passive components improve performance and reliability. The hybrid can achieve low cost by reducing volume and cabling. It also offers improved high-speed performance in digital circuits and analog circuits, and gives better adherence to design specifications by "hot trimming"—circuit trimming to match desired characteristics while the circuit is under electrical test.

Limitations to earlier technology

Before the availability of monolithic integrated-circuit components, the hybrid was recognized as a way to provide multilithic LSI within a single package by using special mounting and interconnecting techniques. Major efforts were devoted to treating of the semiconductor chips to improve the bonding process. Competing techniques of flip-chips, beam-leaded chips, and leadless inverted devices were developed. All of these have been, and are still being, used with success on specific products. However, several factors have reduced their utility in general-purpose applications. These are:

- Limited chip selection;
- Geometry variations between different sources of the same chip type;
- Limitations in substrate design;
- Nonuniform materials and processes for chip attachment;
- More costly components; and
- Growth of LSI into larger chips with more contacts than the specialized bonding process can accommodate.

For example, the hybrid facility at MSR in Moorestown has implemented successful designs with available beam-leaded components and mixes of beam-leaded components and chip-and-wire components, but currently plans no major developments in these older chip techniques.

Hybrids and LSI—competing and working together

As integrated circuits have progressed through the artificial designations of MSI, LSI, and VLSI to the availability of both commercial LSI and custom VLSI with thousands of components per chip, some of the earlier-designed hybrids have been replaced. However, hybrids have also

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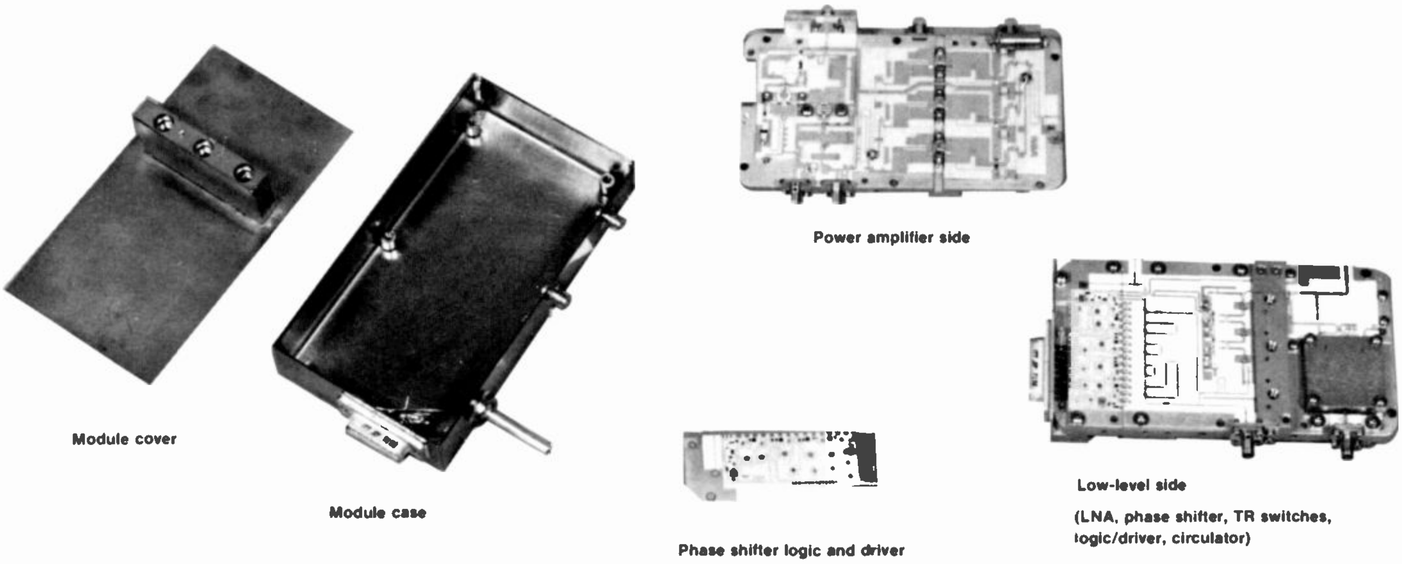

Fig. 1
Microwave assembly is made with thin-film sputtering, has connections of thermocompression gold ribbon.

progressed to higher complexity and larger sizes. The hybrid is an ideal mounting and interconnection mechanism for the larger custom/LSI chips using single-diffusion technology. The hybrid also has significant advantages when the requirements are:

- Very-high-frequency operation;
- Adjustment of circuit parameters in production;
- Very high or low power;
- Combination of monolithic types; and
- Combination of monolithics and passive elements.

Hybrid status at MSR

Hybrids can be made using either thick-film or thin-film technology.

The basic thick-film process in current use at Moorestown uses rf-sputtered thin-film molybdenum on a 99.5%-alumina substrate, with an overlayer of sputtered gold that is then electroplated with gold to an 0.4-mil metal thickness. A photoresist is applied and developed with the desired artwork patterns and the metal is etched to the substrate, leaving conductor where desired. This process provides excellent control of materials and dimensions for single-layer microwave circuits. It has the advantage of direct use of artwork on the substrate without an intermediate screen, as required for thick film, and thereby provides fast turnaround for engineering small quantities of circuits.

Both engineering and production sputtering equipments are installed at Moorestown. Although many substances can be deposited by sputtering, we have selected the moly-gold materials set to provide optimum characteristics of adhesion, bondability, and conductance for microwave circuits. Substrate-to-component connections and connections between substrates are made by thermo-compression gold wire or ribbon welding. Fig. 1 shows a typical microwave assembly made by this process.

The basic thick-film substrate processes have not changed, although advances in design techniques, materials, and machinery have contributed to an order-of-magnitude increase in complexity and size.

Combining thick- and thin-film processes on the same substrate provides the advantages of each. For example, the wide range of resistor values and high power capability of thick-film inks combined with the high accuracy of thin-film conductors provides an improved means of constructing microwave and high-speed digital circuits.

Design automation aids hybrid design and production.

The practical implementation of very large and complex hybrids has been aided significantly by the design automation facilities and programs for hybrid designs[1,2] that use the CUTTER and AUTODRAFT programs developed at Moorestown. When experienced people use these facilities and programs, it is possible to cut design time by a factor of three. Also, the design review, manufacturing review, and modifications, plus accurate artwork, assembly drawings, and documentation can all be done from a single data base.

Examples of hybrid circuits

Very-high-speed circuits are possible with hybrids.

High-frequency digital circuit tests using microwave design techniques have compared packaged components on printed circuit boards with unpackaged components mounted and connected by thick-film hybrids. The typical maximum clocking speed for the hybrid in a pseudo-random code logic configuration was 800 MHz, whereas the printed-circuit board configuration was inoperable above 500 MHz. This has made it practical to deliver equipment capable of performing logical functions at 640 MHz. The thick-film hybrid shown in Fig. 2a operates at 640 MHz with good tolerance to variations of power supply and drive levels. It is constructed of micro-strip conductors between the top and bottom of the substrate, with gold ribbon bonding through laser-drilled holes in the substrate to make short ground

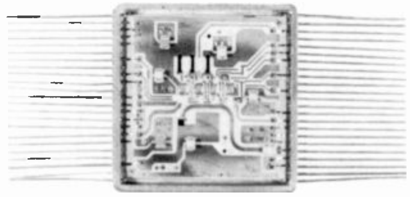

Fig. 2a
Higher-frequency digital operation is possible with hybrid circuits than with packaged components on pc boards. Thick-film hybrid here is capable of 640-MHz operation. Package is 1.25" square.

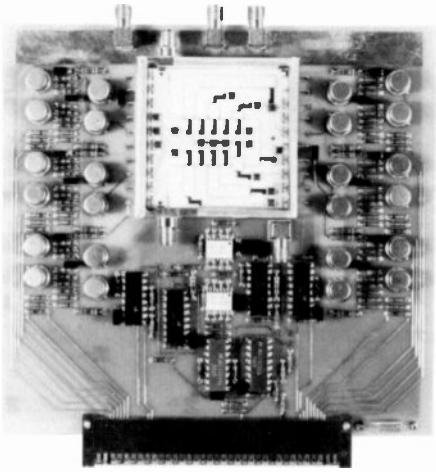

Fig. 2b
Companion delay-line hybrid to the one in Fig. 2a uses both thick- and thin-film technology. Board is roughly 6½" square.

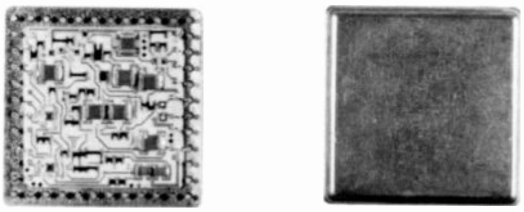

Fig. 3
"Hot-trimmed" video amplifier has its circuit characteristics adjusted while it is operating and undergoing test. This method gives performance chaıacteristics that could not be obtained otherwise. Substrate is 1.25" square.

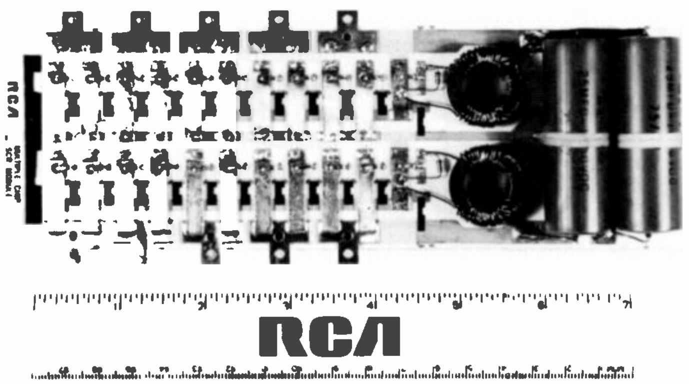

Fig. 4
Largest single-substrate hybrid produced at Moorestown, this 8-by-3-inch modulator. circuit can accommodate 1000 V at 500 A.

connections from bottom to top. Two-layer gold thick-film conductors plus resistors and insulators are on top, and a thick-film ground is on the bottom.

Fig. 2b illustrates a companion hybrid, which is a 6-bit electrically-controlled delay line constructed with both thick-film resistors and conductors and alternatively with thick-film resistors and thin-film conductors, with no discernible difference in performance. Delays of 25 to 1675 picoseconds of the 640-MHz digital pulse train are provided by PIN-diode switching within the 2"×2" module.[3]

"Hot trimming" improves analog circuits.

The video amplifier[4] shown in Fig. 3 is an example of a circuit set that is adjusted in production by "hot trimming" to match characteristics from circuit to circuit. It has provided improved gain tracking, dynamic range, bandwidth and temperature sensitivity, none of which could be achieved by other construction techniques.

High-power hybrid circuits are possible.

High-power microwave circuits and high-power modulator circuits have been and are being produced at Moorestown. The high-power modulator circuit shown in Fig. 4 is the largest single-substrate hybrid produced at Moorestown; it measures 8"×3". Capable of switching 500 A at 1000 V, its calculated dissipation is 750 W. The unit is fabricated with thick-film conductors and resistors on an 0.1" beryllia substrate and can be either air- or liquid-cooled.[5] The 22 active devices are SCRs.

Module families standarize product lines, improve reliability, and lower cost.

The MSR main product line of high-performance tracking radars has required large numbers of active components. Over the past twenty years, a remarkable improvement in component packaging density has been made, by a factor of 2000 to 1, in progressing from vacuum tubes to discrete solid-state devices to integrated circuits. Simultaneously, performance requirements have increased so that the number of integrated circuits now contained in a modern phased-array radar (AN-SPY-1) has reached 50,000. In order to reduce cost and increase productivity and reliability, MSR has developed standard modules that can be used within a product and from product to product. The standard module families include comprehensive circuit rules, including wiring rules from module to backplane to rack.

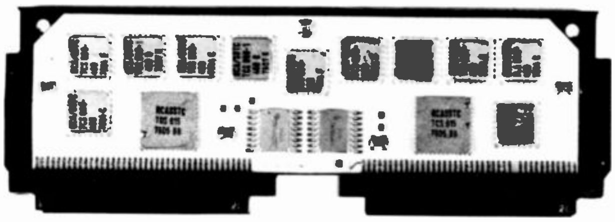

Fig. 5a
Leadless hermetic packages (LHPs) used on this hybrid make 100% automated testing possible. High yields are possible because individual LHPs can be fully tested before assembly. Standard plug-in module shown measures 1.4 by 5 inches.

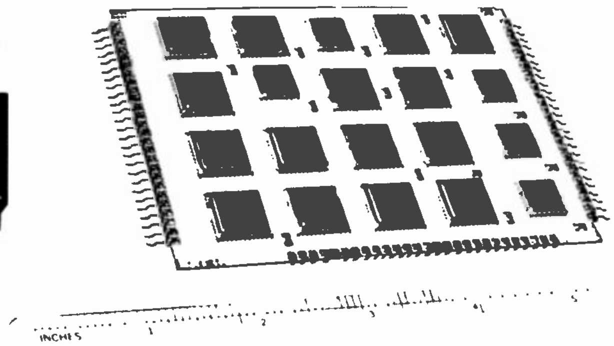

Fig. 5b
Forty active chips are on this complex hybrid, which measures 3 by 4 inches. LHPs make such complex substrates possible.

Complex high-yield hybrids

With the introduction of higher-speed circuits and LSI in standard dual-in-line and flat packs, it became evident that the area occupied by the hermetic package was the limiting factor in achieving packaging density and speed. Although hybrid packaging with uncased components would provide full performance and density advantages, the size of the hybrids was limited by yield.

Low yields were basically caused by the inability of assuring complete performance capabilities of chips before assembly and the cost of repairing large hermetic packages. Three major requirements must be met for producing complex high-yield hybrids:

1) 100% burn-in and test of semiconductors
2) 100% test of substrates
3) Simultaneous assembly of components to substrate.

All three of these advances have been made practical by assembling components in ceramic leadless hermetic packages (LHPs), in which active components are mounted, sealed, burned in, screened, and tested, thereby providing performance assurance before assembly. Multiple LHPs are mounted to multiple-layer thick-film substrates by simultaneous reflow soldering, which subjects components to minimum temperature-time stresses and provides excellent mechanical, thermal, and electrical connection to the substrate. Since mounting pads are constrained to the fixed dimensions of the LHP, it is cost-effective to implement fixtures to contact all mounting/interconnection pads on the substrate. These pads are spaced to accommodate individual "Pogopin" fixtures, which can provide interconnections for 100%-automated conductor-continuity and short-circuit tests before assembly with active devices.

By combining 100% component test, 100% substrate test, and simultaneous assembly, it has been possible to achieve 95% yield at initial assembly of production hybrids, even when using dozens of very complex LSI chips.

Assuming some devices will fail during assembly or in use, the ceramic substrate, with its multiplicity of small LHPs, offers advantages in fault isolation and repair over large hermetic packages. All pads are available at the junction between LHP and substrate, and each LHP can be individually heated and removed, then replaced by resoldering.

This technology has been used to design and build a set of standard plug-in modules with substrates measuring 1.4"×5" (Fig. 5a). It also leads to successful implementations of very complex hybrids, such as the 3"×4" unit shown in Fig. 5b, which contains 40 active chips of many types of LSI.

The future for hybrids

Printed circuit boards may eventually be replaced.

The basic hybrid technology has matured to a firm standing in providing performance and packaging-density advantages that can be achieved in no other way. In many cases, cost advantages are also shown as indicated by the availability of many commercially available assemblies in hybrid form. Substantial improvements in materials, processes, and machinery are being implemented in the industry. Among the most notable are the introduction of fine-line non-noble metal systems and automated equipment, both of which will further reduce cost, improve yield, and increase the maximum area available to the hybrid designer. With concurrent advances in the semiconductor art to larger chips, it should become practical to produce complete functional systems economically on hybrid substrates and replace printed circuit boards in many applications.

Automated testing and assembly will make hybrids more economical.

The availability of hermetically sealed chips on film that can be tested and screened before assembly to the substrate promises to provide high assembly yield and long life without hermetic package sealing. Also, enhancement of design automation programs with direct interfaces to numerically controlled assembly and test machinery will improve system economics and increase the economic use of hybrid techniques.

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2. Ramondetta, P.W., and Smiley, J.W.; "Design automation for complex CMOS SOS LSI hybrid substrates," *RCA Engineer*, Vol. 22, No. 1 (Jun Jul 1976) p. 35.
3. Designed by D.D. Freedman.
4. Designed by D.J. Demsey and E.L. Henderson.
5. Designed by D. Pruitt.

Hybrids—a look at the total cost

B.T. Joyce

Size, weight, performance, volume—these have been the traditional hybrid microcircuit driving requirements. But hybrids can also be cost savers, even in low volume applications, if total system cost is the basis.

The AN/USM-410 Automatic Test System provides an interesting opportunity to make cost comparisons between hardware produced using conventional discrete parts and hardware produced using equivalent hybrid microcircuit packages. Actual equipment has been built both ways so that historical data and factory cost estimates were available to make such comparisons on a total-build basis.

AN/USM-410 Automatic Test System

The AN/USM-410 is a third-generation, computer-controlled automatic test system. Typical of such equipment is the packaging arrangement of consoles and rack-mounted chassis suitable for depot, van, and shelter installations. Size and weight are not generally driving forces to the design.

Hybrid microcircuits found a very important place in this rack-mounted equipment, providing performance improvements. In addition, the hybrids were cost effective, a result primarily from the size reductions in the attendant equipment. There were fewer circuit boards, less chassis, a smaller rack, less labor in putting things together and getting them working—all acting to offset the higher initial cost of completed hybrids compared with the piece parts they replace. The reasons for using hybrids in the test system in the first place are presented in the remaining part of this paper along with the results of some cost comparisons of the discrete-part circuits and the substituted hybrid microcircuits.

A major problem that has plagued automatic test systems for years has been the interface between the tester and the unit-under-test (UUT). Whenever a test system serves a variety of different UUTs, special adapter cables and test-adapter boxes would proliferate. Such interface hardware makes the unique interconnections to the UUT and augments the test system with special loads and interface circuits. The procurement, logistics support, and change control of such adapters for fielded UUTs become very cumbersome and a major expense to the user. In the AN/USM-410 Automatic Test System, RCA introduced a Programmable Interface Unit as a viable solution to this problem. The Programmable Interface Unit (Fig. 1) provides 128 identical universal-test-point circuits, each of which can, under program control, be connected to a UUT interface line for measurement purposes or for excitation from a selected dc, ac, or pulse stimulus. The number of universal test points that can be provided in a given system is flexible because of the modular construction of the unit. Fig. 2 shows one of the dual-universal-test-point boards used in the Programmable Interface Unit.

Even though the Programmable Interface Unit simplifies interface adapters and eases test programming and test

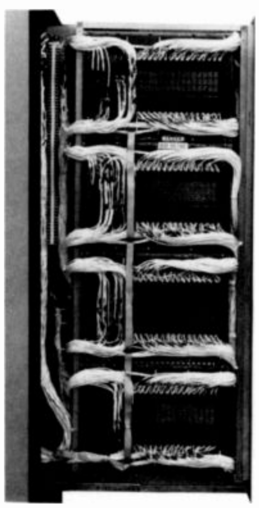

Fig. 1
Programmable interface unit replaces the myriad special adapters and cables of previous systems by placing universal test points under program control.

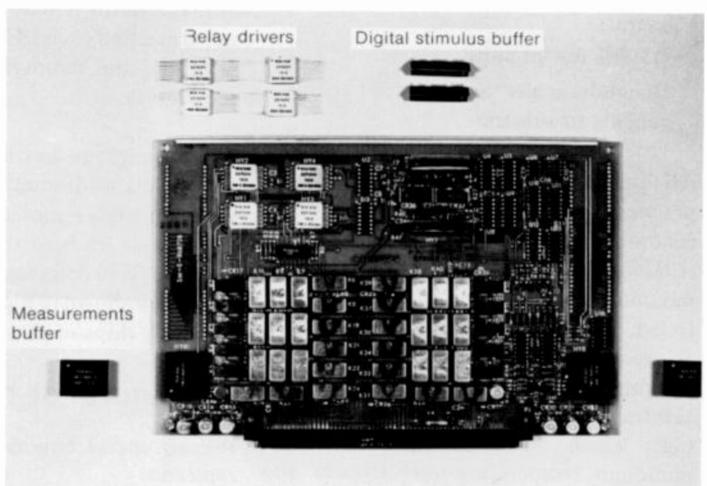

Fig. 2
Dual-universal-test-point board. Sixty-four such boards are used in the programmable interface unit. The hybrid microcircuits used on this board are arranged around the periphery of the board.

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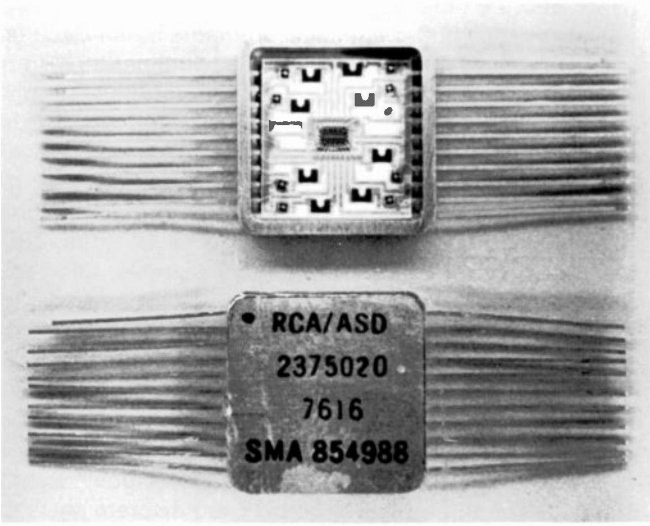


Fig. 3
8-channel, latching relay driver was the first circuit to be partitioned for hybridizing because it could be used on other boards of the main test system as well as on the universal test point board. A relatively uncomplicated hybrid, the circuit involves a dual, quad-latch integrated circuit, eight chip transistors and eight identical resistors. The thick-film substrate is solder mounted with gold-germanium in a 22-lead flat pack. The package is hermetically sealed with gold-tin solder. Substrates are printed on a multiple-image plate, sixteen circuits at a time. The circuit itself provides eight latched outputs, each of which can sink up to 100 mA of load current to ground.

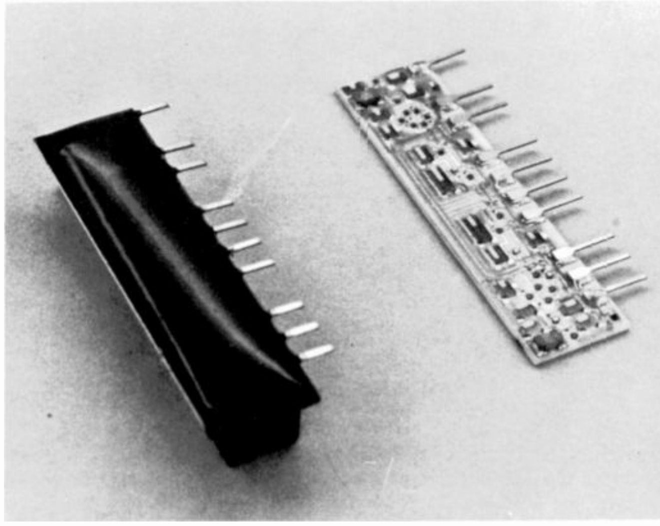


Fig. 4
Digital stimulus buffer hybrid is made up of 10 beam-lead diodes, 12 beam-lead transistors, 2 chip capacitors and 18 thick-film resistors. The package has leads for edge-type connection to a PC board. The conformally-coated circuit is provided with a heat sink to permit power dissipation of 2 W under maximum specified load conditions. In the test system, the digital stimulus/buffer is used to drive a unit-under-test with signals whose *high* and *low* voltage levels are programmable over a range of -20 V to + 20 V. The pulse width and pulse repetition rate are also controllable from programmable switching signals.

program maintenance, the unit itself is clearly complex and represents an increase in the cost to the test system hardware. Thus, the designers had to drive these costs down. Furthermore, the unit presented potential technical problems because of possible large physical size. Conventional discrete-circuit packaging methods would lead to a physically large unit that would be more susceptible to system noise problems and performance degradation from line capacitance and resistance. The designers were motivated, therefore, to use hybrids to reduce the physical size of the unit to manageable levels. Cost/performance tradeoffs studies revealed that despite the low production quantity, three circuits of the universal test point board could be converted to hybrid packages without cost penalty. These circuits are:

1) 8-channel, latching relay driver (Fig. 3).
2) Digital stimulus buffer (Fig. 4).
3) Measurements buffer (Fig. 5).

Hybrids vs discretes—cost comparison

The case for using hybrids has often been lost in the past by a superficial comparison of so-called parts costs. Fig. 6 dramatizes how such comparisons of "parts" costs can be misleading. Here the cost of each AN/USM-410 hybrid microcircuit, treated as a purchased part, is compared with the cost of the discrete piece-parts it replaces. The costs shown here, and at all other places in this paper, have been adjusted to reflect a factory-sell level appropriate to deliverable equipment. Note that, in the simple comparison of parts costs, these particular hybrids run from two times to three times more expensive than the piece-part equivalents.

Clearly, the cost study must penetrate beyond the basic costs of parts.

The hybrid, indeed, is more expensive than the piece parts it replaces simply because of the labor content added to produce a completely functioning circuit. Permitting objective cost comparisons, the AN/USM-410 provides two good baseline configurations of printed circuit boards, one associated exclusively with the relay driver circuit function

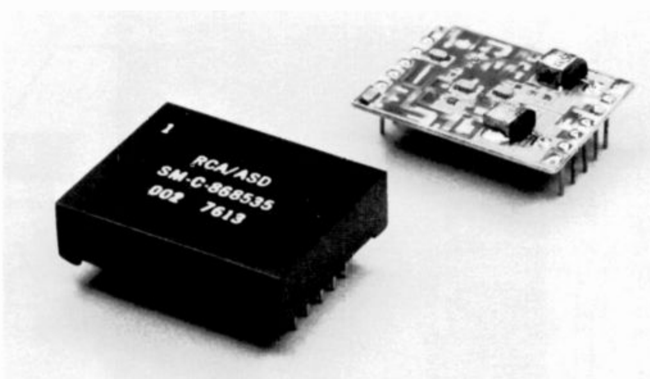


Fig. 5
Measurements buffer hybrid is a high-performance, unity-gain video amplifier used from dc to 10 MHz as a buffer between input signals from a unit-under-test and the measurements electronics of the test system. The hybrid packaging uses chip-and-wire construction. Chips are protected by encapsulation from the relatively benign environment seen by this class of equipment. In the manufacture of this hybrid, functional trimming techniques are used to optimize the gain and frequency response of the circuit.

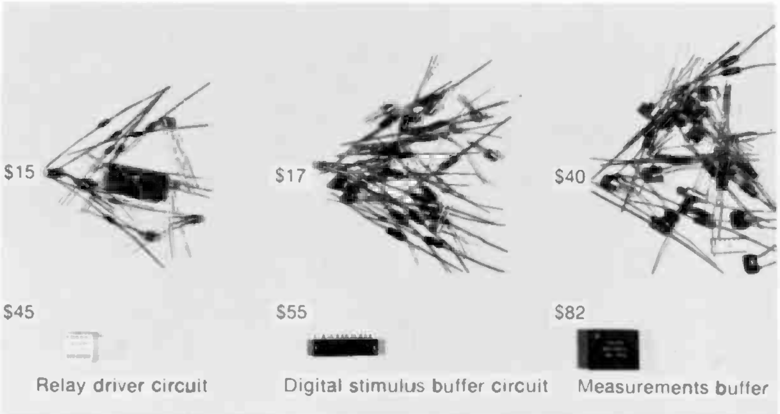


Fig. 6
Comparison of parts cost (hybrid vs. discrete) can be very misleading, mainly because the labor content involved in assembling the discretes has been ignored.

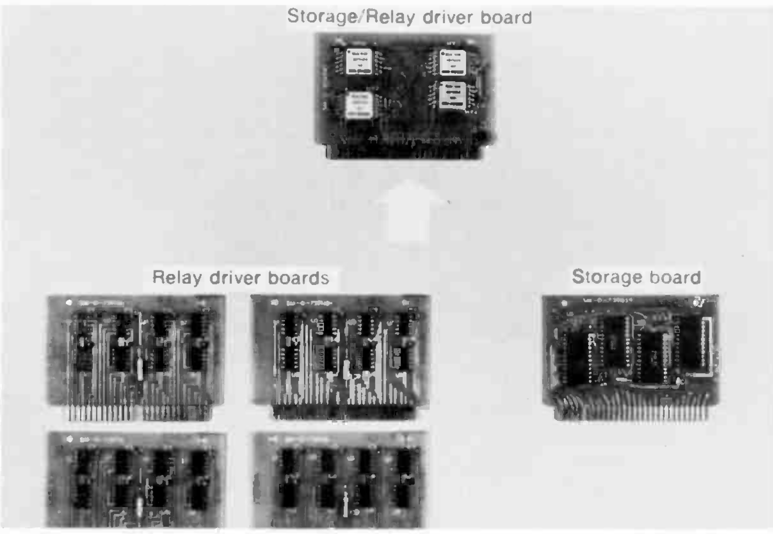


Fig. 7
Hardware reduction from the use of a hybrid relay driver with obvious savings in board fabrication, assembly, and test.

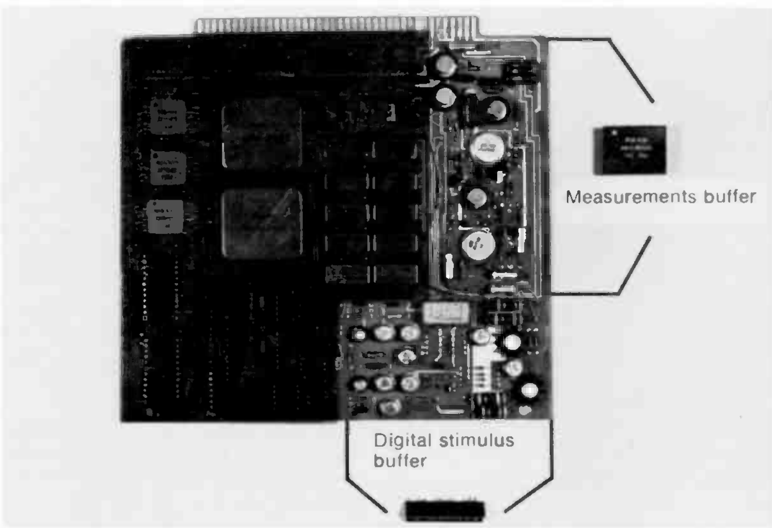


Fig. 8
Universal test point board (early version) shows another dramatic hardware (thus cost) reduction.

and the other associated primarily with the digital stimulus buffer and measurements buffer circuits. Fig. 7 shows the evolution of a combination of four 8-channel, latching relay driver circuits first configured with discrete parts (integrated monolithic circuits) spread out on four identical relay driver boards and one storage board. The hybrid packaging allowed these five boards to be replaced functionally by one board with obvious cost savings in board fabrication, assembly, and test. Similarly, the Automatic Test System has provided an opportunity to get a thorough comparison of costs for the two versions of the digital stimulus buffer and the measurements buffer. Fig. 8 shows an earlier circuit board configuration of a single universal test point for the programmable interface unit. Unlike the dual universal test point board shown in Fig. 2, this board used discrete parts to implement the functions of the two buffer circuits. But again, the two different arrangements provide good sources for cost comparisons.

The basic elements of recurring cost must be reviewed for an objective comparison of the cost of each circuit function in discrete form and in hybrid form. These recurring costs are:

- Electrical material (parts)
- Printed-circuit-board fabrication
- Assembly labor of PC board
- Test labor of PC board
- Labor and material associated with next level of assembly
- Manufacturing engineering and support labor

There are, of course, non-recurring costs that can be considered but will not be included in any detail in this paper. In general, most of the differences in non-recurring costs for the subject hybrids and their discrete-part equivalents were associated with the design layouts. The hybrid microcircuit layouts were indeed more difficult to perform and ranged in cost between $1500 and $4000 apiece.

Results of cost comparison: each hybrid microcircuit comes out looking better than the discrete parts it replaced.

Table I summarizes each element of cost allocated to the hybrid version and the discrete-part version of each of the three circuits. The table is divided into three groups of two colums each—one group for each of the circuit functions. Starting with the cost of the basic parts and treating the hybrid itself as a finished part, costs are compared for each major element.

After "basic parts" costs, the next element of cost examined is that for "PC-board fabrication." Here, actual (unpopulated) board costs for the finished products in both discrete and hybrid form were compared. Thus, in the case of the relay driver, the total cost for the five boards using discrete parts (see Fig. 7) was divided by four to allocate $36

Table I
Cost comparison of discrete vs hybrid circuits. The costs are based on circuit functions in quantities of 500 to 1000. The costs (at factory sell) are rounded-off to the nearest dollar.

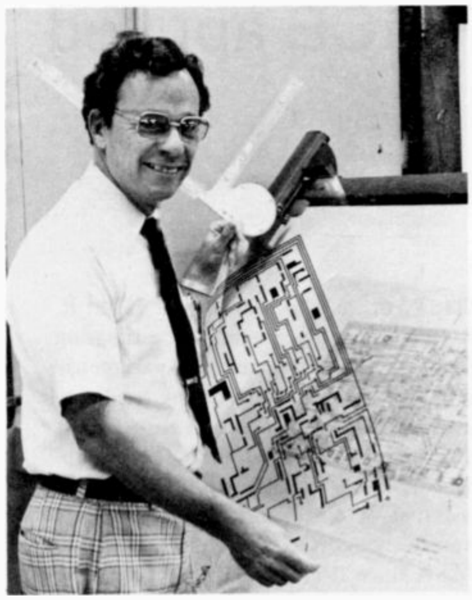
	Costs per circuit function					
	Relay driver		*Digital stimulus buffer*		*Measurements buffer*	
	DIS	HYB	DIS	HYB	DIS	HYB
Basic parts (material)	$15	$45	$17	$55	$40	$82
PC-board fabrication	36	7	16	1	19	2
Assembly to PC board	15	2	17	1	16	1
Circuit test	1	—	2	—	2	—
Chassis mat'l/ass'y	12	7	12	7	12	7
Mfg. eng'g & support	6	1	9	1	10	1
Total costs	$85	$62	$73	$65	$99	$93
Relative costs	100%	93%	100%	89%	100%	94%

DIS: circuit using discrete parts
HYB: circuit using hybrid technology

to the PC-board cost for a single 8-channel relay driver function in discrete form; and the cost of the single board using hybrids was divided by four to allocate $7 to that same function in the hybrid version. Similarly, costs for PC-board fabrication were allocated to the discrete and hybrid circuit functions for the digital stimulus buffer and the measurements buffer making use of cost records associated with these boards and taking into account the relative area utilization of the circuits on the boards.

The cost figures shown for "assembly to PC board" are derived simply. The large differences here are a fundamental result of the substantially different number of parts being handled for the discrete versions compared with the hybrid versions. Although the dollars associated with PC-board "circuit test" are small compared with other cost elements, a parenthetical note is worth making. The discrete-part versions of the circuit functions in general are still very much subject to failure at board test and costly diagnostic testing and rework must follow with potential degradation of an entire board. The cost for comparable testing, malfunction finding, and rework in the hybrid microcircuit is already built into the so-called piece-part cost of the completed hybrid.

The next cost element, "chassis mat'l/ass'y," is concerned with carrying the circuit function costs to the next level of assembly. Thus, if the number of boards in a system is reduced, so too are the number of connectors that have to be assembled and wired in a chassis and the number (or size) of chassis and racks to handle the boards for a given system-level complement of circuit functions. For the universal-test-point configuration of the AN/USM-410 Test System, a half-rack of hardware with hybrids does the same job that two half-racks of hardware do with discrete parts. Thus, costs for the two versions, apportioned to single circuit functions, are shown.



Brad Joyce has been directly involved with the product design and application of hybrid microcircuits since 1971. He has previous experience as a design manager for signal processing electronics, digital computers, and automatic test equipment.

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The last cost element, "mfg eng'g & support," compares the support costs per circuit function for manufacturing methods engineers, test methods engineers, and material control people.

The last line provides the total factory costs in the manufactured equipment for each of the three circuit functions. Each hybrid microcircuit comes out looking better than the discrete parts it replaced.

Conclusions

Hybrid microcircuit packaging has long answered a need where size, weight, and performance have been driving requirements. Hybrids may now seriously be considered as cost effective even in relatively low production quantities if the total costs of manufacture in the end-item equipment are accounted for and, in particular, if the beneficial effects of miniaturization are recognized.

Acknowledgments

I want to give special recognition to the engineers who designed the electrical circuits for the hybrids so successfully used in the AN/USM-410; to B.A. Bendel for the 8-channel Latching Relay Driver, to R.P. Percoski for the Digital Stimulus Buffer; and to D.F. Dion for the Measurement Buffer. Both Mr. Bendel and Mr. Percoski designed the Programmable Interface Unit with its universal test point approach and performed the initial cost analyses supporting use of hybrids in the AN/USM-410.

PRICE applied

F.R. Freiman

The PRICE model estimates costs accurately and inexpensively; comparable conventional estimates now average 40 to 50 times the cost of a PRICE estimate.

PRICE, or, as *Business Week*[1] called it, "RCA's uncanny system for estimating costs," is a computerized parametric modeling system for estimating hardware development and production costs. It has been under almost continuous development at RCA since about 1962. For the past five or six years it has been used extensively by RCA, and under contract to NASA since 1971 and the Air Force since 1972. PRICE was first offered commercially to industry in August of 1975. By the end of 1976, more than twenty-five major industrial organizations and government agencies had contracted to use PRICE.

Top-down extrapolation approach

As described in detail in the Jun/Jul 1976 issue of the *RCA Engineer*,[2] PRICE was formulated as a universal system to generate cost-estimating relationships for a range of products or systems. In essence, it extrapolates past experience to predict costs. It predicts equipment development and production costs for a wide variety of products, both electronic and mechanical, when provided with proper experience factors and new-product descriptions.

```
            AIRBORNE RADAR  MIL-SPEC  DEC 1,1976

            INPUT DATA
            QTY       200. PROTOS   10.0 WT      45.000 VOL      0.780 MODE      1.
            QTYSYS      1. INTEGE  1.000 INTEGS   1.000 AMULTE 125.000 AMULTM 125.000

            MECH/STRUCT
            WS     10.000 MCPLXS  0.0    PRODS    4.200 NEWST    0.900 DESRPS    2.000

            ELECTRONICS
INPUT       USEVOL  1.000 MCPLXE  0.0    PRODE    4.300 NEWEL    0.000 DESRPE    2.000
DATA        PWR     0.0   CMPNTS     0.  CMPID    0.0   PWRFAC   1.000 CMPEFF    1.000

            ENGINEERING
            ENMTHS    6.0 ENMTHP     6.0 ENMTHT     0.0 ECMPLX   1.200 PRNF      0.200

            PRODUCTION
            PRMTHS   25.0 PRMTHF     0.0 LCURVE  0.0    ECNE     0.0   ECNS      0.0

            GLOBAL
            YEAR    1976. ESC      8.300 PROJCT  1.000  DATA     1.000 TLGTST    1.000
            PLATFM  1.000 SYSTEM   1.000 PPROJ   1.000  PDATA    1.000 PTLGTS     1.00

            PROGRAM COST          DEVELOPMENT       PRODUCTION       TOTAL COST
            ENGINEERING
             DRAFTING                    252.              24.             276.
             DESIGN                      937.              73.            1010.
             SYSTEMS                     150.               0.             150.
             PROJ MGMT                   194.             328.             522.
COST         DATA                         61.              16.              77.
              SUBTOTAL(ENG)             1594.             441.            2036.

            MANUFACTURING
             PRODUCTION                    0.            6707.            6707.
             PROTOTYPE                   734.               0.             734.
             TOOL-TEST EQ                 97.             199.             296.
              SUBTOTAL(MFC)              831.            6906.            7737.

              TOTAL COST                2426.            7347.            9773.

            VOL       0.760 AVCOST   33.54 TOTAL AV PROD COST   36.74 LCURVE  0.897
            WT       45.000 ECNE     0.072 ECNS     0.021 DESRPE 0.494 DESPRS  0.210

CHECK       MECH/STRUCT
VALUES      WS       10.060 WSCF    12.821 MECID    0.0   PRODS  4.200 MCPLXS  5.602
            ELECTRONICS
            WE       35.000 WECF    44.872 CMPID    0.0   PRODE  4.300 MCPLXE  7.903
            PWR     182.399 CMPNTS   4053.                PWRFAC 1.000 CMPEFF  1.000

            SCHEDULES
SCHEDULES   ENMTHS    6.000 ENMTHP  14.874 ENMTHT 24.679 ECMPLX 1.200 PRNF     0.200
            PRMTHS   25.000 PRMTHF  50.229 AVER. PROD RATE PER MONTH           7.927

            COST RANGES           DEVELOPMENT       PRODUCTION       TOTAL COST
COST             FROM                   2122.            6121.            8242.
RANGES           CENTER                 2426.            7347.            9773.
                 TO                     2874.            9162.           12036.
```

Fig. 1
Typical PRICE estimate starts with input data, such as size, weight, and quantity of the system under evaluation (an airborne radar in this example). Outputs include a range of cost estimates and production rate.

An attractive feature of the PRICE system is the ease and speed with which these cost predictions are obtained. The trained PRICE user gathers data about a proposed product, asking a few simple but cogent questions of the engineers planning the equipment. He enters these data on PRICE input forms, one for each different equipment in the system.

He then accesses the time-shared computer in which the PRICE model resides, using a local terminal connected to the computer by telephone line. Using this real-time terminal, after giving his user password, he enters the PRICE data, line by line, into an input file and instructs the computer to "run PRICE," specifying the output format desired. Within minutes, the terminal prints the output sheet (Fig. 1), giving the development, production, and total costs for each equipment, including the costs of integrating and testing the equipments as a complete system. Provisions are made to rapidly modify or correct any or all of the inputs and just as rapidly see the effects of these changes on costs. Using the method just described, it is possible to thoroughly cost out a multimillion dollar system in as little as two hours.

Since the PRICE model predicts from a "macro-" or top-down, rather than the "micro-" or bottoms-up, parts-cost approach of conventional estimating, it is not as sensitive to missing input data as is the latter. Obviously, the more you know about the physical charactersitics of the end product being considered, and the more basic descriptors you can supply, the more precisely PRICE can predict costs. But because the model uses basic hardware descriptors such as weight, volume,

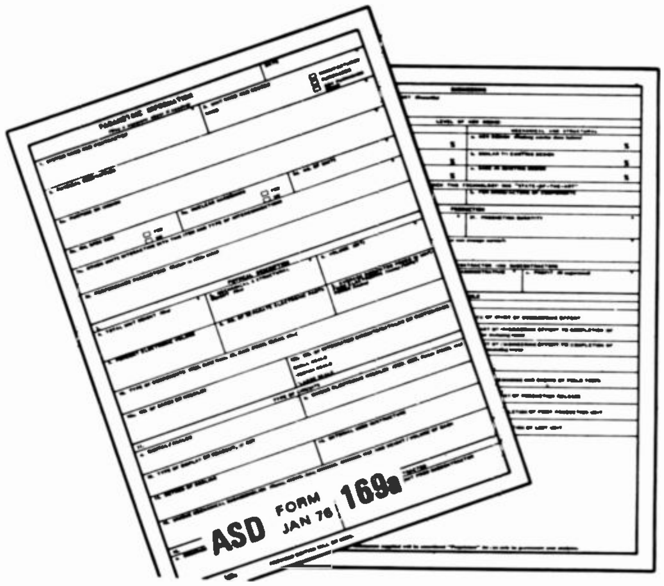

Fig. 2
PRICE is an input for source selection at some government agencies; Air Force Form ASD-169 is one example.

technology, percentage of existing designs, and the planned engineering and production schedules, unknown factors can be omitted and the model will calculate them.

When the PRICE model is calibrated with empirical values that represent an organization's way of doing business and their product line, the PRICE estimates become a reflection of the history of that organization and provide an indication of how the organization will perform on the new project under consideration for bidding. Since PRICE can be operated with a minimum of inputs, the manpower required to generate early estimates is significantly reduced. Thus, only a minimum investment need be made prior to the bid/no-bid decision.

PRICE is being used effectively in early configuration trade-off studies. As already mentioned, alternate configurations can be entered and virtually instant economic impact assessments made. Highly sophisticated and costly technical approaches can be quickly identified, and perhaps modified to a cleaner, simpler, and more cost-effective approach.

Although PRICE can be used to advantage throughout the various stages in the evolution of an equipment or system, perhaps its greatest value has only begun to be appreciated. Because of its universality and the way it handles the effects of both technology and economic changes, PRICE has been able to predict the future costs for a proposed system or product. Because of the rigor of its algorithms and structure, it has proven many times to be more accurate in forecasting a system's costs than the technologists who have proposed or evolved the new system.

Decisions to invest in a new product depend not only on market forecasts of consumer demand, but also hinge upon the profitable selling price of that new product. That depends upon development, design, and production costs—the investment an organization must make to bring the product to the market. Industrial history is replete with examples of mistakes made as a result of poor cost predictions based on intuitive and conventional methods. Mistakes can be made in both directions. Underestimating costs can lead to resource-draining expenditures in bringing the product to market, and manufacturing costs that preclude a marketable price. On the other hand, many products have been left undeveloped or postponed because of inflated cost estimates, only to be scooped later by the competition.

Where to use PRICE

The universality of the PRICE model and its adaptability to the ideosyncracies of various organizations have led to its widespread acceptance. Applications through the entire sequence of a product's history are described below.

The single most profitable time to use PRICE is during the concept stage of a program.

Using PRICE here allows meaningful decisions to be made before configurations are frozen. Many users are applying PRICE during the concept period to trade off configurations and schedules, and in general to assist in establishing a basic program concept that they will propose to their customers. Many PRICE customers are using PRICE to assist them in making bid/no-bid decisions.

Another common application is to establish cost targets at the proposal stage for bottoms-up estimating.

PRICE not only will provide an estimate of overall system costs, but also will provide a breakdown of the costs for the constituent equipments in that system. Done early enough in the proposal cycle, this breakdown will provide planning budgets to the specialty design groups.

The most obvious use of PRICE is to review the finished proposal pricing before it is sent to the customer.

Several years ago, Irving K. Kessler, RCA Group Vice President, mandated that all proposals to the government in excess of $1 million be run through PRICE to check the reasonableness of the proposed costs to the customer. When the PRICE output differs significantly from the detailed estimate, there must be a valid reason, since PRICE follows the organization's experience trend.

Some government agencies use PRICE as one of their many tools in the source-selection process. Indeed, the Air Force often requests that data for direct input to PRICE be submitted with proposals, on Form ASD-169 (Fig. 2). The use of PRICE in the source-selection process should not be limited to government source selection of contractors, for it is also an applicable tool in selecting subcontractors.

PRICE can also be used to establish Work Breakdown Structure (WBS) budgets after the job is won.

If PRICE was used properly in the proposal stage, a good start has already been made in allocating funding via the WBS.

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Because of its methodology, PRICE can be applied anywhere along the product development cycle.

It will predict future costs whether it is used at the start of a program or part way through. If an accurate definition of the work yet to be done can be made, PRICE will create an estimate to complete a project far more accurately than that obtained by subtracting the amount of money spent from the original estimate.

What some users are doing

A major west coast aerospace company has set up a central PRICE activity that coordinates seven different locations and sixteen trained PRICE users. They use PRICE in all phases of a program. Their electronics division uses PRICE as the principal ingredient of their bid/no-bid decisions. Additionally, all budgetary estimates going to corporate headquarters for review and approval are supplied on the basis of PRICE outputs, with no other supporting documentation provided.

Frank Freiman, as Director, PRICE Systems, is responsible for developing and using parametric modeling systems for engineering and management planning and decision-making purposes. He invented the PRICE methodology described here. His latest invention is the PRICE software model, a universal parametric model that predicts costs for design of an extended variety of computer programs.

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At RCA Automated Systems in Burlington, the STE/ICE (automated engine testing) program equipment was processed through PRICE very early in a design-to-cost program. Prototype hardware parameters and production schedules were input to PRICE to provide a comparison with the very challenging design-to-cost goal. Estimates of the hardware parameters expected to result from the planned design approach were also input at that time. The design team then got under way with confidence based on PRICE results that the goal of reducing production cost by one-half was achievable and that the planned design approach would yield the required cost reduction. During the system design phase, PRICE was employed to check vendor estimates for a critical subassembly as well as to characterize the design parameters of this subassembly when configured to meet the assigned cost target. The current estimate (1977) of both the STE/ICE system production cost and the cost of the purchased subassembly remain well below the established cost targets.

Another major west coast aerospace facility has a senior scientist who routinely evaluates every program in the concept stage and helps scientists and engineers make early trade-off studies in both hardware and schedules. He is functioning virtually as a one-man design review team, devoting all of his time to early-concept evaluations.

He made a recent study on two airborne digital processor assemblies. The existing processor design primarily uses integrated circuits. The engineering department felt that the production cost could be reduced if both assemblies were redesigned, to be functionally the same, but using LSI. Management imposed the constraint that the redesigned LSI version of the processor must cost 20% less in production than the present model; otherwise, it would not be cost-effective to bother with the redesign. This figure, with the quantities involved, would determine the breakeven point to recover the cost of redesign.

Both assemblies were entered into the PRICE design-to-cost mode, the target cost established for each assembly set at a value 20% lower than its present integrated-circuit version's cost, and the PRICE model was run. The output of the PRICE model in the design-to-cost mode is the design geometry required to meet the specified target average unit cost in production. Moreover, the estimated cost of the engineering redesign program is contained in the PRICE outputs being used for the decision. Using this, the reasonableness of the 20% breakdown point could also be verified.

In the case of the first assembly, engineering judged that they would be able to meet the indicated specifications. In the case of the second assembly, they decided that the requirements were, at this time, too severe. The decisions were made: Assembly No. 1—proceed with the redesign; Assembly No. 2—do not proceed with the redesign.

An east coast space operation recently used PRICE to measure the reasonableness of bottoms-up estimating on a major satellite proposal. They did that by running the ECIRP (PRICE spelled backwards) procedure on some recent satellites. ECIRP is a procedure that allows the derivation of empirical factors such as electronic and structural complexity from product history. The derived empirical factors were used as inputs to PRICE, giving a high degree of confidence that the established cost targets for the new project were empirically credible. The same operation also uses PRICE routinely for budgetary estimates and applies it on a regular basis to check out subcontractor cost proposals.

How can an RCA engineer use PRICE?

Engineers who plan new products or systems must be concerned with the economics of the development and production costs.

Configuring a new project with an unrewarding result is not good business. It also does not pay to produce a system whose cost exceeds that of other devices with equivalent performance. Moreover, a new product usually has many alternative design arrangements involving varying technologies, a mix of purchased items, or advancing the state of the art. Each variation will have an associated cost picture. Therefore, knowing the economics of each approach is important in determining the best technological direction to take.

An engineer can also use PRICE to determine the time needed to develop and design, as well as produce, the new systems. PRICE provides outputs that are credible indications of the times required. With this knowledge, an engineer can more wisely select the technology scheme or concept that is most economically feasible.

PRICE has its limits.

It requires the ability to estimate the weight and size of the design being considered. PRICE's philosophy is that the physical make-up of the equipment required to make a system perform generates its cost, rather than the performance itself. For example, one can design and build a computer using tubes, but it would require many racks of equipment with their inherent cost. The same computer requirements can be met by a design using an LSI technology. This advanced computer would be smaller and probably outperform the tube system, and moreover would be far more economical.

The average cost of processing a PRICE study to complete a "black box" is about $50. This includes the engineer's preparation and PRICE Systems costs. There are procedures within PRICE that will render production and development costs with minimal ancillary output information, which would reduce the cost to about $20 per "black box." Conventional estimates to the same level of detail now average 40 to 50 times the cost of using PRICE.

Getting aboard PRICE.

To get started with PRICE, a contract must be given to RCA PRICE Systems for a year's use of the model. One unlimited access to the model for one year's use will cost $30,000. In addition, there is a computer charge, which averages about $5 per study. To use the model, an engineer must be trained. This involves a two-week PRICE course given at Moorestown or Hollywood every month. Fig. 3 shows a typical PRICE class. After successfully completing the course, the engineer user is given the privilege of exercising the model. The two-week course is an intensive "hands-on" program, in addition to a thorough education in the computing procedures of the PRICE model. Trainees are instructed to correctly determine and prepare input information. Specialized instruction is given toward identifying and correcting erratic, distorted, or otherwise impossible descriptive information. There are many data checks built into the model that limit the processing of faulty parametric inputs.

More detailed information regarding the character of the model, its processing, and variable operating procedures is available through the PRICE Operations group in Moorestown.

Fig. 3
Learning to use PRICE: Two-week "hands-on" courses on using the PRICE model are given each month.

PRICE stands the test.

On face value, the PRICE model appears to be an overwhelming and impossible tool. Because of the claims made for PRICE, it initially generated more skepticism than positive response. To establish the model's credibility and confirm the claims that are made for it, interested engineers would have to test the model. This procedure involves inputting descriptive information about a concept that has been developed and produced. Based on the limited input data, the model will generate a "predicted" cost. The calculated costs can be compared to the actual expenditures. If they agree reasonably, the test has confirmed the model's predictability and claims of its capabilities.

This testing procedure is possible because there is a PRICE procedure that causes its mathematical regressions to revert to the economic and technological conditions of any past point in time to 1946. For example, if 1965 is used as an input, the user can enter design information that was known in 1965 and the model will process it from that point. Literally hundreds of such tests performed over the last five years have proved the claims made for PRICE. Virtually every PRICE customer has tested the model in this manner to assure that the PRICE method is appropriate to his products and organizational procedures.

Conclusion—PRICE is right

From the applications described, the advantages of using PRICE are manifest. Its universal applicability, its varied modes, and the speed with which its estimates are obtained, combined with the cost savings over conventional estimating, make PRICE invaluable as a management tool. Indeed, as confidence in PRICE grows within an organization, conventional cost estimating may be used less and less frequently. Readers within the RCA engineering community will recognize the advantage obtained by competitors who use PRICE, and will want to use one of the many RCA personnel who are trained in PRICE to assist in costing their proposals.

The PRICE system is being continually updated and improved by the RCA PRICE staff, and tested by both customers and staff. New models are under development to cover life-cycle cost and software estimating. As these and other improvements go "on line," PRICE becomes increasingly valuable to users and to RCA as an expanding "product line."

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Economic modeling: how Solid State Division predicts business trends

L.O. Brown

The Solid State Division is using several economic forecasting models to predict business turns, positive and negative, that affect near-term operations and profitability.

Four factors characterize the solid state industry:
- Extreme volatility to economic swings.
- Rapid technological advancement.
- Proliferation of applications.
- Changing customer requirements.
- Continued price erosion despite inflation.

Under these conditions, successful performance cannot be based on "gut feeling" entrepreneurship alone. The solid-state supplier must also have a good insight into the immediate marketplace and reasonable forecasts of both the micro and the macro spheres of the economy.

In the past, as part of the planning process, Solid State Division has tracked trends in end-equipment development and production and has qualitatively assessed the effects of changes in the macro economy on sales and operations. Lacking, however, were the tools and methods required to allow quantitative analysis of such change, so that realistic long range plans could be produced and undesirable bottom-line impacts minimized.

Following the sharp business decline in the third quarter of 1974, the Solid State Division embarked on a program to select and develop improved methods of economic tracking and modeling to fulfill these needs. This program was aimed at defining indicators that would forecast the probability of turns in business, both positive and negative, that would affect near-term (one to six quarters) operations and profitability. Through this program, it was hoped that pending economic change could be identified in sufficient time to develop and activate contigency plans.

From the myriad concepts explored to date, a handful have emerged that appear to fulfill the objectives of the project. In retrospect, if such concepts were available eight years ago, they would have provided a nine to twelve month "early warning" of both the 1970 and 1974 downturns and would have signaled the end of recession and return to a more normal business state three to six months earlier. Thus, in both recession and recovery, sufficient warning could be provided to allow retrenchment or expansion to meet future conditions and minimize the "bottom-line trauma."

In this paper, some of the concepts and methods of economic modeling currently being used by the divison are briefly examined as to: the insights they may provide into the nature of the business under study, their value as leading indicators of change, and their capabilities of producing realistic near-term forecasts of sales. Mathematical details of the techniques used are not given in the paper, but can be furnished to others who may need similar programs to supplement their planning.

Consumption/inventory model

The consumption of components (semiconductors) in sales of end-use equipment was one of the first models investigated and developed. The value of such a consumption model to a component manufacturer supplying parts to the end-equipment industry could be threefold:

- When compared with component shipments, it can show component inventory status at the end-equipment manufacturers' level, and signal turns in component sales when large inventory accumulations are evident (downturns) or when previously accumulated inventories are being eliminated (upturns).
- When compared to new orders and the total orderboard, it can provide insight into the "reality" of the orderboard and indicate the possibility of "double ordering" (because of product scarcity) by the user industries.
- Through a correlation of the component inventory status with general economic trends, changes in an equipment manufacturer's policy regarding inventory turnovers may be identified and the effect of such policy changes on near-term component sales can be anticipated.

In developing the consumption model, an "input/output" coefficient is developed for the specific component under consideration. This coefficient represents the value of the component in the "average" end-equipment unit. The I/O coefficient is then multiplied by the value of the shipments

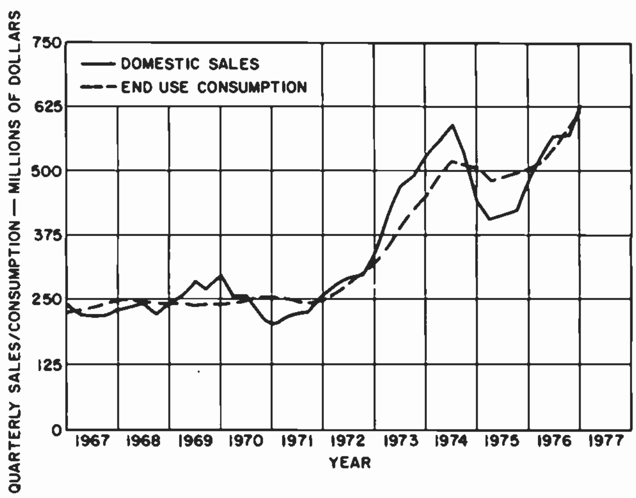

Fig. 1
Consumption vs sales for solid-state components. The difference between estimated end use of semiconductor devices and solid state domestic sales shows change in inventory.

of end-equipment to obtain the consumption of the component under study.

Results of the procedure, as applied to the domestic sale of semiconductors, are shown in Fig. 1. In this figure, the estimated domestic consumption of semiconductors (semiconductor use in end-equipment shipments) is compared with semiconductor sales to the equipment manufacturers. The change in inventory in any given quarter will, of course, be the difference between the components received in that quarter and the component content of the end equipment shipped in that quarter. This is change in total, or "pipeline," inventory, and includes unused components in stock and components in work-in-process and in unshipped finished equipment. Total inventory is then calculated as the integral of inventory change plus the inventory that existed at the "zero time" of the model.

A plot of the inventory for semiconductors derived from the consumption model described above is shown in Fig. 2.

Every manufacturing industry maintains a certain "desired" inventory level to support continued operation. The actual level of this desired inventory may be influenced by several factors, such as length of time to restock, current level of production and sales, and cost of maintaining the inventory. In the model, only the current business level is taken into consideration, and thus the desired level of inventory in any given quarter is entered as a constant times the component content of the end-equipment shipments of the previous quarter. An estimate of excess inventory is then made by subtracting the desired level from the total, (Fig. 3).

A comparison of Figs. 1 and 3 shows that downturns in semiconductor sales occurred during the first quarter of 1970 and third quarter of 1974, respectively. Inventory accumulation, however, began in the first quarter of 1969 and 1973 and progressed sufficiently to indicate a future turn in sales by the third quarter of 1969 and 1973.

Since the onset of inventory accumulation is a good indicator of future downturn in sales, the Solid State Division revises and updates this model on a quarterly basis. Further, even longer lead time in predicting slowdowns is obtained through the use of econometric forecasting models for both consumption and sales of solid-state devices.

Econometric forecasting models

As used in SSD, econometric modeling is the generation of mathematical functions representing factors in the micro economy (e.g., sale of semiconductor devices) in terms of macro economic factors as independent variables. In developing such equations, a linear relationship between variables is assumed and coefficients for each independent variable assigned through the use of least-square-deviation techniques over a historical base. Multiplicative models may be developed using the same techniques by relating the logarithms of the dependent and independent variables. Confidence in the derived model(s) may be gained through correlation with the original dependent variable, calculation of the standard error of the model, and through other statistical tests.

Such models are of value in the business planning cycle to:

- Produce forecasts.
- Gain insight as to product demand in various segments of the macro-economy through a study of the coefficients of the model.
- Investigate the effect of pricing and other competitive actions on sales.

While the generation of a micro model, such as product sales, is relatively straightforward, forecasting with the models usually requires the availability of a viable forecast of the accounts in the macro economy. Since the process of generating good macro economic forecasts on which to base micro forecasts is both complicated and costly, services such as Data Resources Inc., Chase Econometrics, or Wharton Econometrics are often used. The Solid State Division uses Data Resources, Inc., and results presented in this discussion are based on their macro forecasts.

Two statistically viable micro-econometric models have been generated using these methods: the first, total domestic sales of solid-state devices; and the second, the consumption of solid-state components in end-equipment shipped by the equipment manufacturer. Both models have been projected forward through 1977 using the December forecast of the general United States economy as seen by Data Resources, Inc. Model results are shown in Fig. 4. Major differences between these curves and those of Fig. 1 are the result of seasonal adjustment of dependent

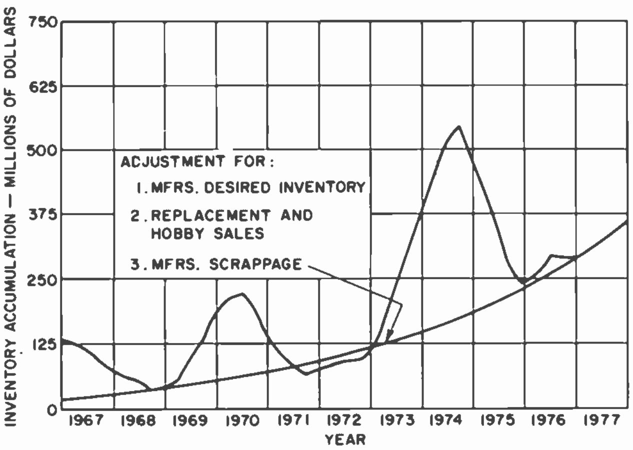

Fig. 2
Inventory for semiconductors derived from the consumption model of Fig. 1.

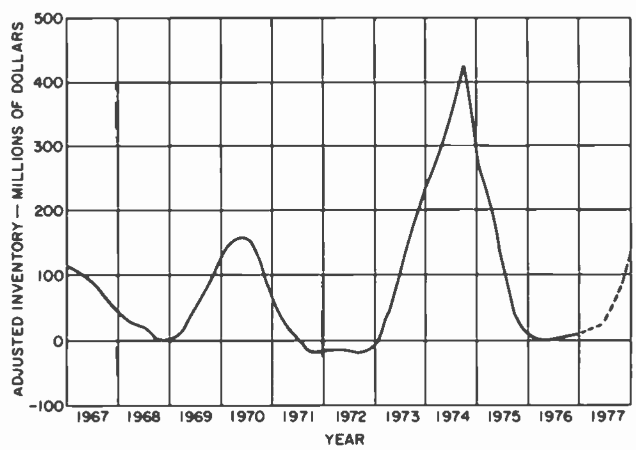

Fig. 3
Excess inventory is estimated by subtracting the "desired" inventory level from the total given in Fig. 2.

variables prior to modeling, the small errors inherent in the models and, of course, the forecast for 1977. The excessive growth noted in the forecast of solid-state sales in the third and fourth quarter of 1977 (over the growth of end-use consumption) indicates the potential of an excess inventory accumulation in late 1977.

The least-square regression techniques used in the definition of the models not only aid in the selection of economic accounts explaining the dependent variables (solid-state sales or end-use consumption) but covertly build into the model the consumer's, merchant's, and manufacturer's behavioral patterns inherent in the history of the independent variables. Further, each point in time of the solid-state series can be considered, in an economic sense, as the equilibrium point (or intersection) of the product supply and demand function, other parameters being equal. Thus, a solid-state price variable was introduced into the model. Since the model form used is multiplicative, the coefficient of regression of this price variable can be considered as the average elasticity of demand for solid-state devices, with respect to price. From this coefficient, the industry elasticity of demand is estimated to be (with respect to price) approximately -0.48. This figure indicates that a 10% decrease in price will increase total sales volume by less than 5%.

Other techniques

While the two models described briefly above constitute a significant portion of the effort underway in the Solid State Division, several other important techniques are used in the process of economic analysis and planning.

Consensus forecasting is simple, relatively inexpensive, and reasonably accurate.

In consensus forecasting, a trade organization requests marketing research people from a number of companies to simply estimate the total dollar volume of sales of various semiconductor products for the industry over a number of years. The statistical report produced is an effort to average the various estimates. There is no discussion or reporting of individual company sales prices, market shares, or any other such matter. The report is available to anyone who wants it. While simple in concept and relatively inexpensive to carry out, the method is valuable (and has relatively good accuracy) in producing both short- and long-range forecasts on which to base long-range planning.

Cahners method compares industry growth against a selected indicator.

The Cahners Method of forecasting, developed by the Research Department of Cahners Publishing Company, is basically a method of comparing the moving annual growth (sales) of an industry with the moving annual growth of a selected indicator that has been found to correlate with, and lead, the industry under consideration. By relating history of the turning points of the indicator to turning points of the industry under study, and slope relations between turns, an estimate of future industry turning points and growth can be made. Typical indicators that may be used are: Housing Starts, Dow-Jones Industrial Average, Free Reserves, or composites of several individual series, such as the composite of 12 leading indicators published by the Department of Commerce. While conceptually and mathematically unsophisticated and lacking in accuracy, this procedure is relatively inexpensive and will produce fairly reliable trend information as to business turning points and the approach (or continuance) of growth or recessional modes in the short-term future.

The indicator tracking method allows visual correlation between the industry and related economic series.

Least expensive of the techniques discussed, but probably of equal importance to techniques such as the Cahners Method discussed above, is the tracking of economic series related to the industry under consideration. Such series may be chosen either from the vast number of series published regularly by the Department of Commerce and the Federal Reserve Board, or may be obtained as a mathematical combination of such series. Such indicators are readily interpreted (as to their relationship to the industry) through graphical display over history. The advantage of this type of display is that trends of the economic series can be visually established and related to the trend of the industry series. Published series found to have high correlation with Solid State Industry sales and used within the Division include: Consumer Durables, Manufacturer's Durables, Consumer Sentiment Index, Private Housing Starts, and Gross National Product. Derived series used are a measure of discretionary income (disposable income less non-discretionary items such as food, clothing, household expense, transportation expense, and consumer debt liquidation), and an inventory index generated as a ratio of quarterly growth of manufacturing and trade inventories to the quarterly growth of expenditures for goods capable of being inventories. All series used to generate these indicators are published on a regular basis and are in the public domain.

The inventory index is shown in Fig. 5. Economic recessions, as defined by the Department of Commerce, are shaded areas in the Figure. As shown, each period in which the ratio has exceeded a value of one has been followed by a recessionary period, with the exception of the period from 66:1 through 67:3. While most components in the GNP showed marked decline in this period, large increases in military spending resulting from Vietnam war buildup

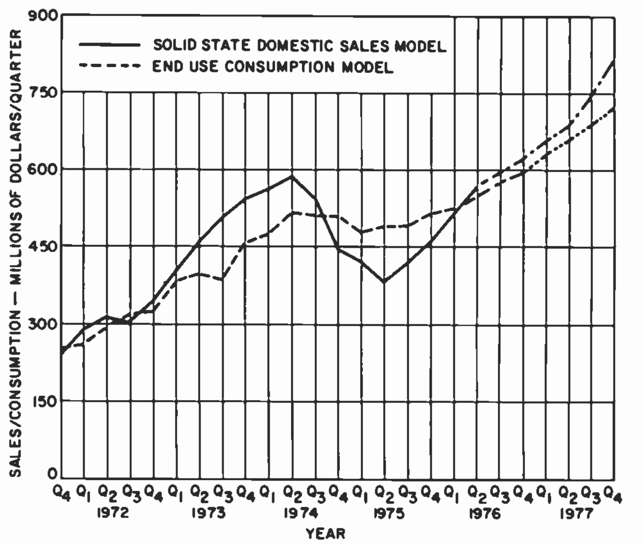

Fig. 4
Domestic sales/consumption model for the solid state industry.

prevented the total real GNP from the decline required (by the Department of Commerce) to define recession. A projection of the index, using the December forecast from the Data Resources, Inc., indicates the possibility of "excessive" inventory growth beginning in the first quarter of 1978.

Simple least-square methods involve modeling of an industry series with a single economic variable.

The econometric models discussed above are frequently referred to us as least-square multiple regression analysis since the technique involves the modeling of an industry series with several economic series simultaneously. This process is relatively expensive since it requires a large computerized data base as well as considerable computer analysis time. With the relatively inexpensive programmable and statistical calculators presently available, a simple, one-variable regression model may be generated at relatively low cost. While not yielding the accuracy or business insight of the multiple regression models, business trends and turning points can be more accurately predicted than with the two methods just described, particularly if the independent variable exhibits a good lead time over the industry-dependent variable. Further, most of the time series that may be considered as independent variables for such models are available as "hard copy" in journals such as *Business Conditions Digest* and *Economic Indicators*. An example of this technique is shown in Fig. 6. In this figure, annual growth in solid-state domestic sales is shown as a function of the annual growth of the U.S. GNP (current dollars) slipped by one quarter. All major turns in the growth of the industry are clearly matched with turns in the growth of the GNP.

Conclusions

Economic modeling is valuable in providing a better insight into the solid-state business. The program has further been of value in the development of long-range strategies and plans.

In developing the program, a reasonable balance has been maintained between program cost and value obtained. The program is not completed: new models must continue to be generated and added to those already in place, old models must be continually modified and updated to conform to the latest data and forecasts of the macro economy, and analysis and interpretation of model results must be provided to generate the economic scenario against which logical long- and short-term plans can be made. Only through such well-based planning can advantage be taken of available opportunities, and contingencies met, for the best interest of the Division and the Corporation. Since no major recession has occurred since the initiation of the program, the true value of it to the Division has yet to be tested and proven. Through the technique of "forecasting history," however, reasonable confidence has been established in the ability of the program to fulfill its objectives.

Lloyd Brown joined the Market Research Staff of the Solid State Division in 1973. Since the downturn in 1974, Dr. Brown has devoted his major effort to developing a better understanding of the interrelationship between solid state sales and the general economy.

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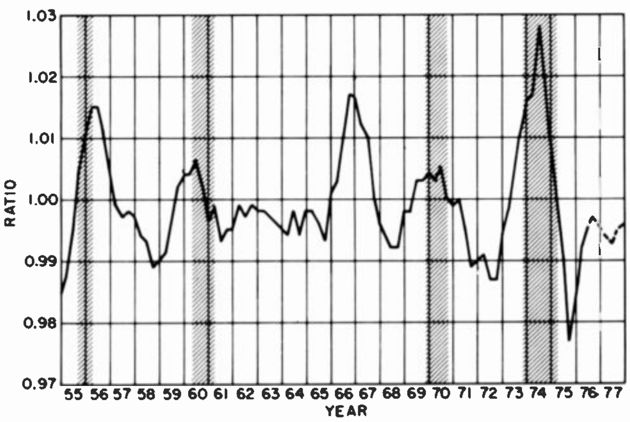

Fig. 5
Inventory index as derived from the indicator method of economic modeling.

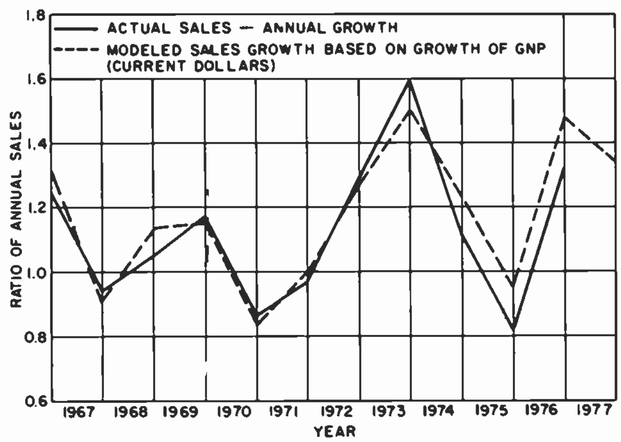

Fig. 6
Least-square method showing growth in solid-state domestic sales as a function of annual growth of U.S. GNP.

NBC Engineering—a fifty-year history

W.A. Howard

Part II: NBC's engineering "firsts" continue, from the beginnings of color tv up to today's computerized stations.

The beginnings of color television

Work on color television began as early as 1930 in the RCA Laboratories. As in the development of black-and-white television, there was a very close working relationship between NBC and RCA engineers, since NBC studios and transmitting facilities were the proving grounds for color television.

As early as 1940, RCA demonstrated the first color television system to the FCC, and on March 20, 1941, NBC used a field-sequential mechanical system to broadcast the first color signals from the Empire State Building. This system required a rotating color disc on both the camera and receiver.

Compatible color replaced the mechanical system.

Color television developed very slowly during the war years, but in 1946 RCA Laboratories presented the first public demonstration of an all-electronic color television system. The following year, members of the FCC witnessed a demonstration of "compatible color," a color picture that could be received not only on a color receiver, but also on any standard black-and-white set. Compatibility was very important to the success of color television, since so many homes already had black-and-white receivers.

In 1951, NBC and RCA engineers began an intensive schedule for field-testing all-electronic, compatible color television. NBC engineers had developed and installed a complete color facility at the Colonial Theatre, New York, using the most modern lighting, switching, and technical developments available at that time. This installation was America's first large-scale color television production studio and became the proving ground for the country's present color television system.

Again, the NTSC was called upon to formulate standards for a new television system in the United States. The NTSC worked from January 1950 to July 1953, undertaking the most comprehensive examination ever made into the principles and practice of a color television system. NBC engineers played an important role in this committee, with representation on all of its task forces. The final report totaled 18 volumes, 4100 pages.

Early in 1953, an NBC/RCA Liaison Committee on Color Television was formed to get ready to meet the demands for color equipment that were certain to arise after the approval of the proposed NTSC standards. On June 25, 1953, NBC and RCA engineers petitioned the FCC to adopt the compatible technical signal specifications demonstrated by NBC and RCA and approved by the NTSC.

On December 17, 1953, the FCC gave its long-awaited approval to compatible color television standards and authorized NBC to transmit using them. On the day of the FCC approval, NBC used the new compatible-color standards to broadcast programs to its entire television network.

This historic event in television was followed immediately by many more color firsts for NBC. The Tournament of Roses Parade, in Pasadena, Cal., was carried in full color by the entire NBC television network on January 1, 1954, making it the first major event televised on the new standards from a location outside the studios. The pickup was made with a new NBC color mobile unit that had been engineered and fabricated by NBC Engineering. This event also marked the first west-to-east color transmission on the new color standards.

Color television meant major changes in equipment, studios, and techniques.

The year 1954 saw the beginning of a major program for NBC Engineering to supply color facilities for the NBC network and owned stations. Studios, transmitters, switching systems, and all distribution equipment had to be colorized. New techniques had to be developed for testing transmission facilities, including the NBC network.

The first large color studio completed was the Brooklyn I studio in New York, which provided approximately 15,000 square feet of staging area. This was followed in 1955 with the Center Theatre, Ambassador Theatre, and large studios on 67th Street, New York. The Ziegfield and Hudson Theatres were added in 1956. For color film, the Radio City 4G/J film studio complex, with six RCA TK-26 color film cameras, went on the air in 1954. The 5H film facilities, with six additional cameras, were added in 1955.

"Color City," in Burbank, Cal., a $7 million project, went on the air on March 27, 1955, completing a major project by NBC engineers. This scored another first for NBC, as Color City was the first studio facility in the United States built from the ground up for color television. The most modern

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Bill Howard's photo and biography appeared with the first part of this article. (Vol. 23-2 Jun/Jul)

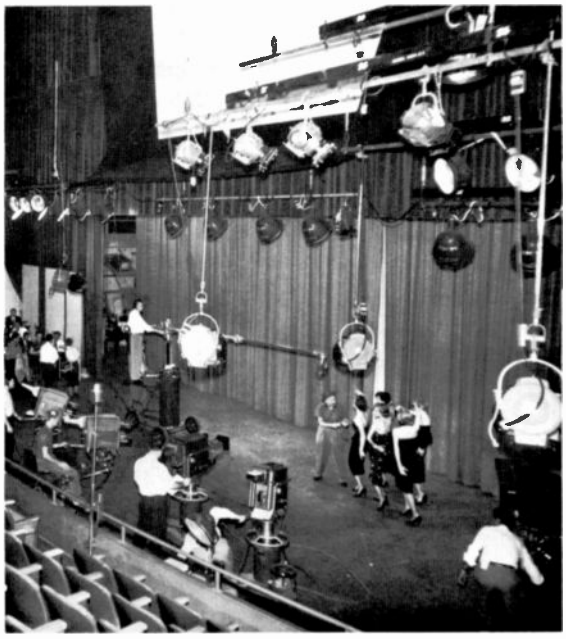
and finest color facility in existence at that time, it originated many of NBC's early color shows and earned a reputation in the industry as the ultimate in technical quality.

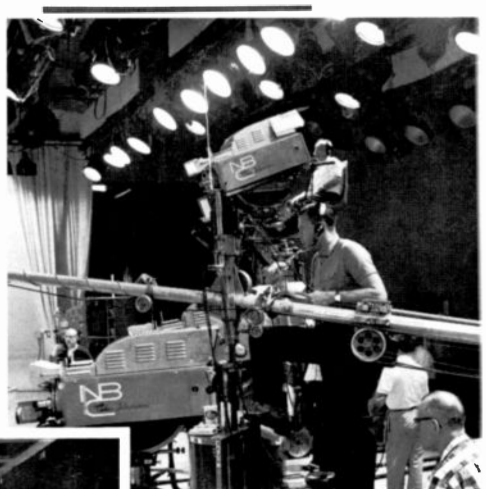
The year of 1955 marked many milestones in color broadcasting. A full Broadway production of *Peter Pan* was done in color with the original stars, Mary Martin and Cyril Ritchard. This show attracted a then-record audience estimated at 65 million viewers. The first color broadcast of a President—Eisenhower's commencement address at West Point—was telecast using the new NBC color mobile units. The first color coverage of a World Series (Yankees vs. Dodgers) was distributed to the entire NBC network. Another first for NBC and the NBC engineers was on April 15, 1956, when WMAQ in Chicago went on the air with its all-color facilities, making it the first station in the United States to offer 100% color programming.

The 1950s and early 1960s were years of pioneering for color television, and NBC Engineering made important contributions to its growth. NBC Laboratories developed many of the techniques and signals that are used industry-wide today for testing amplifiers, switching systems, and network facilities, (e.g., multi-burst, stair steps, and window test signals). The sine-squared pulse, also used industry-wide, was introduced in this country from Europe by an NBC engineer, Ralph Kennedy.

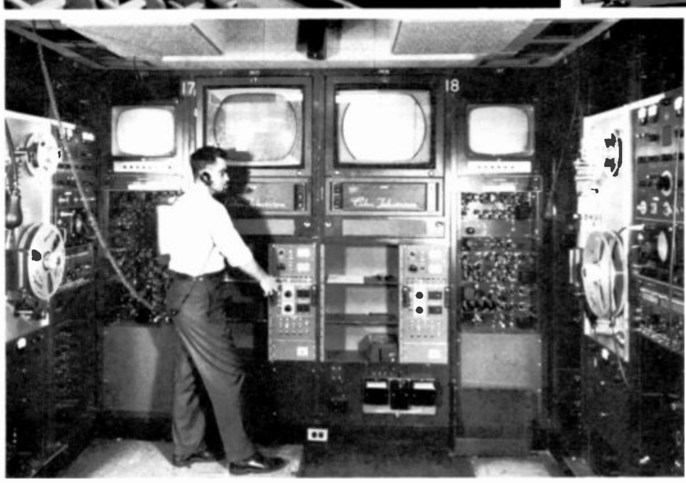
Other developments originating in the NBC Laboratories prior to 1960 included all types of video effects such as chroma key, a color television effect in which a foreground scene can be electronically placed in a still or moving background scene without having the background show through the foreground. These developments were the forerunners of the highly specialized video-effect systems used in all modern-day switching systems.

By 1965, color television had mushroomed to an annual retail sales level of more than $3 billion in the United States, and NBC had converted a major part of its facilities to color. In announcing their 1965-66 programming, NBC offered 95.8% of its schedule in color, thus making NBC the first "Full Color Network."





1 Jimmy Durante rehearsing at Color City, Burbank, the first studio facility built for color television from the ground up. 2 Charles Schadel operating one of the first RCA color video tape recorders (TRT-1) in the late 1950s. 3 The color chimes logo, used from the 1950s through the early 1960s. 4 TK-41 color cameras during rehearsal at the Colonial Theatre in New York, where field testing of the NTSC color standards was done. 5 Color film equipment installed at WRCV, Philadelphia, as part of the big changeover to color.



Engineering leadership at NBC

O.B. Hanson, an outstanding engineer and administrator, served as Chief Engineer of NBC from its formation in 1926 until 1954, a span encompassing major technological developments in both radio and television. Robert E. Shelby followed Hanson as Vice-President of Engineering and Operations until his death in 1955. Andrew L. Hammerschmidt then held that position until 1961, and was followed by William H. Trevarthen, who served until his retirement in 1973. John R. Kennedy then became Vice-President, Operations and Engineering, a post that he presently holds. Frank L. Flemming has been Vice-President, Engineering, NBC Television Network, since 1969.

Contributions by NBC engineers

In viewing the many contributions made by NBC engineers over the past 50 years in the broadcast field, it is evident that the rapid expansion of technology has made many of them now obsolete. However, at the time of their development, these contributions served important functions to NBC and the broadcasting industry. It is impossible in this article to name all of the engineers who made major contributions; however, there are a few whose accomplishments have been extremely important to the growth and development of NBC.

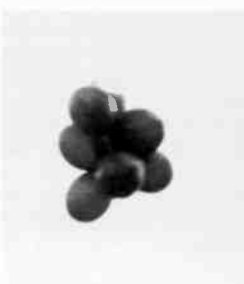
One such engineer, Lew Hathaway, served in the NBC Engineering Department from 1929 to 1972, a span of 43 years, during which radio and television grew from its infancy to a multi-billion dollar industry. He was granted 37 U.S. patents in radio and television, won three major awards from professional societies, and received two Emmy nominations.

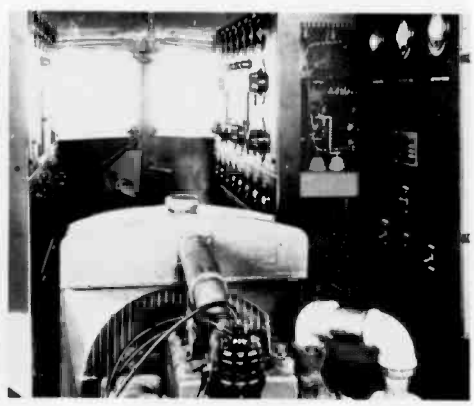
In 1972 the National Academy of Television Arts and Sciences awarded NBC Engineering a "Citation for Oustanding Engineering Development" of the "hum bucker," a video transformer developed by Mr. Hathaway that is used industry-wide today by broadcasters and telephone companies on remote pickups. Another of his developments was interleaved sound, an emergency audio-transmission facility for television that uses gaps in the frequency spectrum of the video signal. This system is still in use today on the NBC network between New York and Burbank.

Vernon Duke, a veteran of 37 years with NBC Engineering, was granted over 20 U.S. patents and made major contributions to the development of studio and film cameras, kinescope recording, video tape, and film processing. He also served on many industry committees and authored several industry standards in the area of television film.

Television tape

The first quadruplex video-tape recorder was demonstrated to American broadcasters in March of 1956. This system of recording and playing back television signals became universally accepted by the broadcast industry; using tape as a method of delayed broadcast and show syndication revolutionized television.





However, the first quadruplex tape recorders could not record and play back color signals. NBC was well on its way to becoming all-color, so color tape was necessary. NBC and RCA engineers developed a color heterodyne system for recording color on magnetic tape, and the following year (1957), NBC began the first delayed broadcast of color shows out of its Hollywood studios. A year later the operation was transferred to the new NBC Burbank studio, where eight color recorders served the entire NBC network. By 1961 there were sixteen recorders in Burbank, twenty in New York, and all the owned stations were using color video-tape machines.

NBC made other contributions to video tape by developing remote start-stop and mode selection for all of their recorders. By 1960, the NBC Burbank engineers had developed a double system for recording and editing with video tape using a 16-mm magnetic sound recorder and a 16-mm kinescope recorder. A number of the NBC specials were edited with this system. Today, large video tape complexes with modern electronic editing systems have been installed in Burbank and New York, with approximately 30 color tape recorders at each location.

Remotes and mobile units

Over the span of radio and television broadcasting, a large part of NBC's programs have originated from "remotes," or locations outside the studios. In order to have the best coverage for sports, news, and entertainment originating at these "remote" locations, NBC Engineering has been responsible for engineering custom mobile units providing the same production facilities as the fixed studios.

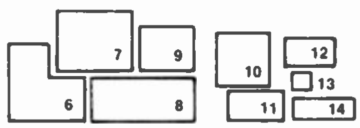
The network's inaugural radio program on the evening of November 15, 1926 was a remote originating from the Grand Ballroom of the old Waldorf-Astoria Hotel on 5th Avenue, the present site of the Empire State Building. A four-hour program featuring some of the finest talent available originated from this remote and was transmitted by telephone lines to the NBC control room at the AT&T Building for distribution to the network's 21 radio stations.

Mobile units date back to the early days of radio.

In the early years of radio, NBC's large fleet of mobile units using rf microphones and radio relay equipment covered many historic events, including the Hindenburg tragedy at Lakehurst, New Jersey in 1937. NBC engineers also used shortwave radio to bring news from outside the United States. A good example was the 1938 Munich crisis. Atmospheric conditions cut off the American broadcasters from immediate access to the event in Munich, Germany, so NBC engineers set up a shortwave circuit by way of Africa and South America to New York. Thus, on NBC exclusively, Americans heard the words of Prime Minister Chamberlain telling how Hitler would "come half way to meet me" in Munich.

Television's first mobile unit, engineered and designed by NBC, appeared on the New York streets on December 12, 1937. This unit was used for experimenting with and field-testing black-and-white television. When television was introduced to the American public in 1940, it was also via a remote, this time originating from a mobile unit at the New York World's Fair. And when NBC transmitted the first major network program on the newly adopted NTSC color standards, a remote of the 1954 Tournament of Roses Parade, it was done with new NBC color mobile units.

NBC Engineering also pioneered with "crash" television units equipped to operate on their own power while in



6 NBC's first mobile unit used a balloon-hoisted antenna. Engineer is Milton Kitchen. **7** NBC mobile units covered the *Hindenberg* tragedy, May 6, 1937. Cortney Snell, extreme left, was the engineer doing the pickup. **8** Mobile unit and *Hindenberg* a year earlier. **9** Interior of early mobile unit, showing generator in foreground and relay transmitter at rear. **10** Color mobile units field-tested NTSC standards in the early 1950s, later toured the country when standards were approved. **11** Black-and-white unit of the early 1950s. **12** America's first mobile television station as it appeared on its delivery to NBC on December 12, 1937. One unit was for pickup, the other for transmission. **13** NBC's logo from the 1960s until 1976. **14** Color mobile unit used in the 1960s and 1970s.

motion, maintaining continuity of sound and picture. On July 12, 1952, the first crash unit appeared on the streets of Chicago with its own power generator and microwave transmitter, transmitting sound and pictures back to the studio. In order to meet the requirements for participating in the presidential inaugural parade that year, a Cadillac limousine was outfitted to follow the full length of the parade without losing picture or sound. These units were the predecessors of the more modern units now used daily in today's "electronic journalism" operations.

Mobile television vans eventually became as well-equipped as the studios.

The first of the large multi-van remote units were designed and constructed by NBC Engineering and began operating in 1966 for sporting events. These units are also used for the Apollo launchings and pickups and the Miss America pageant. The first NBC unit of this type consisted of three forty-foot trailers—one each for camera equipment, production, and carryall.

The technical equipment supplied with these trailers was the same as supplied with any of NBC's fixed studios in New York or Burbank. It consisted of up to six color cameras, solid-state switching and effects equipment, quadruplex video tape recorders, instant replay and "slo-mo" equipment, and an audio console providing at least 30 microphone inputs. The units have been updated periodically to include newly developed equipment, such as character generators and slide storage equipment.

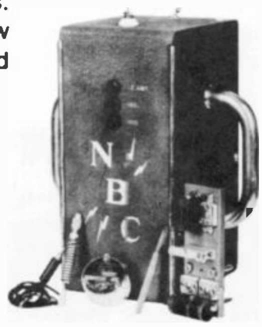
The mobile units designed later used more modern and compact equipment and so reduced the size and number of vans, but still provided the same production facilities. NBC today operates four of these large units out of New York and Burbank, with several smaller units at the owned stations in Chicago, Washington and Cleveland.

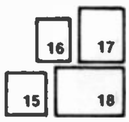
Portable cameras and electronic journalism

From the "walkie-talkie" to the "walkie-lookie."

NBC has been a pioneer and leader in developing and using wireless or rf microphones over a period of many years. The first use of an rf microphone system was in the 1936 Easter Parade on 5th Avenue, New York, with the transmitter and antenna concealed in a top hat. This was followed by later developments in the laboratory—in 1937, NBC's "beer mug" miniature transmitter operated in the 30-37 MHz band with a transmitter power output of 0.15 watt. The following year, a 2-watt uhf backpack transmitter was developed. These units, which were used extensively by the NBC news and sports departments for many years, were the predecessors of the complex systems used today that have two-way communication provided by a cue channel and a high-quality program channel. NBC's coverage of political conventions by radio began in 1928. The rf microphones used in these conventions were developed in the NBC Laboratories and soon became famous as "walkie-talkies."

NBC's television coverage of political conventions began on an experimental basis in 1940. At the 1952 political conventions in Chicago, NBC unveiled a portable rf-connected camera developed by NBC and RCA engineers. It was soon labeled the "walkie-lookie," as a companion to





15 Three-watt backpack remote radio transmitter of the late forties. **16** The famous uhf "beer mug" remote radio transmitter, developed in 1937. **17** NBC's first rf microphone system, used at the 1932 New York Easter Parade, was hidden in the top hat, with antenna projecting out. **18** Harry Truman being interviewed via NBC rf microphone during one of his famous strolls. **19** Engineer John Crampton demonstrates the "walking tv station" at the 1964 Democratic Convention. **20** RF-connected camera and beer mug radio microphone being used at 1956 convention. **21** NBC's peacock logo, used from the beginnings of the "Full Color Network" until 1976. **22** Correspondent Nancy Dickerson holding the ultraviolet-beam sound transmitter used at the 1964 conventions. Receiver is at left. **23** Modern TK-76 electronic journalism camera.

the "walkie-talkie." At that convention, NBC engineers also introduced the "crash truck," a tv newsroom on wheels, equipped with self-powered electronic and film cameras and its own darkroom. It was capable of preparing film for projection on the air in less than 10 minutes.

The 1956 and 1960 conventions saw increasing use of portable black-and-white cameras. Although the cameras themselves were small and lightweight, the control packs, microwave transmitters, and antennas were still heavy and bulky for maneuvering on the crowded convention floor. There were also problems with rf interference in the crowded 7-GHz microwave bands.

Two developments from the NBC Laboratories were used for the first time at the 1964 conventions. The first, the "black-beam" sound system, used a transmitter that sent out voice-modulated ultraviolet light. A receiver picked up the light, amplified it, and converted it to a standard audio signal. This system was used extensively from the convention floor and required no FCC license. The other new introduction was the electronic long-lens system developed by Fred Himelfarb. This system could increase the effective focal length of the standard camera lens electronically up to twice its normal magnifying power, so cameras were used extensively for close-ups from the convention floor.

Portable cameras became truly portable with the "walking tv station."

At the 1964 conventions in Atlantic City and San Francisco, NBC introduced a new rf-connected portable camera developed by NBC and RCA engineers expressly for these conventions. Soon labeled the "walking tv station," the system used camera and control units that were smaller and much lighter than for previous camera systems. For the first time, the camera's microwave equipment operated in the 13-GHz band, eliminating most of the noise and interference that had plagued previous microwave-link cameras. The complete package weighed less than 50 pounds and could be carried by one man.

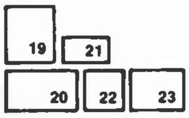
A new "crash" unit developed by NBC engineers was also introduced at these conventions. It was entirely self-contained, using a 5-kW gasoline generator to supply the power to operate all its equipment—two portable cameras, (walking tv stations), a portable video-tape recorder, microwave transmitting and receiving equipment, a video switching unit, and the necessary audio and communications equipment. While the vehicle was traveling at speeds up to 40 miles per hour, pictures taken by a cameraman on the roof could be transmitted via microwave to the main control center or taped for future use.

Between the 1964 and 1968 conventions, NBC and RCA Astro-Electronics engineers developed a portable color back-pack camera that transmitted video information in the 13-GHz band. This camera was used at the 1968 Miami convention for the first time. NBC Engineering has also worked with North American Philips on color rf-connected cameras.

Automation

Early automation used relay logic and steppers.

NBC pioneered the automation of radio and television operations. As the television facilities at Radio City and Television Master Control expanded in the 1950s, a form of automation using relay logic and steppers timed from precision clocks was installed in network switching, so that six channels could be individually preset and switched on a



real-time basis to eliminate human errors. Later this was expanded to the studio 5H control room, which controlled the local television station and provided network break-in. In this system, a complete station break could be preset and switched along with automatic roll-on projectors and tape recorders.

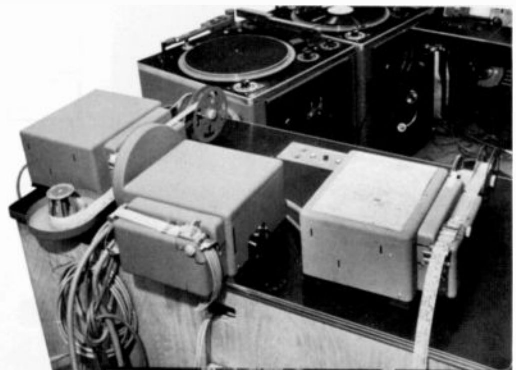
In April of 1958, NBC Burbank went on the air with 12 color video tape recorders, which recorded programs from the eastern NBC network and played them back to the Central Time network one hour later, and the Pacific Coast network three hours later. This automated system used relay logic and sequence-stepping switches electrically pulsed from precision clock impulses. It permitted preset recorders to record or play from specific recordings or playback lines at particular times and for particular intervals. Automatic rewind and cue-up were provided. For further automation, automatic gain control (AGC) amplifiers were used in both the audio and video program path. The color video AGC amplifiers had just recently been developed in the NBC Laboratories.

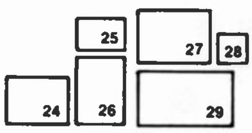
The first completely automatic station to be engineered by NBC was WBUF-TV in Buffalo, NBC's experimental uhf station, which went on the air in 1956. Again, relay logic, sequence steppers, and AGC audio and video amplifiers were used. A paper-tape system controlled the switching and pre-roll of film equipment and tape recorders. A full day's operation could be made up on punched tape and operators were needed only to load film and slide projectors. In 1959, WRC in Washington moved into a new television plant that was also completely automated using basically the same type of system that had been installed in Buffalo.

Computer control became a reality in the mid-sixties.

In the spring of 1962, a new switching central was placed in operation in Burbank, controlling KNBC and the Pacific network. The output switching at that time was done manually by loading information for each channel into preset relays, then putting the preset event on the air by using an enable pulse. The system anticipated, however, the eventual use of a computer for these functions, including storage of a full day's operation. The design of such a system, which was NBC Engineering's first experience with a computerized television system, was already underway. In March of 1966, the computer-controlled switching system was placed in operation in Burbank. A Daystrom Model 636 computer, which has a self-contained core memory of 20,480 words, stores, retrieves, and processes program information for switching three television channels. The programs for each day are fed from a variety of sources, including live studios, film chains, and video-tape recorders. Since the principal interface of the computer is through the keyboard and relay switching system, only three pieces of peripheral hardware are necessary: a tape punch and reader mounted in the main computer cabinet, and an electric typewriter through which the computer writes a log of the operation. Computer control for NBC Burbank has been in use for over eleven years and has been a very successful operation.

In 1969, the NBC Engineering Department began the automation and computer control of the entire NBC network in New York, a seven and one half million dollar project supervised by Frank L. Flemming, Vice-President of Engineering, NBC Network. After many planning sessions with operating personnel and extensive software contributions by the RCA Laboratories, the complex system began to take form. Many features of the system had to be developed, including machine control, a large routing switcher, and video source identification. The system was put into operation in October 1974, on a limited schedule,





24 Bob Lopez using the computer-controlled switching central at Burbank. **25** First automated tv station, WBUF in Buffalo, used paper tape readers to control film projectors and tape recorders. **26** Stepper-switch controllers at WBUF. **27** NBC's old television master control at New York. Originally engineered in the early 1950s, it was in constant use until 1974. **28** NBC's new "N" logo began use January 1, 1976. **29** Bob Post and Robert Waring at NBC's new switching central in 1976. Six separate channels can be controlled by minicomputer for an entire 24-hour day of automatic operation.

since this new system of operations involved changes in many NBC departments. By gradually increasing use of the system, it reached full-time operation (24 hours/day, 7 days a week) during July 1975. This modern and complex system is described in eight articles by NBC engineers in the Apr/May 1976 issue of the *RCA Engineer* (Vol. 21 No. 6).

Conclusion

The 50 years of NBC Engineering has spanned a period of major technological developments in communications that has permitted the nation's 620 low-powered radio stations in 1926 to expand into a multi-billion dollar annual business with over 700 television and 6000 radio stations. NBC engineers have made a major contribution to this development and expansion.

The challenge for NBC engineers in the future is equally as great as it was 50 years ago, with new technological applications and demands now on the horizon—digital television, microprocessors, image sensors, lasers and fiber-optics transmission, and the urgent need for a transparent international interchange system for television.

Acknowledgements

I gratefully acknowledge the helpful suggestions and information supplied by my colleagues in the NBC Engineering Department and thank the personnel in NBC Technical Operations and retirees who have supplied valuable documents and photographs. I would also like to express appreciation to my wife, an English major, for her invaluable contribution.

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The 1977 MIT-RCA Research Review Conference

What's new at MIT?

Computer education at MIT

just what does that young kid after your job know?

As an example of how the field of computer technology has grown, what was once a two-semester MIT graduate course on switching theory has now been squeezed into half a semester of an undergraduate course.

Today, the introductory course at MIT, called Switching Circuits, Logic, and Digital Designs, introduces the basic concepts of combinational logic, sequential circuits, flow diagramming, control modules, A-to-D and D-to-A conversion, microprogramming, and minicomputers. Each student in the course receives a portable laboratory in the form of a briefcase containing superstrips, switches, lights, power supplies, all the components needed for the lab exercises, and tools for assembling circuits. This course is followed by Digital Systems Project Laboratory, in which students use hardware/software tradeoffs, integrated circuits at the SSI/MSI level, and some LSI.

The coursework then broadens out into Minicomputers, Microprocessors, and Advanced Digital Systems, in which students pursue detailed studies of machine architecture, I/O organizations, memories, display terminals, and data communications. Projects in this course require the students to use MSI and LSI hardware and assembly-language programming on various micro- or minicomputers. There is also an undergraduate thesis option available for students with a further interest in the field.

The projects that students demonstrated at the conference were impressive. One, a game called MAZE, used a tv monitor to simulate the sensation of walking in a three-dimensional maze. The object of the game is to move through the maze and avoid being electronically "shot" by its robot inhabitants.

Electronic mail

the question is no longer "if?," but "how?"

Information handling is rapidly dominating the U.S. economy. More than 50% of the nation's workers are now involved with banking, finance, education, purchasing, personnel, accounting, research, etc., rather than the direct manufacturing of goods. The capital investment behind each manufacturing employee is now about $300,000, but only about $2,000 for a typical white-collar worker. This system is changing, though—technology is making its way to the office.

Presently, three different technologies—facsimile, word processing, and computer-based message systems—each with its own particular advantages and characteristics, are competing for the information-transfer market. The eventual winner will depend upon both advances in technology and decisions from the regulatory agencies.

There are presently about 100,000 facsimile machines in the United States; their popularity is based on their ease of use compared to, say, a Telex machine. Most of the communication done on them is alphanumeric, even though they can handle all kinds of graphical inputs. The second type of system, the word processor, now numbers about 110,000 in this country. Most of them do not have any communication capacity, but since the information in them is machine-readable, it could be easily and instantaneously sent electrically, rather than going through the trouble of typing a message out, putting it in a letter, and waiting for the Post Office to deliver it. As a result, the idea of communicating word processors is becoming a standard notion. The third type, computer message systems, provide a number of additional functions besides switching messages back and forth. In them, terminals at a number of locations, perhaps connected through a telecommunications network, contact a central computer that can receive messages, file them, forward them, search for past messages, retrieve data asked for in messages, or perform any number of other services.

Which type of electronic mail eventually dominates the market will depend on how the different systems meet certain performance criteria. For example, terminals must be everywhere, as ubiquitous as telephones, and should be able to be used by untrained operators. Users must be able to maintain privacy for their messages and also be able to authenticate that messages do indeed come from their supposed senders.

Computer-managed parts manufacturing

approaching mass-production economy for job-shop quantities

Machining a complete V-8 engine block in mass production costs roughly about $15, but machining only 100 of the same block would cost about $1500 per assembly. This 100:1 ratio is typical of what it costs to do low-volume manufacturing—a few hundred or few thousand parts per year. Considering that something like 90% of the world's total dollar volume of manufacturing involves items manufactured in quantities under a million per year,

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Ed. Note: Forty engineers representing most RCA divisions recently spent a day at MIT, attending a one-day seminar to learn what's new in the 2000 research projects under way there. Four of the presentations from that seminar are presented here in the form of notes taken by Hans Jenny, Manager of Technical Information Programs for RCA.

productivity increases in this area will bring about tremendous savings.

Several automated systems attacking this problem already exist. Computer control of all the operations in the manufacturing cycle, including transport, can bring mass-production transfer-line economies into discrete manufacturing operations that have traditionally been handled by job shops. Most of the computer-managed systems include a conveyor on which the fixtured parts move to machining stations that have their own complements of cutting tools (anywhere from 10 to 150) somehow arranged into tool banks for automatic insertion into the machines. One Japanese system takes a variety of bar stock as input, machines it, heat-treats it, and grinds it to produce a number of different parts. Another Japanese company has been quite successful in using a group of eight computer-managed lathes to produce parts for stepping motors (rotational parts, housing, cages, etc.) in batches of 30 to 50 per run. This system even uses a robot to put the parts into the machines precisely. These systems often are designed to run wholly unassisted for long periods. In fact, West Germany's Heidelberg Press Co., the world's largest printing press manufacturer, runs its computer-managed system for five days, twenty-four hours a day. The remaining two days are used to prepare for the next week's production.

Note that most of the examples mentioned here are from out of the United States. Computer-managed machining has not really progressed that far in this country. The MIT program is attempting to produce cost-benefit analyses to determine the cost sensitivity of the system inputs, and simulate actual systems so that cost-effective computer-managed systems could be designed rapidly from manufacturing requirements.

Inverse seniority

a layoff can be a good thing

In a cyclical economy, layoffs are inevitable. Here in the United States, unions and management have generally agreed that when layoffs are necessary, workers with seniority will stay on the job and the most recently hired will be out of work. Sometimes, however, as in the automotive industry, laid-off workers receive a very high proportion of their normal salaries (up to 95%). This trend is spreading, and these high benefits are producing a natural reaction in the senior workers—"Why can't *we* get this pay for no work?" At the same time, the low-seniority workers laid off tend to consist largely of minorities and women who have just recently entered the work force and are usually the people who most need the assurance of a steady job.

Inverse seniority reverses this situation, giving the senior workers a well-deserved (and compensated) vacation, while keeping the junior workers on the job. To be workable and equitable, the concept requires that the option for layoff be voluntary with the senior worker, with a right to recall at his or her option, and that there be a reasonable fund giving compensation for the laid-off workers.

Such a system has benefits to both the workers directly affected and society as a whole. For the workers, senior people have the opportunity for longer periods of time away from the job—time for education, travel, fixing up the house, or even trying out new careers, knowing their old jobs are protected. The junior people stay on the job, maintaining a steady income and increasing their job skills. Society benefits because junior workers are kept from being continually laid off after working only a few months and eventually winding up in the welfare system. The senior worker, though, when laid off from a job he is assured of returning to, imposes little or no burden on society.

There has been little experimentation with inverse seniority in the United States, although the basic idea has been used at such companies as International Harvester and John Deere. The Japanese, however, have successfully followed a similar approach for a long time.

What is RCA's connection with MIT?

The worlds of academia and industry are indeed often worlds apart. In an attempt to bring them closer together, MIT established its Industrial Liaison Program, which sets up contacts between MIT scientists and engineers and their counterparts at RCA and a number of other corporations. The MIT-RCA Research Review Conference described here is only one part of this liaison program—RCA engineers also have access to reports from all of MIT's 2000 research projects. For information on how to obtain research reports or more about the subjects covered here, get in touch with **Doris Hutchison,** RCA contact for the Industrial Liaison Program, **Building 204-2, Cherry Hill, N.J., extension PY-5412.**

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Meet your Editorial Representatives

You, as an engineer, have valuable information in your files or in your head. Editorial contacts at your location are available to help you share that information with the rest of the engineering community.

These Editorial Representatives (Ed Reps) can help you present that pet project or idea to a very important group—engineers and engineering management at RCA. Editorial Representatives (for each major activity) are appointed, usually by the chief engineer. Basically, their objectives are to assist authors by stimulating, planning, and coordinating appropriate papers for the *RCA Engineer* and to keep the editors informed of new developments. In addition, they inform the editors of professional activities, awards, publications, and promotions. Somewhere on these two pages, you will find a picture of your Ed Rep and his or her location and phone number. Use the contact to find out more on developing your own contribution to the professional literature.

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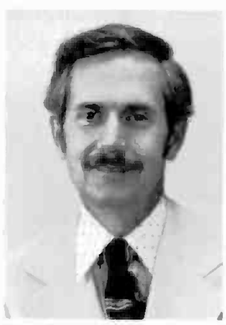

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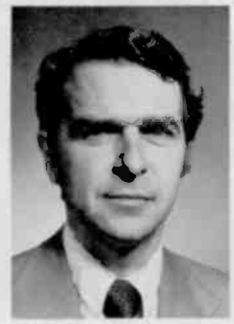

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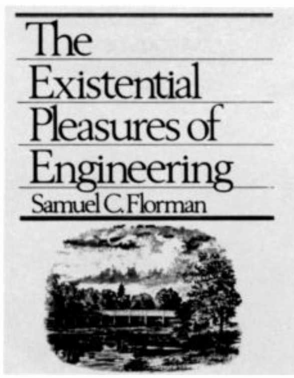
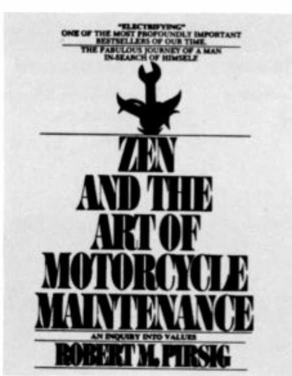
Zen, existentialism, and engineering

H. Kleinberg

The public's lack of understanding of the engineer's work is slowly turning to suspicion and hostility. This growing barrier makes two books "must" reading for engineers.



The Existential Pleasures of Engineering,
by Samuel C. Florman
160 pp. New York
St. Martins Press, $7.95.



Zen and the Art of Motorcycle Maintenance
by Robert M. Pirsig
406 pp. New York
Bantam Books, $2.50.

Strange titles. They seem more satirical than serious, promise to link topics that have nothing obvious in common, and they certainly don't sound like the names of technical books. In the narrowest sense they aren't technical, yet both books have direct and immediate relevance to every engineer.

They are thoroughly serious and deliver exactly what the titles promise, a strong connection between their seemingly unrelated components. And, while they are poles apart in style and approach, both books deal with the same subject—technology, or more precisely, a response to the strong anti-technology mood that pervades the atmosphere today.

The barriers that always exist between the specialist and the public have become increasingly more impenetrable in the past few decades. The natural lack of general understanding of what goes on behind that barrier is slowly becoming suspicion and hostility. It has become vital that the nature of technology and those who practice it be understood by the layman, so these books are especially timely. It is even more to the credit of the authors that they are neither defensively apologetic nor simply satisfied with platitudes about the contribution of technology to the good of mankind. Instead, they actively press the case that engineering and technical work are vigorous expressions of the highest human goals and aspirations.

Despite the common theme, the differences between the two books cover the entire range of writing. Florman, a civil engineer, wrote *Existential* as a direct exposition of the problem—a clear statement of the anti-technology ideas and a point-by-point response; Pirsig, a technical writer, wrote *Zen* as a novel centered around a motorcycle trip, with his thoughts about technology delivered as a series of Chautauquas* composed by the narrator as he and his young son travel. Florman deals primarily with engineering, with the reduction of scientific principles to practical ends; Pirsig treats technology from the angle of peoples' relationship to "things," using as his specific case the problems of fixing a motorcyle. Florman builds his position through copious references from his obviously wide reading on the subject; Pirsig reviews the entire history of Western philosophy and a bit of the Oriental as background to his conclusions. Florman attempts to build a philosophy of engineering that will refute the ideas of the other side; Pirsig undertakes the greatly more ambitious task of showing that both sides can be unified, can be looked at as two different manifestations of the essence of all experience—what he calles Quality.

Of the two, Florman's book is the more easily readable, and if you feel up to tackling only one of them, this should be it. *Zen* is a much more comprehensive treatment of the

*For those of you who are part of the postwar baby boom, a word about Chautauquas is in order. They were cultural and educational programs named after the resort area in New York State where they started, and date back to the days, a century ago, when it was believed that even vacation time should be partly spent in improving one's mind. To that end, series of informative lectures, often held in tents, were organized to bring enlightenment to small towns and outlying areas. While the original resort is still functioning in good health, the touring lecture series have gradually faded with the advent of radio and television, although they have apparently not yet completely died out.

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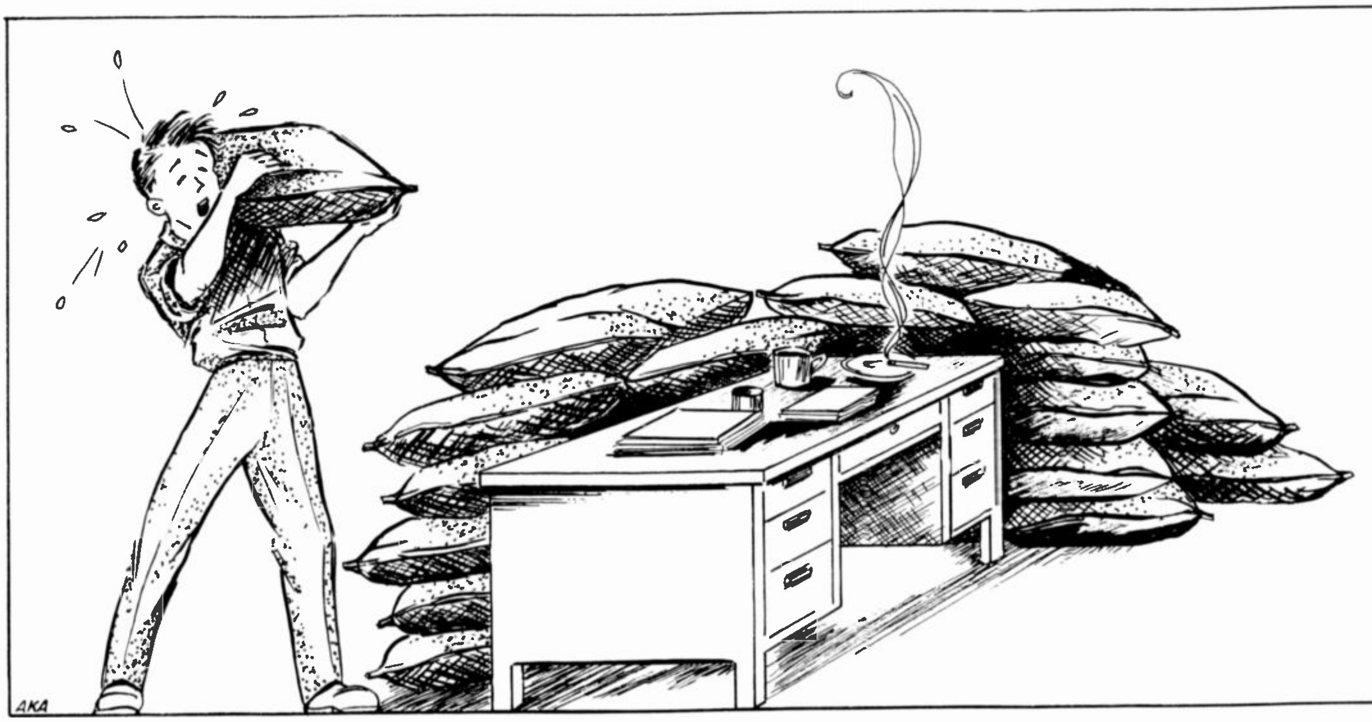

"... **while it would be premature** to pile sandbags around your desk, ... your work as an engineer is under attack."

subject, ranging widely over the history of philosophy and its interaction with the development of science. Judging from my own very limited knowledge of the subject, Pirsig's presentation of the classical ideas is remarkably concise and accurate. His own conclusions are simply that ... his own conclusions, and you may or may not agree with them. Nor are the books's merits as a novel of concern here, except to comment that despite a happy ending, it has the downbeat, slightly depressing mood so characteristic of today's fiction.

But one or both of these books should be required reading for every engineer because, while it would be premature to pile sandbags around your desk or to put bullet-proof glass around your lab bench, it is not too early to recognize the theme of these books—that your work as an engineer is under attack.

The opposition comes not merely from the confused flower children of the 1960s or a small band of extremists of the 1970s; it comes instead from the elite of today's intellectual leadership. If you are even a casual observer of current cultural trends you have probably picked up the message already. It comes through in today's movies, novels, and theater, in the explosion of interest in the mystical and the occult, in the recurrent theme of "dropping out of the system."

Both authors point out that what is under fire here is not merely nuclear energy or computers or supersonic aircraft or any other specific technology. What is being questioned is best expressed in the authors' words:

"An even more serious indictment of engineering is to be found in a curious new philosophy that has been gaining currency since the mid-1960s. It is the doctrine that holds technology to be *the root of all evil*. The proponents of this view are not satisfied to say that technologists have been careless, foolish, or immoral. They see the source of society's problems and men's miseries as lying in the concept of technology itself."

Florman, p. 45

"But now I see that the it was mainly, if not entirely, technology. But, that doesn't sound right either. The 'it' is a kind of force that gives rise to technology, something undefined, but inhuman, mechanical, lifeless, a blind monster, a death force. Something hideous they are running from but know they can never escape."

Pirsig, p. 46

"The founding father of the contemporary anti-technological movement is Jacques Ellul, a theological philospher...(whose) thesis is that technique has run amok, has become a Frankenstein monster than cannot be controlled. By technique he means not just the use of machines, but all deliberate and rational behavior, all efficiency and organization."

Florman, p. 46

It takes a while for an engineer to believe what he is hearing. How can anyone question something so obviously valid as the scientific system? And even when you come to accept the fact that such an idea can be seriously considered by any modern thinker, your first reaction is to point out how much our society depends on technology. The authors are ready with answers.

"There's kind of a glaring inconsistency here, that's almost too obvious to dwell on. If they can't stand physical discomfort and they can't stand technology, they've got a little compromising to do. They depend on technology and condemn it at at the same time. I'm sure they know that and that just contributes to their dislike of the whole situation."

Pirsig, p. 44

"If we are to build a new philosophy of engineering, we must start with a rebuttal of anti-technology. Conceivably we could let the argument go unanswered, except to respond that technology is a necessary evil. But that would not be very satisfying. Besides, it would not give expression to what we know in our hearts; that technology is not evil except when falsely described by dyspeptic philosophers."

Florman, p. 57

If you want a more specific example of the attitudes that the authors are responding to, go see the movie "Logan's Run." It is set in some unidentified future, in an enclosed city in which every human need is catered to by hidden, totally self-contained machinery. The population live their entire lives with no need to do anything but enjoy themselves. The only catch in this Utopia is the system used to control the size of the population—destruction of everyone at age 30. A couple escape from the city, discover the natural world outside, and like what they see. They return to the artificial city and, after performing the mandatory deeds of strength, endurance, and heroism, destroy the machinery. The film closes with what is apparently considered a happy ending as the populace emerges from the ruined prison of technology to live freely ever after in harmony with a benevolent nature.

Without doubt, every engineer who sees the movie will immediately wonder how such a group of totally unskilled and helpless people will cope with what is, in reality, a not very benevolent nature. How will they feed and shelter themselves? How will they deal with such natural phenomena as bacteria and viruses? If any of them survive the first winter, how will they then feel about technology? The questions seem obvious, but not to the film-makers who see life neatly divided into two categories—the oppressive world of machine and logic on the one hand, and the liberating world of nature and feelings on the other.

Both authors attack what they consider the basic fallacy of this negative view—the position that technology is essentially dehumanizing, not only to its helpless victims (the general public), but also to its practitioners (that's you). They respond that technology is not something that has been artificially or subversively grafted onto an otherwise innocent and passive mankind, but instead reflects a fundamental human drive. Designing a tool is as uniquely human an act as writing a poem, because humanity is differentiated from other species as much by its hand as by its brain. Using one is no less creative than using the other, and using both together represents the very best of the human mind and spirit. Far from being dehumanizing, science and technology and working with material things are rewarding and satisfying at a deep emotional level.

Harry Kleinberg is, by nights, the author of *How You Can Learn to Live with Computers*, published by Lippincott this fall. Weekdays, from eight to five, he is Manager of Corporate Standards Engineering in Cherry Hill, N.J.

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In the course of reaching his conclusions, Florman, for all his defense of engineers, gives us hell for refusing to admit that we find our work satisfying, and sometimes even fun. Pirsig makes his essential point that much of the peace of mind so sought after by the mystics can be found in doing good and careful work on something as mundane as an old motorcycle. It would be unfair to more fully summarize their conclusions without adequately developing their reasoning. Such a summary would sound maudlin and, taken out of context, would inevitably collide with the stubborn unwillingness of engineers to think about such "emotional" matters. I would suggest that you read one or both of these books to see whether they express something that you have always known, but have never thought much about.

Ed Note: Is the anti-techology attitude as pervasive as these authors indicate? Has it affected you, your work, or your social life? We'd be interested in hearing readers' views on this problem, which affects us all as engineers. Address correspondence to Editor, *RCA Engineer*, Bldg. 204-2, Cherry Hill, N.J. 08101.

Current modulation of laser diodes gives direct fiber-optic baseband tv

Standard methods for modulating laser diodes are not suitable for the low-frequency requirements of baseband tv. This method provides an economical means of putting closed-circuit tv on a fiber-optic link.

D.R. Patterson

Many wideband fiber-optic communication systems employing laser diodes as light sources use conventional constant-current power supplies. In these systems, a coupling capacitor supplies the ac modulation to the diode and an rf choke arrangement provides power-supply isolation (Fig. 1). This method of modulation has been useful for a wide variety of applications, including flying-spot scanners, document readers, and fiber-optic transmission of wideband rf-type carriers such as the vhf television spectrum from approximately 50 MHz to over 200 MHz.

There are applications, however, that may require the high power density and narrow beamwidth of laser diodes, but do not fully use the wide bandwidth capabilities of the diodes. These applications include baseband television (the 30-Hz to 4.5-MHz signal from a closed-circuit tv camera, video tape recorder, etc.) and its associated pulse distribution, audio, low-frequency facsimile, and digital and remote-control transmissions in optical cables. Here bandwidth requirements are of the order of 10 Hz to 8 MHz. The above-mentioned rf coupling capacitor and choke arrangement are not suitable at these low frequencies.

RCA Laboratories has designed a modulator that allows the necessary low-frequency modulation of the laser diode in a manner that retains the constant-current nature of the basic bias supply. This method allows the low-frequency signal to be transmitted directly without first putting it in the form of an rf carrier before modulating the laser diode.

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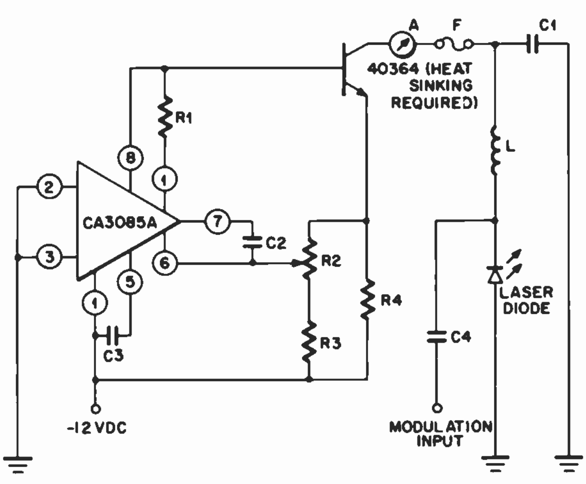

Fig. 1
Laser modulation in typical system is coupled in through capacitor C4, with rf-choke isolation from the power supply. Method shown here, which is for the RCA C30125 cw injection laser system, is not suitable for low-frequency (and thus baseband tv) applications.

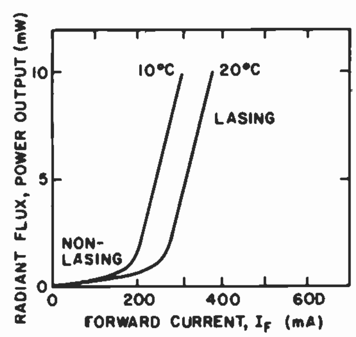

Fig. 2
Transfer curve for typical laser diode (RCA C30127) is steep, requiring a stable power supply; and temperature-sensitive, requiring a feedback cooling system.

Laser device characteristics

Fig. 2 shows a typical transfer curve (optical power output vs. operating current) for an RCA C30127 laser diode as a function of temperature. Two features of the figure are important from a design consideration: 1) above a threshold point, typically 300 mA, the slope of the transfer curve is steep, requiring good power-supply stability; and 2) the operating threshold point is temperature-sensitive.

To stabilize the operating temperature, a small thermoelectric cooler module has been incorporated in a feedback system using a temperature-sensing thermistor located in the base of the laser-diode heat sink. This temperature stabilization system[1] maintains the laser operating temperature to within a few tenths of a degree C.

Constant-current modulator

Fig. 3 shows a conventional current-feedback operational amplifier circuit with an added modulation source, V_{mod}, in series with the reference supply, V_{ref}. Using the concept of virtual grounds at the input of the amplifier, the load current, I_L is given by the expression

$$I_L = (E_r + V_{mod}) / R_s$$

where E_r is an adjustable dc bias voltage (operating or Q point), V_{mod} is the ac modulation voltage, and R_s is the value of a current-sampling resistor.[2] The graph in the upper corner of Fig. 3 shows the constant-current nature of the output for varying load lines.

System design considerations

From a practical standpoint, a number of areas must be considered in designing a suitable modulator power-supply system. The steepness of the transfer curve requires components with good temperature stability to minimize thermal drifts associated with the operating-point bias. Dissipation overrating on the pass devices and current-sampling components is therefore necessary.

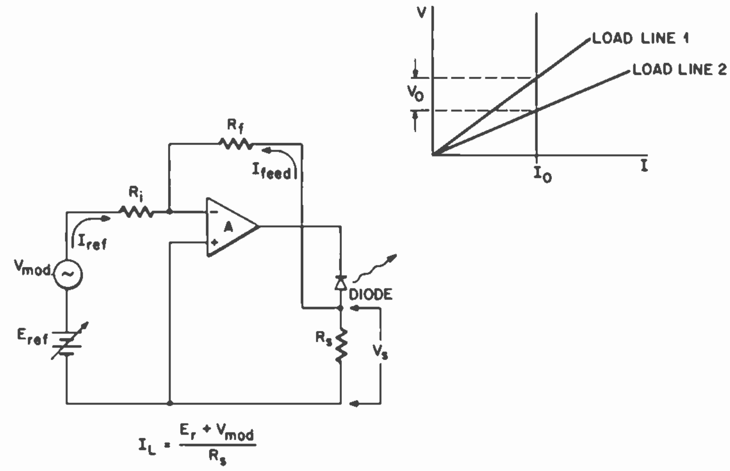

Fig. 3
Constant-current output (right) is a result of op-amp circuit in current-feedback configuration.

Transients are probably the most notorious sources of failures of solid-state laser diodes. These include power-supply turn-on and turn-off transients, in addition to transients supplied by external modulating sources. Cost considerations are likewise important in the design of a suitable commercial system.

The modulator shown in Fig. 4 was constructed with the above design considerations in mind. The CA3085A voltage regulator integrated circuit was found to perform the desired modulation at modest cost, compared to other wideband operational amplifiers, with only a minor change in circuit configuration. A modulation input amplifier and a voltage pre-regulator with current limiting were provided to complete the modulator. To meet present laser-diode operating-current ranges, the modulator has an adjustable operating-point bias range of 120-350 mA and an adjustable modulation capability of 90 mA peak-to-peak.

The circled numbers in Fig. 4 refer to the waveforms shown in Fig. 5. The effects of

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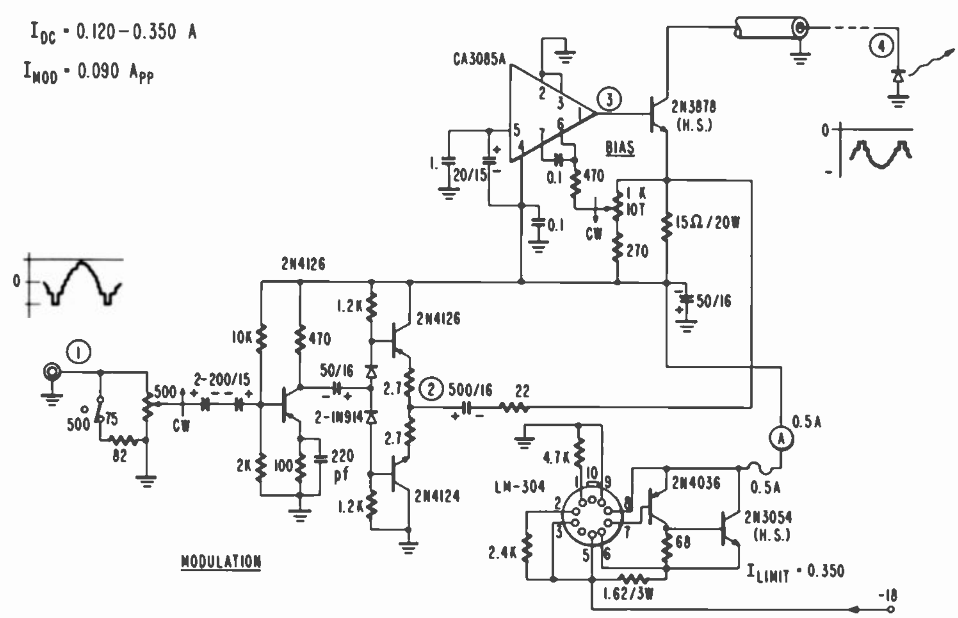


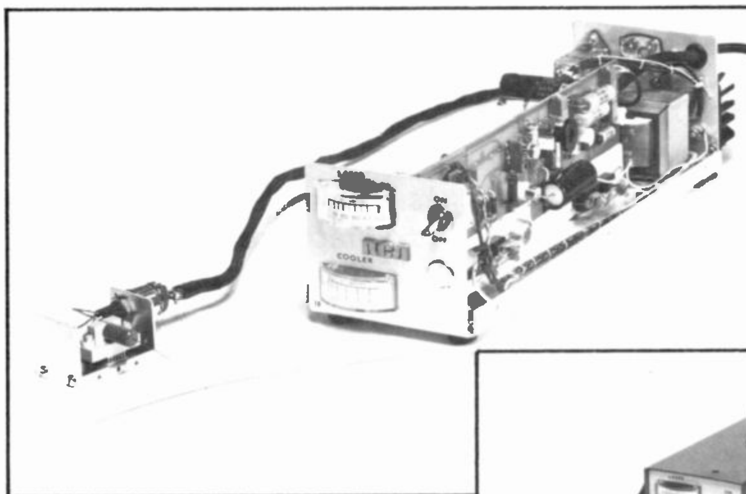
Fig. 4
Modulator circuit uses CA3085A voltage-regulator IC, modulation-input amplifier, and pre-regulator with current limiting. Operating point and modulation capability are adjustable.

feedback on the bandwidth of the system can be noted by comparing the input video sweep signals (10 MHz at a 60-Hz rate) with the voltage drive to the pass transistor and the final constant-current output signal. As the high-frequency information becomes attenuated by the circuit effects, the negative feedback compensates by allowing the gain for the high-frequency information to increase.

The complete unit consists of two pieces. The laser diode, thermoelectric cooler, and thermistor are in one detachable package, and a common power supply, the temperature control, and modulating circuitry are in the second. Fig. 6 shows the finished system with "pig-tailed" optical fiber attached to the removable laser-diode assembly.

Conclusion

A semiconductor laser modulator allows low-frequency (10 Hz to 8 MHz) signals to be inserted within the feedback loop of a conventional constant-current power supply, thereby providing low-frequency capabilities to the present laser power-supply system. The system allows direct modulation of baseband television signals, and an associated audio subcarrier could easily be added.



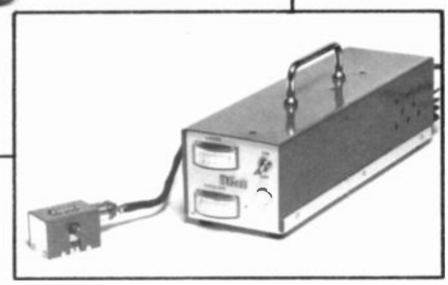


Fig. 6
Finished system with and without covers. Power supply, temperature control, and modulating circuitry are in unit at right; laser diode, thermoelectric cooler, thermistor, and coupling to optical fiber are in unit at left.

Acknowledgments

The laser diodes were fabricated under the direction of Ivan Ladany. The demonstrator unit pictured in Fig. 6 uses a laser diode package developed by James Wittke; it incorporates an optical fiber coupled to the diode mount.

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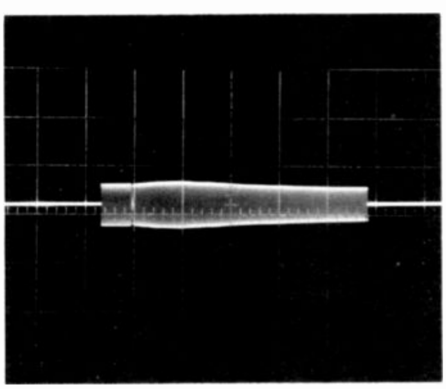
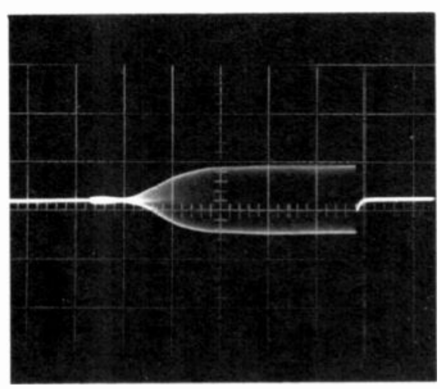
1. Wittke, J.P., Patterson, D.R.; and Ladany, I.; "Stabilization of cw injection lasers," RCA Technical Note TN 1005 or Data Sheet RCA Developmental Laser Types C30127.

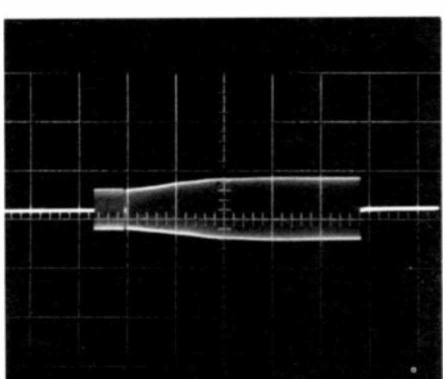
2. See for example, Millman, J. and Tabu, H.; *Pulse, Digital and Switching Waveforms*, New York, McGraw-Hill, Sections 1-8 and 1-9.



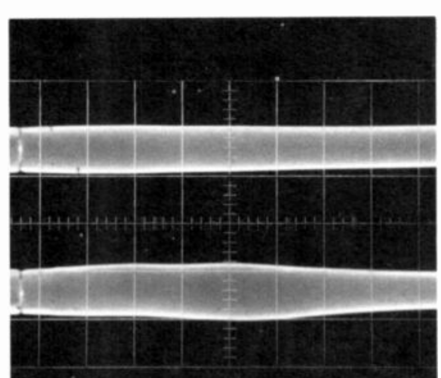
(1) Video input signal
10-MHz sweep
1 V/vertical division



(3) CA3085 IC output
10-MHz sweep
0.1 V/vertical division



(2) Amplifier output
10-MHz sweep
0.5 V/vertical division



(4) Top:
Video sweep input
10-MHz sweep
1 V/vertical division

Bottom:
Output current
10-MHz sweep
20 mA/vertical division

Fig. 5
Waveforms from circuit of Fig. 4 show the effect of feedback on system bandwidth. As the high-frequency information becomes attenuated, feedback has high-frequency gain increase.

The tokamak approach to controlled thermonuclear fusion

H. W. Hendel

As a power source, fusion has a number of potential advantages over fission. Fusion power has yet to be shown as feasible, but second-generation devices now under development should approach the power break-even point.

Power generation by controlled fusion holds the promise of unlimited, inexpensive fuel, and greater safety and negligible environmental hazard relative to fission reactors. Fusion has thus become one of the preferred approaches to solving the world's long-term energy problems, although its feasibility must still be demonstrated. Research towards producing fusion power based on synthesizing the heavy hydrogen isotopes deuterium and tritium into helium has progressed, despite many difficulties, to the point where reaction rates similar to those required for fusion reactors now appear to be within immediate reach. Following up on these recent achievements, next-generation fusion devices are being developed, some of which are designed to generate about 10 MW of fusion power (without conversion to electricity), comparable to the heating-power input, to demonstrate power break-even and scientific feasibility.

The Princeton University Plasma Physics Laboratory (PPPL), under contract to the U.S. Energy Research and Development Administration, has pioneered the development of fusion, with RCA one of its original industrial contractors in the early 1960s. PPPL's Tokamak Fusion Test Reactor (TFTR), now under construction and planned for operation in 1981, is expected to be the first fusion device to operate at reactor-like power densities. It will burn deuterium and tritium, the reference cycle for fusion-power reactors, with the highest reaction cross-section at conditons attainable now. Experimental power reactors are expected to be in operation and producing many tens of megawatts of electricity in about 1985.

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Theory behind the fusion reaction

Energy is liberated in fusion reactions because the binding energy per nucleus for the lightest elements is less than that for those with intermediate mass numbers. Thus, the sum of the masses of the initial, heavy-hydrogen isotopes is greater than the mass of the final reaction products (helium and neutrons), and the excess mass is converted to energy. However, fusion reactions do not occur spontaneously at room temperature. The reacting nuclei are positively charged, and the long-range Coulomb repulsion must be overcome before the short-range nuclear forces can give rise to fusion: the relative kinetic energy of the reacting nuclei must be raised either by acceleration (to $\geqslant$ 10 keV) or by temperature increase (to $\geqslant$ 100 million °C). At this temperature, the fusing isotopes will exist as a fully-ionized net-charge-neutralized ensemble of ions and electrons—a plasma.

Thermonuclear fusion, recognized in the 1930s as the stellar energy source (and thus the origin of solar and, indirectly, fossil power), was applied (uncontrolled) for the first time on earth in the (heavy-) hydrogen or fusion bomb. The large amount of energy released and the unlimited availability of deuterium fuel (tritium is not naturally abundant) in the oceans made controlled fusion-power reactors highly attractive. Each fusion reaction liberates about 20 MeV; the nuclear energy in the deuterium contained in one gallon of water is equivalent to the chemical energy in 300 gallons of gasoline, and the cost of this amount of deuterium is a few cents.

Practical problems and solutions

However, some of the scientific and engineering aspects of fusion reactors were immediately recognized as awesome. For prolific fusion of heavy hydrogen, a temperature of 10^8 °C, much higher than

Table I
Three fusion reactions are now used or projected for use in the next generation of fusion devices—deuteron-deuteron, deuteron-tritum, and deuteron-^{3}He.

d-d →	^{3}He 0.82 MeV	+ n 2.45	First reaction used. d-supply unlimited.
d-d →	t 1.01 MeV	+ H 3.02 MeV	
d-t →	^{4}He 3.5 MeV	+ n + 14.1 MeV	Highest cross-section for present conditions. t is β-radioactive and so has handling difficulties.
d-^{3}He →	^{4}He 3.6 MeV	+ H 14.7 MeV	No neutrons, only charged particles generated. Low cross section at low temperature.

ever previously achieved, must be attained. Thus, with the heat input per nucleus ~ 10 keV, close to one percent of the nuclei in the host plasma must be fused to produce the desired large power multiplication. This corresponds to a long, never-before-reached or even-considered particle confinement time of about one second. The hot plasma must be kept from interacting with the walls of its container, which acts as a heat and particle sink and a source of impurities; in addition, fuel must be replenished and burned-out reaction products must be removed.

One solution to the wall-interaction problem was the "Stellarator." A toroidal (doughnut-shaped) magnetic-confinement plasma device, it was proposed by L. Spitzer in 1951 at Princeton's Astrophysics Department. In the Stellarator, particle motion toward the wall is reduced by a confining magnetic field, directed parallel to the walls, so that the charged particles spiral around the field lines and move parallel to them, but do not connect with the walls easily. Today the tokamak, a Russian version of the toroidal device, has become the major approach, worldwide, to magnetic-confinement fusion and to fusion reactors in general. In tokamaks, plasma temperatures of 10^7 °C and (slowly) fusing plasmas are now produced routinely. This article concentrates on toroidal magnetic-confinement fusion as pursued at the Princeton University Plasma Physics Lab; similar work is carried on at Oak Ridge National Lab, Gulf-Atomic, MIT, and in Europe, Japan, and, with the biggest effort, the USSR.

Reaction characteristics and requirements

All fusion reactions are not created equal.

The characteristics of the fusion reaction chosen determine plasma properties and the device parameters necessary to attain an acceptable fusion reaction rate, the radiation effects, and the effects of the products on the device and its surroundings. The strength of the Coulomb barrier increases with the number of protons in the nucleus, so that the isotopes of hydrogen, having only one proton, have the highest cross-section. For low plasma temperatures, the cross-section rises rapidly with temperature, resulting in sufficiently high reaction rates at ~10 keV. Three reactions are now used or projected for use in the next generation of fusion devices: d-d, d-t, and d-^{3}He. See Table I for details.

Note, however, that even for carefully selected conditions, it may not be possible to favor one reaction and suppress others completely. In d-plasmas, about 50% of all reactions produce tritium, which in turn gives rise to d-t reactions; likewise, in a d-^{3}He mixture, d-d reactions producing neutrons will occur. The fusion power generated supplies both the useful power output and the plasma heating necessary for an ignited reactor to compensate heat losses. As a rule, fusion-reactor plasmas are transparent to neutrons, so the neutron energy must be absorbed outside the plasma and converted into heat. A major fraction of the charged fusion-reaction products is lost (at full energy) from currently available small plasmas, but large, ignited plasmas are expected to receive all heat-input from energetic charged particles. Charged fusion-reaction products must therefore be sufficiently confined so that most of their energy is dissipated into the plasma and the ignited plasma keeps burning without auxiliary heating.

What are the plasma conditions required for breakeven?

The plasma conditions required for a fusion reactor were derived by Lawson in 1959 from power-balance considerations. The fuel must be confined, at approximately the ignition temperature, for a sufficient time τ to generate energy beyond that invested to heat the fuel. Thus, at low density, the confinement time must be long; at high density, the reaction rate ($\sim n^2$ where n is plasma density) is high and confinement time can be short. Lawson's criterion can be expressed in terms of $n\tau$, with an $n\tau > 10^{14}$ s/cm^3 indicating reactor conditions for d-t plasmas. Table II lists approximate reactor conditions and current progress towards these goals.

Table II
Three conditions must be met to achieve a positive power balance in a fusion reactor. Table shows where tokamak-type fusion development stands today.

Condition	*Necessary value*	*Now attained in tokamaks*
temperature	$\geqslant 10^8$°C $\cong$ 10 keV	~ 1.5 keV
density	$\geqslant 10^{14}$ cm^{-3}	$> 10^{14}$ cm^{-3}
confinement time	$\geqslant$ 1 s	~0.1 s

Hans Herdel has been RCA's consultant to Princeton Plasma Physics Laboratory since 1965. He pioneered in collisional drift (or universal) instabilities, their discovery, identification, mode stabilization, and evolution to turbulence; drift-wave-caused diffusion; feedback stabilization of instabilities; anomalous rf-absorption caused by parametric instabilities; and current-driven instabilities in isothermal plasmas.

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The implication of the one-second confinement time in Table II may be appreciated better by expressing it differently—the equivalent mean free path of the ions before fusing is comparable to a trip around the earth. Since the fusion reactor is necessarily limited in size, the confinement of the plasma away from the walls is one of the major problems in fusion research. Moreover, the wall is not only a sink of particles and energy, but it may also become a source of impurity atoms that will be ionized and will cool the plasma by radiation.

The Coulomb-collison cross section is generally a few orders of magnitude larger than the fusion cross section at the relevant conditions. Confinement of the hot plasma might be expected to improve as temperature is increased, because of the reduction of the Coulomb-collision cross-section, q. With increased particle energy, $q \sim 1/E^2$, which results in negligible binary-collision diffusion for fusion plasmas. However, the main contribution to losses from confinement is often caused by plasma instabilities; electric-field fluctuations, by interacting with the charged particles in the presence of the confining magnetic field, can transport plasma to the wall much faster than particle-particle collisions. Wave-particle effects also loom large because of the multitude of instabilities that may be present in plasmas.

A confined plasma is generally not in stable equilibrium; fluctuations and waves may be generated by perturbations from the equilibrium. In addition to unstable modes similar to those occurring in non-ionized gases and fluids, charge separation in plasmas may be restored by electrostatic forces, and displacement of the plasma may be counteracted by magnetic forces; additional eigenfrequencies and modes are related to the confining magnetic field. More than one hundred instabilities have been catalogued. In terms of the reservoirs of free energy available, instabilities can derive their energy from: 1) expansion energy; 2) directed kinetic energy of ions or electrons; 3) magnetic energy; and 4) deviations from the Maxwellian energy distribution. The effects of wave-particle interactions may produce an anomalous "effective" collision frequency, which in turn may generate undesirable (enhanced particle and heat losses) and desirable effects (anomalous resistivity and heating).

The tokamak

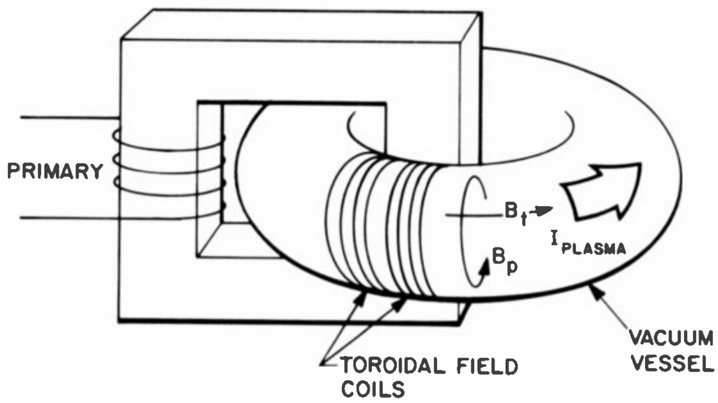
The tokamak, the Russian counterpart of the Stellarator, consists of a toroidal vacuum chamber and a toroidal ~ 5-T magnetic field (1 T (Tesla) = 10^4 gauss) generated by external coils. A transformer induces a current in the plasma contained in the vacuum vessel, so that the plasma doughnut becomes the secondary winding, Fig. 1. The (toroidal) plasma current (~ 10^6 amp) heats the plasma by electron-ion collisions, i.e., resistive, Ohmic dissipation. Moreover, this current also generates a poloidal magnetic field (~ 0.5 T), which, when superposed on the main toroidal field, forms helical field lines and improves plasma equilibrium. A third magnetic field, the vertical field, ~0.1 T, interacts with the plasma current to provide equilibrium by counteracting the major-radius expansion (which occurs in the absence of a poloidal field based on external conductors), and allows the plasma to be positioned inside the vacuum vessel, relative to the major radius, R.

The combination of magnetic fields produces particle orbits having banana-shaped projections.

The strength of the toroidal magnetic field increases towards the center of the torus, $B_t \sim 1/R$. Together with the helical field, this leads to a particle-transport mechanism not present in linear geometry. As a particle moves along a helical field line, starting on the outside of the torus, it spirals towards the inside, i.e., smaller R, where the magnetic field is stronger. The particle may then be magnetic-mirror reflected because of the tendency of strong-field regions to expel a fraction of the incoming charged particles. At the low collision frequencies of fusion plasmas, a small fraction of the particles will be trapped between such magnetic-field mirrors. The projection of the particle orbits into a poloidal cross section is banana-shaped (also shown Fig. 1); hence this type of diffusion is called *banana*, or neoclassical, transport. Expressing the diffusion coefficient as the square of the mean step size times the collision frequency, the step size (banana-width) is determined by the poloidal Larmor radius. Thus, neoclassical diffusion due to the poloidal ion Larmor radius is about two orders of magnitude larger than "classical" diffusion due to the toroidal-field Larmor radius.

High plasma temperatures require special heating methods.

As the plasma temperature increases, Ohmic heating becomes less effective, at about 1 to 3 keV temperature. Different heating methods are necessary for reaching higher plasma temperatures. The most promising and best developed supplementary heating method, beyond Ohmic heating, is neutral beam injection. (Ion beams cannot be used, since ions that penetrate into the magnetic field will also leave the confinement immediately.) Intense beams of energetic atoms (four to six 65-amp beams at 120 keV for the TFTR) are generated by charge-exchanging ion beams; the fast-atom beams penetrate into the plasma until they are ionized, and the beam velocity determines the penetration depth. The energetic ions thus created inside the plasma remain confined, transferring their excess energy to the plasma. Experiments in earlier tokamaks



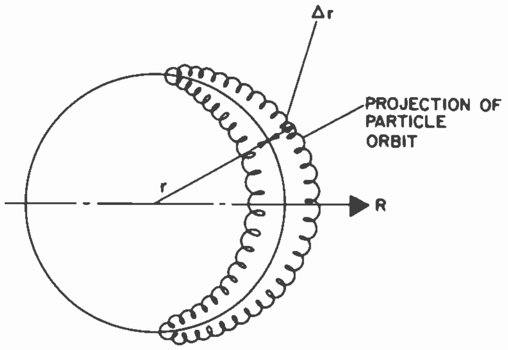


Fig. 1
Doughnut-shaped tokamak uses external coils to generate a strong toroidal magnetic field. The transformer-induced plasma current produces a weaker poloidal magnetic field, and the two combine to form helical field lines. (A third weaker field, the vertical field, if not shown here.)

Banana-shaped particle path results when particle orbit is projected onto poloidal cross section of torus. See text for explanation.

indicated efficient energy transfer of the neutral-beam power to the plasma.

Another heating method is adiabatic compression of the plasma by increasing the magnetic field strength, which was used during earlier experiments at PPPL and found to increase plasma temperature and density as predicted. A third method for auxiliary heating, not yet well documented in larger tokamaks, is rf heating. Generally, the heating frequency is chosen at or near one of the resonances of the plasma, the ion cyclotron and magnetosonic frequencies ($f \sim 50$ MHz), the lower hybrid frequency (~ 1 GHz), and the electron cyclotron and upper hybrid frequencies (~ 100 GHz). RF heating's principal problem is expected to be in operating the power-coupling structures in the hostile vicinity of the fusion plasma, where electrical breakdown may be facilitated by the presence of ions and electrons from the plasma and of secondaries from the nuclear radiation.

The two-component tokamak has some excellent advantages, but one major disadvantage.

Most previous plasma experiments and reactor designs were based on plasmas with Maxwellian energy distribution. The availability of intense, high-energy neutral beams and Ohmically heated tokamak plasmas slightly below the ignition temperature led to the proposal in 1971 at PPPL of a scheme that allows "break-even" attainment under less demanding plasma temperature conditions. In the two-(energy-) component tokamak (TCT), neutral-beam injection of deuterium can be used to generate a high-energy deuterium component, which interacts with the bulk plasma at the higher (nuclear) cross-section of the energetic beam. This increases the reaction rate by an order of magnitude over the Maxwellian-distribution reaction rate of a similar deuterium plasma heated by a (nonfusing) hydrogen beam, as was experimentally shown at PPPL.

Thus, with the TCT method, the fusion power density generated is raised by an order of magnitude, and the $n\tau$ values required by the Lawson criterion to achieve power break-even in a Maxwellian plasma are lowered by an order of magnitude: both the objectionably low power density and the large size of (Maxwellian) magnetic-confinement fusion reactors might be improved. However, an inherent limitation of the TCT is its low power amplification, which is small (2 to 3) relative to the arbitrarily large amplification factors of ignited reactors. In any case, since neutral-beam injection is now the preferred heating method, the two-energy-component regime will have to be traversed and studied as a preliminary to ignition by beam injection.

Where do tokamaks fit into the overall fusion picture?

The tokamak is only one of a number of approaches toward producing controlled fusion power. Each method has its proponents who want it to get the research (and research dollars). Presently, though, tokamaks are more highly developed and appear to have the highest probability of achieving fusion power. RCA's only connection with the tokamak today is the author of this paper, Hans Hendel, who has been a consultant to the Princeton Plasma Physics Laboratory since 1968, through RCA Laboratories.

The major differences among the various approaches lie in their methods of confining the plasma. Stars use gravity, which is cheap and reliable by anybody's standards, but that only works because of the stars' huge masses. Tokamaks use magnetic fields to confine the plasma, but they are not alone in doing so—magnetic-mirror and "theta-pinch" reactors are two more. Laser fusion uses a form of inertial confinement in which very small fuel pellets are heated and compressed by very large laser pulses to produce the fusion "burn." The resulting explosions are thus small enough to be handled by relatively standard systems. After a late start relative to the magnetic-confinement approaches, laser fusion has made considerable progress, but has yet to be shown feasible.

If the nuclear particles chosen are "advanced" fuels, the fusion products will all be charged particles and there will be less neutron-induced structural damage, radioactivity, or environmental problems associated with the neutron flux of other fusion power plants. Another potential advantage with advanced fuel reactions is that, with them, it may be possible to convert the kinetic energy of the charged fusion products directly into electric energy and avoid the steam/turbine/generator system and its problems. Such a fusion system would have to be classified as a "dream" system, however, since it is far from realization.

Good descriptions and explanations of these other fusion programs can be found in "The prospect for fusion power," *Technology Review*, (Dec 76) and "The future with fusion power," *Mechanical Engineering* (Apr 77). For a discussion of fusion power that includes an analysis of its drawbacks (large size and cost, potential differences between the ideal cycles and what the fusion program is likely to deliver), see "Fusion research" in *Science* (Jun 25, Jul 2, and Aug 20, 1976).

—*W.D.L.*

Tokamak scaling looks good.

Another highly promising result of recent tokamak work is the observed scaling of the energy confinement, τ_E, with plasma density, n, and plasma minor radius, a, which indicates the potential for large improvements of the operating conditions. Combining measurements from a variety of tokamaks now in operation, one finds that observed energy confinement scales as na^2 (Fig. 2). The scaling with plasma minor radius is important, since future reactors will necessarily be larger than present devices. The plasma-density scaling

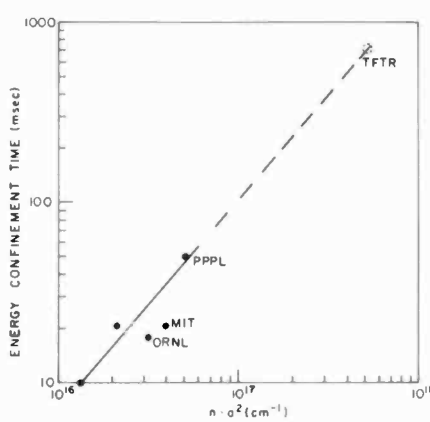


Fig. 2
Tokamaks show strong economy of scale— energy confinement time improves with na^2, the product of the plasma density and the square of the minor radius of the torus.

Table III
Toroidal confinement devices around the world. Experimental power reactors are planned for operation in about 1985.

Device	Location	Year	Major radius R (cm)	Minor radius a (cm)	Current J (10^6amp)	Magnetic field B (T)	Ion temperature T_i (keV)	Neutron density n (10^{14}cm^{-3})	Confinement time τ (s)	Confinement criterion $n\tau$ (s/cm^3)
C-Stellerator	Princeton	1965	100	5		3.5	.04	0.1	10^{-3}	10^{10}
PLT	Princeton	1977	130	45	0.6	4.0	1.0	1	<0.1	$<10^{13}$
TFTR	Princeton	1981	265	110	2.5	6.0	10.0	1	0.1	10^{13}
JT-60	Japan		300	100	3.3	5.0				
T-20	USSR		500	200	6.0	3.5				
JET	Europe		300	125/210 D-shaped	4.8	3.4				

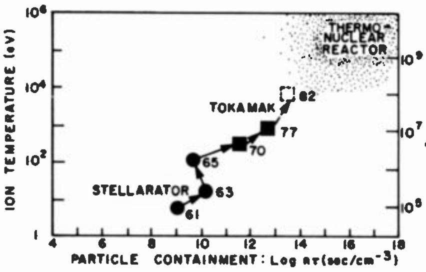


Fig. 3
Reactor conditions take place at log containment value of 14. Graph shows the extensive progress towards this goal that has been attained in a relatively short period of time.

observed is also highly advantageous (the Maxwellian fusion reaction rate is proportional to n^2) and different from classical transport phenomena, which would be expected to reduce τ_E with increasing n. The highest $n\tau$ values have been obtained in a high-magnetic-field tokamak at MIT, where high plasma density ($n=7\times10^{14}$ cm^{-3}) resulted in long energy-confinement times ($\sim10^{-1}$s) and $n\tau$ values well above 10^{13}s/cm^3. The effect of plasma-temperature increase on energy confinement remains to be determined. Fig. 3 and Table III show the progress of toroidal confinement devices toward the fusion goal.

Problems remaining

Assuming that reactor-size plasmas can be confined at sufficient density and temperature to produce large amounts of fusion power, additional obstacles will need to be overcome.

Neutron radiation will affect the lifetime of the tokamak's structural parts.

The first wall adjacent to the plasma, and the neutron absorbing blanket next to it, will be exposed to the full intensity of the unattenuated neutron flux. Radiation damage will severely limit the operating life-time of these structural elements because of helium generation from (n, α) reactions and atomic dislocations. The expected first-wall replacement every 3 to 5 years will substantially affect operation and cost.

There is still radioactive waste, although less than in fission reactors.

A comparison of the radioactive wastes generated in fusion, fission, and liquid-metal fast-breeder reactors indicates that fusion reactor wastes may be less than one-tenth that of fission reactors, and less than one-hundredth of fast breeders. The use of advanced fusion reactions, which produce mainly charged reaction products, and of carefully selected structural materials, may improve the outlook for fusion even more. Fusion waste products generally appear to have a much shorter half-life than fission waste.

Tokamaks are not inherently steady-state power producers.

In reactor design studies, transformer-driven discharges of about one hour are envisaged. The maximum pulse length is determined by the necessity to provide a continuous change of magnetic flux in the plasma to preserve equilibrium. During the current shut-down interval (~3 minutes), the electric output power would be supplied by stored heat. Fuel injection of 300 one-millimeter-diameter frozen fuel pellets per second at a velocity of 5×10^6 cm/s (10 to 100 MeV acceleration voltage) has been proposed in one design.

Impurities must somehow be removed from the plasma.

The prevention of impurity influx or, alternatively, the removal of impurities to maintain an acceptable impurity-ion level, may turn out to be one of the most severe obstacles to fusion. Magnetic "divertors" are planned for some next-generation devices to direct the impure plasma adjacent to the walls into special absorption chambers.

Cost estimates

The cost of electricity from fusion has been estimated to be comparable to that of present power costs. Since fusion fuel costs are negligible, anticipated future price increases of fossil and fission fuels, coming from resource depletion and processing cost escalation, will work in favor of fusion.

The outlook

TFTR will produce reactor-like conditions in the early 1980s; experimental reactors should produce electrical power after 1985.

To assure the operation of fusion-power demonstration reactors in the 1990s, a series of increasingly complex devices is planned, both in this country and abroad (see Fig. 4). The Tokamak Fusion Test Reactor at PPPL (Fig. 5), which is expected to generate about ten megawatts of fusion power under reactor-like conditions (without producing electricity), will represent an intermediate level between today's small, zero-power experiments and the experimental power reactors anticipated to produce electrical power and to demonstrate ignition after about 1985.

The industrial contractor supporting PPPL consists of a team of Ebasco and Grumman engineers. TFTR costs are estimated to be 225 million dollars and initial d-d operation is expected by 1981. The design-operation span is eight years, with

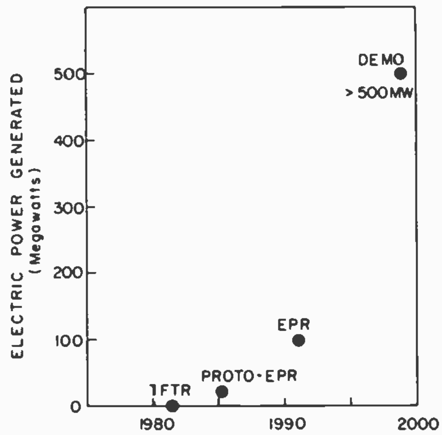


Fig. 4
Fusion power step by step. Tokamak Fusion Test Reactor is scheduled for operation at Princeton in the near future. Then come the prototype and actual experimental power plant in the later 1990s.

four years of tritium use. Early experiments in hydrogen and deuterium will study confinement and scaling laws and will provide operational check-out before the more troublesome tritium is introduced. It is assumed that fusion power densities of $\sim 1\ W/cm^3$ will be attained, which is comparable to those of reactors.

The fusion power generated is predicted to equal the injected neutral-deuterium-beam power (tritium plasmas), so that breakeven conditions should be achieved. In the TFTR, the neutron power will be allowed to escape—there will be no attempt at conversion. The alpha-particle energy from the fusion reaction is expected (on the basis of computer simulation of the orbits) to be largely deposited in the plasma, and should exceed the Ohmic-heating power, resulting in measurable effects on the plasma. The magnetic field strength will be above 5 T and the maximum plasma current 2.5 million amps. The standard pulse length will be one second, but longer pulses are possible. Neutral-beam-injection pulse length will be 0.5 second, with a total of 20 MW of 120-keV neutral-deuterium power delivered to the plasma. The minor and major radii of the device will be 1.1. and 2.65 meters, respectively. Because of the activation resulting predominantly from the 14-MeV d-t neutrons ($10^{12}\ n/cm^2$-s at vacuum wall for 20-MW d-t power), remote handling for maintenance and repair will be necessary. An automatic system will handle the radioactive tritium and supply it to the TFTR. No divertor for impurity reduction is planned. Plasma behavior during operation will be diagnosed by some forty simultaneous methods; for example, six different microwave probes will be available—two 2-mm and 4-mm interferometers and two 4-mm scattering apparatus. All data relevant to TFTR performance and control will be collected by CICADA, the Central Instrumentation Control and Data Acquisition.

Conclusion

Our energy-hungry society is demanding stable solutions to its long-term energy-supply problems. Harnessing controlled thermonuclear fusion will tax all our inventiveness, but it promises reduced environmental hazards relative to fission, and low-cost, abundant, inexhaustible fuel not subject to future price escalation resulting from depletion.

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RCA's early involvement in the fusion effort

RCA engineers were working on fusion power at its very early stages of development with the C-Stellarator, the first toroidal magnetic-confinement fusion device. (The corporation's contribution to the C-Stellarator was summarized in a series of five articles in the Feb/Mar 1961 issue of the *RCA Engineer*.) Beginning in 1957 a group called C-Stellarator Associates managed the development, design, fabrication, installation, and testing of the C-Stellarator research facility specified by the scientists of Project Matterhorn (later renamed the Princeton Plasma Physics Laboratory), Princeton University, and the Atomic Energy Commission. The engineers and scientists of C-Stellarator Associates were drawn from various RCA product divisions, the RCA Laboratories, and the Allis-Chalmers Corp.

RCA Electron Tube Division engineers designed, developed, and built the ultra-high-vacuum system; Broadcast Division engineers, the rf power equipment; and Electronic Data Processing engineers, the control timer and data-handling system. Allis-Chalmers engineers concentrated on the motor-generator, mechanical structure, magnetic field coils, and controls for these subsystems. The C-Stellarator operated until about 1968 and then was modified into the first tokamak outside the USSR, the Princeton ST (Symmetric Tokamak). A summary of RCA's background in plasma and fusion research would be incomplete without mentioning supporting work, during and after the Stellarator effort, done at RCA Laboratories and the operating divisions.

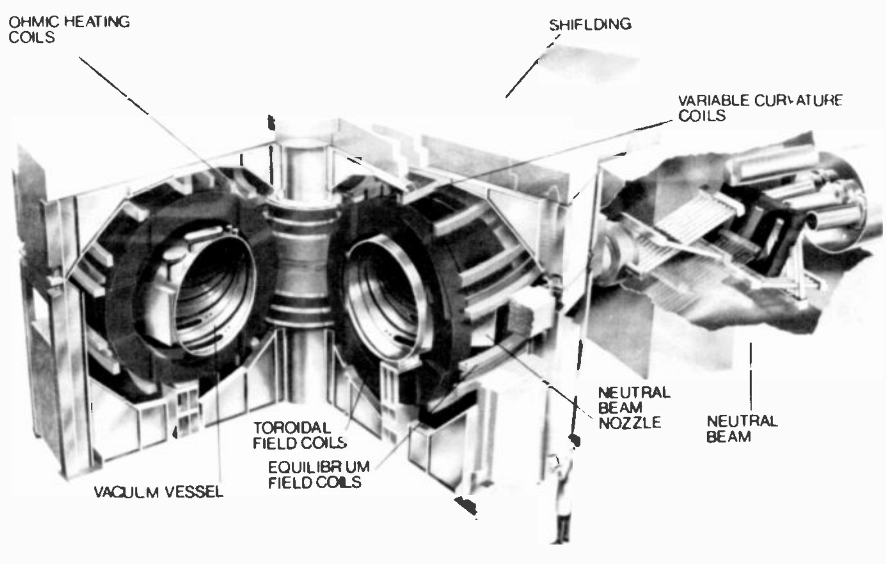

Fig. 5
Tokamak Test Fusion Reactor at PPPL is expected to generate about ten megawatts of fusion power under reactor-like conditions in 1981. It will not generate electricity, however.

Sensurround—building your own earthquake

RCA technicians knew they had a good special-effects system when the "Earthquake" audience asked, "How do they shake the floor?" Integrating Sensurround into theatre sound systems was no easy job, though.

"Earthquake"

E.G. Holub

For many years, Universal Studios felt that the public would have to be offered some sort of "event," not accessible on home tv, in order to attract large audiences into the threatres. People who make up audiences have a certain budget for outside-of-the-home entertainment, and Universal knew they had to provide something very special, so the potential audience would choose to spend their money in a movie theatre, rather than in the ball park or concert hall. One way to make films more attractive was to augment the normal theatre experience with special sound effects. Thus, Sensurround I was created to produce the auditorium-shaking sensations used in the movie "Earthquake."

RCA Technical Services' association with Universal's special-effects activity began in 1974, with the introduction of "Earthquake" and Sensurround I. RCA has now installed approximately 300 Sensurround sound-effects systems in theatres throughout the United States.

Low-frequency sound system

In Sensurround I, low-frequency sound was used to simulate earthquake rumbles and vibrations. The sound was so intense that it could be physically felt in the body as well as heard, so a special sound system had to be designed to augment the theatre's normal sound system. This special system had to be relatively portable and somewhat tailored to each theatre that would use it. Another important design consideration was that the system had to be self-operating after it was installed, so theatre personnel would not have to operate or maintain it.

Early in the project, it was realized that none of the existing standard film recording techniques could effectively record and reproduce sound below 40 Hz, where the frequencies could be physically felt in the body, so each installation was equipped with a low-frequency noise generator. Low-frequency control tones recorded on a special audio track regulated the timing and intensity of the earthquake rumble from the noise generator.

The early 15-Hz system produced good effects, but destroyed speaker after speaker.

Audio-equipment manufacturers were invited to participate in the Sensurround I conception and were asked for equipment designs. The outcome resulted in the use of stock concert-bass horns in the prototype system. For early demonstrations, a General Radio random-noise generator with a lowpass filter simulated the not-yet-designed system generator.

Even though early demonstrations used tuned cabinets (one cubic meter) that had a response tuned to 15 Hz, very low frequencies reproduced at sound pressure levels of about 120 dB (C scale, or flat response) did indeed give the illusion of actual physical vibration and movement. This sound was also physiologically effective when used with visuals depicting earthquake actions.

Therefore, design efforts began with the goal of a 15-Hz system. Many speakers were utterly destroyed while trying to attain the necessary sound pressure levels. Because of this, it was decided that the horn design had to be efficient at these low frequencies.

Designing a horn to operate with a cutoff frequency of 15 Hz theoretically requires a horn mount of about 300 square feet in area.

The low frequency also requires a slow taper rate, meaning the horn would have to be very long. Folding a horn to reduce its length usually degrades the frequency response, but only well above the cutoff frequency. Since the theatres' normal sound systems would handle the higher frequencies anyway, it was considered practical to fold the Sensurround horns.

The horn mouth area was reduced by locating the horn in a corner, so the walls and floor of the theatre formed boundaries and restricted the angle into which the horn radiated. If the horn operates into a small area, the mouth of the horn can be reduced. With a small mouth, some attentuation occurs just above cutoff and there is some frequency-response fluctuation. Since this system did not need to reproduce continuous tones, the uneven response was not important.

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"Rollercoaster"

"Midway"

"Earthquake"

Three horn configurations were developed for the Sensurround system.

Each type of horn used special 18" low-frequency drivers. All three designs (Fig. 1) prevented large cone excursions, which could be destructive to the reproducer.

The first horn is a "W" horn, with two fold-backs to increase the length. Because of its bulk, it is difficult to transport and cannot be used in theatres that require a low-profile horn. The second design, called the "C" horn, is a vertical corner horn that is used where height is a restriction. It uses two 18" drivers and, since it has no internal folds, must be operated into a corner. The third design, the modular "M" horn, is a widely applicable configuration that can be used in multiples by stacking. Each "M" horn contains one 18" driver and is operated into a corner or specially constructed baffling.

The horn driver units were originally standard dynamic speakers, but for Sensurround the *Bl* factor was modified and mechanical positive bias designed into the moving mass. These drivers have voice coils capable of dissipating 1 kW without burning out. Combining high power with long excursions at the desired frequencies in these drivers was another problem, but experimentation produced a combination of cone suspension materials and polymer treatments that yielded the necessary excursion capability and low failure rate.

When the Sensurround activity began, there were only a very few amplifiers available that could deliver more than 300 watts.

As a result, Universal used those manufacturers' equipment that could produce this power. One problem with operating the drivers near resonance is that this makes them highly reactive and so effectively increases the loading on the driving amplifiers. Highly reactive currents are therefore driven back into the amplifier, which can falsely trip output protection circuits and cause loud chirps, squeaks, and buzzes. BGW and Cerwin-Vega amplifiers were found to operate well without these problems.

By limiting the bandwith of the amplifier it could have been manfuactured at a lower cost, but Universal wanted a full-range, general-purpose, high-powered amplifier for potential expansions to Sensurround.

The Sensurround interface

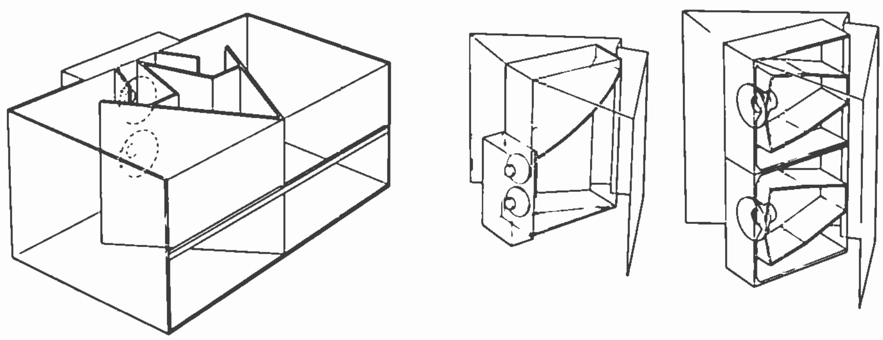
"Earthquake" was released in the three standard theatre film formats; 6-track magnetic sound on 70-mm film, 4-track magnetic sound on 35-mm film, and the old standard single-track optical sound on 35-mm film. The Sensurround effects had to interface with all of these formats.

In reality the term "standard" theatre sound equipment hardly has any meaning today. Some theatres have old subpar systems, others have been updated partially, and still others have new systems. It was thus difficult to design a system that could be quickly installed anywhere.

The final Sensurround I system configuration consisted of the horns required for a given theatre, the amplifiers to drive them, and a special control box integrated into the theatre sound system between the projector changeover switch and the audio power amplifier. See Figs. 2 and 3.

Two tones control the Sensurround effect.

The control electronics accommodates a wide variation in input and output levels and impedances. There are also a digital random-noise generator and filters that generated the earthquake rumble effect. The rumble was turned on and off and otherwise controlled by circuitry tuned to control tones recorded on the audio track of the feature. Sensurround I used two control tones, one at 25 Hz to control the



Recording engineer/producer

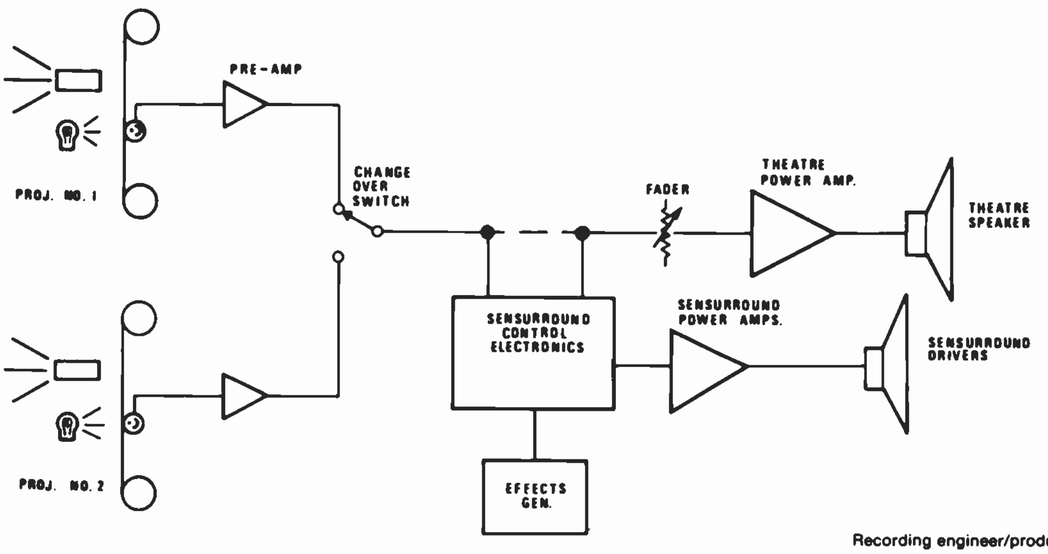
Fig. 1
Three speaker horn types are used in Sensurround. The *W* horn (left) is the largest, the *C* horn (center) is used in height-restricted areas, and the *M*, or modular, horn (right) can be stacked in multiples. Folded configurations are used to increase horn length; special low-frequency drivers are also used.

level of the rumble effect, and another at 35 Hz to combine certain normal soundtrack sounds with the Sensurround rumble for added impact. The control tones are recorded at a maximum level of 30 dB below 100% modulation, and have an analog control range of 10 dB. Tunable active filters separate the control tones.

Because of the closeness of the 25-Hz and 35-Hz tones, the detection filters had to have high Qs to enhance selectively. This, coupled with the low-level control signals, created a filter with a sluggish response time. The Q was therefore reduced and dip filters were added before each control circuit. Some time-constant lag remained, however, that had to be compensated for in the recording of the control tones. The dubbing mixers had to anticipate the action in the picture by turning the control on and off in advance of the screen action.

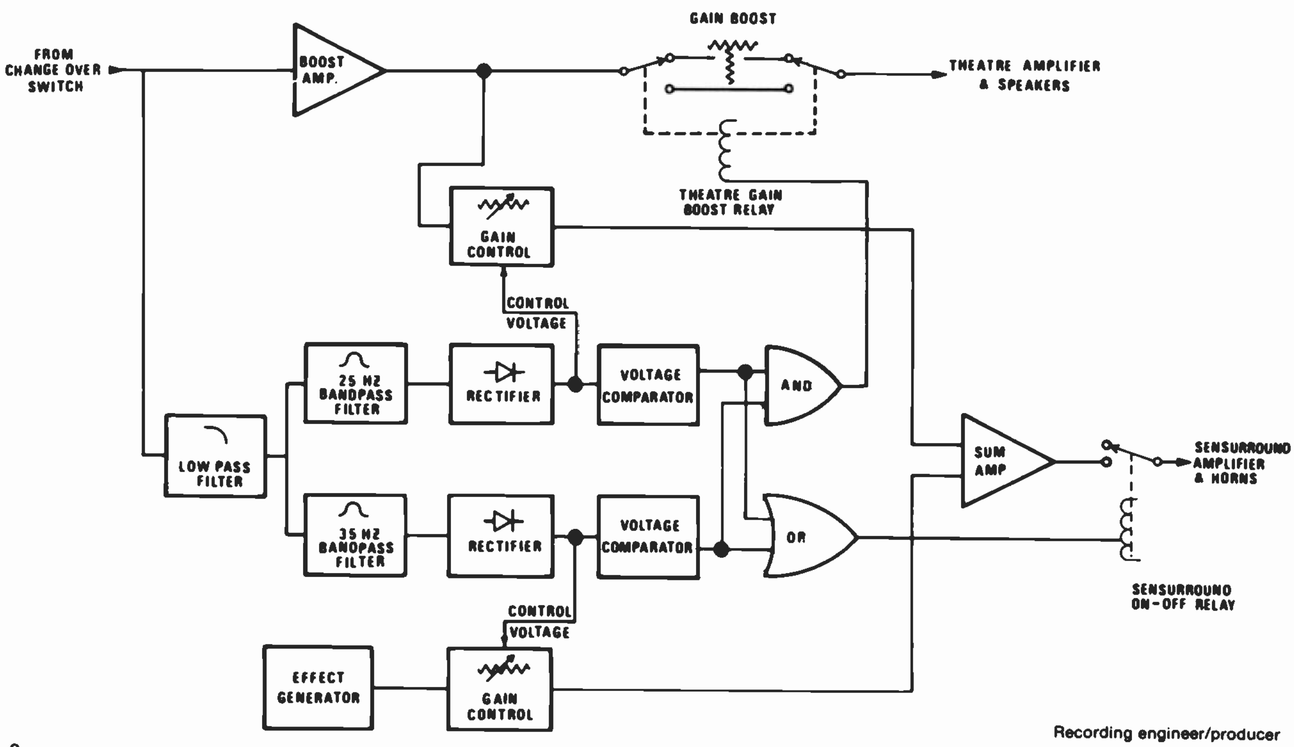
Optical and magnetic-optical sound systems required different formats.

For 35-mm optical sound formats, the control tones are recorded on the normal sound track at a reduced level. For 35-mm magnetic-optical formats, the control tones were recorded on the optical track. Since most magnetic projectors are also equipped for optical sound, the optical sound track was used for control-tone recovery, and, if necessary, an additional



Recording engineer/producer

Fig. 2
Sensurround system is an addition to, and works in parallel with, existing theatre sound systems.



Recording engineer/producer

Fig. 3
Two tones on the soundtrack control the Sensurround electronics. The 25-Hz tone controls the level of the rumble effect and the 35-Hz tone combines normal soundtrack sounds with the Sensurround rumble.

preamplifier was included in the Sensurround control electronics.

When "Earthquake" was recorded on 35-mm as an optical sound print, the control tones were mixed with the normal sound-track material, which was rolled off below 35 Hz so that program sound would not trigger the effects. In the 70-mm format (not used in the United States) two of the six magnetic tracks were devoted to 100-Hz control tones used for effects gating and steering.

During development, Universal found that the normal sound appeared to diminish in intensity when the rumble was activated. To correct this, circuits were added to the control electronics to automatically increase the normal sound track level 6 dB when the effects were gated into operation. This created a good subjective audio balance.

RCA's involvement

The initial planning for "Earthquake" called for 17 theatres to be equipped with Sensurround by the end of the first year of operation. However, nearly 400 theatres showed "Earthquake" by using nonpermanent systems that could be moved to different theatres on demand. Installing and maintaining that amount of equipment in widely dispersed locations throughout the country required a nationwide service organization, and the contract was awarded to Technical Services of the RCA Service Company. Universal specialists trained regional RCA personnel, who in turn went into the field and trained other RCA people. RCA is now handling the installation and maintenance calls within the continental U.S. and has performed the installations in Mexico, South America, and the Caribbean. In addition, for the feature "Earthquake," RCA handled the transfer and installation of equipment into new locations.

The RCA service men work closely with the theatre managers and Universal in evaluating the theatres and installing the equipment. Upon completion of an installation, careful sound pressure level measurements are taken to assure high-quality performance of the system. The system is adjusted until an overall sound pressure level of 95 dB (A scale) is achieved at the center of the theatre, with no more than 110 dB (C scale) 4 feet in front of any horn. These levels are deemed safe for continuous human exposure for periods up to 8 hours.

Murphy's Law and nonstandard sound systems

The Simplex/Norelco XL20 optical sound system presented an interesting problem. The schematic of this one-unit hybrid amplifier is too complex to show here; it has a transistorized preamplifier and a vacuum-tube power amplifier, with transformer coupling between them.

The first attempt to connect this amp to the Sensurround I system was straightforward. The coupling capacitor was opened and the output of the preamp was fed to the Sensurround control electronics; the return from the control electronics went into a newly installed system gain control and then returned to the power amplifier. But, since there was no gain stage in the power amp, the new gain control had to be at maximum in order to obtain normal house levels. Of course, this was not tolerable, so a second attempt to break into the amplifier was made earlier at the coupling capacitor following the first stage of amplification after the photocells. However, at this point the control signals (25-Hz and 35-Hz) did not have enough gain for the Sensurround system.

Finally, the connection was made at the coupling capacitor between the two final transistor stages. Here, the preamp gain and the power amp gain were sufficient, but the frequency response could be affected at this point by the treble and bass controls. Therefore, the bass control setting had to be fixed, because if it were changed, the control-signal levels would be incorrect and the system would work improperly, if at all.

As a result of the experience gained in attempting to install Sensurround where a pickoff point had to be determined prior to disrupting the amplifier circuitry, preliminary measurements were made while running the test films to determine the point of adequate and desirable signal level.

Because of the problems created by systems like the Simplex XL20, in some cases, Universal supplied separate self-contained transistor preamplifiers that tied directly to the sound pickup device to give the necessary preamplification to the control electronics. When the signal was returned to the theatre's amp from the control electronics, it was attenuated down to the pickup input level to run through the sound system in the usual manner. This method avoided interrupting the circuitry of the original sound system and was especially helpful in systems using etched circuits.

Installing Sensurround—problems with nonstandard theatres

Even though Sensurround I was designed for versatility and ease of installation, there were difficulties in matching it to nonstandard theatre sound systems.

A standard theatre sound system historically consists of sound pickups, changeover switching mechanisms, an auditorium-equalization (compensation) panel, power amps, and the sound reproducers, consisting of a crossover network and high- and low-frequency speakers.

However, in the years since the concept of "standard theatre sound system" was conceived, the theatre business prospered, declined, then gradually improved again. During the declining years, many nonstandard economy sound systems were installed. These abbreviated systems used single amplifiers containing preamps and power amps. Changeover switching was done before the amplifier and auditorium equalization was done with simple bass and treble tone controls. Vacuum tubes were replaced with solid-state devices, and photocells were replaced by phototransistors and solar cells. Some older theatre systems were hybrids, with tube preamps and solid-state power amps or vice versa. In other systems the photocells were removed and replaced by higher-gain solar cells, necessitating amplifier circuit changes. Many of these modifications and circuit changes were never recorded.

Stereophonic magnetic sound was introduced in the late 40s, and again the hybriding of systems was compounded. Following the 4-track magnetic sound of the late 40s came the 6-track sound of 70-mm Todd-Ao. Again, newer equipment was added to the older equipment.

Today, a theatre sound system is more nonstandard than standard, so the problems the RCA Service Company theatre men encountered were many and varied.

For example, the Motiograph A7505 sound amplifier would not pass the 25-Hz and 35-Hz control signals at a usable level. This problem was easily corrected, though, by increasing the capacity of the preamps' coupling capacitors.

During the practical work of installation, problems were encountered that seemingly couldn't exist.

Universal had developed a Sensurround setup procedure using special test film that was performed by the RCA man. The final checkout was done with a short reel of the actual film. In some cases, after the setup procedure was performed, the effects from the test reel were intermittent or nonexistent. This problem was resolved and found to be caused by excessive output levels from the preamps at 25 Hz and 35 Hz into the Sensurround control unit.

On the control-tone test films, which were 400 Hz with either a 25-Hz or 35-Hz frequency imposed on the track, the Sensurround control unit would work fine. However, on the sound track of an actual reel many frequencies appeared at once and the control frequencies appeared as a modulation envelope on the normal sound. Since the basic level was too great within the preamp, the soundtrack signals were clipped in final preamp stage before reaching the control electronics. This clipping action destroyed the control tones, and so no effects were present. This problem established a maximum preamp control signal output of about −10 dBm from the preamps.

Some amplifiers did not clip the control tones on excessive sound track input to the control electronics because the low-frequency response was poor. In this case, if excessive signal output was fed to the control electronics, the normal low-freuqency theatre sound would pass through the control-electronics tone filters by brute force and activate the rumbles at the wrong time. Here again, a need was created for a maximum preamp output level to the control unit.

A theatre projection booth can be a high-noise environment.

Xenon arc lamps, high current switching, and brush motors can all cause problems. If the theatre's sound system was not installed with proper attention to grounding, noise could be a problem. Normally the Sensurround I system could work with control signal input levels as low as −40 dBm to the control unit. Experience showed, however, that in high-noise booths where the signal-to-noise ratio was poor, noise would trigger the rumbles. Switch clicks were particularly troublesome. From this experience, coupled with the lesson learned from the ill effects of excessive signal, an optimum level of −20 dBm was established. With this level at the output of the theatre's preamp, the control electronics functioned trouble-free, no matter what was encountered in the projection booth.

Specific installation instructions did not exist for the multitude of sound systems in existence.

The RCA men went to their installation locations, reviewed the system or system diagrams (if available), and determined where the tie-in points would be. Sometimes this turned out to be a complicated procedure—see the insert on the previous page. But the list of problems didn't stop there. Speaker placements sometimes produced acoustical cancellations and dead spots, projector-speed variations changed the control-tone frequencies, transducers and speakers failed, and there were some grounding problems.

Sensurround II

"Earthquake" was so successful—it brought two Academy Awards and good gross profits to Universal—that a second Sensurround picture followed, "Midway." To avoid the field problems that RCA Service Co. had encountered in installing the original system for "Earthquake," Universal developed Sensurround II.

Universal selected to use only the 35-mm optical format for "Midway." The random-noise generator was discarded and the effects sound was recorded directly on the optical track. In order to obtain an effective dynamic recording range of about 100 dB for the Sensurround effect, DBX expansion and noise reduction were introduced as part of the control electronics. To overcome the subpar sound in some systems, solar cells were installed as pickup devices for the "Midway" sound and the control electronics included an optical preamp compensatable to 10 kHz.

The 25- and 35-Hz control tones were retained. However, they no longer controlled the timing and intensity of the effects, but rather directed them through either the front, rear, or all the Sensurround horns.

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The future

Universal recently released "Rollercoaster," the third Sensurround film. It looks as if low frequency may become a permanent part of the moviegoing sound spectrum.

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CMOS reliability

CMOS integrated circuits have been widely accepted because of their low power dissipation, high noise immunity, and wide operating voltage range. These circuit advantages would be worthless if CMOS were not reliable.

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Complementary metal-oxide-silicon (CMOS) integrated circuits have had a major impact on the electronics industry, and have created new areas of application for digital circuits. CMOS digital circuits, because of a number of very significant circuit advantages, including low power dissipation, high noise immunity, and wide operating-voltage range, have become a very widely used logic family.

The RCA series of CMOS devices, first introduced as the COS/MOS CD4000 series in 1968, has gained wide acceptance. The introduction, in 1971, of plastic-encapsulated CMOS integrated circuits was instrumental in achieving even wider acceptance of this popular series.

The COS/MOS product line today includes more than 100 standard parts in the CD4000A series, parts that are used worldwide in applications ranging from battery-operated watch circuits to many functions in the aerospace, computer, automotive, and consumer industries. In addition, a new product line has been introduced, the CD4000B series, which has improved features such as a higher operating-voltage range (3 to 20 V), standardized output drive, symmetrical transition time, and improved electostatic-discharge (ESD) protection networks.

Reliability of MOS integrated circuits

MOS (metal-oxide-silicon) integrated circuits have had a very great impact on the digital electronics industry. Not only have MOS integrated circuits displaced digital bipolar integrated circuits in many applications, but they have made possible a large number of totally new electronics applications. As a result, MOS integrated circuits are at present being produced in unit volumes comparable to those of bipolar integrated circuits.

Because bipolar integrated circuits were available earlier, more information has been published on their reliability than on MOS integrated-circuit reliability. In addition, initial bipolar circuit usage was largely in high-reliability military and aerospace applications; MOS integrated circuits have been used principally in consumer and commercial applications. While early MOS devices were primarily hermetically packaged, a very large portion of all MOS ICs produced today are encapsulated in plastic. Since plastic has also been widely used to encapsulate bipolar integrated circuits, including both digital and linear circuits, a discussion of the similarities and differences between MOS and bipolar ICs follows.

Plastic encapsulated ICs are significantly more reliable today than they were several years ago.

A large percentage of all MOS integrated circuits manufactured are encapsulated in plastic rather than in hermetic packages. Plastic encapsulation provides a number of significant advantages, including lower product cost, freedom from potential problems with loose particles (in molded devices), mechanically strong dual-in-line packages, good resistance to shock and vibration, a no-leak-test requirement, and the possibility of small packages.

A number of possible limitations of plastic-encapsulated integrated circuits have been identified in studies of early plastic encapsulation of both bipolar and MOS ICs. These limitations include moisture-penetration effects, effects resulting from a mismatch in coefficient of linear thermal expansion of plastic relative to silicon and interconnect metals, and the presence of ionic materials and other contaminants in certain plastics.

The knowledge of the potential limitations of certain plastics has led to the use, in recent years, of vastly improved materials and processes for fabrication of plastic-encapsulated devices. An example is the use of high-purity Novolac epoxy plastics with high glass transition temperatures. Modifications in assembly techniques have also been made. As a result of these changes, plastic-encapsulated devices, both bipolar and MOS, are significantly more reliable than devices fabricated a number of years ago.

Humid ambients, such as 85°C/85% relative humidity, constitute a means for greatly accelerating possible failure mechanisms in plastic-encapsulated silicon devices. Consequently, quality control tests, as well as high-humidity tests, particularly under bias conditions, have been used to quantitatively assess the integrity of IC passivation and encapsulation systems, and have been the basis for process improvements. The effect of high humidity conditions on the acceleration of device failure mechanisms has been the basis for a number of detailed studies.

MOS versus bipolar ICs:

There are a number of fundamental differences between MOS and bipolar silicon devices that affect integrated-circuit reliability. Digital MOS ICs differ from digital bipolar ICs principally in the higher substrate resistivity, the use of higher applied voltages, and in the importance of the properties of the gate oxide of MOS devices.

MOS fabrication technology differs from bipolar technology in that the process is simpler. Accordingly, it is easier to attain higher chip complexity with the MOS

Editor's note: Considerably more information was gathered by the authors than could be presented in this brief survey. Readers interested in more information should examine references 1 and 2, which contain further test data, background information, and bibliographic listings that could not be included here because of space limits.

technology and, thus, higher gate-to-pin ratios. Since wire-bond failures are a significant factor in limiting the reliability of small-scale integrated circuits, the MOS technology offers the possibility of significant improvements in equipment reliability by reducing the number of wire bonds and external interconnections. Moreover, the MOS technology offers the possibility of lower power dissipation per function, which in turn improves device reliability by assuring lower chip temperatures during operation. In typical bipolar ICs (TTL), device dissipation is significant. By contrast, dissipation in MOS devices such as CMOS and CMOS-SOS (silicon-on-sapphire) is very low.

The MOS technology has an advantage relative to bipolar devices in that the high current densities in the metal interconnections and, thus, electromigration (current-induced mass transport) is not a common problem. In addition, high current density problems at metal-silicon contacts are less frequent. The high impedance of MOS devices makes multi-level interconnections feasible in complex arrays without significantly compromising circuit properties. Diffused cross-unders in the single-crystal silicon are effective, and if another level of interconnections in addition to that provided by the metallization layer is required, polycrystalline silicon, deposited as part of the silicon-gate process, is very effective. By contrast, an additional level of interconnections in bipolar arrays requires the use of metal-over-metal crossovers, which requires additional technology and introduces possible new failure mechanisms.

Since localized defects in silicon affect integrated circuit reliability, one advantage of conventional monolithic MOS compared to bipolar circuits is that no expitaxial layer is required. Therefore, MOS devices can be fabricated in silicon of better crystallographic quality, with little possibility of stacking faults or of the epitaxial spikes that cause device problems and damage to the masks used for photolithography. Finally, since MOS processing is simpler than bipolar processing and requires less steps, the possibility of manufacturing errors that adversely affect reliability is lower.

Frequently, failure rates for devices of various complexities are lumped together and reported as a failure rate for a particular family. Because MOS devices tend to be more complex than bipolar devices, they would have to have a lower failure rate per gate to have a reported failure rate per packaged part equal to that of bipolar devices. However, for equal complexity, bipolar and MOS are equally reliable.

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MOS ICs make use of many of the same materials and processes as bipolar ICs and small-signal transistors. Accordingly, improvements in silicon materials, oxidation, photolithography, diffusion, metallization, passivation and plastic encapsulation, and in device physics, process control, and electrical characterization have resulted in substantial improvements in the reliability of both types of integrated circuits.

MOS failure modes and mechanisms: opens, shorts, degradations.

Since many processing steps, materials, and construction features are common to both MOS and bipolar ICs, many of the possible failure mechanisms that have been reported apply to both types of devcies. For example, passivation, chip-to-substrate bonding, wire bonding, and package sealing or molding procedures are similar for MOS and bipolar ICs.

MOS failure modes can be classified as shorts, opens, and degradations. Shorts are most commonly the result of dielectric failure of the gate (thin) oxide. Electrical opens may result from microcracks in the metallization at topographic steps, photolithography problems, corrosion of metallization, fusion of metal because of overstress, or open wire bonds. Degradation-type effects are attributable to the motion of ions (such as Na^+) in the SiO_2, or to surface-charge spreading effects and consequent inversion.

Considerable information is available on the distribution of failure mechanisms in devices that failed accelerated stress tests, or that failed during field usage. The principal MOS failure mechanisms are the result of motion of charge in or on oxides, and shorts through gate oxides. There is, however, a considerable variance in the distribution of mechanisms depending on the source issuing the information. Device users, who include electronic-equipment manufacturers, government agencies, and industrial organizations performing government-contract-supported reliability studies, tend to agree that there are large variations between products from different suppliers.

Gate-oxide breakdown may result from localized breakdown at defects, or from

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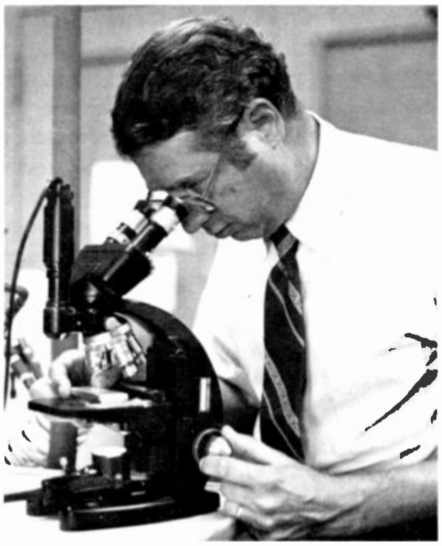

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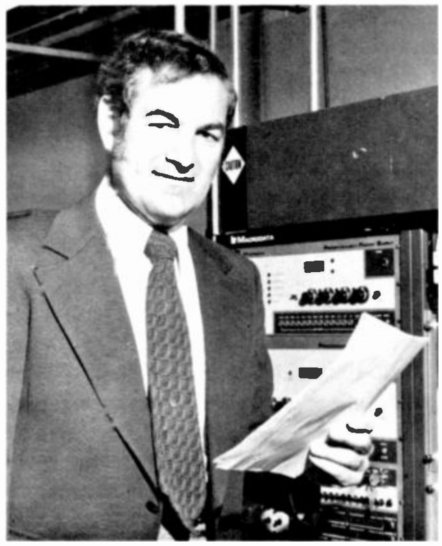

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intrinsic breakdown of thin oxide at input circuits. Breakdown at inputs is principally attributable to overstress resulting from discharges of static electricity of sufficiently high energy. While virtually all MOS ICs contain an input-protection circuit, such circuits vary considerably in design, principle of operation, and effectiveness. Susceptibility of silicon devices to static-electricity effects is not unique to MOS circuits, and has been reported in bipolar integrated circuits.

Several forms of alkali ion migration are possible, including the commonly reported transverse Na^+ ion movement in an electric field at an elevated temperature, and lateral Na^+ ion movement followed by transverse movement. The net result of alkali ion migration is to increase the threshold voltage of p-channel transistors, decrease the threshold of n-channel transistors, or to decrease the field inversion voltage of n-type regions.

Because MOS structures have proven an excellent tool for the study of $Si\text{-}SiO_2$ interface properties, a vast amount of information has been made available for the improvement of the design and control of the device fabrication process.

Aluminum metal corrosion in integrated circuits has been the subject of considerable study in recent years. It has been shown that low-temperature-deposited glass-like inorganic passivation materials can be very effective in reducing the possibility of aluminum corrosion. Opens in aluminum have been shown to occur principally at cracks or pinholes in passivation-glass layers, and specific techniques for detecting and minimizing the occurrence of such localized defects in the integrity of passivation-glass layers have been developed. Specific factors that can result in chemical corrosion of aluminum and electrochemical corrosion at cathode and anode regions have been identified.

Failure rates under actual use (field) conditions are very much lower than failure rates under the accelerated stress conditions typically used by device manufacturers to evaluate reliability.

Some data is available on the reliability of similar devices in hermetic and plastic packages. In general, operating-life failure rates are reported to be several times as high for devices in plastic. It is generally not possible, however, to take the available data and make specific quantitative conclusions relative to the effect of plastic encapsulation on the reliability of a given type of MOS IC. One reason for this is that, even though the same wafer processing is applied to both types, there are many differences in the assembly and test sequences other than just plastic versus hermetic packaging. For example, devices intended for high-reliability applications may be subjected to a more stringent visual inspection criteria, may be assembled under very closely controlled conditions with considerable documentation, may be electrically tested at wide ranges of conditions such as −55°C and 125°C, and may be subjected to various screens, electrical tests, burn-ins and lot acceptance criteria. Obviously, such techniques, while more costly, are effective in eliminating a certain number of potentially less reliable (freak) devices from the main population.

The failure rate of plastic-encapsulated MOS devices can be considered to be the sum of the specific failure rates resulting from failure mechanisms occurring on the chip, in the interconnection system external to the chip, and in the package. While unsuitable plastics can adversely affect the reliability of susceptible chips, plastic encapsulation cannot provide a chip reliability in excess of that which would be encountered in a dry, inert ambient. Accordingly, the reliability of many plastic-encapsulated devices, particularly under lower humidity conditions, is limited by the reliability of the encapsulated chip rather than by any reliability limitations imposed by the plastic.

A failure rate on the order of 0.1%/1000 hours at 85°C at the 60% upper confidence level can be expected for high-quality plastic-encapsulated commercial-type MOS ICs prepared by a mature, well-controlled process. Field failure rates for plastic-encapsulated MOS ICs at operating temperatures up to 55°C can be considered to be on the order of 0.01%/1000 hours (60% upper confidence level). Obviously, variations will occur depending upon type, design, process, manufacturer, screens applied, voltage, and severity of ambient conditions and other specifics of the final application.

A number of manufacturers have shown increases in failure rates of MOS products as a result of increasing operating voltage at accelerated stress conditions, such as during operating-life tests. Possible effects of higher operating voltage on MOS ICs include increased susceptibility to surface-charge spreading and to field inversion, and increased incidence of oxide breakdown. Oxide breakdown in MOS structures has been considered by some to follow Peek's law in that the time to failure is inversely related to the fourth power of the applied voltage.

Generally, an increase in chip complexity will decrease the failure rate per gate or per

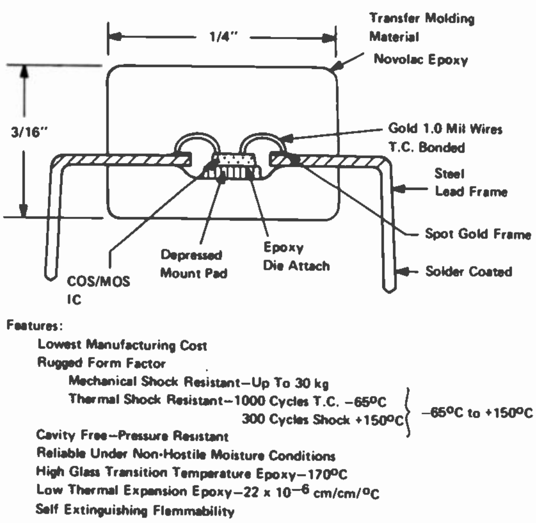

Fig. 1
Dual-in-line plastic (DIP) package, the 1976 system.

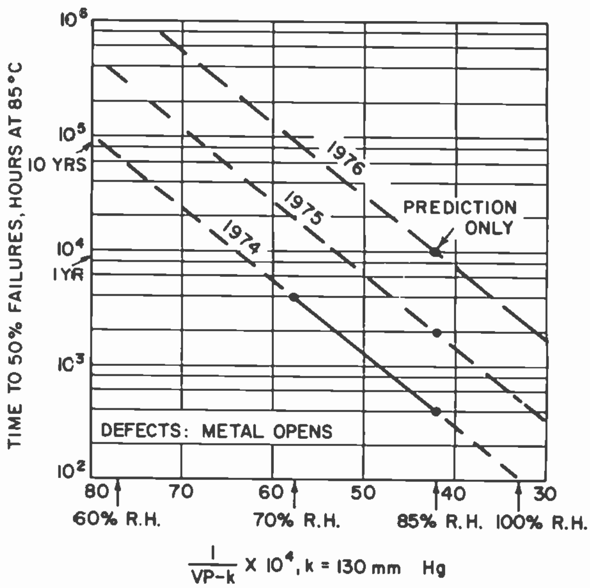

Fig. 3
Vapor pressure versus median-time-to-failure at 85°C. Published acceleration factors show that the 1975-76 plastic packaged product would survive the moisture level in their applications.

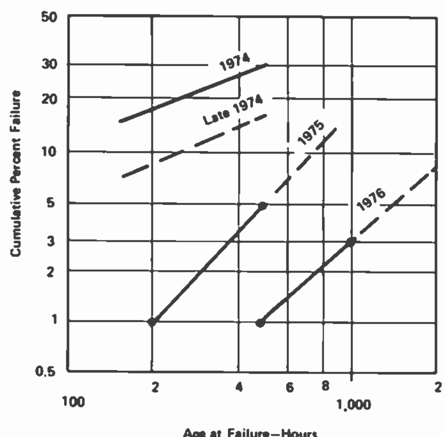

Fig. 2
Weibull plot of 85% relative humidity with temperature-humidity-bias characteristics of RCA CMOS product from 1974 to 1976. Failures plotted for catastrophics only (opens and multiple parameters).

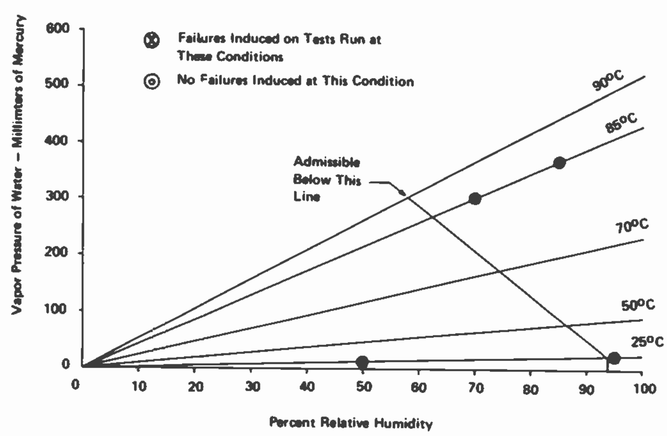

Fig. 4
Lower operating temperatures lower the vapor pressure. This plot is especially useful because it is based on experimental data and is related to water-vapor pressure.

function accomplished. The overall failure rate may be considered as the sum of the failure of wire bonds, failures that would occur with a chip of any size, and chip failures at localized defects, which is an area-dependent factor. The failure rate of wire bonds is simply the product of the failure rate per wire, such as 0.0001%/1000 hours, times the number of wires. The failure rate attributable to localized defects increases with increasing chip area, but is not linearly dependent on the area of the chip; it is considered to increase less rapidly than chip size, because of the tendency of localized defects to cluster rather than to occur at random. (The considerations here are somewhat similar to those which have been shown to apply to the effect of chip size or circuit complexity on IC yield.) Complex ICs are, thus, more reliable per gate, and the use of complex ICs in electronic equipment to perform the same functions as a number of less complex devices will, in general, result in substantially improved equipment reliability.

Reliability of MOS and bipolar ICs is about equal for equal complexity.

In general, reported failure rates of bipolar ICs have been approximately equal to those of MOS ICs of equal complexity prepared by means of mature, well-controlled processes, and operated at the same chip temperature. A number of researchers have reached the conclusion that there is no systematic difference between MOS and bipolar integrated circuit reliability.

The reliability of MOS ICs depends on the design, process, circuit manufacturer, degree of testing and screening, and on the application, as well as the packaging.

Plastic packages are satisfactory for the majority of all MOS IC applications. No major differences in reliability of products of equal functional complexity made by the major MOS technologies (PMOS, CMOS, or NMOS) or of products made with Al or Si gates are evident in the available reliability data. Furthermore, the reliability of MOS devices can be considered to be equal to that of bipolar digital circuits of equal complexity when each type is prepared by a well-controlled process and operated at the same temperature.

CMOS reliability data

Although higher-reliability commercial CMOS devices are being demanded by the industry, cost constraints are always in view. Plastic-packaged CMOS devices are used to satisfy these cost constraints. However, the substitution of lower-cost plastic packages for more expensive hermetic product raises some important issues for integrated circuits, both bipolar and MOS. These issues are usually relatively simple, but can be confusing to designers and component engineers because of the differences in data presentation from various manufacturers of MOS integrated circuits. The basic factors of package selection depend upon:

1) A thorough understanding of the final application environment with respect to temperature, temperature cycling, humidity, salinity, and corrosive chemical contamination.

2) Determination of the system life and, consequently, the component life required.

3) The potential for screening (burn-in, etc.) and the level of stress that can be used.

4) Mechanical requirements of packages in the system.

5) The electrical environment.

Plastic packages—moisture is a consideration.

The long-term reliability of plastic-encapsulated CMOS devices in humid environments is limited by the effects of moisture. Most applications can accept some degradation in device characteristics, but catastrophics (such as opens and shorts) are never acceptable. Moisture entry allows electrochemical corrosion or electroplating of metals to occur.

Externally applied potentials and potentials produced by dissimilar metals affect the metal on the semiconductor chip during operating and non-operating conditions. Extended life in plastic packages depends on choice of metal, plastic encapsulant, passivation layer over the metal system, and resistance to moisture entry into the package during system life.

The moisture that enters the package is often contaminated with soluble salts, such as sodium chloride; the water itself can dissolve some of the ionic species in the plastic and develop an electrolytic solution that will attack exposed metal, especially aluminum. However, aluminum is not the only metal subject to water corrosion. In the presence of water, ionic contaminants, and a potential, most metals will either electrodeposit or undergo electrode reactions that lead to corrosion.

The choice of plastic package, then, must take into account these effects of moisture, and appropriate testing must be performed to establish data that are meaningful in determining the reliability of the device in its application. CMOS devices will dissipate relatively little power; therefore, the silicon-chip temperature rise over the operating ambient will be negligible; consequently, the relative humidity at the surface of the device will not be affected. Increasing temperature at the device surface reduces the probability of moisture failure mechanisms.

The plastic package used by RCA is shown, schematically, in Fig. 1. The choice of materials minimizes both thermal mechanical deformation and moisture failure mechanisms. As plastic encapsulation materials for use with semiconductors improve, and with the maturing of the CMOS technology, greater reliability is found with the overstress tests used to characterize humidity capability. Fig. 2 is a Weibull plot of 85°C/85% relative humidity (R.H.) with temperature humidity bias (THB) characteristics of RCA CMOS product from 1974 to 1976. If the acceleration factors found in the literature are applied to the 1975-1976 product, it will be seen that moisture failures under most application conditions are not to be expected. A plot of vapor pressure versus median-time-to-failure at 85°C for this data (Fig. 3) shows this effect dramatically. The slope of the prediction line used for this data was derived from 1974 product.

Since most operating temperature conditions are less than 85°C, a plot of vapor pressure, temperature, and relative humidity was developed to indicate recommended conditions for plastic. As Fig. 4 shows, lower operating temperatures lower the vapor pressure and make possible operation at high humidity levels. Another factor that must be considered in using plastic-encapsulated product is whether the environmental conditions cause condensation of water vapor (dew point). If dewing occurs, the possible increased presence of water at the chip complicates the determination of the reliability of the plastic package. Moisture absorbed in the plastic at the chip interface provides moisture at the device surface and, if condensation takes place, especially where voids occur at the plastic-to-silicon interface, then more moisture is available for chemical reactions. Water molecules tend to displace the plastic from the device interface.

Table I
Package choice by moisture environment for temperatures between 20°C and 40°C.

Average R.H.	*Comments*	*Package*
100%	Permanent moisture	Frit
75% to 100%	Dewing	Frit
75%	Some dewing	Plastic (5-yr life)
⩽75%	No dewing	Plastic (10-yr life)

With the above information, then, four classes of operation have been identified as to humidity, temperature, and dewpoint considerations. Table I shows these conditions and recommends the package type to be used under each set.

Although the classical method of testing product under controlled conditions has its place, very often in comparing materials one would like to look at the effects at the minimum, maximum, and "out-of-spec" conditions to determine the materials that provide the greatest margin of safety. A recent plastic-encapsulation study shows that the plastic material used in 1976 has a greater margin of safety under conditions of high humidity when the process is 2.5 times maximum limit. The testing of both plastic materials under controlled conditions gives only one part of the data in the total sample space.

Several other tests have been used to determine the reliability of the plastic package. One important test—the reliability-verification-sequence (RVS)—subjects devices to a pressure-cooker stress test (15 psig, 121°C, 24 hrs) followed by a bias operating-life test at 85°C (temperature is maintained below 100°C to prevent the vaporization of moisture forced into the package during the pressure-cooker stage). This test is better than the 85°C/85% R.H. test in calibrating device reliability under application conditions. A device that passes 2 or 3 cycles of this sequence test without a catastrophic failure is a device whose field-usage failure rate should be independent of moisture, if the application is proper. RVS tests were run on plastic package samples that incor-

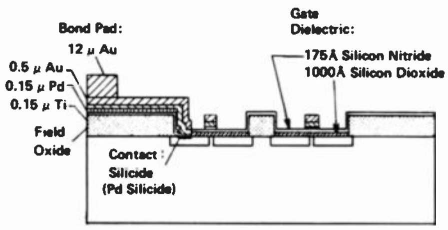

Fig. 5
Trimetal system. Nitride-passivated titanium, platinum, and gold metallization used instead of aluminum can produce reliability results comparable to hermetically sealed package.

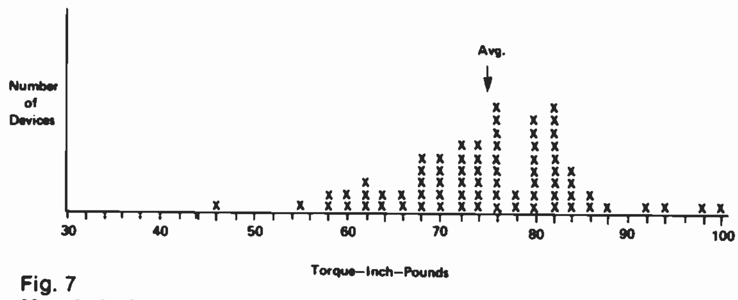

Fig. 7
Mecahnical-torque tests on frit-sealed packages. Normally, 15 in-lbs. of torque strength is sufficient to ensure package integrity under field conditions.

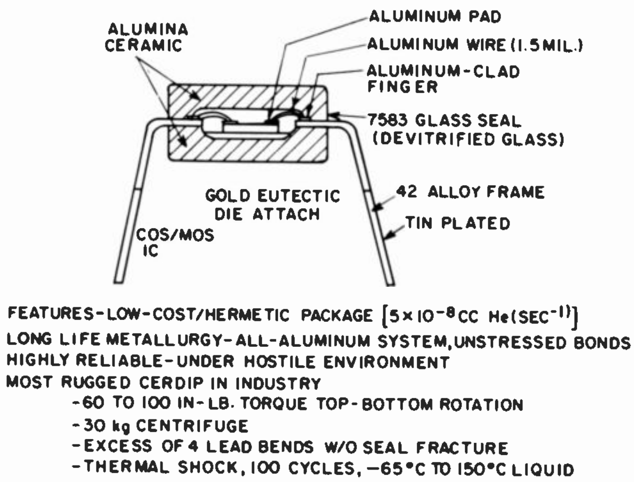

Fig. 6
Frit-sealed package construction. This is the dual in-line CERDIP system that provides low-cost moisture protection by hermetically sealing the package.

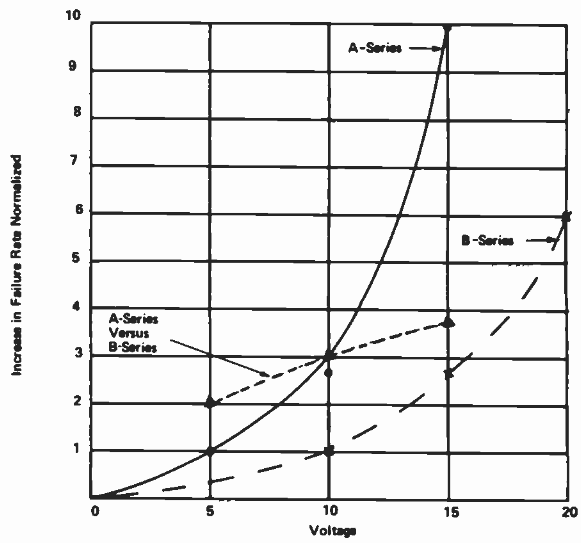

Fig. 8
Applied voltage versus failure rate. Data show how an increase in applied voltage increased the failure rate (at 125°C) for A- and B-series product.

porate the 1975 and 1976 molding systems; new production units were also tested. All the failures were degradational; none were catastrophic (open or short).

Gold chip—the trimetal system improves reliability.

No plastic materials known at this time can offer complete protection against moisture penetration when compared to hermetically-sealed packages. Thus, reliability can be increased substantially by making the chip more hermetic.

CMOS devices processed with gold in place of the aluminum metallization, in addition to a silicon nitride layer, can produce the desired reliability results. The basic construction of the nitride-passivated titanium, platinum, and gold metallization system is shown in Fig. 5.

The silicon nitride provides junction hermeticity while the titanium metal provides adherence to the dielectric and the platinum serves as a diffusion barrier for the gold. In addition to reducing the moisture problems, the use of the trimetal system also reduces effects of mechanisms associated with electromigration, Al-Si and Al-SiO_2 reactions. Because gold ions are soluble in water, gold can be electrodeposited, especially in the presence of the chloride ion. The glass passivation normally employed on the silicon chip prevents the formation of water directly on the gold metallization; the use of epoxy with low chloride content further minimizes the possibility of electrodeposition.

Reliability data for the gold chip in both plastic and hermetic packages shows that much higher stress levels will be obtainable with this chip design in both operating temperature and moisture environments, regardless of packages.

The frit package provides a hermetic seal.

When a hermetic package is desired, the most economical choice for high-volume commercial application is the frit package. Fig. 6 shows that the frit package is a cavity type. The key issues in determining the reliability of the frit package centers obviously around maintenance of hermeticity throughout the life cycle. If hermeticity is not maintained, the frit-package reliability could be worse than that of the plastic package with aluminum-metallized chip under severe moisture conditions. Hermeticity can be affected by severe mechanical or thermal shock; both of which can occur during PC board insertion and wave soldering. In monitoring the mechanical- and thermal-shock capability of a package, emphasis is placed on running highly accelerated tests, such as mechanical torque and liquid-immersion thermal shock. Fig. 7 shows typical mechanical-torque test results. Normally 15 in-lbs. of torque is sufficient to eliminate field problems resulting from loss of package integrity.

Life tests have no value unless the test conditions relate to quantities that can be measured and controlled in the final application.

Semiconductor junction temperature and operating voltage are available parameters that can be measured directly or indirectly. Both qualitative and quantitative descriptions are used to extrapolate the results of life tests to actual use conditions. The most frequently used model is the Arrhenius equation which, basically, states that a certain minimum amount of activation energy is required for reactions to take place.

Life tests of CMOS devices are usually conducted in two modes: static bias life and dynamic operating life. For logic devices, the static bias life test is generally the more severe. For CMOS devices, the activation energy required to predict life is 1.1 eV. With this information, accelerated tests can be conducted on both plastic and frit packages and then extrapolated to use conditions.

Voltage affects failure rate.

Although the life of CMOS devices, like other semiconductors, is considered to have basically an Arrhenius acceleration, voltage is another parameter that substantially affects the failure-rate equation. Electronic components are complex engineering systems, and one should not develop too many analytical equations that attempt to explain all the physical and chemical reactions in terms of failure rate. Good engineering data can be derived empirically for both temperature and voltage characteristics, and can be used to determine how parts will eventually behave in an application. Fig. 8 shows the voltage acceleration factor for both CD4000 A- and B-series product. The presence of a voltage accelerates the mobility of charges on the exterior of the SiO_2 or other surface dielectric, and results in charge accumulation with resultant increases in surface leakage currents. The B-series ICs show less sensitivity to voltage stress than the A-series ICs because B-series devices are operating at a much smaller percentage of actual device breakdown voltage (40% to 60%).

Summary of commercial CMOS package types: each has merits.

Table II is a summary of the main factors that determine the reliability of each package type discussed in this section. There are advantages and disadvantages to each system; no one package has all of the engineering and manufacturing merits

Table II
Plastic versus hermetic package. Main factors that determine reliability of each package type.

	Al, plastic	*Au, plastic*	*Frit*
Life maximum rating	125°C (85°C actual)	150°C	125°C
Acceleration factor over 100°C	10	100 to 400	10
Moisture resistance	Some failure mechanisms	Yes	Yes
Wire bond reliability problem	High temperature and high moisture environment	No	No
Electromigration	Fair	Excellent	Fair
Microcracks	Possible	No	Yes
Barrier quality	n/a	Very good	n/a
Metallurgy	Au-Al	Au-Au	Al-Al
Chip mounting	Low temperature (200°C)	Low temperature (200°C)	High temperature (450°C)
Hermeticity	n/a	Yes	Required
High rel. capability	No	Yes	Yes

Table III
Static discharge (input to *Vss*) versus life. The CMOS frit package was used since higher temperature accelerated tests could be performed.

Test and conditions	*Control*	*One discharge* 100 V	*One discharge* 200 V	*One discharge* 300
Bias life; 12 V, 200°C, 24 hrs				
CD4013AF	1/13*	2/12	2/13	1/12
CD4016AF	3/13	0/12	3/13	1/12
Bias life; 12 V, 200°C, 24 hrs (second sample)				
CD4013AF	1/15	1/15	0/15	1/15
CD4016AF	0/15	0/15	0/15	0/15
CD4011AF	0/15	0/15	0/15	0/15
Bias life; 12 V, 125°C, 168 hrs				
CD4013AF	1/10	1/11	0/10	2/11
CD4016AF	0/10	0/10	0/11	0/11

**Number of failures/number in group tested.*

Table IV
Field-usage operating-life data on CD4000A family of high-reliability integrated circuits (MIL-STD-883 slash-series types)

Satellite	*Oscar-6*[6]	*ITOS D/F/G/H*[1,6]	*Atmosphere Explorer C/D/E/*[2,6]	*Satcom F1/F2*[7]
Time in orbit (months)[5]	32	85.5	49	16.5
Number of units	90	168	7200	1652
Device—hours	2,073,600	2,585,520	84,672,000	9,812,880
Number of failures	0	0	0	0
Failure rate (%/1000 hrs)[3,4]	0.045	0.035	0.001	0.0092
MTTF (hrs)[3]	2,360,000	2,900,000	96,000,000	10,750,000
Total device hours	99,144,000			
Total failure rate[3,4]	0.00092%/1000 hrs			
Total MTTF hrs[3]	108,000,000			

[1]Satellite D orbit time 23 months, F 36 months, G 24 months, H 2.5 months.
[2]AE/C orbit time 34 months, AE/D 4 months, AE/E 11 months.
[3]Failure rates and MTTF presented at 60 percent 1-sided s-confidence level.
[4]Operating temperature range 25°C to 125°C; no acceleration factor used.
[5]Data in table represents field usage through Oct 15, 1976.
[6]Reporting data stopped on OSCAR 6, ITOS D and AE/D
[7]Satcom orbit time; F1, 10 months; F2, 6.5 months.

Table V
MIL-STD-883, method 5005, qualification subgroup C5, 125°C testing.

Detail spec	*Device hrs*	*Device failures Degrad*	*Inop.*
50 gates	387,000	0	0
51 flip flop	258,000	1	0
52 gates	516,000	1	0
53 gates	258,000	0	0
55 buffers	563,000	4	0
56 counters	645,000	3	0
57 shift register	387,000	3	0
Total	3,014,000	12	0

Table VI
CMOS qualification testing—failure rates.

*MIL-M-*38510, *class A*	*MTTF(Hrs)*
3.014×10^6 device hrs at 125°C	
12 degradational rejects	
0.44%/1000 hrs @ 125°C	225,000
0.066%/1000 hrs @ 55°C	1,330,000
0.02%/1000 hrs @ 25°C	5,000,000
Zero functional rejects	
0.03%/1000 hrs @ 125°C	3,300,000
0.0045%/1000 hrs @35°C	22,000,000
0.0013%/1000 hrs @ 25°C	75,000,000

necessary to warrant elimination of the others.

Because there is a greater demand for plastic-encapsulated product than there is for any other package, the attractiveness of the gold chip in plastic increases. The gold chip in plastic offers some of the hermeticity advantages of the frit product and the ruggedness of the plastic-packaged product. In addition, reliability is improved by the presence of silicon nitride, which acts as a complete barrier to alkali-ion movement through the surface of the device. Higher operating temperatures can be achieved by gold-chip devices in plastic than by any other chip type in plastic, and the cost of the gold-chip product will be less than that of frit or Cerdip product.

Electrostatic discharge is becoming less of a reliability threat.

The breakdown of gate oxides because of the discharge of static electricity has been given considerable attention since MOS devices were first introduced. Although the mechanism of failure is well understood, two questions are continually asked, for which industry-wide data is not available.

1) If a device is subjected to static charge and does not fail, will it fail during its expected life under rated stress, i.e., is gate-oxide breakdown a life-related mechanism?

2) Can devices be screened for weak gate-oxide defects by the use of a static-discharge pulse?

Evaluations have been conducted on CMOS parts incorporating protection networks in an attempt to answer these questions. As more precautions are taken against electrostatic discharge by users of MOS devices, and as semiconductor manufacturers develop protection networks that are equal to worst-case electrostatic-discharge experience, this phenomenon will become less of a reliability threat.

The life-test matrix shown in Table III was designed to provide a preliminary insight into latent life-test failures. Devices were stressed at lower electrostatic levels (100 to 300 V) and then subjected to accelerated- and rated-life conditions. No statistical difference was noted between the stressed and control groups. Although more work is required, gate oxide shorts do not appear to be life-related defects.

High-reliability CMOS integrated circuits have operated in space for one hundred million hours with no failures.

A considerable amount of data on devices in ceramic packages has been generated during qualification and conformance testing of CD4000A series CMOS devices to MIL-M-38510, class A specifications. These data indicate excellent package integrity (one failure in a total of 729 devices tested to group B qualification tests), and excellent stability (only one failure in a total of 1504 devices tested to group C qualification tests). Conformance test data on over 2.3 million device-hours of accelerated-stress testing at 125°C on a wide variety of circuits, from gates to MSI devices, show only 5 degradational failures and 3 inoperable failures, which corresponds to a functional failure rate at 125°C of 0.14%/1000 hours, at 60% confidence level.

Accelerated stress type life tests on CD4000B series devices have indicated improved stability at various operating voltages, with relatively less senstitivity of devices to voltage stress than with CD4000A series devices. The higher reliability of B-series devices is attributed to ability to electrically test devices at higher voltages, and to operation at a small percentage of actual device avalanche breakdown voltage.

Functional and dc parameter testing on CD4000B-series parts is performed at 2.8 V and at 22 V, whereas CD4000A-series devices are tested at 2.8 V and at 17 V. An improved input-protection circuit is being incorporated in all new B-series devices.

Recent data on reliability of 9110 CMOS integrated circuits in satellites are given in Table IV. These data represent a total of over 100 million device-hours of operation of CD4000A-series devices with no failures, corresponding to a failure rate of 0.00092%/1000 hrs at a 60% confidence level.

Qualification test data submitted to the Defense Electronic Supply Center in 1976 for 23 CMOS part types shows excellent reliability (Tables V and VI). Test specifications require that 129 units be tested for 1000 hrs each; one failure is allowed. Only 12 degradational rejects were found in the testing and no inoperative failures were noted, indicating that the parts reliability at 25°C is approaching that of the satellite field data presented in Table IV.

Radiation hardening may allow future CMOS circuits to withstand 10^6 rads (Si).

Ionizing radiation constitutes a specific type of environmental stress that can produce severe degradation in the electrical properties of silicon integrated circuits. Early MOS devices were shown to be sensitive to ionizing radiation. Degradation of MOS devices, for example, was shown to occur at a level as low as 10^3 rads (Si).

Recent studies have generated a considerable amount of information concerning the effect of the thermally-grown oxide purity, growth conditions, and annealing conditions on susceptibility to radiation damage. As a result of these studies, it is now possible to modify the processing conditions to produce CMOS integrated circuits with considerably improved radiation hardness. CMOS ICs guaranteed (by testing) to withstand 1×10^5 rads (Si) are now commercially available with typical devices capable of withstanding 2 to 3×10^5 rads (Si), and with devices capable of withstanding 10^6 rads (Si) in several instances. Continuing research and development in this area is expected to produce further improvements, with production devices specified as capable of withstanding 10^6 rads (Si) a possibility in the near future.

Summary and new product trends

CMOS technology is now maturing to the degree that improved performance and reliability equaling and surpassing that of bipolar devices is a reality. The understanding of the basic failure mechanisms of CMOS devices has led to substantial process and material improvements that either eliminate or minimize the effects of these mechanisms in circuit applications. Improvements in plastic materials and process innovations, such as ion implantation, improved passivation layers, improved metallization, and improved designs are examples of the factors that have increased CMOS reliability.

The introduction of the higher voltage CD4000B-series product with improved electrostatic-discharge protection (equivalent to TTL) is an example of the innovations in CMOS processing that lead to improved reliability in circuit performance, especially as more application experience is gained.

Future CMOS improvements are likely to occur in the area of high-speed devices—for example, in devices employing the silicon-on-sapphire (SOS) technology.

Recent trends in CMOS fabrication technology include improved designs, use of ion implantation, improved photolithography, improved metallization, improved passivation, and the use of improved processes which permit very high chip complexity. Ion implantation provides a high purity, very closely controlled source of dopant atoms which permits tighter distributions of electrical characteristics of transistors (threshold voltages of n-channel and p-channel transistors), and thus improved reliability. High chip complexity makes possible higher gate-to-pin ratios, and thus decreases the probability of failure due to wire bonds, packages, or external interconnections of various types (such as soldered connections in electronic equipment). Moreover, with high-complexity chips, the failure rate per logic gate tends to be lower than that of gates on low-complexity chips. CMOS, because of low dissipation per gate, can be used to fabricate very complex chips without introducing reliability problems which result from excessively high chip temperatures. By contrast, TTL integrated circuits, and to some extent PMOS and NMOS circuits, have problems with power dissipation in large chips.

The above-described advantages, added to high noise immunity and other advantages, have resulted in very wide use of CMOS integrated circuits in electronic systems, with predictions of even wider usage in the next several years.

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Various sources of information on MOS IC reliability were used in the preparation of this article. In addition to the published literature, the sources include manufacturers' brochures, compilations by independent testing laboratories, releases by device users, reports by government agencies, and reports by organizations performing government-supported contracts.

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CMOS/SIS—a planar process that may improve on SOS

C.E. Weitzel

Silicon-on-sapphire technology holds great advantages for integrated circuits, but the silicon-in-sapphire process improves on SOS by allowing higher packing densities.

CMOS/SOS has been heralded as the next step in the evolution of CMOS integrated circuits. CMOS/SOS offers the advantages of CMOS—low power consumption and high noise immunity—along with higher speed and better isolation of SOS. A planar SOS technology, however, is needed to achieve higher packing density with this better isolation.

CMOS/SIS (silicon in sapphire) is distinct from other planar SOS processes in that the silicon islands are imbedded into the sapphire substrate. This is accomplished by creating holes in the sapphire substrate prior to epi growth. The silicon epi is then grown in the standard manner, and the silicon that is not in a hole is polished away. This results in a perfectly planar surface.

The manufacturing process

The first step in the SIS process (Fig. 1) is to define the ion-beam milling mask on a polished sapphire substrate. Since sapphire mills at about one-third the rate of other readily available materials, the mask must be over 2.0 μm thick if 0.6-μm deep holes are to be milled. Deposited SiO_2 and p+ doped polysilicon have been used to define geometries as small as 0.20 mil. At a pressure of 8×10^{-5} torr, an accelerating potential of 900 V and beam current density of 0.60 mA/cm^2, the 0.6-μm-deep holes are milled in 60 minutes. Following the removal of any remaining masking material, the wafers are cleaned and then fired in H_2 at 1200°C for 30 minutes.

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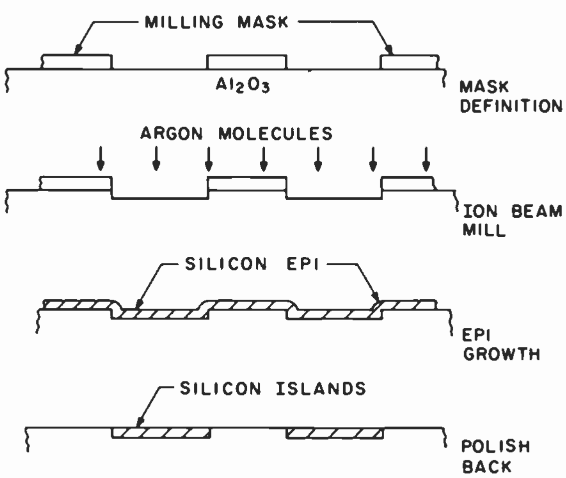

Fig. 1
Four-step process produces silicon islands in the sapphire substrate. From top, mask is placed on substrate, 0.6-micrometer-deep holes are milled out, silicon epitaxial film is grown over the entire substrate, and excess silicon is polished away by diamond.

After the silicon epitaxial film is grown in the standard manner by the pyrolysis of silane, the silicon that is not in the holes is polished away by using 1/4-μm diamond. Presently, this is a hand operation. The sapphire substrate acts as a very good polishing stop because of its hardness and chemical inertness. From this point on, any one of a number of standard SOS processes can be used to fabricate devices. In this work, the p+ polysilicon-gate deep-depletion process was used[1] to manufacture n-channel deep-depletion transistors and p-channel enhancement-mode transistors. Fig. 2 shows a cross-sectional view of an SIS transistor. If the silicon is polished perfectly flat with the surface of the sapphire substrate, the polysilicon gate will encounter a small step in traversing the silicon island because of the difference in density between SiO_2 and silicon.

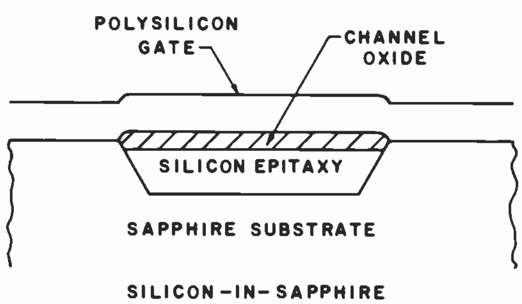

Fig. 2
SIS transistor is made with any standard SOS process, using the final step of Fig. 1 as the starting point.

SIS transistor characteristics

Electrical characterization of CMOS transistors fabricated using the SIS technology indicates that device parameters are almost identical to CMOS/SOS transistors fabricated in the conventional manner. FET mobilities of

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over 450 $cm^2/V\text{-}s$ were measured on n-channel deep-depletion transistors and over 200 $cm^2/V\text{-}s$ on p-channel enhancement-mode devices. The leakage current of fully turned-off devices approaches 100 pA per mil of channel width for a device with a source drain spacing of 0.4 mil at $V_{DS} = 5.0$ V, as shown in Fig. 3. Leakage current at $V_G = 0$ is somewhat higher because of low threshold voltages and parasitic n-channel edge transistors, which have even lower threshold voltages. Edgeless n-channel devices in which the channel region does not include the silicon island edge did not show the higher edge-leakage current. Parasitic edge transistors are also observed in conventionally processed SOS devices.[2] Also, both p-channel and n-channel devices have exhibited no bias-temperature instability problems (Fig. 4). The B-T stressing was done at 250°C for 15 minutes with +10.0 V applied to the n-channel gates and −10.0 V applied to the p-channel gates. In addition to test transistors, a small integrated circuit (71 mils by 79 mils) was fabricated with the SIS technology. At wafer probe, the SIS wafers showed slightly higher yield than the control wafers.

Conclusions

These experimental results indicate that CMOS/SIS offers the advantages of conventional SOS with the addition of a planar surface. It should be possible to translate this planarity into tighter packing density and, at the same time, maintain the excellent isolation offered by an insulating substrate.

Acknowledgments

The author is indebted to Z. Turski, D. Capewell, T. Pawlicki, and L. Barlow for their technical assistance.

References

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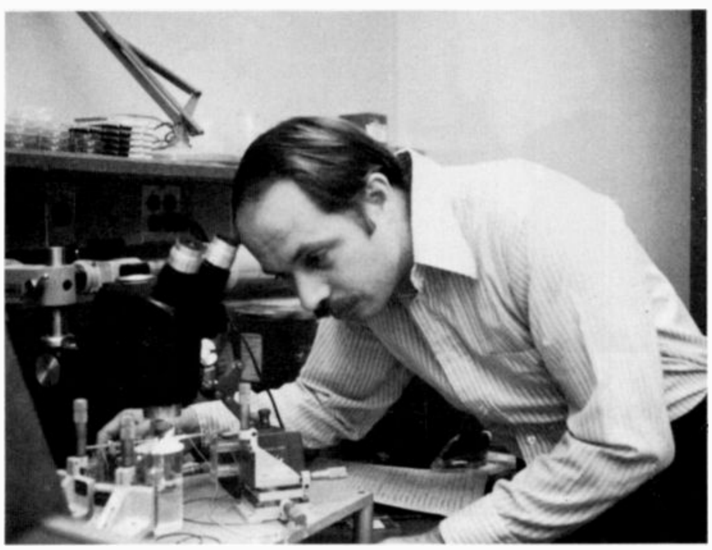
2. Flatley, D.W. and Ham, W.E.; "Electrical instabilities in SOS/MOS transistors," Electrochemical Soc. Fall Meeting, 1974, Abstract #198.

Charles Weitzel joined the Integrated Circuit Process Research group at RCA Laboratories in 1973. He has done research and development in many areas of SOS/MOS transistor processing. However, his main interest has been in studying the effect of sapphire substrate variables on MOS transistor characteristics.

Contact him at: **Integrated Circuit Technology, RCA Laboratories, Princeton, N.J. Ext. 3339**



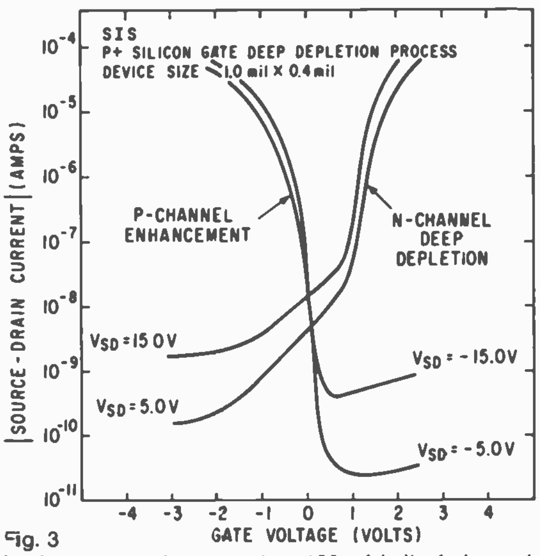


Fig. 3
Leakage current approaches 100 pA/mil of channel width on fully turned-off device. Curves are for p+ silicon-gate deep-depletion process for a 1.0 x 0.4-mil device.

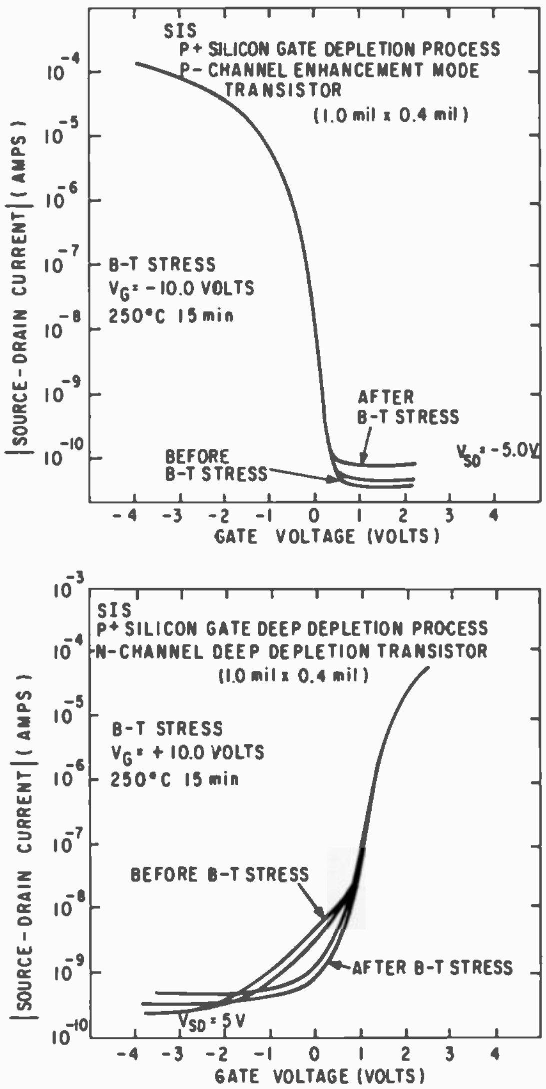


Fig. 4a (top) and 4b
Bias-temperature instability is not a problem with either p-channel (top) or n-channel (bottom) devices.

Model aircraft—a total hobby

R. Lieber

Model aircraft involves the hobbyist in the total cycle—concept, production, competition—thereby generating a sense of personal accomplishment and satisfaction.

In this age of specialization, model aircraft building and flying is a hobby that allows, indeed requires, the individual to be a generalist and assume all of the roles associated with the construction and use of an end product. The hobbyist is at once an entire corporation in miniature, and identity with his product is complete.

The model aircraft movement is at least 50 years old and has a well-developed organization at both the international and national levels. International competition is sponsored along the lines of the Olympic games, while other less formal meetings are carried out at the national and local levels. The organizational structure provides the forum for the free exchange of ideas and, as an important byproduct, an introduction to new friends from diverse walks of life and from many parts of the world.

Categories of model aircraft

Model aircraft fall into three broad categories: 1) free flight; 2) control line; and 3) radio control.

Free-flight models are those over which the modeler has no real-time control.

All basic adjustment of the flight path must be built into the aerodynamics of the model. Final trim to a desired trajectory is accomplished by a series of limited-duration test flights, each followed by small adjustments to the flight surfaces. Free-flight models range from delicate rubber-strand-powered indoor models to rugged engine-powered outdoor aircraft. Within this range is the towline glider, which is towed like a kite to the release altitude, and the hand-launch glider, whose launch motive power is the human arm.

Control-line models fly in a circular path at the end of thin constraining wires.

The wires provide the control link for the modeler, who stands at the center of the flight path. Model classes include replicas that duplicate both the form and flight characteristics of full-scale prototypes, as well as those designed for all-out speed or varying degrees of maneuverability. Models designed for moderate maneuverability perform precisely defined aerobatic patterns, while others proportioned for extreme response are used in a free style of flying in which two aircraft are pitted in a combat-like performance.

The radio-control category allows for the ground control of the model flight with only line-of-sight limitations.

This category includes scale versions of full-scale prototypes in which the details are taken down to the rivet

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Indoor free-flight models are covered with condenser paper or very thin transparent film. The covering gives the structural framework a spider-web appearance. Complete models often weigh less than 1/100 ounce; flight durations as high as 50 minutes have been recorded.

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This engine-powered outdoor model is constructed of balsa wood covered with 1-mil mylar, and weighs 20 ounces. This model has engine thrust greater than model weight, allowing for very fast vertical ascent. Engine runs are limited to 10 seconds by an onboard mechanical timer that cuts off the engine fuel supply and initiates the glide portions of the flight.

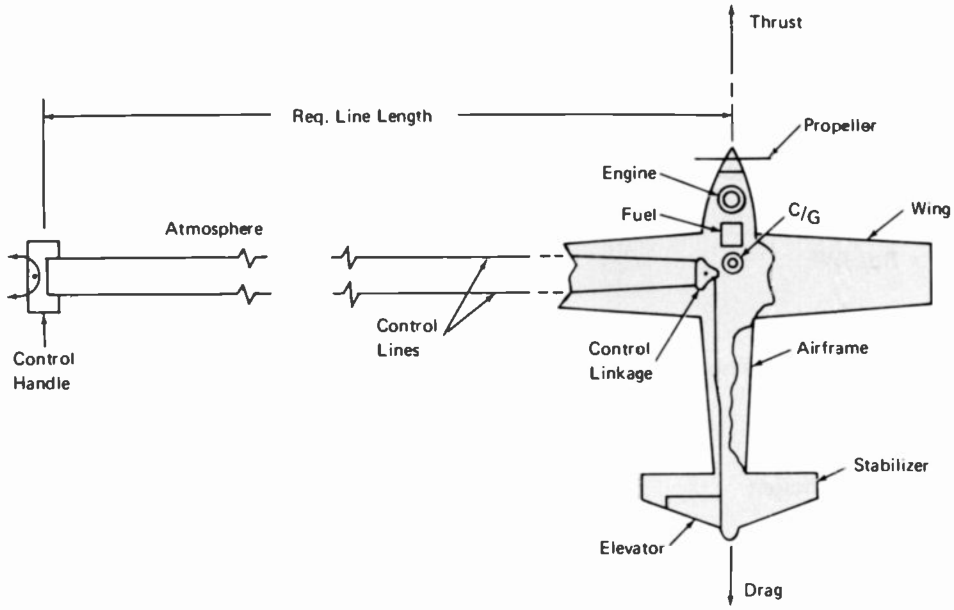

Fig. 1
Control-line system, showing how control lines, through linkage, operate the elevator for altitude control.

heads and weathered paint, as well as aircraft that specialize in precision aerobatics, pylon racing, and both slope and thermal soaring. Although the workmanship requirements in all model categories are high, the radio-control category also places a premium on the ability of the hobbyist as a pilot.

My interest is centered on free-flight power and control-line speed models. To give *RCA Engineer* readers some idea of what's involved in the model aircraft hobby, I would like to describe some of the design considerations and construction techniques that are applied to the all-out speed model.

The control-line speed model

A sketch of the control-line speed model as a system is shown in Fig. 1. The model is controlled in altitude by rotating the control handle. Handle motion is transmitted through the control lines and converted to elevator deflection by means of the control linkage in the airframe. The sensitivity of the model to control motion depends upon the

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Radio-control model scale replica of a two-place 1930's mail plane. It fully matches the original's scale measurements, finish, and interior details. The flight characteristics include realism of speed and control that match the real plane to an astonishing degree.

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Control-line stunt model class is designed for exceptionally smooth response through aerodynamic layout. This model weighs 3 pounds and flies about 50 mi/h. Construction is of balsa, foam, and hardwood, with a final paint finish.

location of the center of gravity, C/G, with respect to the wing and stabilizer, and C/G is chosen to provide a flight path at a desired altitude with a minimum elevator deflection.

In terms of Fig. 1, the speed performance, *V*, of the system is described by Eq. 1.

$$V = K\,[BHP(E)/(AS + BdL)]^{1/3} \qquad (1)$$

where

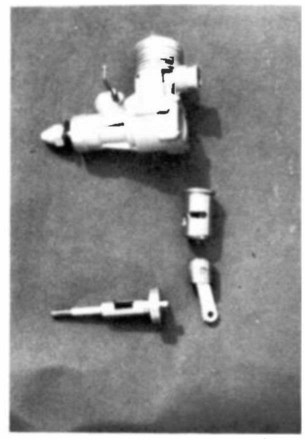
BHP is the engine/fuel system brake horsepower
E is the propeller efficiency
A is the model drag coefficient
S is the wing area
B is the control-line drag coefficient
d is the control-line diameter
L is the uncovered control line length (2 lines)
K is a constant including air density

The goal of the model aircraft hobbyist is to attempt to control the parameters of the performance equation within well-defined competition rules, in order to achieve maximum speed.

The engine

Top engine performance, BHP, is a paramount requirement for speed. Short of having a machine shop, the modeler must carefully purchase an engine by considering manufacturing specification sheets, manufacturer reputation, and any past performance data on the engine in question. After purchase, a break-in period of several hours is required to seat the rotating parts and to establish the piston-to-cylinder fit. A good racing engine with proper fuel system will output 1 BHP at 28,000 r/min. This is equivalent to your 150-cubic-inch Ford engine putting out 1000 BHP!

The racing engine is of two-cycle sleeve-valve design. The essential parts of the power train are shown to emphasize the design simplicity. Fuel is drawn in through the front intake, passed through the crank-shaft, and valved into the combustion chamber by the piston acting to uncover slots in the sleeve. Combustion products are exhausted from the rear by similar piston-sleeve action.



Charles Lieber

The propeller

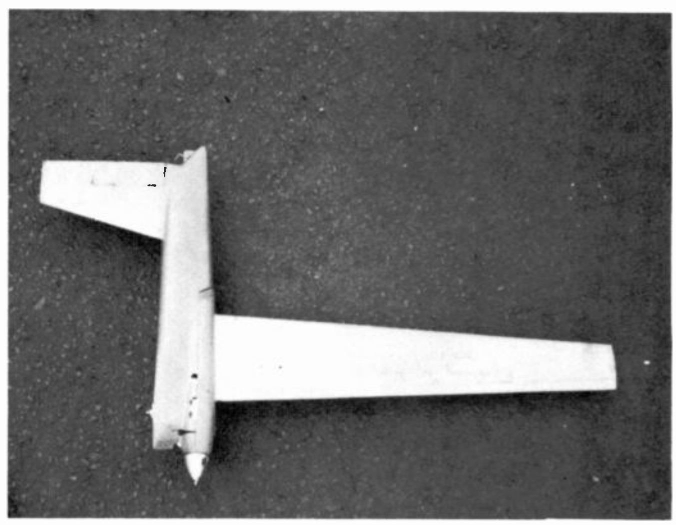
The BHP of the engine must be coupled to the plane through the propeller. The prop must absorb the engine output and convert it to thrust with maximum efficiency at the peak speed of the model. Prop choice is a flight-test procedure, but here the theory of propellers is used to establish the range of test to be carried out. Because of the high r/min operation, the props are molded of special fiber glass or carbon strands impregnated with epoxy.

The airframe

The drag of the model must be minimized while maintaining structural integrity under conditions of high vibration and air load. Structurally, this means that the airframe must have good damping characteristics as well as high tensile strength. Aerodynamically, this leads to enclosure of all operating parts in a smooth shell. Also, parts outboard of the engine thrust line need to be minimized because they are flying at speeds progressively faster than those closer to

Academy of Model Aeronautics

This 5-foot wing span, 7-pound radio-control model is propelled at 100 mi/h through a precision aerobatic pattern by a 2-hp engine. The radio-control system uses feedback position servos in the model to regulate engine speed, retract landing gear, and move at least three independent aerodynamic control surfaces.



Charles Lieber

Control-line model of the international speed class. This model is constructed mainly of fiberglass and magnesium. It weighs 17 ounces ready to fly, and is capable of speeds in excess of 150 mi/h. The asymmetric design results from analysis of drag contributions by the airframe and control lines.

the center of the flight circle, and their drag force is increasing as the square of their speed. This in part leads to the asymmetric shape of the control-line model shown in the photo of the author.

The basic airframe is molded of fiberglass cloth and epoxy. This construction results in a very clean model of minimum wall thickness, yet possessing the required structural properties. The steps in this construction begin with the carving of a form whose outside dimensions are those of the required part. A urethane or silicone material is poured over the form, resulting in a semi-rigid mold that has good dimensional stability, high tolerance of undercuts, and no draft requirements, i.e., parts are easily removed from the mold. Fiberglass cloth, impregnated with epoxy, is then laid up in the mold and allowed to cure. The part is removed from the mold as a complete assembly after the excess material is trimmed.

The control lines

In the class of speed model I am describing, the line diameter and the total line length from the center of the flight circle to the engine thrust line are specified. One might expect that the line drag force would then be fixed. Not so! The drag coefficient, *B*, is a very strong function of the spacing between the lines during flight. This is shown in Fig. 2. Every effort must be made to minimize the line spacing. In addition, the line drag is proportional to the line length uncovered by the model wing. This latter point is another reason for the asymmetrical model shape. Here, within wing structural limits, an attempt is made to streamline the lines by enclosing them within the wing.

Conclusion

After all the theorizing, design, purchasing, construction, engine break-in, test, and competition flying are complete, I look back with a good deal of satisfaction on the labor that resulted in my personal creation. Regardless of whether the results are a success or failure, the important thing is that I can say, "I did the whole thing."

Recommended reading

If you are interested in learning more about model aircraft, write to the Academy of Model Aeronautics, 815 15th Street, N.W., Washington, D.C. 20005. Also, three magazines that cover this hobby are available at newsstands and hobby shops. They are *Model Builder, Model Airplane News*, and *Flying Models*.

Reprint RE-23-1-22
Final manuscript received March 31, 1977.

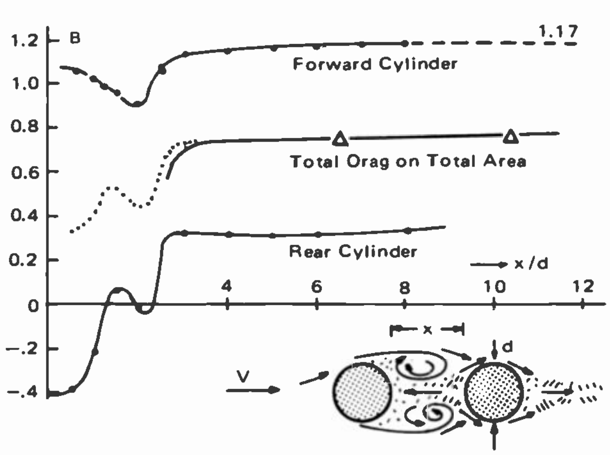
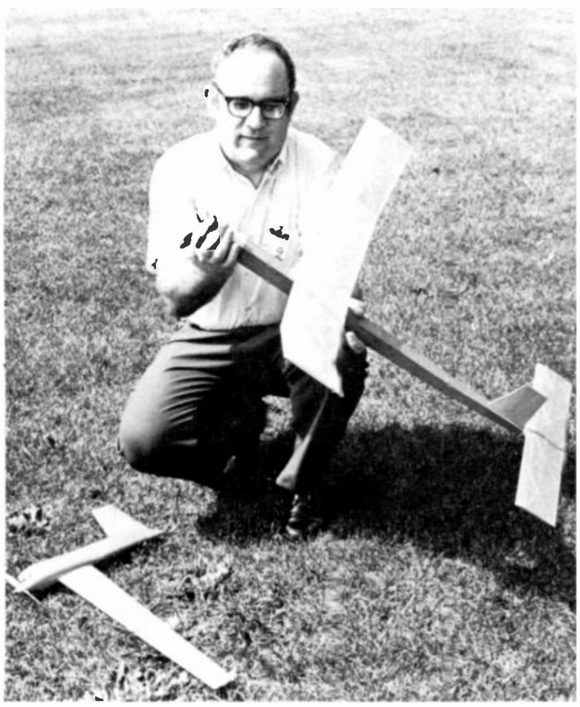


Fig. 2
Drag coefficients of two circular cylinders, one placed behind the other. The graphs show that as the lines get closer and closer, there is a reduction in drag coefficient.



Bob Lieber has been responsible for systems engineering of radar and guidance projects since coming to RCA in 1952. He has written papers in the fields of radar, satellite navigation, and missile guidance systems, and was a recipient of the 1962 David Sarnoff Outstanding Achievement Award. In the field of model aircraft he has contributed papers on speed performance factors and propeller theory. He has been an active aeromodeler since 1938.

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Systems Engineering
Missile and Surface Radar
Moorestown, N.J.
Ext. PM-3035

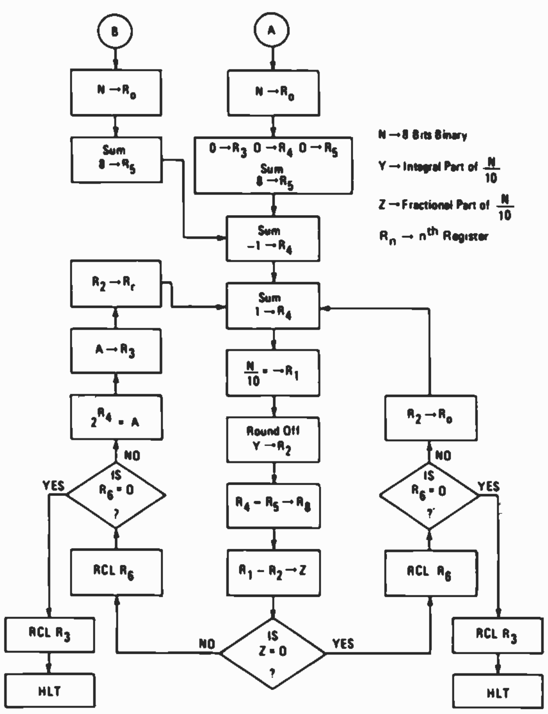
Engineering and Research Notes

Binary-to-decimal conversion program for a programmable calculator

A.R. Campbell
Missile and Surface Radar
Moorestown, N.J.
Ext. PM-2510

Binary-to-decimal number conversion, often needed when working with digital equipment, can require laborious raising to powers and addition. This program, designed for an SR-52 calculator, provides a convenient method of converting 8-, 16-, 24-, and 32-bit words to their decimal equivalents.

To use the program, binary words are entered into the calculator eight bits at a time, most significant bit first. (Since the SR-52 has a 10-digit mantissa, the program ignores the first two digits entered and only operates on the last eight binary digits.) The user then presses the SR-52's user-defined key A, and the program displays the decimal answer.



Reprint RE-23-2-18
Final manuscript received June 8, 1977.

Here's a typical 8-bit conversion:

ignored

1 1 1 1 1 1 0 1 0 1 0 ←—— 1) Enter binary number in display.

8 bits

2) Press A key.

2 3 4 ←—— 3) Calculator displays decimal equivalent.

To obtain 16-, 24-, and 32-bit conversions, do the above operation for the first eight bits, but for each additional eight bits entered, press the user-defined key B, which will sum that 8-bit conversion with all previous conversions, to a maximum of 32 bits.

The conversion algorithm is shown here in flowchart and SR-52 program-listing form. It works by performing repeated divisions by 10, splitting the dividend into integral and fractional parts, and then looking to see if the fractional part is a 1 or 0. If it is a 1, the program raises 2 to appropriate power and sums it into register 03. After the program has looped through eight bits, it recalls register 03 and halts.

Location	*Codes*	*Keys*			
000 - 003	46 11 42 00	*LBL	A	STO	0
004 - 007	00 00 42 00	0	0	STO	0
008 - 011	03 42 00 04	3	STO	0	4
012 - 015	42 00 05 08	STO	0	5	8
016 - 019	44 00 05 01	SUM	0	5	1
020 - 023	94 44 00 04	+/−	SUM	0	4
024 - 027	46 79 01 44	*LBL	*6	1	SUM
028 - 031	00 04 43 00	0	4	RCL	0
032 - 035	00 55 01 00	0	÷	1	0
036 - 039	95 42 00 01	=	STO	0	1
040 - 043	51 78 43 00	SBR	*5	RCL	0
044 - 047	04 75 43 00	4	—	RCL	0
048 - 051	05 95 42 00	5	=	STO	0
052 - 055	06 43 00 01	6	RCL	0	1
056 - 059	75 43 00 02	—	RCL	0	2
060 - 063	95 90 68 43	=	*if0	*8	RCL
064 - 067	00 06 90 67	0	6	*if0	*7
068 - 071	02 45 43 00	2	y^x	RCL	0
072 - 075	04 95 44 00	4	=	SUM	0
076 - 079	03 43 00 02	3	RCL	0	2
080 - 083	42 00 00 41	STO	0	0	GTO
084 - 087	79 46 67 43	*6	*LBL	*7	RCL
088 - 091	00 03 81 46	0	3	HLT	*LBL
092 - 095	68 43 00 06	*8	RCL	0	6
096 - 099	90 67 43 00	*if0	*7	RCL	0
100 - 103	02 42 00 00	2	STO	0	0
104 - 107	41 79 46 78	GTO	*6	*LBL	*5
108 - 111	75 93 05 54	−		5	)
112 - 115	57 00 52 22	*fix	0	EE	INV
116 - 119	52 22 57 42	EE	INV	*fix	STO
120 - 123	00 02 56 46	0	2	*rtn	*LBL
124 - 127	12 42 00 00	B	STO	0	0
128 - 131	41 00 01 05	GTO	0	1	5

COSMAC Applications Contest Winners

First place:

John Kowalchik
Solid State Division
Mountaintop, Pa.

A *COSMAC-based autopatch control for amateur repeaters*
First prize is a COSMAC Evaluation Kit and Microterminal.

Second place:

Thomas Lenihan
RCA Laboratories
Princeton, N.J.

A/D-based burglar alarm system
Second prize is a COSMAC Evaluation Kit.

Third place:

Victor Auerbach
Astro-Electronics
Princeton, N.J.

COSMAC Microtooter

Vince Battaglia
Mobile Communications Systems
Meadow Lands, Pa.

COSMAC-controlled battery-charger/efficiency-tester

Leonard Borkon
Solid State Division
Lancaster, Pa.

Microprocessor control of a CB radio antenna to minimize VSWR

Third prize is a choice of a Microtutor or a COSMAC VIP.

Future issues of the *Engineer* will have descriptions of the winning entries. Valid entries were also received from:

David Costello
Missile and Surface Radar
Moorestown, N.J.

Programmable audio waveform generator

Miguel Negri
NBC
New York, N.Y.

Remote control of NBC facilities

Frank Panzarino
Globcom
New York, N.Y.

Oscilloscope generator cartridge

Mark Riggle
Missile and Surface Radar
Kwajalein, Marshall Is.

Music synthesizer system

Patents

Automated Systems

R. Depierre| G.J. Forgays
H.H. Behling| W.C. Curtis
Airborne moving-target indicating radar system—4034373

R.C. Guyer
Optical adjustment device—4037942 (Assigned to U.S. Government.)

W.J. Hannan
Adaptor for inter-relating an external audio input device with a standard television receiver and an audio recording for use therewith—4040088

R.E. Hanson
Method for determining engine monent of inertia—4036049 (Assigned to U.S. Government.)

L.R. Hulls| S.C. Hadden
Filter which tracks changing frequency of input signal—4032852

J.A. McNamee
Vibrometer—4041775 (Assigned to U.S. Government.)

Avionics

C.A. Clark, Jr.
High voltage protection circuit—4041357

C.A. Clark, Jr.| R.A. Ito
Radar contour edge restore circuit—4038655

M.I. Hussain
Pulse stream identification circuit—4041486

Broadcast

L.J. Bazin
Apparatus for automatic gamma control of television color signals—4038685

D.M. Schneider| L.J. Bazin
Video blanking circuit—4038687

L.J. Thorpe| B.E. Nicholson
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Defect detection and compensation—4038686

E.W. Christensen, 2nd| J.K. Kratz
Beam adjustment assembly for a cathode ray tube—4032872

L.A. Harwood
Chroma-burst separator and amplifier—4038681

L.A. Harwood
Complementary field effect transistor signal multiplier—4032967

M.L. Henley| L.E. Smith
Raster centering circuit—4032819

M.N. Norman
Brightness control apparatus—4044375

Distributor and Special Products Div.

F.R. Dimeo| W.J. Bachman
Insulator for an antenna—D244866

Government Systems Division Staff

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Method of preparing portions of a semiconductor wafer surface for further processing—4035226

Laboratories

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Television signal processing apparatus including a transversal equalizer—4041531

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Electro-optic device—4032340

A. Bloom| D.L. Ross
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A. Bloom| R.A. Bartolini| H.A. Weakliem
Method of improving the sensitivity of organic volume-phase holographic recording media—4032340

C.J. Busanovich| R.M. Moore
Method of forming and treating cadmium selenide photoconductive bodies—4034127

J.E. Carnes
Smear reduction in CCD imagers—4040092

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Electron mulitplier with beam confinement structure—4041342

C.A. Catanese| J.A. Rajchman| J.G. Endriz
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Avalanche transistor operating above breakdown—4041515

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J.J. DiPiazza
High-resolution fluorescent screen and methods of making and using the same—4039838

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Circuit for elimination of surface charge integration—4038581

I. Drukier| E. Mykietyn
Interconnection means for an array of majority carrier microwave devices—4034399 (Assigned to U.S. Government.)

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Temperature-stable non-magnetic alloy—4042382

A.H. Firester
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R.A. Grange
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J. Guarrachini
Disc master positioning apparatus for a recording system—4040089

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H. Kawamoto
Four-layer trapatt diode and method for making same—4038106 (Assigned to U.S. Government.)

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L.S. Napoli| R.R. Marx
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J.B. Halter
Method and apparatus for electromechanical recording of short wavelength modulation in a metal master—4044379

A.F. McDonie
Electron emitter including porous antimony—4039887

G.I. Morton| R.C. Huener
Reduction of parasitic bipolar effects in integrated circuits employing insulated gate field effect transistors via the use of low resistance substrate contacts extending through source region—4035822

O.H. Schade, Jr.
Capacitance memories operated with intermittently-energized integrated circuits—4034239

O.H. Schade, Jr.
Complementary field effect transistor amplifier—4038607

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L.F. Heckman, Jr.| J.B. Pickard
High power coaxial cavity resonator tunable over a broad band of frequencies—4034320

V.E. Hills| L. Wu
Selectively powered flip-flop—4042841

M.V. Hoover
Complementary symmetry FET mixer circuits—4032851

T.W. Kisor
Package for semiconductor components—4037267

Special Contracts

E.M. Ball
Vacuum tube gas test apparatus—4038616

Pen and Podium

Recent RCA technical papers and presentations

To obtain copies of papers, check your library or contact the author or his divisional Technical Publications Administrator (listed on back cover) for a reprint. For additional assistance in locating RCA technical literature, contact RCA Technical Communications, Bldg. 204-2, Cherry Hill, N.J., extension PY-4256.

Automated Systems

D.R. Bartlett
New-technology ATE in support of the YAH-64 advanced attack helicopter—AIAA, Orlando, FL (7/11-13/77)

M.J. Cantella
Application of the high-resolution return-beam vidicon—*Optical Engineer* (5-6/77)

R.F. Gerenz
A methodology for improving the strategic warning process—*J. of Defense,* Special Crises Management Issue (5/77)

R.F. Gerenz
Data fusion—Electronics in NORAD Symp., Air Force Academy, Colorado Springs, CO (9/13-14/77)

J.J. Klein
A high performance tv camera for multiplexing of parallel FLIR video—IRIS-25th National Infrared Information Symp., San Francisco, CA (6/15/77)

F.P. McGurk|R.A. Asmussen
Novel production engineering techniques used on the AN/GVS-5 hand held laser rangefinder—Advances in Laser Engineering Seminar, SPIE, Hughes Aircraft, Culver City, CA (8/26/77)

D.A. Priestley
New-technology automatic test system simplified interface with ARTADS—AFCEA Seminar, Ft. Monmouth, NJ (9/15/77)

N.B. Wamsley
Infrared techniques automate diagnostic test generation process—20th Midwest Symp. on Circuits and Systems, Lubbock, TX (8/15-16/77)

Government Communications Systems

G.J. Brucker
Transient test of a CMOS bulk microprocessor—IEEE Nuclear & Space Radiation Effects, Williamsburg, VA (7/12/77)

G.J. Brucker
Circumvention and interaction of CMOS/bulk peripherals with CMOS/SOS memory in transient environment—IEEE Nuclear & Space Radiation Effects, Williamsburg, VA (7/12/77)

G.J. Brucker
Characteristics of CMOS/bulk and SOS memories in a transient environment—IEEE Nuclear & Space Radiation Effects, Williamsburg, VA (7/12/77)

Dates and Deadlines

Upcoming meetings

Ed. Note: Meetings are listed chronologically. Listed after the meeting title (in bold type) are the sponsor(s), the location, and the person to contact for more information.

OCT 16-21, 1977—**119th Technical Conf. and Equipment Exhibit** (SMPTE) Century-Plaza Hotel, Los Angeles, CA **Prog Info:** SMPTE, 862 Scarsdale Ave., Scarsdale, NY 10583

OCT 25-27, 1977—**Electro-Optics/Laser '77 Conf. and Expo.,** Anaheim, CA **Prog Info:** Bill Ashman, Industrial & Scientific Conference Management, Inc., 222 W. Adams St., Chicago, IL 60606

OCT 25-27, 1977—**Semiconductor Test Symp.** (IEEE) Hyatt House, Cherry Hill, NJ **Prog Info:** John A. Bauer, Test Symp., PO Box 2340, Cherry Hill, NJ 08034

OCT 25-28, 1977—**Radar Intl.-RADAR 77** (IEEE *et al*) IEE, London, England **Prog Info:** IEE, Conf. Dept., Savoy Place, London, WC2R OBL England

OCT 26-28, 1977—**Ultrasonics Symp.** (IEEE) Del Webb's Towne House, Phoenix, AZ **Prog Info:** Fred S. Hickernell, Motorola, Inc., 8201 E. McDowell, Scottsdale, AZ 85252

OCT 31-Nov 1, 1977—**Joint Engineering Mgmt. Conf.** (IEEE *et al*) Stouffer's Inn, Cincinnati, OH **Prog Info:** Paul H. Bluestein, Paul H. Bluestein & Co., 3420 Section Rd., Cincinnati, OH 45237

NOV 2-4, 1977—**Automatic Support Systems for Advanced Maintainability (AUTOTESTCON)** (IEEE) Dunfey's Hyannis on Cape Cod, MA **Prog Info:** E.B. Galton, AUTOTESTCON 77 c/o RCA, PO Box 588, Burlington, MA 01801

NOV 6-10, 1977—**Engineering in Medicine and Biology Conf.** (IEEE) Hilton, Los Angeles, CA **Prog Info:** AEMB, Suite 404, 4405 East-West Hwy., Bethesda, MD 20014

NOV 8-10, 1977—**Mechanical Engineering in Radar** (IEEE) Sheraton Natl., Washington, DC **Prog Info:** Harry C. Moses, Naval Research Lab., Code 5307, 4555 Overlook Ave., Washington, DC 20375

NOV 8-10, 1977—**MIDCON** (IEEE) O'Hare Conv. Ctr., Hyatt Regency, Chicago, IL **Prog Info:** W.C. Weber, Jr., EEEI, 999 N. Sepulveda Blvd., El Segundo, CA 90245

NOV 8-11, 1977—**COMPSAC '77 (Computer Software & App. Conf.)** (IEEE) Sheraton-O'Hare, Chicago, IL **Prog Info:** Stephen S. Yau, Dept. Computer Sci., Northwestern Univ., Evanston, IL 60201

NOV 8-11, 1977—**Magnetism & Magnetic Materials Conf.** (IEEE) Raddison Hotel, Minneapolis, MN **Prog Info:** C.D. Graham, Jr., Univ. of Penn., Dept. of Metallurgy and Matls. Sci., Phila., PA 19174

NOV 13-17, 1977—**NAEB Convention,** Washington, DC **Prog Info:** James A. Fellows, NAEB, 1346 Connecticut Ave., N.W., Washington, DC 20036

NOV 14-16, 1977—**Second Annual Intl. Videodisc Programming Conf.** (IVDC) New York, NY **Prog Info:** IVDC, PO Box 102, Cooper Sta., New York, NY 10003

NOV 27-DEC 2, 1977—**ASME Winter Annual Mtg.** (ASME) Hyatt Regency, Atlanta Hilton, Atlanta, GA **Prog Info:** ASME, 345 E. 47th St., New York, NY 10017.

M. Nguyen| R. Pickholtz
Bounds for the queue in loop system—Computer Performance Modeling Symp., New York, NY (8/16/77)

Missile and Surface Radar

R.D. Bachinsky
Fragment wake modeling—AIAA/BMDSC, Stanford Research Institute, Menlo Park, CA (7/26-27/77)

M.W. Buckley
Project management—Co-Chairman, AMA Seminar, Montreal, Que. (6/8-9/77)

J.O. Neilson| W.J. Paterson| G.W. Suhy
Simulations for sizing large radar control computers—Modeling and Simulation Conf., U. of Pittsburgh, Pittsburgh, PA (4/22/77)

N. Rosenfeld
Development of microprocessors and microprocessor-based systems using an off-the-shelf microcomputer—IEEE workshop in microprocessors, U. of Penna., Phila. PA (6/10-12/77)

H. Urkowitz
Clarity in windows—*IEEE Spectrum*, Letter to the editor (7/77)

L. H. Yorinks
Large feed displacements in an offset reflector antenna—1977 Intl. IEEE/AP-S Symp. (6/21-24/77)

Laboratories

D.A. de Wolf
Optical coherence through turbid media—OSA Topical Mtg. on Optical Propagation through Turbulence, Rain, and Fog, Boulder, CO (8/9-11/77)

D.A. de Wolf
Light beams in turbulent air: diagram techniques—OSA Topical Mtg. on Optical Propagation through Turbulence, Rain, and Fog, Boulder, CO (8/9-11/77)

A.H. Firester| M.E. Heller| P. Sheng
Knife-edge scanning measurements of subwavelength focused light beams—*Appl. Optics*, Vol. 16 No. 7 (7/77) pp. 1971-74

W. Kern
Chemical etching of dielectrics—Electrochem. Soc. Symp. on Etching, Washington, DC (5/76). Also in "Etching for Pattern Definition," Electrochem Soc. (1976) pp. 1-18d

T. Takahashi| O. Yamada
Cathodoluminescent properties of yttrium aluminum borate—*J. Electrochem. Soc.*, Vol. 124 No. 6 (6/77) pp. 955-58

J.P. Wittke| I. Ladany
Lateral mode selection in semiconductor injection lasers—*J. Appl. Physics*. Vol. 48 No. 7 (7/77) pp. 3122-24

C.R. Wronski
Photovoltaic properties of discharge-produced amorphous Si—*Technical Digest*, 9th Solid State Devices Conf., Tokyo, Japan (8/30-31/77)

C.R. Wronski| D.E. Carlson
Surface states and barrier heights of metal amorphous silicon Schottky barriers—*Solid State Communications*, Vol. 23 (9/77) p. 421

DEC 1-3, 1977—**Semiconductor Interface Specialist Conf.** (IEEE) Carillon Hotel, Miami Beach, FL **Prog Info:** W.R. Hunter, IBM, Thomas Watson Res. Ctr., PO Box 218, Yorktown Hts., NY 10598

DEC 5-6, 1977—**Chicago Fall Conf. on Consumer Electronics** (IEEE) Ramada-O'Hare Inn, Des Plains, IL **Prog Info:** Richard Sudges, Rockwell Intl./The Admiral Group, 1925 N. Springfield Ave., Chicago, IL 60647

DEC 5-7, 1977—**Intl. Electron Devices Mtg.** (IEEE) Hilton, Washington, DC **Prog Info:** Courtesy Assoc./Susan Herman, 1629 "K" St., N.W., Washington, DC

DEC 5-7, 1977—**Natl. Telecommunications Conf.** (IEEE) Marriott Hotel, Los Angeles, CA **Prog Info:** Stanley A. Butman, 4800 Oak Grove Dr., Pasadena, CA 91103

JAN 16-18, 1978—**Integrated and Guided Wave Optics** (OSA) Salt Lake City, UT **Prog Info:** Optical Soc. of Am., 2000 L St., N.W., Washington, DC 20036

JAN 24-26, 1978—**Reliability & Maintainability Conf.** (IEEE *et al*) Biltmore, Los Angeles, CA **Prog Info:** D.F. Barber, POB 1401, Branch PO, Griffiss AFB, NY 13441

JAN 30-FEB 1, 1978—**Automated Testing for Electronics Manufacturing**, Marriott, Los Angeles, CA **Prog Info:** Sheila Goggin, ATE Seminar/Exhibit, 167 Corey Rd., Brookline, MA 02146

FEB 7-9, 1978—**Conf. on Laser and Electro-Optical Systems** (OSA) Town and Country Hotel, San Diego, CA **Prog Info:** Optical Soc. of Am., 2000 L St., N.W., Washington, DC 20036

FEB 15-17, 1978—**Intl. Solid State Circuits Conf.** (IEEE, U. of Penna.) Hilton, San Francisco, CA

MAR 21-23, 1978—**Industrial Applications of Microprocessors**, Sheraton, Phila., PA **Prog Info:** W.W. Koepsel, Dept. of E.E., Seaton Hall, Kansas State Univ., Manhattan, KS 66506

Calls for papers

Ed. Note: Calls are listed chronologically by meeting date. Listed after the meeting (in bold type) are the sponsor(s), the location, and deadline information for submittals.

JAN 16-18, 1978—**Integrated & Guided Wave Optics** (OSA) Salt Lake Hilton, Salt Lake City, UT **Deadline Info: 10/20/77** to Amnon Yariv, Cal. Inst. of Tech., Pasadena, CA 91109

MAR 22-24, 1978—**Vehicular Technology Conf.** (IEEE) Regency, Denver, CO **Deadline Info: 10/15/77 to** John J. Tary, U.S. Dept. of Commerce, OT/ITS, 325 Broadway, Boulder, CO 80302

APR 24-26, 1978—**Electronic Components Conf.** (IEEE) Disneyland, Anaheim, CA **Deadline Info: 10/28/77 to** John Powers, Jr., IBM Corp. Hdqtrs, Dept. 836 IB, 43 Old Orchard Rd., Armonk, NY 10504

MAY 6-11, 1978—**American Ceramic Soc. 80th Annual Mtg., Electronics Div.** (ACS) Cobo Hall, Detroit, MI **Deadline Info: (Title and author) 11/15/77; (50-wd ab) 12/1/77 to** Henry M. O'Bryan, Bell Laboratories 6D-307, 600 Mountain Ave., Murray Hill, NJ 07974

MAY 9-12, 1978—**Intl. Magnetics Conf.** (Intermag) Florence, Italy **Deadline Info: (2-pg digest) 12/15/77 to** David A. Thompson, IBM, Thomas J. Watson Research Ctr., PO Box 218, Yorktown Heights, NY 10598

JUN 26-29, 1978—**Conf. on Precision Electromagnetic Measurements** Conf. Ctr., Ottawa, Ont. **Deadline Info: (ab) 1/15/78 to** Andrew F. Dunn, Natl. Research Council, Montreal Rd., Ottawa, Ont. KIN6N5

JUL 16-21, 1978—**Power Engineering Soc. Summer Meeting** (IEEE) Los Angeles, CA **Deadline Info: 2/1//78 to** G.A. Davis, Southern Calif. Edison Co., POB 800, Rosemead, CA 91770

Engineering News and Highlights

Hillier honored by Electron Microscopy Society

Dr. James Hillier, Executive Vice President and Senior Scientist, received the Electron Microscopy Society of America's Distinguished Award for his pioneering efforts in the development of early electron optical instrumentation on the North American continent. The award was presented to him at the EMSA's Awards Luncheon in Boston on August 24, 1977.

Dr. Hillier is well known in the field of electron microscopy and for his role in encouraging the growth of this instrument as a research technique of wide importance in biology, medicine, chemistry and other sciences.

Between 1937 and 1940, while a research assistant at the University of Toronto's Department of Physics and at the Banting Institute of the University's medical school, he and a colleague, Albert Prebus, designed and built the first successful high-resolution electron microscope in the Western Hemisphere.

New Products Laboratory formed

William M. Webster, Vice President, RCA Laboratories, and **D. Joseph Donahue,** Division Vice President, Operations, Consumer Electronics Division, recently made a joint announcement of the formation of a New Products Laboratory. Its purpose will be to facilitate the planning, project identification and the timely development of new products.

Jay J. Brandinger, Division Vice President, Engineering, Consumer Electronics Division, appointed **J. Peter Bingham** Chief Engineer of the New Products Laboratory.

This Laboratory will be responsible for introducing improvements into the current product line and for developing new electronics products. The New Products Laboratory will interface with RCA Laboratories as technical feasibility of new ideas is established and with the Consumer Electronics Product Design activity when economic and market feasibility have been determined. The function having this responsibility was formerly located at RCA Laboratories. It will now be centered in Indianapolis.

The Consumer Products Research effort will continue at the RCA Laboratories in Princeton and will interface with the New Products Laboratory.

To the Editors:

Because of the review nature of my article, [U.S. color television fundamentals," *RCA Engineer*, Vol. 23 No. 1, pp. 64-75], I obviously had to draw upon information originating from a very large group of individuals who contributed to the development of the NTSC Color Television System. I thereby express my thanks and appreciation to all concerned.

Accordingly, an additional reference inadvertently not cited, useful to those interested in more information regarding this topic may be found in the book by John Wentworth, entitled *Color Television Engineering*, McGraw Hill, 1955. It contains much of the early background material used as a basis for the review article.

D.H. Pritchard

Promotions

Solid State Division

Joseph Banfield from Member, Technical Staff to Leader, Technical Staff, Metallurgical Technology group of the Materials and Processes Laboratory.

Missile and Surface Radar

Katharine Purdum from Senior Member, Engineering Staff to Member, Project Management Staff, AEGIS Computer Programs.

Charles Profera from Principal Member, Engineering Staff to Staff Administrator, IR&D Programs, Systems and Advanced Technology.

Staff announcements

Solid State Division

Thomas T. Lewis, Director, Electro-Optics Operations, announced the organization as follows: **Clarence H. Groah,** Manager, E/O Operations, Administration and Product Control; **Leonard W. Grove,** Manager, Manufacturing—E/O; **David L. Brubaker,** Manager, Manufacturing—Special Parts; **Leonard W. Grove,** Acting, Production Control; **William H. Hackman,** Manager, CAT Scanner; **Richard J. Miller,** Manager, E/O Fabrication; **Richard Phillips,** Manager, Photo Engineering; **Donald C. Reed,** Manager, Custom Tube Manufacturing; **Kenneth A. Thomas,** Manager, Finishing; **Fred A. Helvy,** Manager, E/O Engineering; **Ralph W. Engstrom,** Senior Member, Technical Staff; **Fred A. Helvy,** Acting, Applications Engineering—E/O; **Fred A. Helvy,** Acting, Process and Material Development; **Daniel L. Thoman,** Manager, Product Development; **Thomas T. Lewis,** Acting, Product Marketing; **Thaddeus J. Grabowski,** Manager, Market Planning; **N. Richard Hangen,** Manager, Market Planning; **Edward F. McDonough,** Manager, Market Planning; **Carlton L. Rintz,** Manager, Market Planning; **Ronald G. Power,** Manager, Solid State Detectors—Canada; **Eugene D. Savoye,** Manager, E/O Solid State Technology; **Thomas W.**

Edwards, Leader, Silicon Engineering; **William H. Henry,** Manager, Silicon Manufacturing; and **Fred R. Hughes,** Manager, Solid State Emitters.

Philip R. Thomas, Division Vice President, Solid State MOS Integrated Circuits, announed the organization as follows: **Gerald K. Beckmann,** Manager, Operations Planning and Administration; **John A. Ekiss,** Director, MOS Manufacturing Operations; **Peter J. Jones,** Director, Product Marketing, MOS; **John P. McCarthy,** Manager, MOS Special Programs; **Norman C. Turner,** Director, MOS Engineering; and **Robert O. Winder,** Director, MOS Systems.

John A. Ekiss, Director, MOS Manufacturing Operations, appointed **David S. Jacobson** Manager, Photomask Operations.

Commercial Communications Systems Division

Joseph P. Ulasewicz, Division Vice President and General Manager, appointed **Donald L. Neff** Manager, Operations Control, Mobile Communications Systems, Meadow Lands, Pa.

Research and Engineering

Howard Rosenthal, Staff Vice President, Engineering, appointed **John D. Bowker** Manager, RCA Frequency Bureau.

John D. Bowker, Manager, RCA Frequency Bureau, announced the organization as follows: **Norman B. Mills,** Manager, New York Office Frequency Bureau; and **Edward E. Thomas,** Manager, Washington Office Frequency Bureau.

RCA Laboratories

James L. Miller, Director, Manufacturing Systems and Technology Research Laboratory, announced the organization as follows: **Istvan Gorog,** Head, Optical Electronics and Process Control Research; **Marvin A. Leedom,** Head, Mechanical and Instrumentation Technology; **James L. Miller,** Acting Head, Manufacturing Systems; and **D. Alex Ross,** Staff Engineer.

Fred Sterzer, Director, Microwave Technology Center, appointed **Ho-Chung Huang** Head, Microwave Processing Technology Research.

Marvin A. Leedom, Head, Mechanical and Instrumentation Technology, appointed **William G. McGuffin** Manager, Instrumentation.

David D. Holmes, Director, Television Research Laboratory, appointed **Ronald L. Hess** Head, Deflection and Power Supply Systems Research; **Stanley P. Knight** Head, Signal Conversion Systems Research; and **Robert M. Rast** Head, Systems Technology Research.

Nathan L. Gordon, Staff Vice President, Systems Research, appointed **Paul M. Russo** Head, TV Microsystems Research.

Government Systems Division

James Vollmer, Division Vice President and General Manager, appointed **Paul E. Wright** Division Vice President, Engineering.

Patent Operations

Harold Christoffersen, Director, Solid State and Electronic Systems, announced that **Donald S. Cohen,** Managing Patent Attorney, will assume the responsibility for Solid State Device and Processing Activities.

Consumer Electronics Division

Jay J. Brandinger, Division Vice President, Engineering, announced the organization as follows: **J. Peter Bingham,** Chief Engineer, New Products Laboratory; **J. Peter Bingham,** Acting Manager, Signal Systems and Components; **Cortland P. Hill,** Manager, Product Design and Test Technology; and **Eugene Lemke,** Manager, Display Systems.

Edmund W. Riedweg, Plant Manager, Bloomington, appointed **John M. Wright** Manager, Technical Coordination.

Obituaries

Charles M. Odorizzi, a retired Executive Vice President of RCA, died August 23. He was appointed to the staff of the President in 1969 and served on the staff of the Chairman of the Board until his retirement in 1973. Mr. Odorizzi served as a member of the RCA Board of Directors from 1957–1974.

Prior to joining RCA in 1949 as Vice President in charge of service for the RCA Victor Division, he held several top management positions outside the company. He became Senior Executive Vice President, Services, in 1968, with responsibility for over-all supervision of RCA Global Communications, Inc., RCA Service Company, Parts and Accessories, and The Hertz Corporation. At other times during his career he had responsibility for RCA Victor Record Division, RCA International Division, the Broadcast and Communications Products Division, Corporate Licensing activities, and RCA Magnetic Products Division.

Henry P. Lemaire, formerly Chief Engineer of Memory Products Division, Needham, Mass., died recently. He joined RCA in 1959 and after a brief time was in charge of Advanced Development for the Memory Products Division where he supervised the development of ferrites for new applications, high-temperature ferrites, and high-speed memories. Mr. Lemaire remained with that division when it was sold to Digital Equipment Corporation in 1972. He later became vice president, component manufacturing and engineering.

Recent books by RCA authors

Kleinberg

Blicher

How You Can Learn to Live with Computers

Harry Kleinberg
Published by J.B. Lippincott Company

The following description appears on the inside flap of Harry Kleinberg's book. Harry, Manager of Corporate Standards Engineering, Cherry Hill, N.J., and a former computer engineer, also has an article in this issue of the *RCA Engineer*, pages 44-46.

"You don't have to have a private lab at M.I.T. to understand the basics of the computer, according to computer expert Harry Kleinberg. Written in clear, jargon-free language for the layman, *How You Can Learn to Live with Computers* dispels the many myths and fears that surround computers and explains the remarkably simple principles on which they operate.

For some, the computer heralds a new age of liberation, where mental drudgery will be as outmoded as physical labor and social decisions will be made with speed and correctness. For others, it foreshadows an Orwellian world where humanity's every action and thought will be controlled by the Machine.

Harry Kleinberg argues that neither vision is true, and traces his own long acquaintance with this amazingly versatile invention to illustrate exactly what the computer can and cannot do. You may be surprised to learn that computers don't solve problems, make decisions, or think; that words like "intelligence" and "memory" assume entirely different meanings when applied to the computer; and that a computer possesses no oracular power beyond the limitations of the person who programs it. For anyone who fears that a computer may someday claim his job, *How You Can Learn to Live with Computers* tells you just how much of your work a computer might be expected to perform.

Humorous, sensible, insightful, *How You Can Learn to Live with Computers* presents both the comic and the serious sides of the machine—and concludes that it will indeed revolutionize your life, but in ways that you may not expect."

Thyristor Physics

Adolph Blicher
Published by Springer-Verlag

Thyristor Physics presents concisely the physical principles underlying the operation and performance characteristics of the class of p-n-p semiconductor switch known as the thyristor. The book is directed to semiconductor-device physicists and designers, students, and those electronic-circuit designers who wish to apply thyristors creatively without the limitation of considering them only as "black boxes." The book endeavors to present an up-to-date account of the advances in understanding the operation, potentialities, and limitations of thyristors as switching-circuit elements.

Following an introduction to basic device theory, the author discusses the static and dynamic properties of silicon controlled rectifiers, triacs, gate-turn-off thyristors, and reverse-conductivity thyristors. The final chapter of the book is devoted to thyristor-circuit basics.

This volume is the first in the English language devoted almost entirely to thyristor physics.

Dr. Adolph Blicher was manager, Advanced Devices and Applications, of the Solid State Technology Center, RCA Laboratories, Somerville, N.J. at the time of his retirement in 1972. He joined RCA Solid State Division, Somerville, N.J. in 1955 and was in charge, over a period of years, of the development of a very great variety of semiconductor devices such as low- and high-frequency transistors, thyristors, integrated circuits, solar cells, varactor and tunnel diodes, vidicon targets, light emitting diodes, etc.

Licensed engineers

When you receive a professional license, send your name, PE number (and state in which registered), RCA division, location, and telephone number to: *RCA Engineer*, Bldg. 204-2, RCA, Cherry Hill, N.J. New Listings (and corrections or changes to previous listings) will be published in each issue.

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William D. Lauffer, Jr., Cherry Hill, N.J.; Del.-5243.

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