ALPHA & OMEGA SEMICONDUCTOR

Power MOSFET Basics

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1. Basic Device Structure

Power MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) are the most commonly used power devices due to their low gate drive power, fast switching speed and superior paralleling capability. Most power MOSFETs feature a vertical structure with Source and Drain on opposite sides of the wafer in order to support higher current and voltage. Figure 1a and 1b show the basic device structures of Trench and Planar MOSFETs respectively. Trench MOSFETs are mainly used for <200V voltage rating due to their higher channel density and thus lower on-resistance. Planar MOSFETs are good for higher voltage ratings since on-resistance is dominated by epi-layer resistance and high cell density is not beneficial. The basic MOSFET operation is the same for both structures. Unless specified, the N-channel trench MOSFET is discussed in this application note.

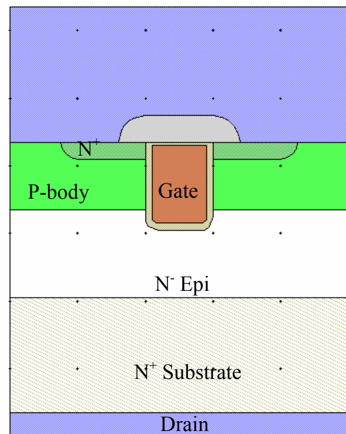

Figure 1a: Trench MOSFET Structure

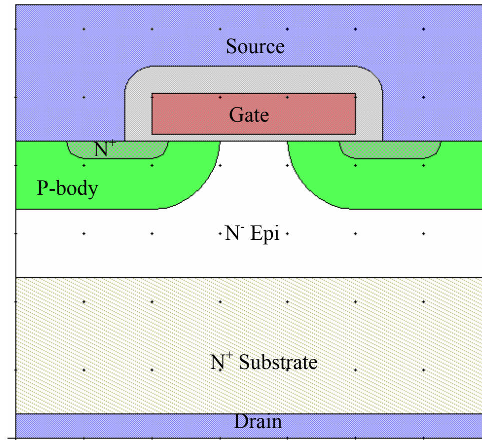

Figure 1b: Planar MOSFET Structure

2. Breakdown Voltage

In most power MOSFETs the N^+ source and P-body junction are shorted through source metallization to avoid accidental turn-on of the parasitic bipolar transistor. When no bias is applied to the Gate, the Power MOSFET is capable of supporting a high Drain voltage through the reverse-biased P-body and N^- Epi junction. In high voltage devices, most of the applied voltage is supported by the lightly doped Epi layer. A thicker and more lightly doped Epi supports higher breakdown voltage but with increased on-resistance. In lower voltage devices, the P-body doping becomes comparable to the N^- Epi layer and supports part of the applied voltage. If the P-body is not designed thick or heavy enough, the depletion region can punch-through to the N^+ source region and cause lower breakdown. But if it is over designed, the channel resistance and threshold voltage will also increase. So careful design of the body and Epi doping and thickness is needed to optimize the performance.

In the datasheet, BV_{DSS} is usually defined as the drain to source voltage when leakage current is 250uA. The leakage current flowing between source and drain is denoted by I_{DSS}. It is measured at 100% of the BV_{DSS} rating. As temperature increases, I_{DSS} increases and BV_{DSS} also increases for power MOSFETs.

3. On-State Characteristics

We consider here power MOSFET under two different modes of operations: the first quadrant operation and the third quadrant operation.

First-Quadrant Operation:

For an n-channel MOSFET, the device operates in the first quadrant when a positive voltage is applied to the drain, as shown in figure 2. As the gate voltage (V_G) increases above the threshold voltage (V_{TH}), the MOSFET channel begins to conduct current. The amount of current it conducts depends on the on-resistance of the MOSFET, as defined by

$$R_{DSON} = V_D / I_D$$

For sufficiently large gate overdrive ($V_G >> V_{TH}$), the I_D-V_D curve appears linear because the MOSFET channel is fully turned on. Under low gate overdrive, the drain current reaches a saturation point when $V_D > (V_G-V_{TH})$ due to a pinch-off effect of the channel.

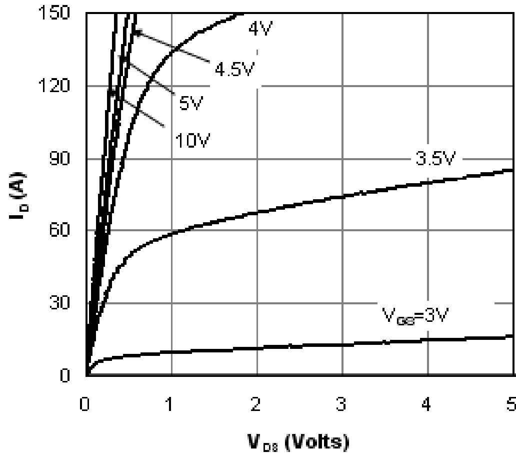

Figure 2: On-region characteristics (first-quadrant operation)

For a trench MOSFET, R_{DSON} consists of the following components:

- R_S: source resistance
- R_{CH}: channel resistance
- R_{ACC}: resistance from the accumulation region
- R_{EPI}: resistance from the top layer of silicon (epitaxial silicon, also known as epi); epi controls the amount of blocking voltage the MOSFET can sustain
- R_{SUBS}: resistance from the silicon substrate on which the epi is grown

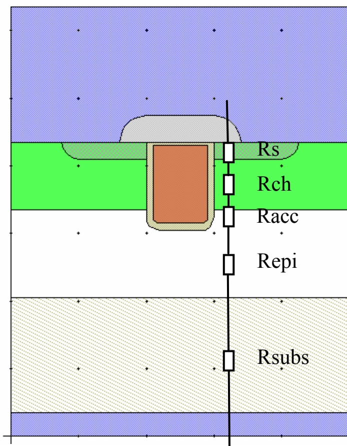

Figure 3a: R_{DSON} components of a trench MOSFET

For a planar MOSFET, the R_{DSON} components are similar to that of a trench MOSFET. The primary difference is the presence of a JFET component. As devices scale down to smaller dimensions, R_S, R_{CH}, R_{ACC} are reduced because more individual unit cells can be packed in a given silicon area. R_{JFET} on the other hand suffers from a "JFET"-effect where current is constrained to flow in a narrow n-region by the adjacent P-body region. Due to the absence of R_{JFET}, trench MOSFETs benefit from high density scaling to achieve very low R_{DSON}.

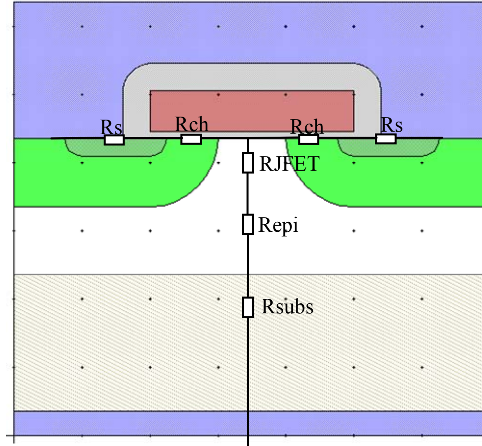

Figure 3b: R_{DSON} components of a planar MOSFET

The channel resistance (R_{CH}) is highly dependent on the amount of the gate overdrive. R_{CH} decreases with increasing V_{GS}. R_{DSON} initially decreases rapidly as V_{GS} increases above V_{TH}, indicating the turning-on of the MOSFET channel. As V_{GS} increases further, R_{DSON} drops to a flat region because the channel is fully turned on and the MOSFET resistance is limited by the other resistance components.

R_{DSON} increases with temperature due to the decreasing carrier mobility. This is an important characteristic for device paralleling.

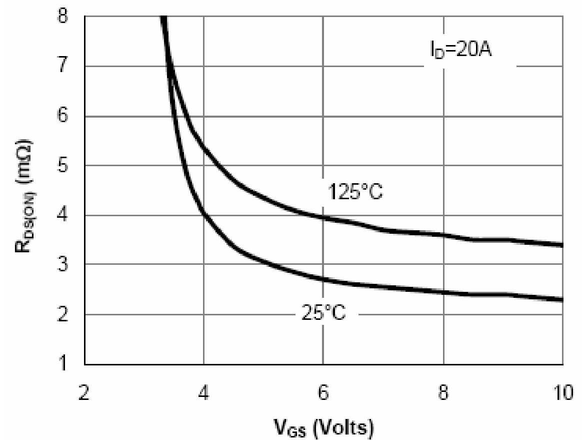

Figure 4: R_{DSON} vs. gate bias and temperature

Threshold Voltage

Threshold voltage, $V_{GS(TH)}$, is defined as the minimum gate bias which can form a conducting channel between the source and drain. For power MOSFETs, it is usually measured at the drain-source current of 250uA. Gate oxide thickness and doping concentration of the channel can be used to control the $V_{GS(TH)}$. Typically, 2~4V is designed for gate drive of 10-15V. With the scaling down of the CMOS technology, the gate drive of the power MOSFET drops to 2.5-4.5V. Therefore, lower threshold voltages of 1-2V are needed for these applications. The threshold voltage has a negative temperature

coefficient, which means it decreases with increasing temperature.

Transconductance

Transconductance, g_{fs}, which is defined as the gain of the MOSFETs, can be expressed as the following equation:

$$g_{fs} = \frac{\Delta I_{DS}}{\Delta V_{GS}}$$

$$g_{fs} = \frac{\mu_{n} C_{OX} W}{L_{CH}}$$

It is usually measured at saturation region with fixed V_{DS}. The transconductance is influenced by gate width (W), channel length (L_{CH}), mobility (μ_n), and gate capacitance (C_{OX}) of the devices. g_{fs} decreases with increasing temperature due to the decreasing carrier mobility.

Third-Quadrant Operation:

Third-quadrant operation for power MOSFET is common in DC-DC buck converters, where current conduction occurs under at V_{DS} (for an n-channel MOSFET). Current flows in the reverse direction compared to first-quadrant operation. The same R_{DSON} components apply.

Under relatively low current, the on-state characteristics for the third-quadrant operation are symmetric to that of the first quadrant operation. We may assume the same R_{DSON} for both types of operation.

Differences appear only under sufficient large current, and therefore sufficient large V_{DON}. When V_{DON} approaches the forward drop voltage of the body diode, the body diode starts to conduct. As a result, the current increases and no current saturation behavior is observed.

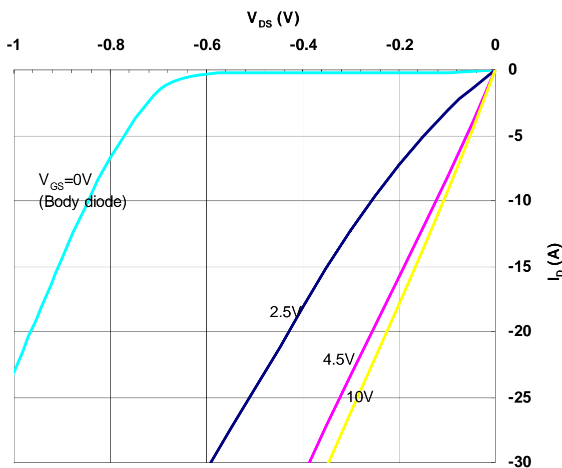

Figure 5: Third-Quadrant Operation

4.

Capacitance

The MOSFET's switching behavior is affected by the parasitic capacitances between the device's three terminals, that is, gate-to-source (C_{GS}), gate-to-drain (C_{GD}) and drain-to-source (C_{DS}) capacitances as shown in Figure 6. These capacitances' values are non-linear and a function of device structure, geometry, and bias voltages.

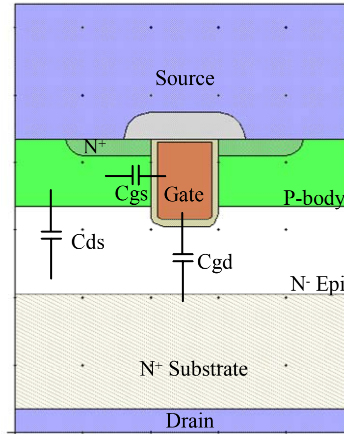

Figure 6: Illustration of MOSFET parasitic capacitances

During turn on, capacitors C_{GD} and C_{GS} are charged through the gate, so the gate control circuit design must consider the variation in this capacitance. The MOSFET parasitic capacitances are provided in the data sheet parameters as C_{ISS}, C_{OSS}, and C_{RSS}:

$C_{GD} = C_{RSS}$

$C_{GS} = C_{ISS} - C_{RSS}$

$C_{DS} = C_{OSS} - C_{RSS}$

C_{RSS} = small-signal reverse transfer capacitance.

C_{ISS} = small-signal input capacitance with the drain and source terminals are shorted.

C_{OSS} = small-signal output capacitance with the gate and source terminals are shorted.

The MOSFET capacitances are non-linear as well as a function of the dc bias voltage. Figure 7a shows how capacitances vary with increased V_{DS} voltage. All the MOSFET capacitances come from a series combination of a bias independent oxide capacitance and a bias dependent depletion (Silicon) capacitance. The decrease in capacitances with V_{DS} comes from the decrease in depletion capacitance as the voltage increases and the depletion region widens.

Figure 7b shows that the MOSFET gate capacitance also increases when the V_{GS} voltage increases past the threshold voltage (for low V_{DS} values) because of the formation of an inversion layer of electrons in the MOS channel and an accumulation layer of electrons under the trench bottom. This why the slope of the gate charge curve increases once the voltage goes beyond the Q_{gd} phase.

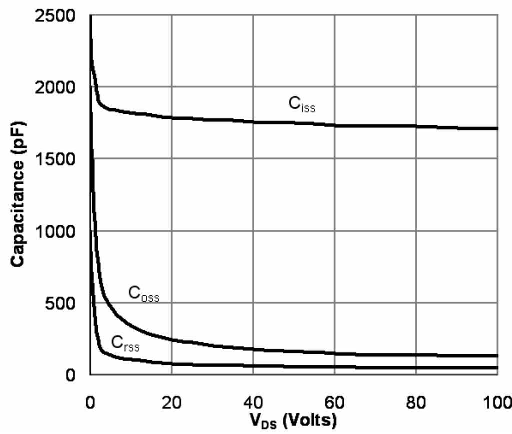

Figure 7a: Typical variation of Capacitances with V_{DS}

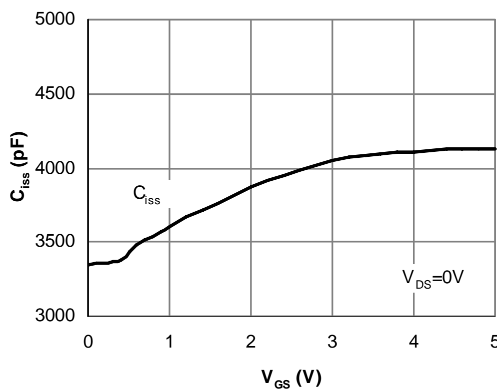

Figure 7b: Typical variation of C_{iss} with V_{GS}

5. Gate Charge

Gate charge parameter can be used to estimate switching times of the power MOSFET once the gate drive current is known. It depends only on the device parasitic capacitances. This parameter is also weakly dependent of the drain current, the supply voltage, and the temperature.

A schematic the gate charge test circuit and its waveform is shown in Figure 8. In this circuit a constant gate current source I_g charges the gate of the device under test, while drain current I_D is sourced. Measuring V_{GS} vs. gate charging time provides a direct indication of the energy spent to switch drain current from 0 to I_D as the Drain voltage swings from V_{DC} to its on-state voltage.

Before the gate current is turned on, the DUT withstands all the supply voltage V_{DC}, while the voltage V_{GS} and the drain current are zero. Once the gate current Ig flows, the gate-to-source capacitance C_{GS} and gate-to-drain capacitance C_{GD} start to charge and the gate-to-source voltage increases. The rate of charging is given by I_G/C_{ISS}. Once the voltage V_{GS} reaches threshold voltage of the power MOSFET, drain current starts to flow. The gate voltage continues to rise to the plateau voltage V_{GP} ($V_{GSTH}+I_D/g_{FS}$), while the voltage across the DUT remains equal to V_{DC}. The charge (Ig*time) needed to reach this state is Q_{GS}. Once the drain current reaches I_D the drain voltage starts to fall. At this period of time, V_{GS} remains constant at V_{GP}. The gate current is used to charge the C_{GD} capacitance and Ig= C_{GD}. dV_{DS}/dt . The plateau phase ends when V_{DS} reaches its on-state value. The gate charge injected during this plateau phase is Q_{GD} and is often used to estimate voltage transition times and switching loss.
Next, the DUT gate continues charging to its final value, and the drain-to-source voltage becomes equal to R_{DSON} x I_D. The gate-to-source voltage is free to rise with a slope controlled by the gate charging current and the C_{ISS} (which is higher at $V_{GS}>V_{TH}$ as shown in figure 7b, leading to a lower slope in the gate charge curve) until the gate-to-source voltage reaches its maximum value. This gate charge is the total gate charge Q_G.

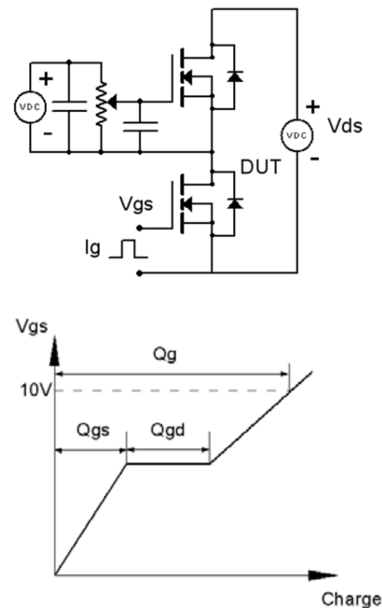

Figure 8: Gate charge test circuit & waveform

6. Gate Resistance

The power MOSFET gate presents an impedance like an RC network to its gate drive. The equivalent R is referred to as the gate resistance Rg. The gate resistance is caused by the finite resistance of the Polysilicon gate conductors, and the metal and contact structures that route the gate signal to the pad for connection to external package leads. For polysilicon gate power trench MOSFETS, the resistance of the gate electrode depends on doping level and type (N type or P-type) of polysilicon material, gate trench geometry and the device layout arrangement. N-type trench power MOSFETs usually have lower gate resistance than that of P-type trench power MOSFETs for the same device layout due to lower sheet resistance of N-type in situ doped polysilicon.

Most switching devices are 100% final tested for Rg using LCR meters

7.

Turn-on and Turn-off

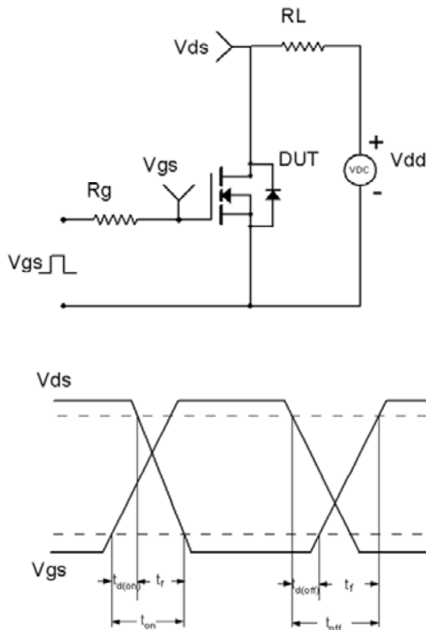

Figure 9: Resistive switching test circuit & waveforms

Power MOSFET datasheets often contain the resistive switching characteristics, which depend on R_g, C_{iss} and C_{rss}. While practical measurements are influenced by parasitic inductances and gate drive details, we examine the basic physics here. Figure 9 shows the power MOSFET resistive switching test circuit and waveforms.

$t_{d(on)}$ – Turn-on Delay Time
This is the time from when V_{gs} rises over 10% of the gate drive voltage to when the drain current rises past 10% of the specified current. At the moment of $t_{d(on)}$, V_{GS} reaches up to the threshold voltage V_{TH}. This period is controlled by the time constant $R_g.C_{iss}$.

t_r – Rise Time
This is the time between the drain current rising from 10% to 90% of load current. This depends on the V_{TH}, transconductance g_{FS} and the time constant $R_g.C_{rss}$.

$t_{d(off)}$ – Turn-off Delay Time
It is the time from when V_{gs} drops below 90% of the gate drive voltage to when the drain current drops below 90% of the load current. It is the delay before current starts to transition in the load, and depends on $R_g.C_{iss}$.

tf – Fall Time
It is the time between the drain current falling from 90% to 10% of load current. This depends on the V_{TH}, transconductance g_{FS} and the time constant $R_g.C_{rss}$.

8.

Body Diode Forward Voltage

V_{SD} is a measure of the forward voltage drop of the integral body diode, by applying a set current to the source. The applied current is typically 1A and is specified in the datasheet along with the maximum limit of forward voltage drop. Figure 10 shows typical forward I-V characteristics for the diode at two temperatures. For AOS SRFET, the typical V_{SD} is lower than that of a normal MOSFET, with typical value of 0.4V; this low V_{SD} can help to reduce power loss during diode conduction duration. SRFET is therefore an ideal choice for low side FETs for DC-DC conversion, and other applications where a certain period of body diode conduction is needed.

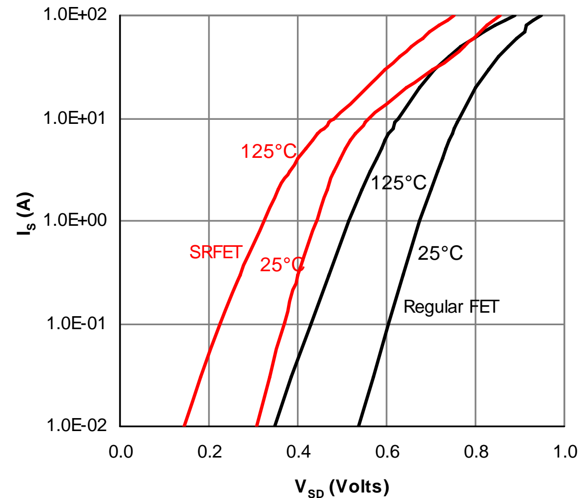

Figure 10: Body-Diode forward Characteristics

9. Body Diode Reverse Recovery

MOSFET parasitic body diode reverse recovery occurs during diode switching from the on-state to the off-state, because its stored minority charges must be removed, either actively via negative current, or passively via recombination inside the device. There are three dynamic parameters listed in the datasheet for diode reverse recovery:

t_{rr}: body diode reverse recovery time
I_{RM}: body diode reverse peak current
Q_{rr}: Body diode reverse recovery charge, defined by

$$Q_{rr} = \int_{trr} i_{sd}(t)dt$$

the area within the negative portion of the diode current waveform.

The above parameters vary with test condition, such as applied voltage V_{DS} and di/dt etc. The parameter definitions and test circuit are shown in Figure 11.

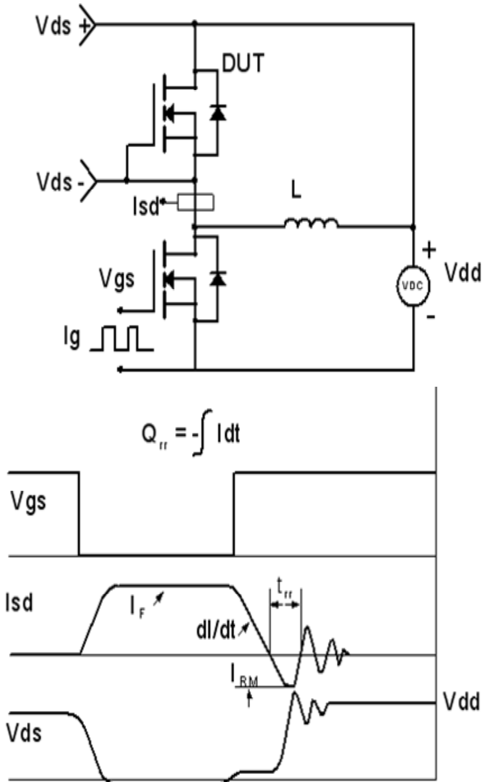

Figure 11: Diode reverse recovery test circuit & waveforms

The gate and source of DUT are shorted to test the body diode. A control device is subjected to a double pulse. The current ramps in the lower control device, and freewheels through the DUT body diode when the control device turns off. When it is turned on again by the second pulse, the DUT body diode must recover before the control FET voltage can drop.

During diode reverse recovery, its reverse current also goes to the lower FET in Figure 11, along with the load current; in addition, the reverse recovery di/dt can cause large voltage overshoots (Ldi/dt) due to circuit stray inductance. These voltage overshoots are minimized if the di/dt during the second phase of the t_{rr} (after crossing I_{RM}) is kept low. Such a diode is said to have soft recovery. Lower Q_{RR} leads to lower switching loss. This is often the largest single component of switching loss in a switching converter.

AOS SDMOS and SRFET have been designed with advanced technology specifically to improve body diode reverse recovery performance with low Q_{rr} and good softness coefficient compare to regular MOSFETs, which can greatly reduce the voltage overshoot, and improve the overall efficiency.

10.

Avalanche capability and ratings

Physics of avalanche breakdown

As the voltage of a power MOSFET is increased, the electric field increases at the body-epi junction. When this field reaches a critical value E_C (about 3E5V/cm in Si), avalanche multiplication of carriers occurs, leading to an abrupt increase in current. Avalanche multiplication is not a destructive process. However, since the current flow path involves hole current flow I_H (=I_D) in the path shown in Figure 12, there is the possibility at high current density of turning on the parasitic bipolar when $V_{BE}=I_H*(Rp+Rc)>0.7V$. When this occurs, the gate can no longer turn-off the FET current. Also, since the BVCEO is typically lower than the MOSFET breakdown, current filaments into the weakest cell where local non-uniformities first cause the parasitic bipolar to turn-on. From this basic description it follows that:

- Failure occurs above a critical current density (even for short low energy high voltage pulses)
- High values of Rp (body pinch resistance under the source) and Rc (contact resistance) degrade UIS capability
- High density cell construction reduces the length of the current path. This decreases Rp, and increases the critical current density at which failure occurs.
- Since both Rp and Rc increase with temperature, and the emitter-base turn on voltage V_{BE} decreases with temperature, UIS capability decreases with temperature.

If avalanche capability is tested at lower currents over a long duration, the energy dissipated $I_{pk}/2*BV*t_{AV}$ heats the device. The failing current is therefore determined by the peak temperature the device reaches during this event. Since large chips have a greater heat capacity, they have higher UIS capability in this mode of operation.

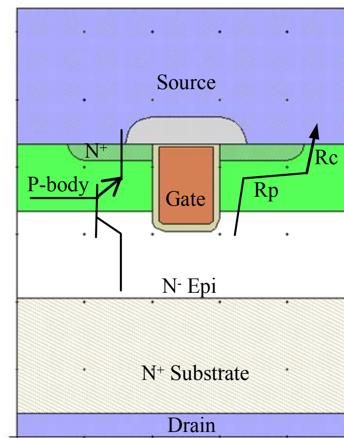

Figure 12: Trench MOSFET cell construction. Parasitic NPN is shown, along with parasitic base resistances Rp and Rc

Avalanche ratings

Power MOSFETs may be driven to voltages in excess of rated $V_{DS(MAX)}$ due to inductive spikes during circuit operation. Therefore, manufacturers commonly specify single and repetitive ratings, and many perform 100% single pulse testing on shipped units.

Typical single pulse ratings are captured using time in avalanche curves as shown in figure 13. These are guaranteed performance data, and the actual point of destruction is above this level. As expected, avalanche capability decreases with temperature for the same time duration. The current capability decreases with longer times in avalanche at a given starting junction temperature due to heating during the avalanche event.

These curves are generated using the circuit in figure 14, where the current is ramped up in the device under test through an inductor. When the device turns off, since the inductor current cannot be interrupted, the device voltage flies up to the breakdown voltage of the device. When the device turns off, the switch in series with the supply V_{dd} is also turned off, forcing the current to freewheel though the diode. Now the voltage across the inductor is –BV, which causes the current to ramp down to zero. Using different inductors, one may obtain different times in avalanche. The basic equations relating Energy, current, time and inductance are listed below:

$$E_{ar} = \int i_L \times V_{DS} dt = \frac{1}{2} \times i_{pk}^2 \times L$$

$$t_{av} = \frac{i_{pk} \times L}{BV}$$

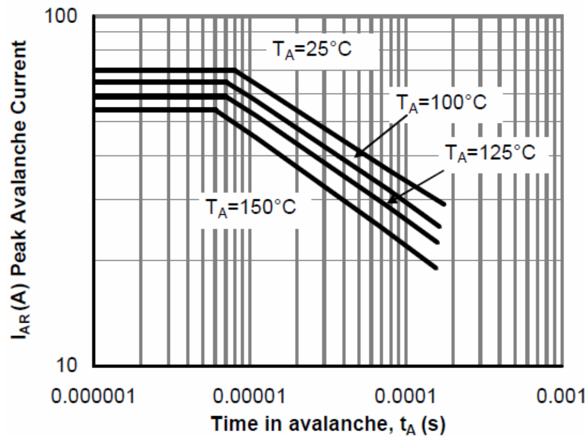

Figure 13: Time in avalanche vs. Peak current as a function of temperature

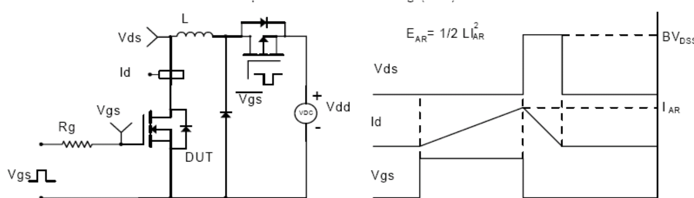

Figure 14: Test circuit used for UIS (avalanche) measurements

Repetitive ratings:

If a power MOSFET is subjected to repetitive UIS pulses, its junction temperature undergoes an increase in average value, based on the average power dissipated as well as peaks of temperature with each pulse. When the current density is high enough, and the peak temperature is high enough, the device can fail from the same mechanisms as described for single pulse avalanche.

No common standard is being used for specifying repetitive avalanche ratings. Two methods are described here.

Method 1: Select a small inductor, say L=1μH, with duty cycle of 0.01, f=100kHz. Increase the current until average temperature reaches T_J =150C to set I_{AR}. Or increase current until destruction occurs and de-rate to establish the I_{AR} rating. This method has the disadvantage that it only relates to one inductor and one frequency. If the frequency is raised, I_{AR} drops. If the inductor is higher, I_{AR} drops. In fact, if the frequency is low enough such that the device returns to its starting T_J (25C) after each pulse, well designed power MOSFETs will have E_{AR}=E_{AS}, and I_{AR}=I_{AS}.

Method 2: Do not distinguish E_{AR}, E_{AS}, and I_{AR}, I_{AS} since they are the same at low enough frequency. The user may use the time in avalanche curves for short time durations to estimate the maximum allowable current in avalanche, beginning with an estimate of starting T_J from the average power dissipation P and thermal resistance.

$$P = 0.5 fLI^2$$

$$T_J = \frac{P}{R_{\theta JA}}$$

11.

dV/dt ratings

Power MOSFETs fail from excessive drain source dV/dts under various scenarios. In each case, the failure is caused by displacement or conduction current flow via Rp+Rc, leading to turn-on of the parasitic bipolar, and consequent failure of the device by the same mechanism described before for avalanche failures.

- If the gate is shorted to source via a resistor, and a fast dV/dt applied between Drain and source, the displacement current C_{oss}*dV/dt flows under the source, and can develop sufficient voltage drop across Rp+Rc to exceed the V_{BE} (0.7V) of the parasitic bipolar. Due to the low Coss values of most modern power MOSFETs, this current is low even for dV/dts of 10-50V/ns, and is not considered a major failure mode. If however, the resistance shorting the gate to source is large, the C_{rss}*dV/dt current will develop enough voltage drop across it to turn on the gate, leading to current flow which if unconstrained, can lead to device failure.
- During body diode reverse recovery, hole current flows out of the source contact via R_p+Rc. This current adds to and often far exceeds the C_{oss}*dV/dt current at also flows as the voltage develops across the body diode of the FET. Since the diode stored charge and its removal is non-uniform, the diode recovery dV/dt failure is seen at lower values of dV/dt. The failure mechanism is again caused by turn-on of the parasitic bipolar. If the gate-source shorting resistor is too large, there is the further possibility of exacerbating the dV/dt current by turning on the gate of the MOSFET by developing sufficient voltage across the resistor as it sinks the C_{rss}*dV/dt current.
- Both modes of dV/dt failure get worse with temperature.

12.

Thermal Resistance Characterization

Junction Calibration

Before the thermal resistance of any device is to be measured, a calibration curve must be made. Each silicon device has its own unique calibration, but once determined, is valid for any package it may be put into.

The calibration curve is measured by treating the device as a diode and forcing a 10mA sense current (I_S) and measuring the forward voltage drop (V_{FSD}) at each junction temperature. A sample calibration curve for a device is shown in Figure 15. On subsequent thermal resistance tests, the same 10mA sense current will be forced through the device and the junction temperature will be calculated from the resulting forward voltage drop.

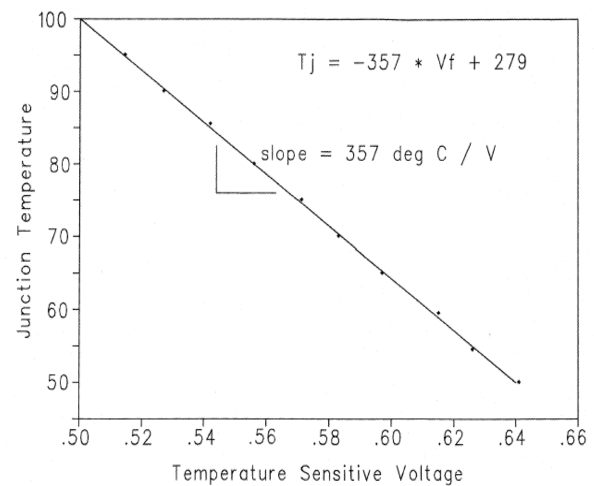

Figure 15: Sample Temperature Calibration Curve.

Junction-to-Ambient/Lead/ Case Thermal Resistance

The junction-to-ambient thermal resistance $R_{\theta JA}$ is defined as the thermal resistance from the device junction to the ambient environment. The junction-to-lead thermal resistance $R_{\theta JL}$ is the thermal resistance from the device junction to the drain lead of the device. For larger devices (Ultra SO8 and bigger) with a back exposed drain pad, the $R_{\theta JC}$ must also be measured. $R_{\theta JC}$ is defined as the thermal resistance from the device junction to the device case. Both can be calculated from the following equation:

$$R_{\Theta JX} = \frac{T_J - T_X}{P_D}$$

Where T_J is the junction temperature of the device, it can be read out from junction calibration curve by measuring forward voltage drop at different junction temperature. T_X is the ambient, lead or case temperature depending on whether $R_{\theta JA}$, $R_{\theta JL}$ or $R_{\theta JC}$ is being measured, and P_D is the power dissipation of the device, which is calculated by input voltage and current.

Transient Thermal Heating Curve, Junction to Ambient/ Case

Transient thermal curves can be used to estimate instantaneous temperatures resulting from power loss on a transient basis. These curves can be Junction to Ambient or Case based. Namely they are characterizing transient thermal impedance form device junction to ambient or case.

The thermal measurement machine applies a single pulse with various durations; junction temperature is read again by measuring forward voltage drop after each single pulse. This measures the 'single pulse' transient thermal curve. Based on single pulse curve, a 3 or 4 stages RC network is simulated to generate the rest curves in Transient Thermal Heating curve group, as show in Figure 16.

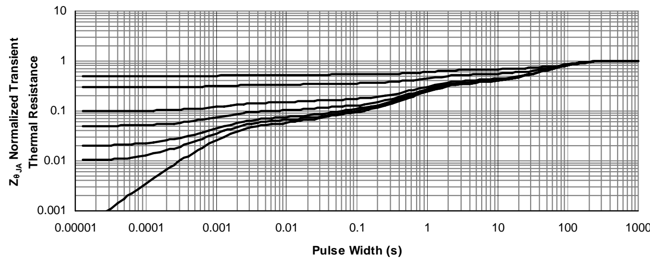

Figure 16: Sample Transient Thermal Heating Curve based on Junction-to-Ambient measurements.

13.

Power Dissipation

Power dissipation P_D and P_{DSM} are the maximum power that is allowed for device safe operation. Power dissipation is calculated using the following formula:

$$P_D = \frac{T_{J(\max)} - T_C}{R_{\Theta JC(\max)}}$$

$$P_{DSM} = \frac{T_{J(\max)} - T_A}{R_{\Theta JA(\max)}}$$

P_D is based on junction to case thermal resistance. To achieve power dissipation of P_D, case temperature needs to be maintained at 25°C.

P_{DSM} is based on junction to ambient thermal resistance. The device is mounted on a 1 square inch 2 oz. copper PCB, and P_{DSM} is the power that raises T_j to 150°C

14. Safe-Operating Area

SOA (FBSOA) curves define the maximum value of drain to source voltage and drain current which guarantees safe operation when the device is in forward bias.

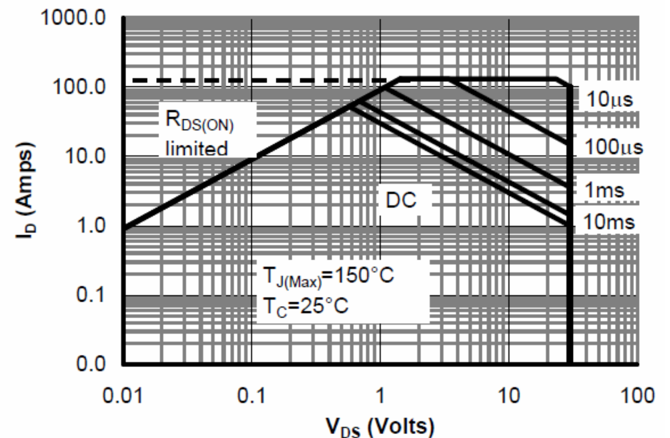

Figure 17: Maximum Forward Biased Safe Operating Area

The right hand vertical boundary is maximum drain to source voltage (V_{DS}).

The upper horizontal limit is maximum pulsed drain current (I_{DM}).

The slope on left had side is limited by drain to source on resistance ($R_{DS(ON)}$)

The paralleled lines in the middle are the maximum drain to source current for different pulse widths. These currents are determined by the transient thermal impedance.

15.

Current Ratings

Continuous Drain current - I_D and I_{DSM}

Excluding package limitations, the continuous Drain Current I_D and I_{DSM} is the maximum drain current corresponding to P_D and P_{DSM}.

$$I_D = \sqrt{\frac{P_D}{R_{DS(on)\max} @ T_{J(\max)}}}$$

I_D will be de-rated with increasing case temperature, as shown in Figure 18, based on the reduced power dissipation allowed.

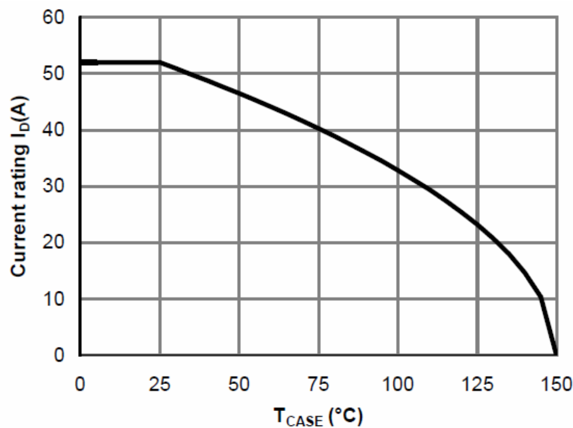

Figure 18: Current rating vs. case temperature

Package Limitation

Continuous current rating is limited by two factors:

1. thermal resistance
2. package limitation

Package limitation usually refers to bond wire current handling capability. The conventional way to rate bond wire current limit is based on bond wire fusing temperature, which is not correct because:

1. Wire temperature can not exceed 220°C, or it will cause the degradation of the plastic molding compound.
2. In most cases the silicon resistance is ~10 times higher than wire resistance. Most of the heat is generated on the silicon surface. The hottest spot is on silicon.

Silicon maximum junction temperature is lower than 220°C, that's why bond wire fusing problem doesn't exist in most of the cases. Bond wires fuse only when devices fail. Please refer to application note [MOS-006] on AOS website.

Pulsed Drain Current - I_{DM}

Pulsed Drain Current is rated for 260µs current pulse. The value on datasheet is the lower value of the following two:

1. Actual single pulse current measurement with 260µs current pulse.
2. Calculation based on transient thermal resistance at 260µs pulse duration.

Reference:

[1] B. J. Baliga, "Fundamentals of Power Semiconductor Devices", 2008.
[2] Application notes MOS-006, "Power MOSFET Continuous Drain current rating and Bonding wire limitation', www.aosmd.com.