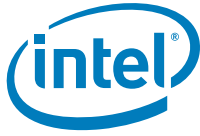


Intel[®] Xeon Phi[™] Processor x200 Product Family

Thermal/Mechanical Specification and Design Guide (TMSDG)

June 2017

Revision 002



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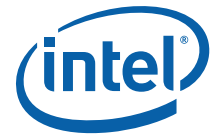
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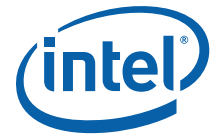
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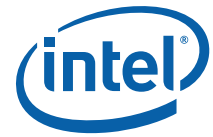
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Revision History

Document Number	Revision Number	Description	Revision Date
334785	001	Initial release.	August 2016
334785	002	<ul style="list-style-type: none">• Section 3.3.3 - Updated contact area plating information.• Section 4.1.2 - Updated note regarding Nut Durability Spec.• Appendix B - Updated Intel and vendor P/Ns.• Appendix E - Updated assembly mechanical drawings.• Appendix F - Updated Topside KOZ Drawing.	June 2017

1 Introduction

1.1 Objective

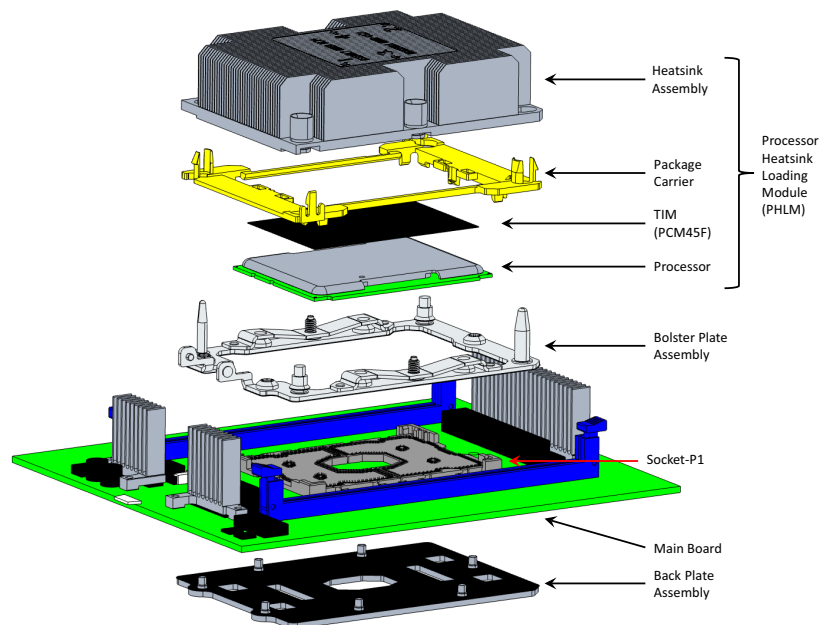
This document provides processor thermal/mechanical specifications and design guidelines for development of thermal and mechanical solutions for the Intel® Xeon Phi™ Processor x200 Product Family. This second generation Intel Xeon Phi product family now offers a line of socketed processors in addition to a line of PCIe* card-based coprocessors; but the coprocessor offerings are not discussed in this document.

Throughout this document, unless specified otherwise, the term “processor” represents any member of the Intel Xeon Phi Processor x200 Product Family; where distinction is necessary, the term “processor with fabric” will represent the Intel Xeon Phi™ processor with integrated Intel® Omni-Path Fabric (Intel® OP Fabric).

1.2 Scope

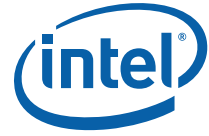
Figure 1-1 provides a conceptual illustration of the processor mechanical assembly. Explicit hardware design and assembly details are provided in Section 2 through Section 5 of this document.

Figure 1-1. Processor Mechanical Assembly



The components and information described in this document include:

- Processor package mechanical design specifications and integration guidelines.
- Processor socket mechanical design specifications and integration guidelines.
- Processor and heatsink mechanical retention assembly design specifications and system design and integration guidelines.
 - Back and bolster plate assembly design details, including loading targets.



- Reference designs for the Processor Heatsink Module (PHM).
- Board and system integration and design guidance.
- Processor thermal specifications and design guidance, reference board and reference air-cooled thermal solution (which includes the reference heatsink).

Thermal and mechanical design aspects which directly impinge on the processor package and the socket (by extension) must be treated as design specifications. Consideration of mechanical retention assembly loading targets and physical design attributes as specification or recommendation depends on the degree to which the user adopts the reference design.

The purpose of this specification and design guide is to describe and document these design requirements, as well as the mechanical retention approach and the reference thermal solution from Intel, for the processor. Guidelines for designing a thermal solution that meets product lifetime requirements will also be discussed.

This document is intended for use by:

- Board and system thermal and mechanical designers.
- Designers and suppliers of processor thermal solutions.

The guidelines recommended in this document are based on experience and simulation, and preliminary work done at Intel while developing the processor. This work is ongoing and the recommendations and specifications are subject to change.

1.3 References

Table 1-1 lists additional resources to assist with processor mechanical and thermal design solutions. For a complete list of documentation, contact your local Intel representative or go to www.intel.com.

Table 1-1. Related Documents

Document	Document Number	Notes
<i>Intel® Xeon Phi™ Processor x200 Product Family Datasheet, Volume One: Electrical</i>	334710	1
<i>Intel® IA64 IA32 Architecture Software Developers Manual</i>	325462	2
<i>European Blue Angel Recycling Standards</i>		3
<i>Environmental Product Content Specification for Suppliers and Outsourced Manufacturers</i>	18-1201	4

Notes:

1. Available at <http://www.intel.com/content/www/us/en/processors/xeon/xeon-phi-processor-x200-product-family-datasheet.html>
2. Available at <http://www.intel.com/content/dam/www/public/us/en/documents/manuals/64-ia-32-architectures-software-developer-manual-325462.pdf>
3. Available at <https://www.blauer-engel.de/>
4. Available at https://supplier.intel.com/static/EHS/Environmental_Product_Content_Specification.pdf



1.4 Terminology

Table 1-2 provides a list of common terms used in this document, along with a brief description.

Table 1-2. Terms and Terminology (Sheet 1 of 2)

Terms	Terminology
BOL	Beginning of Life, initial time period relevant to product quality and reliability testing
Bypass	Bypass is the area between a passive heatsink and any object that can act to form a duct. For this example, it can be expressed as a dimension away from the outside dimension of the fins to the nearest adjacent surface.
DTS	Digital Thermal Sensor: On-die circuit used for estimating local die temperature which is then converted to a digital value.
EOL	End of Life, final time period relevant to product quality and reliability testing
FSC	Fan Speed Control, algorithms developed to optimize cooling vs air flow vs acoustics, etc.
IFP Cable	Intel® Fabric Passive (IFP) internal cable assembly enables high speed, low loss data connections between the Intel processor and chassis connections to an external fabric interface.
IHS	Integrated Heat Spreader: a component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.
KOZ	Component Keep-Out Zone usually provided for a board or system to avoid mechanical interference or performance problems.
LEC54A	Linear Edge Connector 54 pin, high speed, low loss, edge connector designed specifically for Intel Xeon® Phi processors with integrated fabric interconnects.
LGA	Land Grid Array processor package and socket interface
MCDRAM	Multi-Channel Dynamic Random Access Memory
PECI	Platform Environment Control Interface, standard for thermal management using DTS, is a one-wire interface that provides a communication channel between Intel processor and chipset components and external monitors.
PHM	Processor - Heatsink - Module
Ψ_{CA}	Case-to-ambient thermal resistance, a thermal performance characterization parameter (Ψ_{CA}). A measure of thermal solution performance using total package power. Defined as $(T_{CASE} - T_{LA}) / (\text{Total Package Power})$. T_{CASE} is the IHS temperature at a specific location and T_{LA} is the local ambient air temperature. The heat source should always be specified for Ψ measurements. The unit is °C/W.
Ψ_{CS}	Case-to-sink thermal resistance, a thermal performance characterization parameter. A measure of thermal interface material performance using total package power. Defined as $(T_{CASE} - T_{SINK}) / (\text{Total Package Power})$.
Ψ_{SA}	Sink-to-ambient thermal resistance, a thermal performance characterization parameter. A measure of heatsink thermal performance using total package power. Defined as $(T_{SINK} - T_{LA}) / (\text{Total Package Power})$.
SKU	A processor Stock Keeping Unit (SKU) to be installed in either server or workstation platforms. For the Intel® Xeon Phi™ Processor x200 Product Family, different SKUs will be distinguished by different marketing names and offer e.g., different numbers of cores, clock frequencies, etc.
SMT	Surface Mount Technology
SRO	Solder Resist Opening.
T_{CASE}	The case temperature of the processor measured at specific locations on the topside of the IHS, this is typically above the geometric center of a particular die (but may not coincide with the geometric center of the IHS).
$T_{CONTROL}$	$T_{CONTROL}$ is a static temperature setting used as a trigger point for fan speed control.

**Table 1-2. Terms and Terminology (Sheet 2 of 2)**

Terms	Terminology
TDP	Thermal Design Power: The power envelope in which the design is expected to operate normally without the need for throttling or other performance reduction operational modes. The thermal solution should be designed to dissipate this target power level. TDP is not the maximum power that the processor can dissipate.
TIM	Thermal Interface Material: The thermally conductive compound between the heatsink and the processor IHS. This material fills the air gaps and voids, and enhances the transfer of the heat from the processor IHS to the heatsink.
T_{LA}	The local ambient air temperature near the inlet of the thermal solution. This temperature is usually measured at the upstream air of the heatsink.
T_{SA}	The system ambient air temperature external to a system chassis. This temperature is usually measured at the chassis air inlets.
U	A unit of measure used to define server rack spacing height. 1U is equal to 1.75 in, 2U equals 3.50 in, and so forth.

2 Processor Mechanical Design

2.1 Processor Package Mechanical Specifications

This section provides an overview of the processor package mechanical design and integration. The package serves as the primary interface between the processor silicon die and the rest of the system. The package provides electrical signaling and power delivery as well as thermal transmission, mechanical physical attach, dimensional scale translation and structural strength and stiffness. A solid understanding of the processor design targets provides the necessary foundation to identify and establish thermal and mechanical design requirements for the main board and the system.

To ensure compatibility with the processor and the Intel Xeon Phi Processor x200 Product Family-based platform, the mechanical processor retention and thermal solution must meet the requirements and keep-out zones of both the processor and the LGA3647-1 socket. This section provides specific package-related thermal and mechanical design guidance.

2.2 Processor Package Description

The processor is a multi-chip package consisting of the processor silicon die and eight MCDRAM chips, all housed in a Flip Chip (FC) Land Grid Array (LGA) package that interfaces with the main board via an LGA3647-1 socket. The package incorporates an Integrated Heat Spreader (IHS) attached to the top surface of the package substrate. The processor die and MCDRAMs are mounted on the substrate beneath the IHS and are thermally connected to the IHS via Thermal Interface Material (TIM).

The package IHS serves as the mating surface (interface) for the processor thermal cooling solution, such as a heatsink or cold plate. The IHS transfers the non-uniform heat from the die surface to the TIM on the base of the heatsink or cold plate, resulting in a heat flux that is more uniform and spread over a larger surface area (though not the entire IHS area). This allows more efficient heat transfer out of the package to an attached cooling device.

The bottom side of the package has 3647 lands arranged in a hexagonal pad array which interfaces with the LGA3647-1 socket. [Figure 2-1](#) and [Figure 2-2](#) show cross-sectional sketches of the processor package components and how they are assembled.

The package components include the following:

- Processor die
- MCDRAMs
- Fabric die (processor with fabric only)
- Package substrate
- Thermal Interface Material (TIM)
- Integrated Heat Spreader (IHS)
- LGA lands (LGA3647-1 socket interface)
- Discrete components (top side)
- Discrete components (bottom side)



Figure 2-1. Processor Package Assembly Sketch

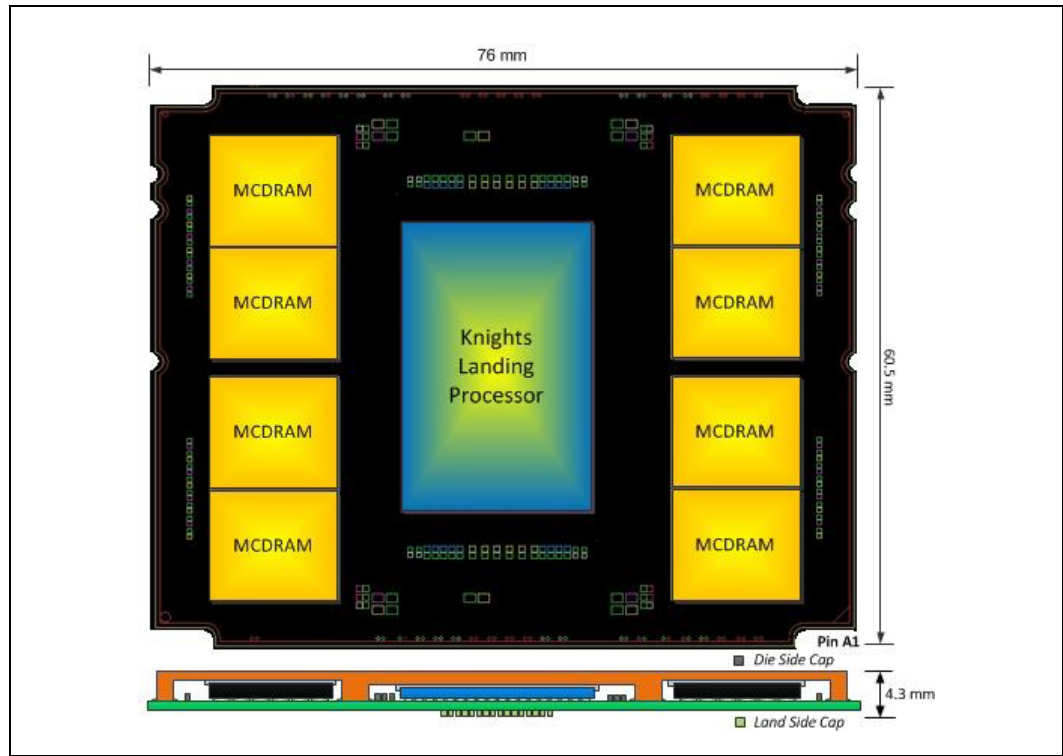
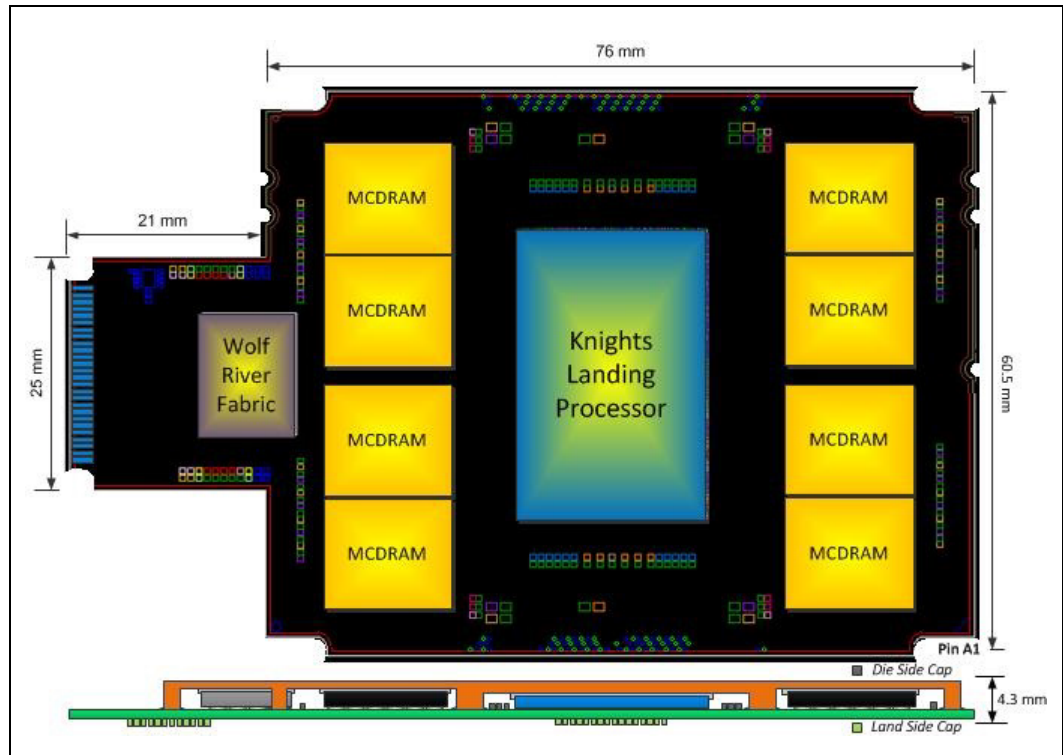


Figure 2-2. Processor with Fabric Package Assembly Sketch



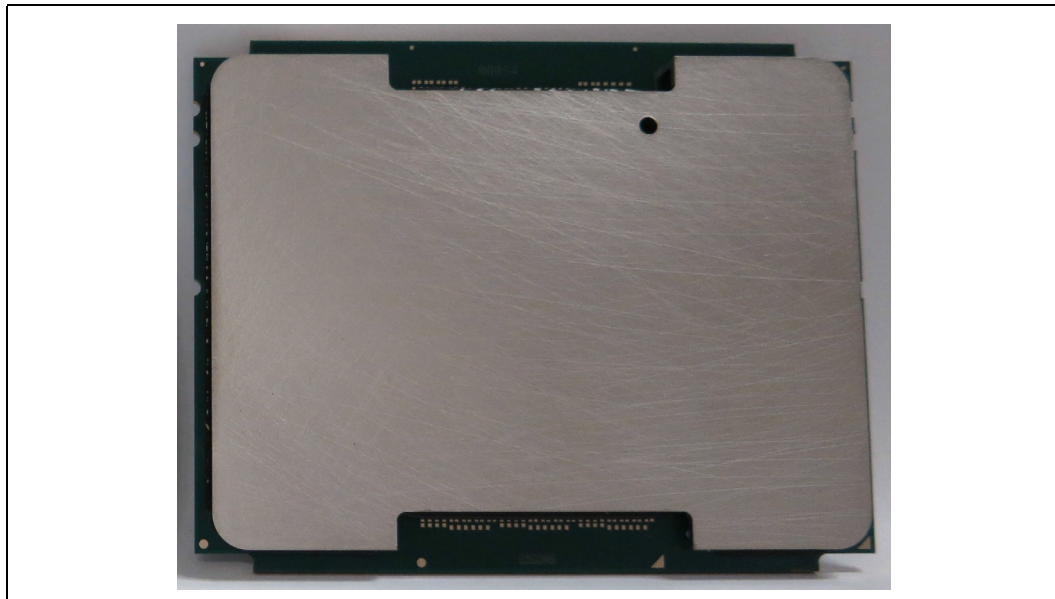
These conceptual figures are not drawn to scale, and important design details may have changed (e.g., keying). The Pin 1 fiducial can be seen in the lower-right corner of these figures. Refer to [Appendix C](#) for the latest details on package dimensions and features.

2.3 Package Mechanical Dimensions

The processor package is 76 x 60.5 mm (outside dimensions) and approximately 4.3 mm thick (bottom side of substrate to top of IHS, not including the Land Side Capacitors [LSCs]). The processor with fabric package is similar in size, but includes a 25 mm wide extension centered on one edge; the extension protrudes out roughly 21 mm and provides gold-finger contacts for fabric cable connection.

[Figure 2-3](#) shows a photograph of the IHS on a processor.

Figure 2-3. Processor with the Integrated Heat Spreader



Notes:

1. The hole in the IHS above allows for outgassing during TIM material curing. A second hole is added to the processor with fabric IHS to assist with substrate alignment.
2. The Pin 1 fiducial is shown in the lower-right corner of this figure.

The processor package mechanical drawings are provided in [Appendix C](#). These processor package mechanical drawings include dimensions necessary to design a thermal solution for the processor, including:

- Package dimensions and tolerances (height, length, width, etc.)
- IHS dimensions and tolerances
- IHS parallelism, flatness, and tilt
- Land dimensions
- Fabric package extension dimensions (processor with fabric only)
- Reference datum

The processor connects to the main board through a surface-mount-type LGA socket. A description of the socket can be found in [Section 3](#) and socket drawings are provided in [Appendix D](#).



2.3.1 Package Critical-to-Function Attributes

The processor package land dimension details, base material, plating material and plating thickness are provided in [Appendix C](#). The following is a list of package Critical-to-Function (CTF) attributes. CTF values are detailed on the processor package drawings in [Appendix C](#):

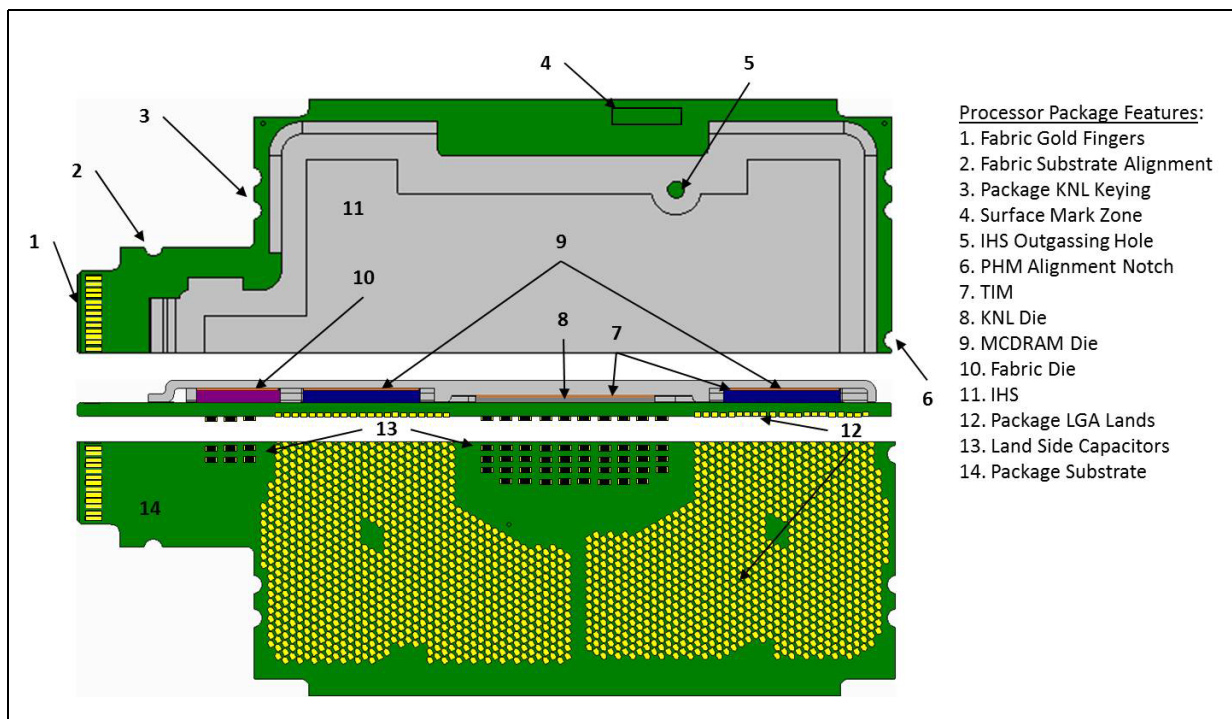
- Package Alignment Length
- Package Alignment Width
- Package Substrate Thickness
- Land Length
- Land Width
- Land True Position (Pattern Relating)
- Land Co-planarity
- Substrate Flatness

2.3.2 Other Processor Package Specific Design Attributes

Refer to [Table C-1](#) for additional information on package markings, KOZs, tolerances, parallelism, and tilt. Key package features and design attributes are enumerated below in [Figure 2-4](#), these include:

- Package Product ID socket keying notch
- Package PHM alignment keying notch
- Package Pin 1 Indicator (shown in [Figure 2-5](#) and [Figure 2-6](#))

Figure 2-4. Processor with Fabric Package Features and Design Attributes



2.4 Processor Mass

The processor mass is 88.8 g, and the processor with fabric mass is 91.4 g. This includes the mass of all components integrated on the processor package.

2.5 Processor Material

The table below lists some of the package components and associated materials.

Table 2-1. Processor Materials

Component	Material
Integrated Heat Spreader	Nickel Plated Copper
Substrate	Halogen Free, Fiber Reinforced Resin
Package Lands	Gold Plated Copper
Fabric Edge Connector Fingers	Gold Plated Copper

2.6 Processor Markings

Refer to [Table C-1](#) for detailed information on package surface mark and enabling mark zones.

Figure 2-5. Processor Top and Bottom View

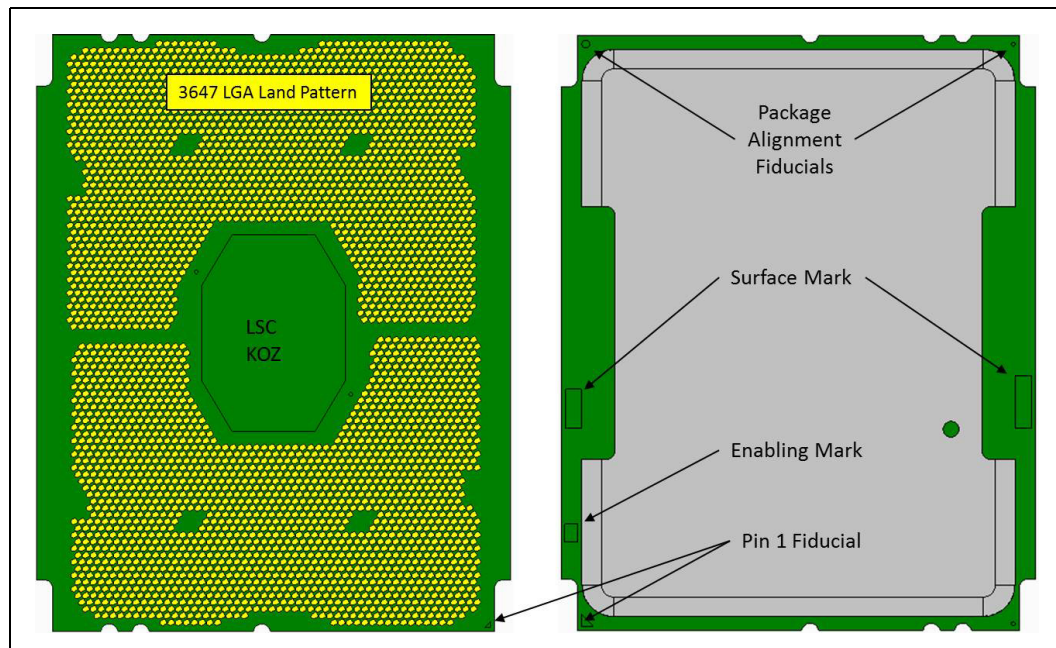
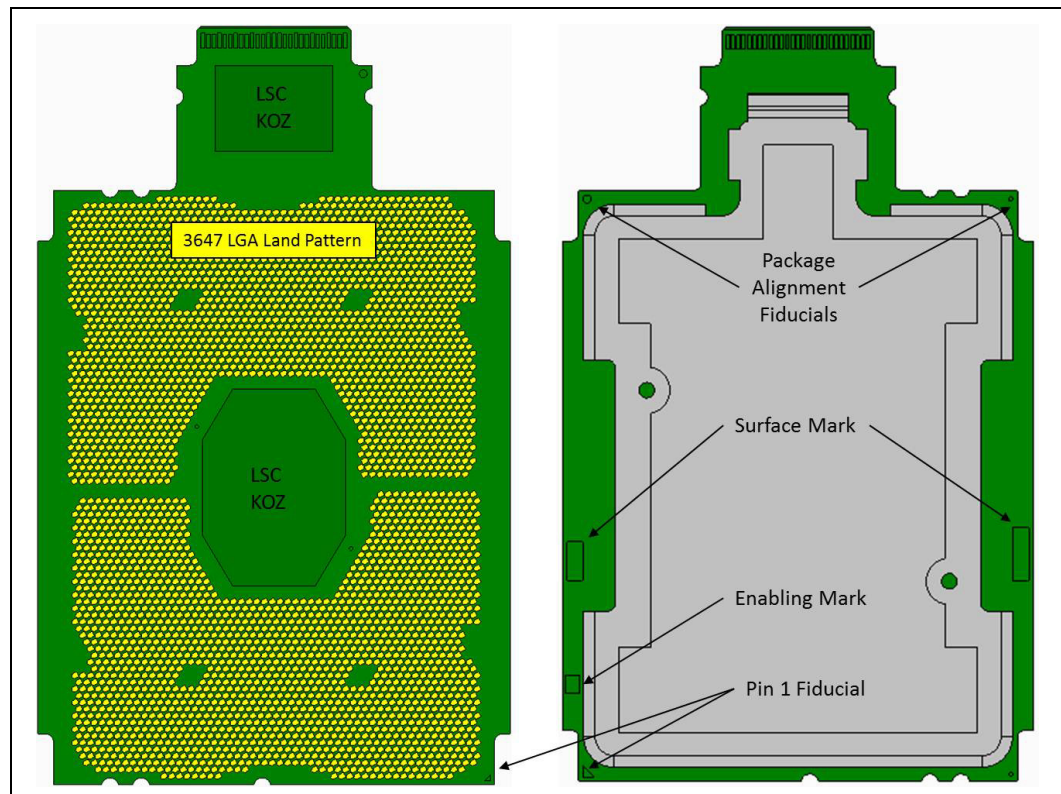


Figure 2-6. Processor with Fabric Top and Bottom View



2.7 Processor Mechanical Load Specification

Refer to [Section 3](#) and [Section 4](#) for the mechanical loading specifications.

2.8 Processor Insertion Specification

Socket Insertion Cycling:

- The processor can be inserted into and removed from an LGA3647-1 socket 30 times.

IFP Cable Attachment Cycling (processor with fabric only):

- Mating and unmating of the processor package and the Linear Edge Connector (LEC54A) on the Intel Fabric Passive (IFP) cable limit is 15 cycles.

2.9 Processor Handling Guidelines

The processor package may contain components on the top or bottom side of the package substrate. To remove the processor from its shipping container or the tray, grab and hold the processor along its long edges.

Avoid contacting the processor bottom side lands and/or gold fingers, and always use Electrostatic Discharge (ESD) protective procedures and equipment.



When installing the processor into the socket, care should be taken to ensure that the processor is properly oriented, that is, the processor pin-1 is in the same direction as the socket pin-1, and that there are no contaminations or foreign material on the land pads or gold fingers.

In cases where the processor is not installed into the socket, it should be placed or stored in the appropriate tray or container in order to avoid damaging the package substrate or its bottom side components.



3 Socket Mechanical Design

3.1 LGA3647-1 Socket Overview

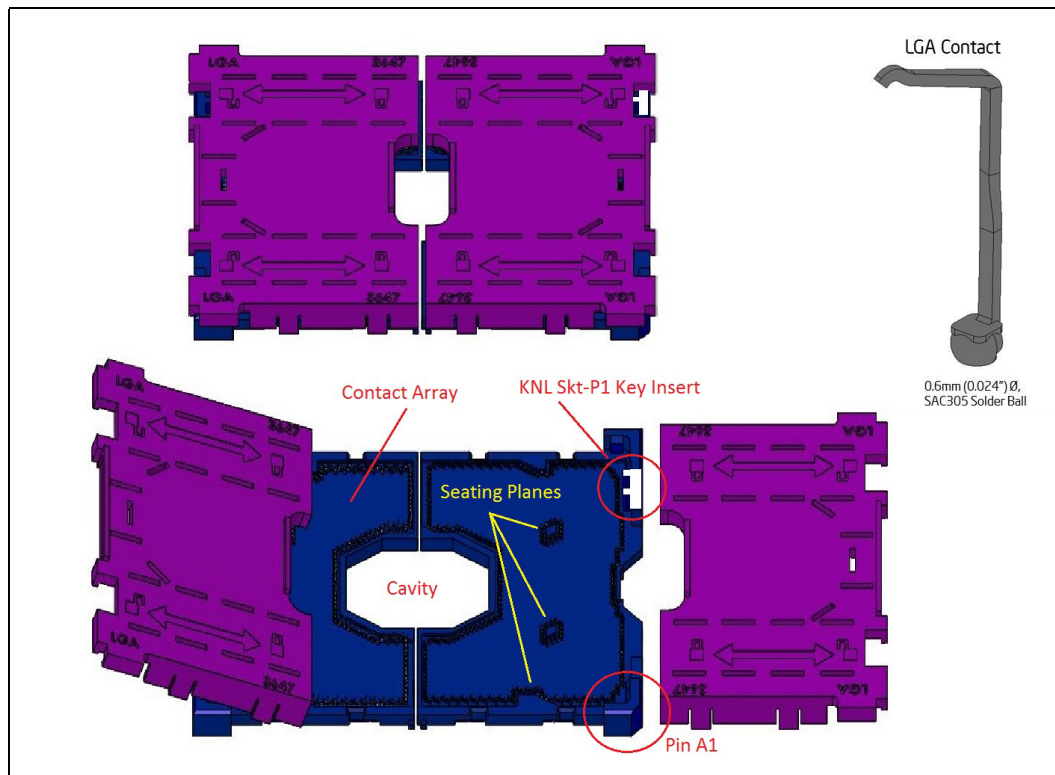
This section describes the Surface Mount (SMT) Land Grid Array (LGA) socket for the processor. The socket contains 3647 pins and provides I/O, power, and ground connections from the main board to the processor package.

Socket definitions listed in this section are provided for design guidance only. Contact vendors for explicit and detailed design guidance. Socket vendor contact information is provided in [Appendix B](#).

The socket has four main components, the two halves comprising the socket body and the Pick-and-Place (PnP) covers for each half. The socket set is delivered by the supplier with PnP covers attached to each appropriate half of the socket body. The main body of the socket, which is made of electrically insulated material with resistance to high temperature, houses the socket contacts. Key components of the socket are the main body of the socket, socket contacts, surface mount features, and the protective covers.

Due to the large size of the socket, it is made of two C-shaped halves. The two halves are not interchangeable and are distinguishable from one another by the keying colors and by the pin A1 indicator: The left half keying insert (can be molded) is the same color as the body; the right half keying insert is white; and the right half also has a molded chamfer for pin A1. [Figure 3-1](#) illustrates the socket features. Keying features (wall protrusions) within the contact array area and raised edges of the socket body help align the package with respect to the socket contacts.

Figure 3-1. LGA3647-1 Socket Assembly with PnP Covers



3.1.1 Socket Features

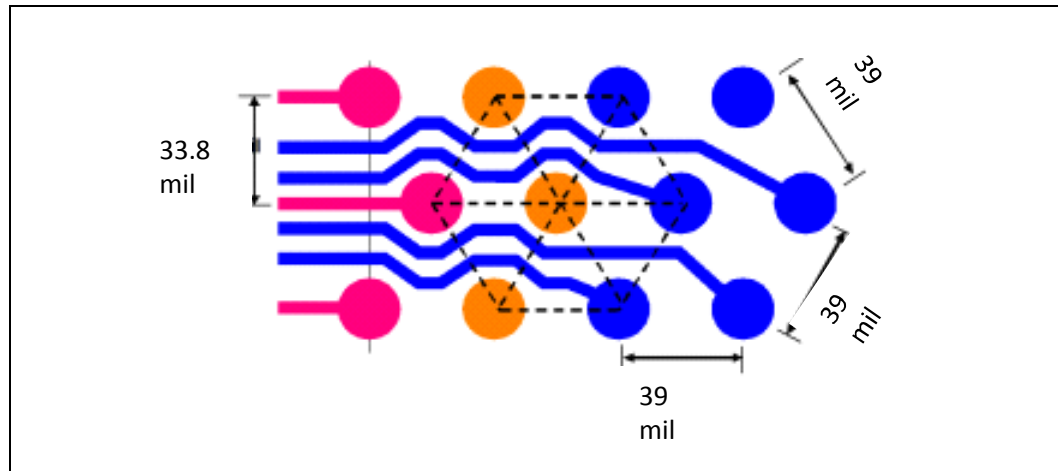
LGA3647-1 socket attributes are listed in [Table 3-1](#). The socket incorporates a roughly rectangular pin grid with a hexagonal depopulation region in the center of the array and selective depopulation elsewhere; see [Appendix D](#). The pin field geometry is a hexagonal array as shown in [Figure 3-2](#) below. The tips of the socket pin contacts extend above the surface of the socket to make contact with the pads located at the bottom of the processor package.

Solder balls enable the socket to be surface-mounted to the main board. Each contact has a corresponding solder ball. Solder ball position may be at an offset with respect to the contact tip and base. Socket BGA ball hexagonal array ball-out pattern shown in [Figure 3-2](#) increases contact density by 12% while maintaining 39 mil minimum via pitch requirements.

Table 3-1. LGA3647-1 Socket Attributes

LGA3647-1 Socket	Attributes
Socket Wall Exterior Dimension	82 mm (L) x 62 mm (W)
Socket Wall Interior Dimension (Package Size)	76.16 mm (L) x 56.6 mm (W)
Pitch (hexagonal pattern)	0.8585 mm (X) x 0.9906 mm (Y)
Ball Count	3647

Figure 3-2. Hexagonal Array in LGA3647 Socket BGA Ball Footprint



The socket cover is intended to be reusable and recyclable. It enables socket pick-and-place during main board assembly. The socket cover also protects the socket contacts from contamination and damage during board assembly and handling.

Features of the socket include:

- Contact housing
- Processor package keying
- Package seating plane
- Side walls for package alignment
- Center cavity for the processor secondary side and main board primary side components

3.1.2 Socket Mechanical Requirements

3.1.2.1 Attachment

The socket is designed for Surface Mounted Technology (SMT) assembly onto the main board. The board assembly process and sequence may be different from one design to another and may require multiple assembly steps. The socket will be attached to the main board solely via its 3647 solder balls. There are no additional external methods (screws, extra solder, adhesive, etc.) to attach the socket.

The socket is tested against mechanical shock and vibration requirements such as those listed in [Appendix A](#) under the expected use conditions with all assembly components under the loading conditions outlined in [Section 3.1.2.2](#). Customer dynamic loading should not exceed these levels.

3.1.2.2 Socket Loading and Deflection Specifications

[Table 3-2](#) provides loading and board deflection specifications for the LGA3647-1 socket. These mechanical load limits should not be exceeded during component assembly, mechanical stress testing, or standard drop and shipping conditions. All dynamic requirements are under room temperature conditions while all static requirements are under 125 °C conditions.



Table 3-2. Socket Loading and Deflection Specifications

Parameter	SI Units			Notes
	Min.	Max.	Unit	
Static Compressive Load per Contact	10	25	gf	1
Static Compressive Load, Total (BOL)	180	300	lbf	2, 5
Static Compressive Load, Total (EOL)	138	300	lbf	2
Dynamic Compressive Load	N/A	132	lbf	3
Board Transient Bend Strain - 62 mil board	N/A	480	$\mu\epsilon$	4
Board Transient Bend Strain - 93 mil board	N/A	450	$\mu\epsilon$	4
Board Transient Bend Strain - 120 mil board	N/A	420	$\mu\epsilon$	4

Notes:

1. The compressive load applied by the package on each LGA contact for required electrical performance.
2. The total compressive load applied by the heatsink onto the socket through the processor package.
3. The quasi-static equivalent compressive load applied during the mechanical shock. Dynamic compressive limit has been calculated using the assumption of 2X dynamic amplification factor at CPU location using a 600g heat sink and a 50G table input. The product application can have flexibility in specific values, but the ultimate product of mass times acceleration times corresponding amplification factor should not exceed this dynamic compressive load limit.
4. Maximum allowable strain below socket BGA corners during transient loading events (i.e., slow displacement events) which might occur during board manufacturing, assembly or testing. See the *LGA3647-1 Board Flexure Initiative (BFI) Strain Guidance Sheet*. Contact your Manufacturer Certified Quality Engineer (CQE) representative for this datasheet.
5. The Min. Total Static Compressive Load (BOL) specification only applies to the processor with fabric. (The processor without fabric only requires that the Min. Total Static Compressive Load (EOL) be met over its lifetime.)

The minimum static total compressive load ensures socket reliability over the life of the product and that the contact resistance between the processor and the socket contacts meets the specified values.

3.2 Socket Critical-to-Function Interfaces

The following is a list of Critical-to-function (CTF) attributes for the main board layout and assembled components' interface to the socket. All sockets manufactured meet these specified CTF attributes.

- Socket Package Alignment Cavity Length and Width, and Datum Profile¹
- Fine Alignment (Datum) Guiding Feature Chamfer Dimension
- Socket Body Length and Width, and Intermediate Alignment Profile
- Intermediate Alignment Guiding Feature Chamfer Dimension
- Socket Height (from Package Seating Plane to MB after SMT)¹
- Seating Plane Co-planarity¹
- Through Cavity Length and Width, and X and Y-Position
- Stand-Off Gap (Solder Ball Seating Plane to Stand-Off)
- Solder Ball Feature Relating True Position
- Solder Ball Co-planarity before SMT
- Contact Height Above Seating Plane¹
- Contact True Position¹

1. Dimensions are to be measured at pre and post SMT.



- Contact Co-planarity¹
- PnP Cap Keep-in-zone Flatness¹

3.3 Socket Components

3.3.1 Socket Housing

The socket housing material should be thermoplastic or equivalent, UL 94 V-0 flame rating, temperature rating and design capable of maintaining structural integrity following a temperature of 260 °C for 40 seconds, which is typical of a reflow/rework profile for solder material used on the socket. The material will have a thermal coefficient of expansion in the XY plane capable of passing reliability tests rated for an expected high operating temperature, mounted on low loss, low/High Tg FR4-type main board material. The creep properties of the material will be such that the mechanical integrity of the socket is maintained for the stress conditions outlined in [Appendix A](#).

3.3.1.1 Housing Color

The color of the socket housing will be dark as compared to the solder balls to provide the contrast needed for OEM's pick-and-place vision systems. Components of the socket may be different colors, as long as they meet the above requirement.

3.3.1.2 Socket Insertable Alignment Keys

The alignment keys for the package-to-socket alignment, and to ensure that the correct package is inserted into the socket, should be insertable keys with the option of a molded key for the left socket half only.

3.3.1.3 Package Installation/Removal Access

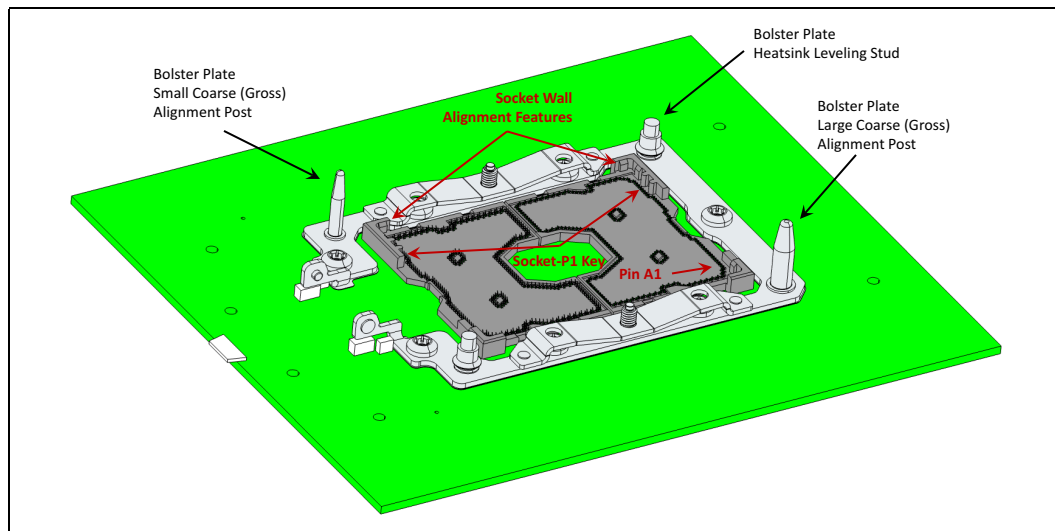
Access will be provided to facilitate the manual insertion and removal of the package. No tool should be required to install or remove the package from the socket.

3.3.1.4 Package Alignment/Orientation

A means of providing fixed alignment and proper orientation with the pin A1 corner of the processor package will be provided. There are three different levels of package alignment:

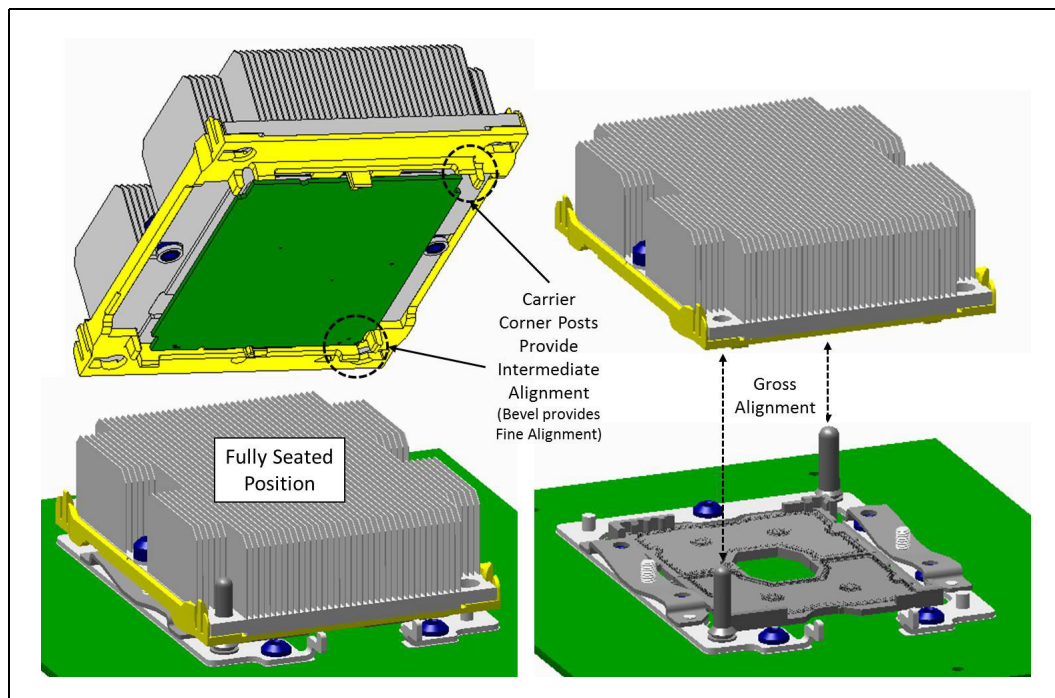
- The first level is called gross alignment, which occurs due to the Bolster Plate posts and corresponding PHLM holes.
- The second level is called intermediate alignment, which utilizes the socket exterior corner walls with a 1.25 mm by 1.75 mm chamfer at the guiding portion.
- The third level is called fine alignment, which relies on the socket corner inner surfaces (datum walls) with a 0.75 mm by 1.00 mm chamfer at the guiding portion.

Figure 3-3. Socket-P1 and Bolster Plate Assembly Alignment Features



The socket also has two orientation posts or protrusions (keys) placed on opposite sides of the socket as noted in [Appendix D](#). The package substrate will have keying notches at the corresponding locations. When package keying notches align with socket orientation posts, it prevents the package from being mistakenly installed with a 180° in-plane rotation (also refer to [Appendix C](#)). The package sits flush on the socket contacts when aligned.

Figure 3-4. Socket-P1, Mechanical Retention Assembly and PHM Alignment





3.3.1.5 Socket Seating Plane for Package

The socket seating plane for the package defines the minimum package height from the main board. See [Section 2](#) for details on package and IHS height above the main board. The datum is defined by the top surfaces of seating plane standoffs which cause a hard stop of package over the socket when the package and socket are loaded. There are primary socket seating planes and secondary socket seating planes.

- Primary seating planes are located at areas where contacts are depopulated and around socket cavity and center split locations as illustrated in [Figure 3-1](#) and [Appendix D](#).
- Secondary seating planes are interstitial seating planes, which are small islands within a pitch range and around each core pin except for manufacturing keep-outs. Refer to [Appendix D](#) for more details.

Both primary and secondary seating plane areas and numbers of the seating planes are maximized to avoid significant creep of the housing material when being loaded. However, the seating plane standoffs should not touch the LGA lands on the bottom of the package. Intel recommends that the nominal height of interstitial seating planes be the same as the nominal height of primary seating planes, but the highest points of interstitial seating planes will be no higher than the highest points of primary socket seating planes. The seating plane co-planarity needs to meet the specification after the socket has been mounted (soldered) to the board. Refer to [Appendix D](#) for details.

3.3.1.6 Strength of Socket Housing Material

The material of the socket housing is required to have a minimum yield strength of 35 MPa at 90 °C to minimize the risk of seating plane deformation.

3.3.1.7 Socket Standoffs

Standoffs will be provided on the solder ball side of the socket base to ensure the minimum socket height after solder reflow and to prevent socket housing over deflection after being loaded. It is required that wherever there is a top side primary socket seating plane for a package, there should be a corresponding standoff on the bottom side. A gap between the solder-ball seating plane and the standoff prior to reflow is required to assure sufficient ball collapse during the surface mount process.

3.3.2 Markings

All markings required in this section can withstand a temperature of 260 °C for 40 seconds, which is typical of a reflow/rework profile for solder material used on the socket, as well as any environmental test procedure outlined in [Appendix A](#), without degrading. Socket marks are visible after it is mounted on the main board. Each socket body half is marked with the following:

- Socket Name: LGA3647-1 (preferred font type is Helvetica Bold [min. 4 pt, or 1.5 mm]).

This mark is stamped or laser-marked as shown in the drawings.

- Manufacturer's Insignia (font size at supplier's discretion).

This mark is molded or laser-marked into side wall of the socket.

Both marks are visible after the socket has been surface-mounted to the main board, with bolster plate assembly and pick-and-place cap installed.

- Lot Traceability - Each socket body half is marked with a lot identification code to allow traceability of all components, date of manufacture (year and week), and

assembly location. The mark is placed on a surface that is visible after the socket has been mounted on the main board, with bolster plate assembly and pick-and-place cap installed. In addition, this identification code is marked on the exterior of the box in which the unit is shipped. The preferred font type is Helvetica Bold [min 4 pt, or 1.5 mm].

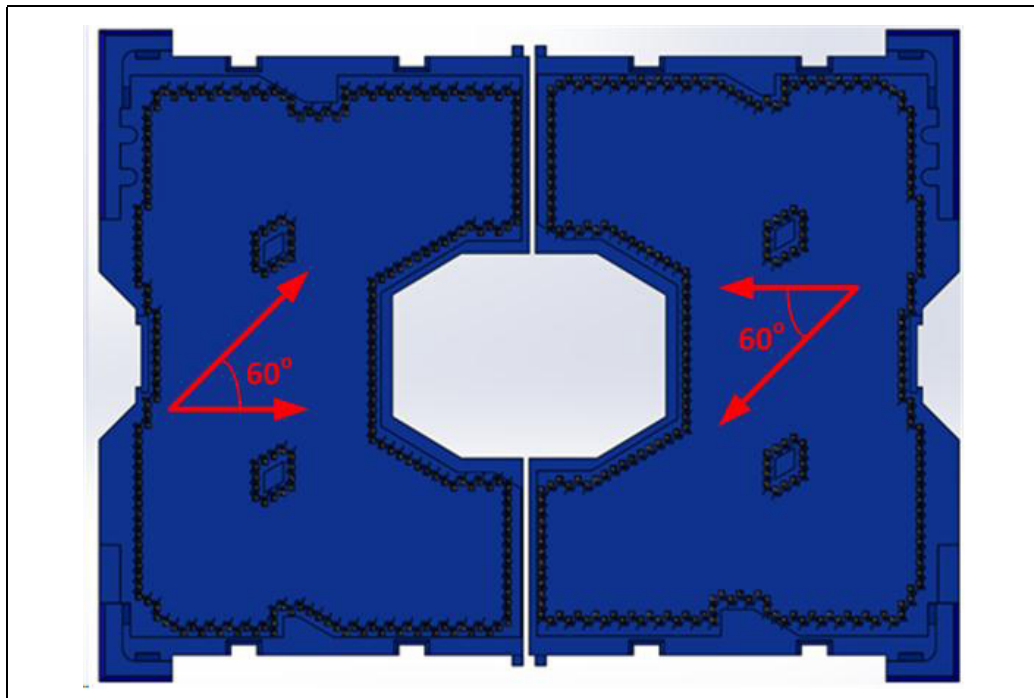
This mark may be laser-marked.

- Visual Aids - The socket will have Pin A1 and package/socket alignment keys.

3.3.3 Socket-Package Contact Characteristics

- Contact Count - The total number of top-side contacts is 3647.
- Layout - The contacts are laid out in two “C” shaped regions opposing each other as shown in [Figure 3-5](#). The arrows in the figure indicate the wiping orientation of the contacts in the two regions to be 60° about the horizontal axis. There are 1823 and 1824 contacts in the right and left halves of the socket, respectively.

Figure 3-5. LGA3647-1 Socket Contact Orientation



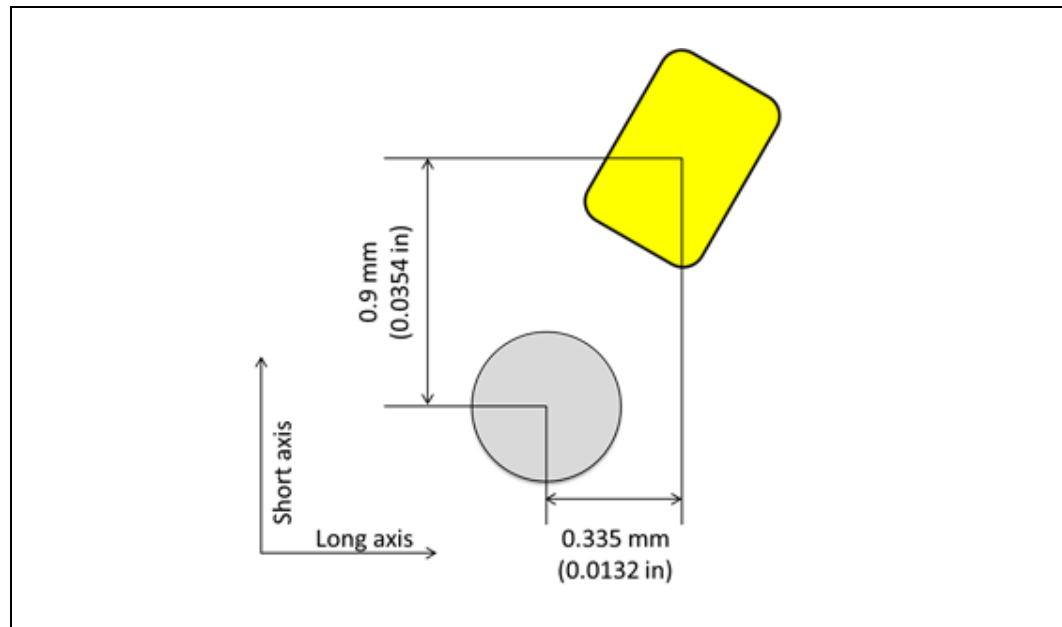
- Contact Base Material - High-strength copper alloy.
- Contact Area Plating - For the area on the socket contacts where the processor lands will mate, there are two SKUs: One with 0.381 μm [15 μinches] and one with 0.762 μm [30 μinches] minimum gold plating thickness, both versions are over a 1.27 μm [50 μinches] minimum nickel under-plating in critical contact areas (area on socket contacts where processor lands will mate) is required. No contamination by solder in the contact area is allowed during solder reflow.
- Paddle - If a paddle is used, the paddle area should be nickel plated to a minimum nickel thickness of 1.27 μm [50 μinches]. The paddle should have sufficient compliance to assure the solder joint reliability under the load conditions in [Table 3-2](#).

- Lubricants - For the final assembled product, no lubricant is permitted on the socket contacts. If lubricants are used elsewhere within the socket assembly, these lubricants must not be able to migrate to the socket contacts.
- Co-Planarity - The co-planarity profile requirement for all contacts on the top side of the socket is defined in [Appendix D](#).
- True Position - The contact pattern has a true position requirement with respect to applicable datum in order to mate with the package land pattern. Refer to [Appendix D](#) for more details.
- Stroke/Load - The maximum vertical height of the contact above the package seating plane is defined in [Appendix D](#). The vertical stroke of the contact will, under all tolerance and warpage conditions, generate a normal force load to ensure compliance with all electrical requirements of the socket. The cumulative normal force load of all contacts must not exceed the load limits defined in [Table 3-2](#).

3.3.3.1 Contact/Pad Mating Location

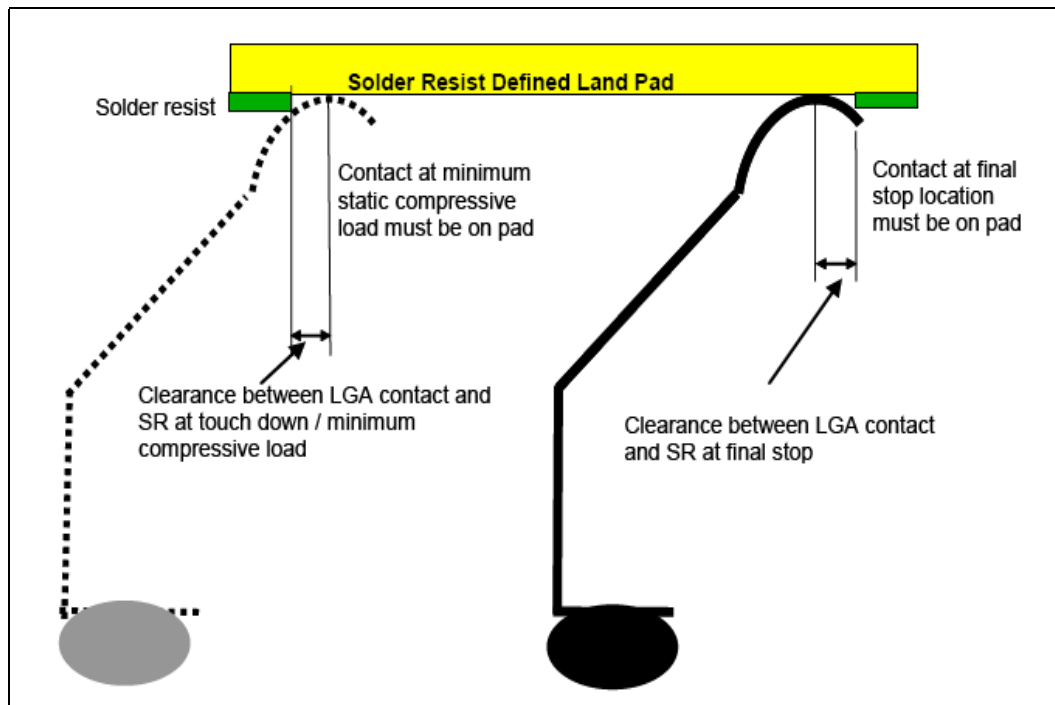
The offset between processor package LGA land center and solder ball center is defined in [Figure 3-6](#). All socket contacts should be designed such that the contact tip does not damage solder resist defining the LGA land during actuation and remains within the substrate pad boundary as illustrated in [Figure 3-7](#). All sockets will also not interfere with solder resist at minimum static compressive load per contact as stated in [Table 3-2](#) and at final installation after actuation load is applied. This requirement includes all the X-Y tolerances such as socket size, substrate size, and pad true positional tolerance, as defined in [Appendix D](#). Also Intel recommends that the contact tip remains within the substrate pad before any actuation load is applied.

Figure 3-6. Offset between LGA Land Center and Solder Ball Center



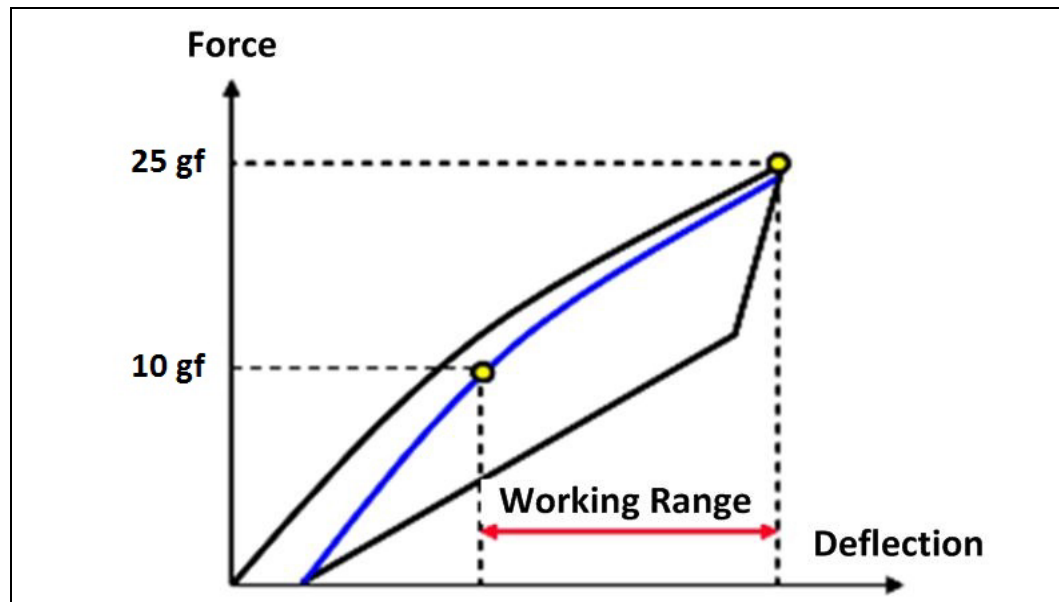
Note: All dimensions are in mm.

Figure 3-7. Offset between LGA Land Center and Solder Ball Center



3.3.3.2 Contact Load-Deflection Curve

The contact should be designed with appropriate spring rate and deflection range, as illustrated by the blue curve in Figure 3-8 to ensure adequate contact normal force in order to meet BOL (upper boundary) and EOL (lower boundary) performance targets at all contact locations. Minimum contact normal force should make the contact meet the electrical requirements. The maximum contact normal force should meet the specification in Table 3-2. The LGA contact working range is defined as the difference of contact deflection at the minimum contact load and the nominal contact deflection.

Figure 3-8. Contact Force Versus Contact Deflection Range


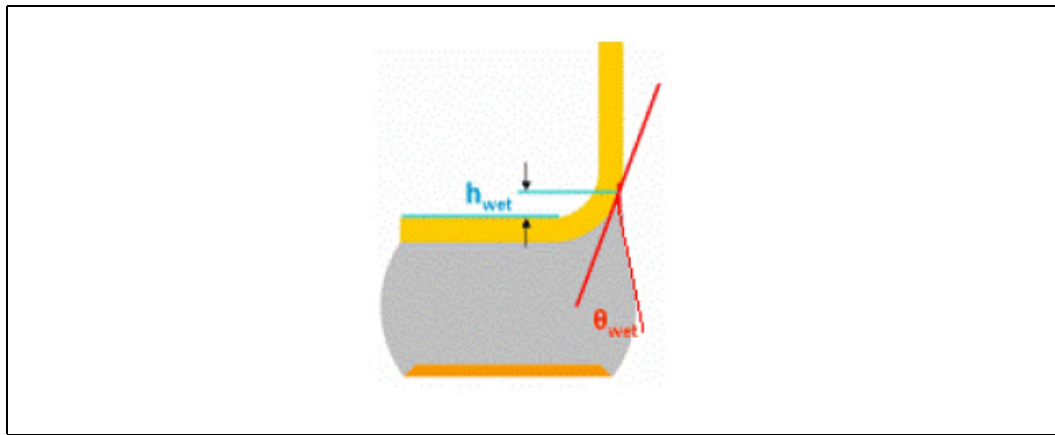
3.3.4 Solder Ball Characteristics

- Solder Ball Count - The total number of solder balls is 3647.
- Layout - The solder balls are laid out in two “C” shaped regions, as shown in [Appendix D](#).
- Material - Lead free SAC (SnAgCu) solder alloy with a silver content between 3% and 4%, with a melting temperature of approximately 217 °C will be used. The alloy will be compatible with standard Lead free processing such as immersion silver and Organic Solderability Preservatives (OSP) main board Surface Mount Technology (SMT) applications as well as a SAC alloy solder paste.
- Co-Planarity - The co-planarity (profile) requirement for all solder balls on the underside of the socket is defined in [Appendix D](#). The specification is applicable to all temperature ranges when surface mounting the socket onto the main board.
- True Position - The solder ball pattern has a true position requirement with respect to applicable datum in order to mate with the main board land pattern. Refer to [Appendix D](#) for details.

3.3.4.1 Solder Ball Wetting Angle for Paddle Design

To minimize the risk associated with shock, vibration, and transient bend stresses, the solder ball wetting angle must be controlled via ball attach process optimization such that the post SMT wetting angle defined in [Figure 3-9](#) is less than or equal to 90 degrees. In the event that a correlation can be identified between wetting height (also defined in [Figure 3-9](#)) and wetting angle, the wetting height may also be used as a measurable success criterion.

Figure 3-9. Wetting Angle and Wetting Height



3.4 Socket Size

The socket size will meet the dimensions as shown in [Appendix D](#), allowing full insertion of the package into the socket without interference. This information should be used in conjunction with the reference main board keep-out drawings provided in [Appendix F](#) to ensure compatibility with the reference thermal mechanical components.

3.5 Actuation and Insertion Requirements

3.5.1 Package Translation

The socket should be built so that the post-actuated seating plane of the package is flush with the seating plane of the socket. Movement will be along the axis normal to the seating plane.

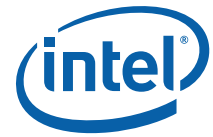
3.5.2 Insertion/Removal/Actuation Forces

Any actuation will meet or exceed *SEMI S8-95 Safety Guidelines for Ergonomics/Human Factors Engineering of Semiconductor Manufacturing Equipment*, example Table R2-7 (Maximum Grip Forces), available at <http://www.semi.org/>.

The socket is designed so that no force is required to insert the package into the socket, and no tool is required to insert or remove the package

Table 3-3. PnP Cover Ergonomics Requirements

Direction	Description	Min.	Max.	Comments
Vertical	Closed position at 260 °C	0.75 lbf	-	While holding at reflow temp.
	Closed position at room temperature.	3 lbf	22 lbf	Pull off force for cap removal.
In and Out of Plane	Shock	0.8 lbf	-	During shipping.
In-Plane	Removal	-	1.7 lbf	Will meet Ergonomic requirements.
	PnP Cap	-	-	+/- 3.5 mils placement accuracy; in-plane slack.



3.6 Orientation in Packaging, Shipping, and Handling

Packaging media supports high-volume manufacturing. Media design will be such that no component of the socket (solder balls, contacts, housing, and so on) is damaged during shipping and handling. Each part number will be shipped from suppliers in separate Joint Electron Device Engineering Council (JEDEC) trays; for example, all left halves of the socket in one tray and all right halves in another. Tray height could be taller than standard.

3.7 Pick-and-Place and Dust Cover

The pick-and-place cover retention will be sufficient to support the socket weight during lifting, translation, and placement. The pick-and-place cover removal force should not exceed 1.7 lbf in the horizontal direction, during manual operation. The pick-and-place cover ergonomics requirements are listed in [Table 3-3](#).

The pick-and-place cover will have openings so that the Pin A1 and keying inserts are visible. To facilitate high-volume manufacturing, the socket should have a detachable cover to support the vacuum type pick-and-place system. The cover will remain on the socket during reflow to help prevent contamination. The cover can withstand 260 °C for 40 seconds (typical reflow/rework profile) without degrading.

The cover design should allow use of a tool to remove the cover. The force required for removing of the cover should comply with the applicable requirements of *SEMI S8-0999 Safety Guidelines for Ergonomics/Human Factors Engineering of Semiconductor Manufacturing Equipment*. The removal of the cover should not cause any damage to the socket body nor to the cover itself.

A separate socket dust cover, a single part covering both halves of the socket, is provided for use after socket and main board integration for use as a protective device to prevent damage to the contact field during handling. See [Appendix E-27](#) and [Appendix E-28](#).

3.7.1 Socket and Pick-and-Place Cover Durability

The socket will withstand 30 cycles of processor insertion and removal. The maximum part average and single pin resistances must be met when mated in the 1st through 30th cycles.

The socket pick-and-place cover will withstand 15 cycles of insertion and removal.

3.8 Keep-In/Keep-Out Zone

Socket keep-in and keep-out zones are identified on the main board to ensure that sufficient space is available for socket placement and to prevent interference between the socket and other components on the main board. These areas are illustrated in [Appendix F](#). It is the responsibility of the socket supplier to identify any required deviation from design guidance identified here.

4 Retention Assembly Mechanical Design

4.1 Mechanical Retention Assembly

Unlike previous Intel processors that use an integrated loading mechanism or ILM, the processor is designed to work with a spring-loading mechanism to provide retention to the main board and the heatsink. Refer to [Appendix E](#) for specific mechanical design details.

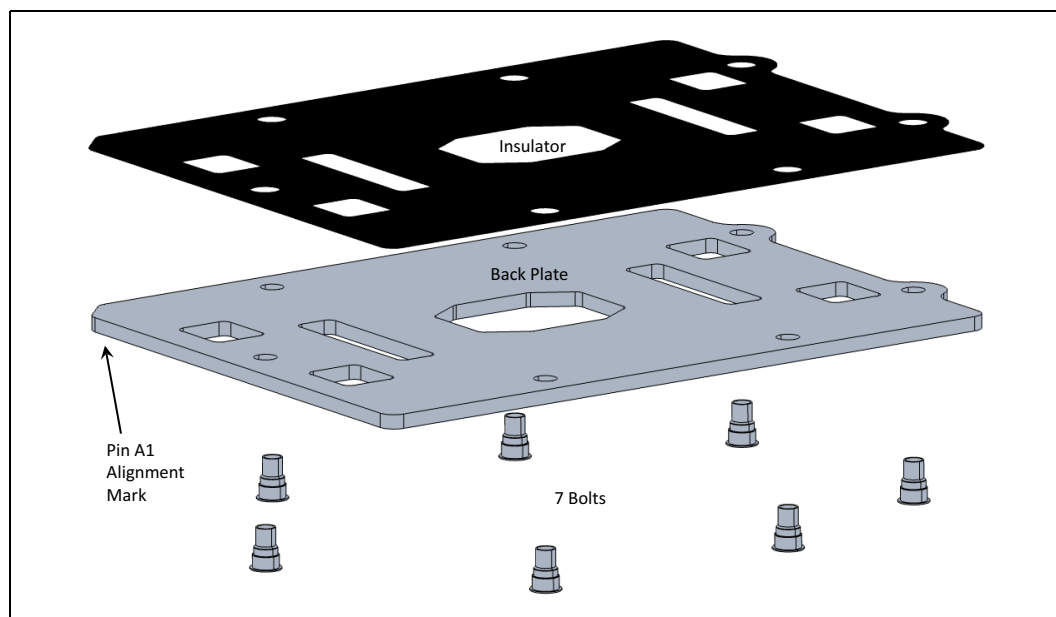
The main components of the socket stack for the processor are:

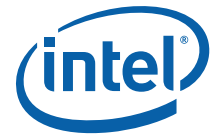
- Backplate
- Bolster plate with spring
- Processor package clip or carrier
- Heatsink

4.1.1 Backplate

The backplate provides structural rigidity to the entire heatsink and processor package retention on the topside of the main board, and helps ensure long-term solder joint reliability. It is 2.2 mm thick and made of carbon-steel material. There are cutouts for component placements on the backside of the main board or socket. The backplate has a total of seven holes for threaded bolts to attach it to the bolster plate on the opposite side of the main board. The number and location of the holes is determined through structural analysis. Between the metal backplate and the main board lies an insulator to isolate the backplate from the routing and vias on the backside of the main board. The total thickness of the backplate and insulator is 2.5 mm.

Figure 4-1. Backplate and Insulator with Mounting Screws



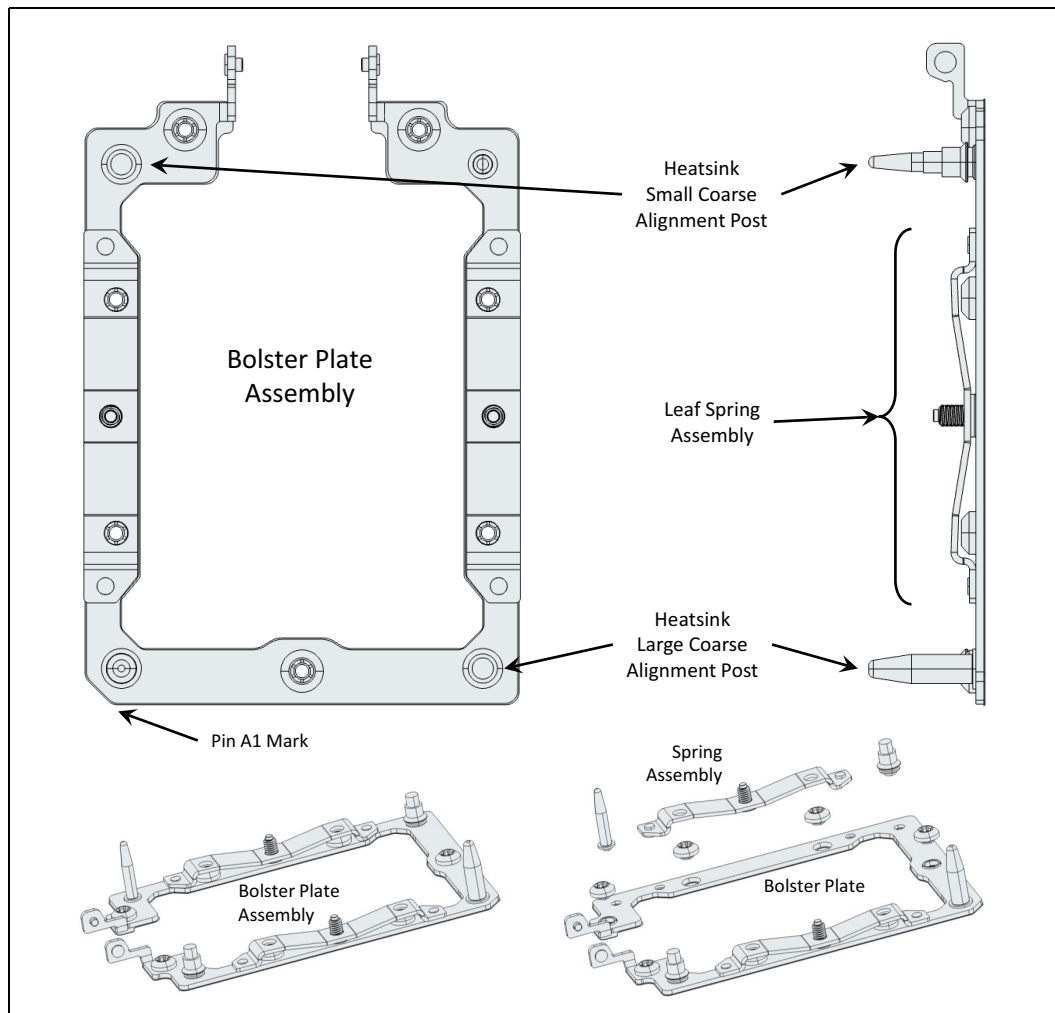


4.1.2 Bolster Plate with Spring

The bolster plate is an integrated subassembly that includes two corner guiding posts placed at opposite corners, nuts to mate with the back plate, and two springs that attach to the heatsink via captive screws. The corner posts guide the Processor Heatsink Module (PHM) as it is lowered over the socket. The corner posts act as coarse position constraints in the X-Y direction to prevent the PHM from moving and potentially damaging the processor package or socket. The springs on either side of the bolster plate are attached via small rivets. The springs attach to the heatsink via screws. The bolster plate screws tighten in nuts on the center of the heatsink. The springs are pulled upward as the heatsink is lowered and tightened in place, creating a compressive force between socket and heatsink. The resulting socket-to-processor contact force ensures maximum contact areas between socket pins and processor package lands, as well as between package and heatsink. The springs provide 180-250 lbf. The springs include stoppers on their outer edges, to prevent movement of the heatsink in the Z-direction due to forces parallel to the main board. The entire bolster plate and spring assembly with nuts and bolts is expected to be supplied as a single unit by vendors.

Note: The PHLM heatsink nuts and bolster plate studs are rated to a durability specification of 12 installation and removal cycles, when using the reference designs with lubrication. Lubrication is required on the bolster plate threaded studs and heatsink nut threads. This is based on the visual inspection criteria of no observed dust/shavings greater than 0.5 mm in length as seen from the naked eye from 24 inches away with direct overhead lighting under cool white fluorescent light conditions [60-120 Ft-Candle (645-1293 LUX)] or equivalent, and a viewing time of one visual pass of 5-7 seconds for each surface. Refer to [Appendix E, "Retention Assembly Mechanical Drawings"](#) for details on the hardware.

Figure 4-2. Bolster Plate and Spring



4.1.3 Processor Package Carrier

The carrier is an integral part of the Processor Heatsink Module (PHM). The processor package is inserted into the carrier, then the Thermal Interface Material (TIM) and heatsink are attached. The carrier design will grab onto the package, and keying features will match cutouts on package. Hook-like features on the four corners of the carrier will grab onto the heatsink. The carrier design changes depending on whether the processor package does or does not integrate fabric.

Figure 4-3. Processor Package Carrier

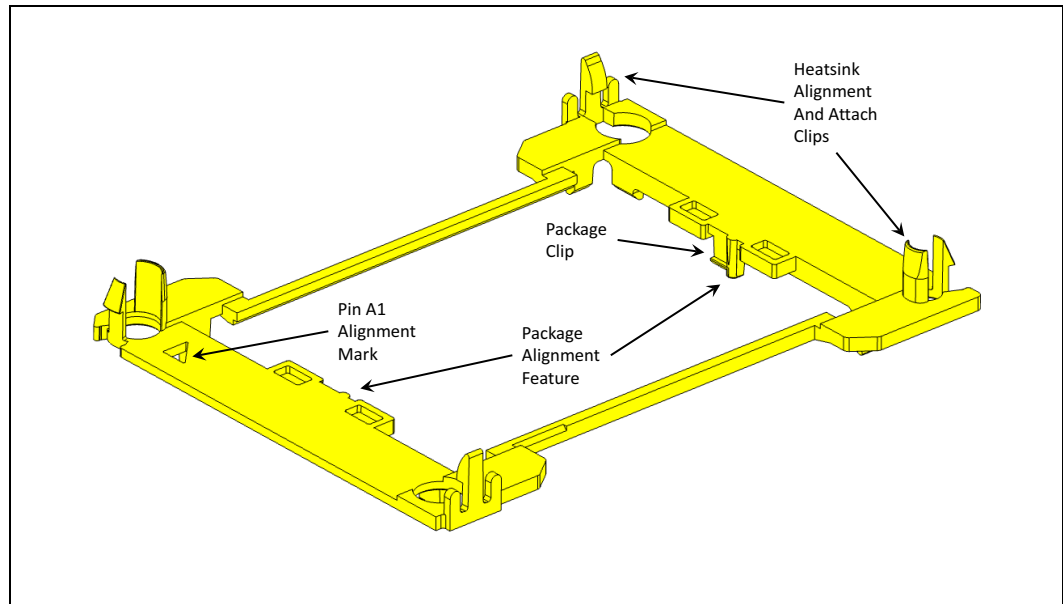
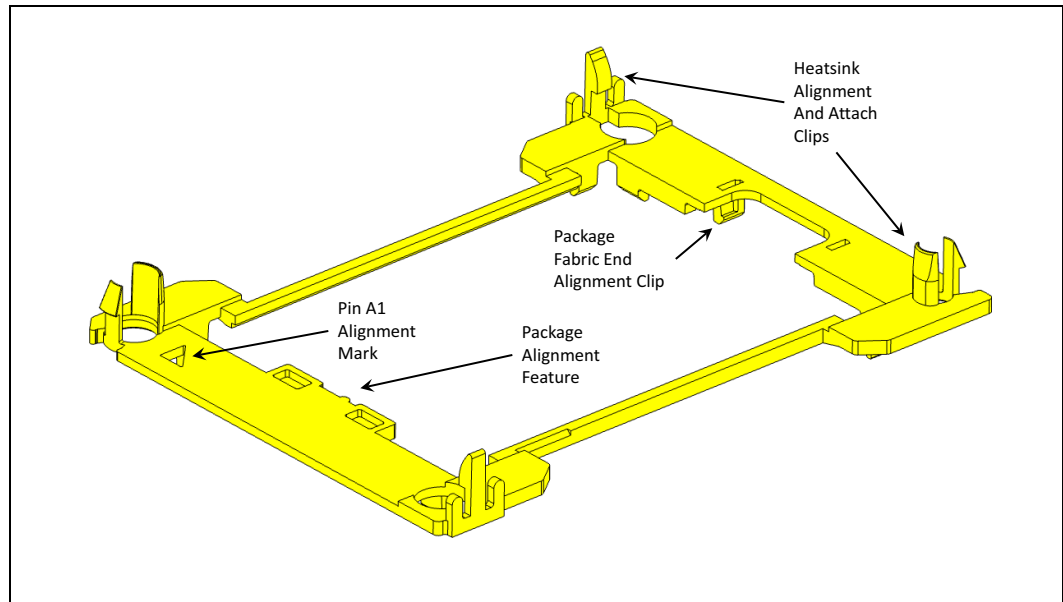


Figure 4-4. Processor with Fabric Package Carrier

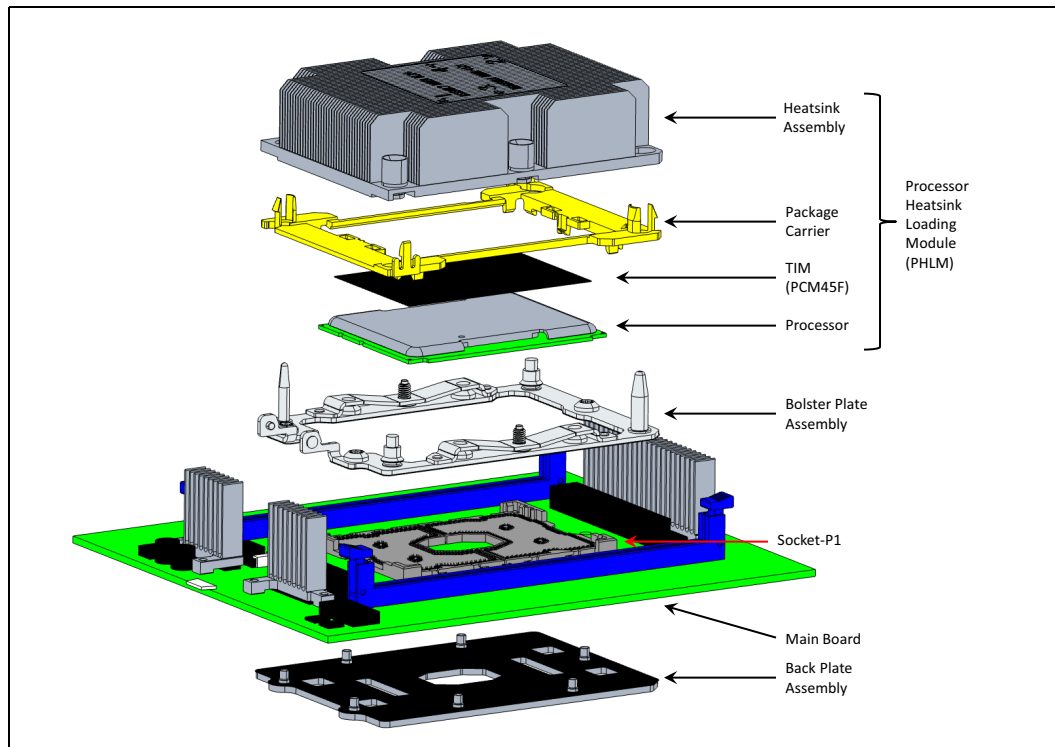


The keying features on the carrier ensure the processor package snaps into the carrier in only one way, and the carrier itself can be attached to the heatsink in only one orientation.

4.1.4 Heatsink

Intel’s heatsink solution requires a maximum volume of 83 mm x 110 mm x 27 mm. It is made of a copper base with aluminum fins. There are 50 fins in total, each 0.3 mm thick. The heatsink is integrated into the PHM which is attached to the bolster plate springs via two captive nuts (T-30 Torx bit) on either side of the heatsink. The bolster plate is held in place around the socket by the back plate.

Figure 4-5. Processor Mechanical Assembly



4.2 Mechanical Load Specifications

The bolster and the back plates are defined to meet the socket loading requirement and to support the mass of the PHM in the socket during shock and vibration. PHM retention mechanism has three critical functions:

- Deliver the force to seat the processor into the socket contacts.
- Distribute the resulting load evenly through the socket solder balls.
- Ensure electrical integrity/performance of the socket and package.

Mechanical specifications for the retention mechanism are defined to meet the requirements stated above.

**Table 4-1. Bolster Plate Mechanical Load Specifications**

Parameter	Min.	Max.	Notes
Total Heatsink Static Compressive Load	138 lbf (EOL)	300 lbf (BOL)	1, 3
Dynamic Load (with heatsink installed)	N/A	132 lbf	1, 2
TIM Activation Pressure	20 psi	N/A	

Notes:

- These specifications apply to uniform compressive loading in a direction perpendicular to the IHS top surface.
- Dynamic loading is defined as heatsink mass (0.6 kg) x 50 g load superimposed for an 11 ms duration average on the static load requirement.
- Bolster plate designs for the processor with fabric must meet an additional criteria (min. total static compressive load, BOL), as given in [Table 3-2](#). To achieve this, additional factors such as loading module tolerances, package stack tolerances, load degradation, etc. must be considered.

Table 4-2. Back Plate Design Criteria

Parameter	Value	Note
Material thickness	2.2 mm	To meet the PCB secondary side clearance requirement. Does not include insulator thickness.
Insulator thickness	0.178 mm	
Tensile yield strength	250 MPa	
Flatness	within 0.2 mm	Measured in unconstrained state, see drawing notes in Appendix E-1 .
PEM* Insert Pull-out Force	667 N	Self-clinching backplate studs
PEM Insert Torque Out	2.25 N-m	Self-clinching backplate studs
Outside perimeter	81.6 x 108.6 mm	Customizing beyond this perimeter of back plate should meet the reliability objectives.
Cavity (7 total cutouts)		See back plate mechanical drawings for details.

Table 4-3. Bolster Plate Design Criteria

Parameter	Value	Note
Material thickness	1.5 mm	To meet the PCB primary side clearance requirement
Insulator thickness	0.178 mm	
Tensile yield strength	758 - 930 MPa	
Flatness	1.0 mm	Measured in unconstrained state, see drawing notes in Appendix E-4 .



4.3 Heatsink Mechanical Requirements

The mass of the heatsink (HS) should not exceed 600 g. The heatsink mass limit and the use of a back plate have eliminated the need for Direct Chassis Attach retention in some implementations. Direct contact between back plate and chassis pan will help minimize board deflection during shock. [Table 4-4](#) lists heatsink mechanical attributes.

Table 4-4. Heatsink Mechanical Attributes

Attribute	Target	Comments
Stiffness ¹	> 600 lbf/mm > 1250 lbf/mm > 1400 lbf/mm	Short span point load Long span Short span distributed load
Flatness	0.077 mm (manifesting)	Processor local flatness zone in drawing
Base Thickness	> 4.5 mm w/ Cu HS base	Requires new PHM clip for thickness > 4.5 mm (reference HS base = 4.5 mm)
Static Load (Max)	< 300 lbf	Thermal validation at 200 lbf shown
Dynamic Load (Max)	< 132 lbf	Based on 600 g HS. Current HS mass = 424 g

Notes:

1. Heatsinks that do not meet or exceed these stiffness specifications will not be capable of providing the long term loading that the LGA3647 socket requires. These stiffness specifications are related to socket reliability; any potential thermal impact due to heatsink base deflection at lower stiffness levels needs to be determined separately.



5 Board and System Design Guidelines

5.1 Mechanical Design Considerations

The processor mechanical retention assembly design and reference thermal solution provided are appropriate for a Intel Xeon Phi Processor x200 Product Family-based platform reference board integrated into a half-width 1U air-cooled server rack enclosure. Any use of these components in a platform or configuration different from the Intel reference platform requires a complete thermal and mechanical design and validation in accordance with the customer design criteria. Also, if customer thermal and mechanical validation criteria differ from the Intel criteria, the reference solution should be validated against the customers design criteria. In all cases, customers must validate their thermal and mechanical solution in accordance with their design and environmental validation criteria, and should not rely solely on these design guidelines.

5.1.1 Components Volumetric

The baseboard Keep-Out Zones (KOZs) on the primary and secondary sides and height restrictions under the enabling component region are shown in detail in [Appendix F](#). The overall volumetric keep-in zone encapsulates the processor, socket, and the entire thermal/mechanical enabling assembly.

5.1.2 Components Mass

The Static Compressive Load should also be considered in dynamic assessments.

Direct contact between back plate and chassis pan will usually help minimize board deflection during shock.

Table 5-1. LGA3647-1 Socket and Retention Component Mass

Component	Mass ¹
LGA3647-1 Socket Body, Contacts and PnP Cover	42 g (21 g per half)
Backplate Assembly	134.8 g
Bolster Plate Assembly	62.1 g
Processor Package	Processor: 88.8 g Processor with Fabric: 91.4 g
Carrier	Processor: 6.8 g Processor with Fabric: 6.2 g
Heatsink	< 600 g ²

Notes:

1. May vary from supplier to supplier.
2. The reference heatsink mass is 424 g.



5.1.3 Package/Socket Stack-up Height

The integrated stack-up height (from the top of the board to the top of the IHS) of a processor package and LGA3647-1 socket with the processor fully seated in the socket is 6.99 ± 0.352 mm.

1. This data is provided for information only, and should be derived from:
 - a. The height of the socket seating plane above the main board after reflow, given in [Appendix D](#).
 - b. The height of the package, from the package seating plane to the top of the IHS, and accounting for its nominal variation and tolerances that are given in [Appendix C](#).
2. This value is derived from a 3σ Root-Sum-Square (RSS) calculation.

5.2 Printed Circuit Board (PCB) Design Considerations

5.2.1 Allowable Board Thickness

The components described in this document (namely back plate, bolster plate and heatsink assemblies) support nominal board thicknesses in the range of 1.575 - 2.362 mm (0.062" - 0.093"). (The overall range including tolerances is given in [Appendix E-1](#).) Boards outside this range may require modifications to the back plate and heatsink retention.

5.2.2 Reference Board Layout

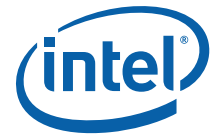
The processor reference board is a single node PCB 173 x 360 mm (6.8 x 14.2 inches) intended for a 1U rack (half width). In principle two boards could be arranged side-by-side in a 1U rack, allowing 2 nodes per 1U in a full width rack. Denser configurations may be possible, but are not considered in this document.

5.2.3 Board Keep-outs

Each of the components described in this document may require an area beyond its physical size to accommodate component movement. In identifying the board keep-outs one should also consider board and system assembly processes and tools. As a reference, recommended board keep-out drawings (PCB top and bottom side) for the LGA3647-1 socket, bolster plate, back plate and heatsink are made available in [Appendix F](#). PCB keep-outs include attach hole locations and sizes, component height limits in the vicinity of the socket, and recommended areas to allow access to the socket for processor installation.

5.2.4 Suggested Silkscreen Marking for Socket Identification

Intel is recommending that the socket name be silkscreened adjacent to the socket such that it is visible after the bolster plate is installed.



5.2.5 Board Deflection

Exceeding the maximum Board Deflection called out in [Table 3-2](#) may result in socket solder joint failure. Board deflection under the LGA3647-1 socket will be kept to an acceptable level by adhering to the following conditions:

1. Following the design objectives of the Intel reference heatsink and back plate
2. Maintaining compliance to maximum static compressive load values

Placement of board-to-chassis mounting holes also impacts board deflection and resultant socket solder ball stress. Customers should explore the impact of mechanical shock for their designs as their heatsink retention, heatsink mass and chassis mounting holes may vary.

5.3 Fabric Cable Assembly Design Guidance

This section applies only to designs supporting the processor with fabric.

- CPU Package Mechanical Design: Refer to [Section 2](#) and [Appendix C](#) for the processor with fabric package design details.
- Socket-P1 (LGA3647-1): The same socket supports both the processor and the processor with fabric. There are no additional socket design issues to consider.
- Mechanical Retention Assembly Design: Refer to [Section 4](#) and [Appendix E](#) for the processor with fabric mechanical retention assembly design details. Note that only the carrier differs for the two variations of the processor package (with and without fabric).

In addition to the processor with fabric package and carrier differences noted above, the designer also should consider how the fabric interface is connected in the platform. This connection is accomplished using the Intel Fabric Passive (IFP) cable. Additional IFP cable-specific design information may be included in a future revision of this design guide.



6 Thermal Specifications and Design Guidelines

6.1 Thermal Specification Overview

The processor is a Multi-Chip Package (MCP), meaning it has integrated multiple silicon devices onto the processor substrate. These devices include the processor (CPU) die, eight Multi-Chip DRAMs (MCDRAMs) and, in some configurations, a networking (or fabric) controller die. See [Figure 2-1](#) and [Figure 2-2](#). Although there are multiple components on the processor package, there will be a single Integrated Heat Spreader (IHS) on the MCP which serves as an interface to the system thermal solution.

The MCP requires the thermal solution to maintain die temperatures within the specified operating limits for all devices in the MCP. Any attempt to operate the processor or other die outside these limits may result in permanent damage to the processor and potentially other components within the system. Maintaining the proper thermal environment is key to optimal and reliable, long-term processor and system operation.

A complete thermal solution includes both component- and system-level thermal management features. Component-level thermal solutions can include active or passive heatsinks attached to the processors' IHS. Typical system-level thermal solutions may consist of system fans combined with ducting and venting.

6.1.1 Thermal Design Power (TDP) and T_{CASE} Specifications

[Table 6-1](#) and [Table 6-2](#) list the Thermal Design Power (TDP) and T_{CASE} values for the different processor SKUs, under both CPU- and memory-centric workloads.

Table 6-1. TDP and T_{CASE} Specifications - 215W/230W SKUs

Workload	Processor		Processor with Fabric	
	CPU Centric	Memory Centric	CPU Centric	Memory Centric
CPU Power	185W	147W	185W	147W
Memory Power	30W	68W	30W	68W
IOP Fabric Die Power	N/A		15W	
Total Power	215W		230W	
CPU Die Maximum T_{CASE}	82 °C	N/A ¹	84 °C	N/A ¹
MCDRAM Die Maximum T_{CASE}	N/A ²	72 °C	N/A ²	75 °C
Fabric Die Maximum T_{CASE}	N/A		N/A ³	
Minimum T_{CASE}⁴	5 °C			

Notes:

1. Memory-centric workloads: CPU T_{CASE} is expected to be lower than the maximum CPU T_{CASE} target.
2. CPU-centric workloads: Memory T_{CASE} is expected to be lower than the maximum memory T_{CASE} target.
3. Fabric die T_{CASE} targets: The fabric die is expected to remain below its maximum allowable temperature for all workloads, as long as the thermal solution provides adequate cooling to the CPU and MCDRAM die.
4. ASHRAE thermal envelopes allow scenarios where the data center ambient temperature may drop below 5 °C, down to 0 °C. However, the processor silicon temperatures are expected to quickly rise above 5 °C once operational. Contact your Intel representative if you believe your data center implementation warrants further consideration of minimum operational temperatures down to 0 °C.



Table 6-2. TDP and T_{CASE} Specifications - 245W/260W SKUs

Workload	Processor		Processor with Fabric	
	CPU Centric	Memory Centric	CPU Centric	Memory Centric
CPU Power	215W	177W	215W	177W
Memory Power	30W	68W	30W	68W
IOP Fabric Die Power	N/A		15W	
Total Power	245W		260W	
CPU Die Maximum T_{CASE}	72 °C	N/A ¹	74 °C	N/A ¹
MCDRAM Die Maximum T_{CASE}	N/A ²	N/A ¹	N/A ²	N/A ¹
Fabric Die Maximum T_{CASE}	N/A		N/A ³	
Minimum T_{CASE}⁴	5 °C			

Notes:

1. Memory-centric workloads: CPU T_{CASE} is expected to be lower than the maximum CPU T_{CASE} target. The MCDRAM die are expected to remain below their maximum allowable temperature, as long as the thermal solution provides adequate cooling to the CPU die.
2. CPU-centric workloads: Memory T_{CASE} is expected to be lower than the maximum memory T_{CASE} target.
3. Fabric die T_{CASE} targets: The fabric die is expected to remain below its maximum allowable temperature for all workloads, as long as the thermal solution provides adequate cooling to the CPU and MCDRAM die.
4. ASHRAE thermal envelopes allow scenarios where the data center ambient temperature may drop below 5 °C, down to 0 °C. However, the processor silicon temperatures are expected to quickly rise above 5 °C once operational. Contact your Intel representative if you believe your data center implementation warrants further consideration of minimum operational temperatures down to 0 °C.

CPU-centric workloads are those applications that are heavily compute-intensive and are able to concentrate the code and data within the processor’s on-die cache. These applications would be expected to maximize the power consumption of the CPU silicon and reduce the MCDRAM power. As an example, applications that make extensive use of the Intel® Advanced Vector Extensions (Intel® AVX) instructions would be considered CPU-centric.

Memory-centric workloads would typically be working with data sets that require significant transfers between the processor silicon and the on-package MCDRAMs, or perhaps even the off-package DDR4 system memory. These applications would be expected to maximize the power consumption of the MCDRAM silicon and reduce the CPU die power consumption.

Thermal Design Power (TDP) of the processor is not the same as the absolute maximum possible power draw. TDP is the maximum continuous power dissipation that has been measured when running commercially-available benchmarks and applications. Applications often have very short duration power spikes (10s to 100s of micro-seconds) above TDP. These short power spikes are not thermally significant, but they do require the power delivery system to be designed appropriately.

What happens in the unlikely event that an application is developed that continuously draws more power than TDP? The answer depends on a variety of factors, but one of the key factors is the system ambient temperature. If the ambient temperature is below the maximum specified for the chassis, the thermal solution may have enough headroom to keep the processor within its defined temperature range. If the ambient temperature is close to maximum, the processor may reach, or exceed, its maximum permissible operating temperature. In this situation, the system and processor will pursue multiple actions to ensure staying below temperature targets.



Thermal validation considerations: Due to the challenges involved with measuring real-time power on operational processors, Intel recommends using a Thermal Test Vehicle (TTV) to validate the platform thermal solution. The TTV enables precise control of the CPU, MCDRAM and Fabric die power dissipation, and ensures accurate, precise and repeatable T_{CASE} temperature measurements.

6.1.2 Case Temperature Geometry and Influence Factors

The processor MCP requires careful monitoring and control of temperatures on multiple silicon die inside the package. The case temperature is defined as the temperature measured at various locations on the surface of the Integrated Heat Spreader (IHS) above these component die hot spots. The IHS maximum case temperature (T_{CASE}) specifications for the processor and MCDRAM die are listed in [Table 6-1](#). No case temperature is required for the fabric die.

Three case temperature (T_{CASE}) locations are defined for the processor MCPs: one for the processor die and two options for the MCDRAM die. See [Figure 6-1](#) and [Figure 6-2](#) for the T_{CASE} locations.

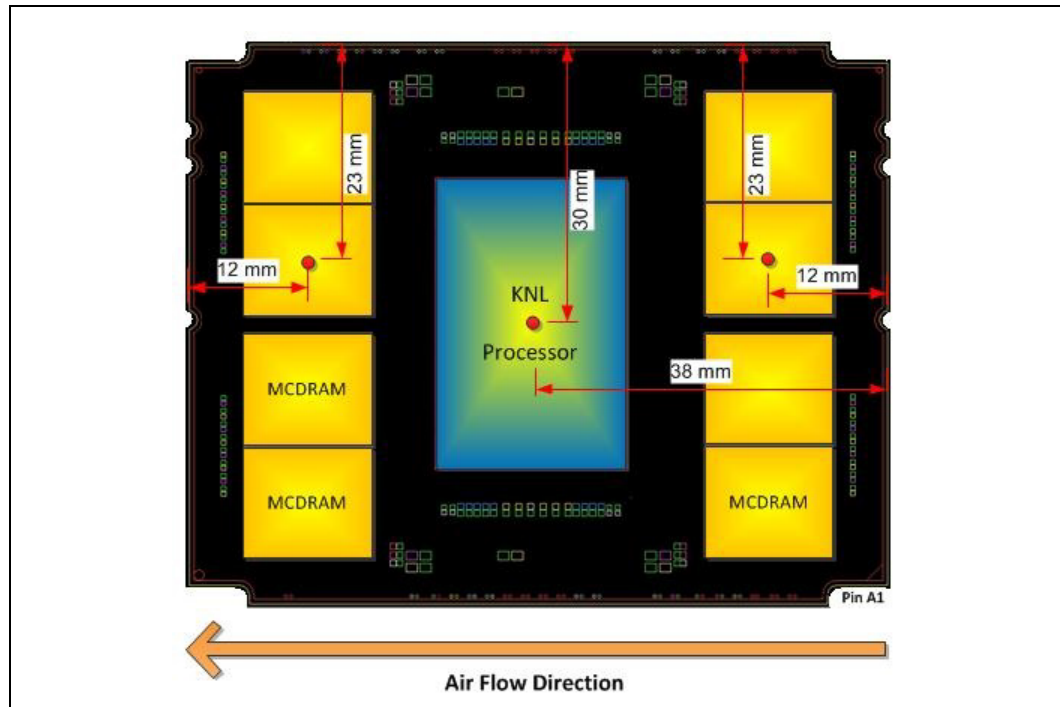
Which MCDRAM T_{CASE} location to measure depends upon the direction of airflow through the heatsink. Use the location that is downstream from the processor die (meaning the air moving over the MCDRAM has been preheated by the processor die) as this will ensure the worst case MCDRAM conditions are evaluated. The thermocouple location for the MCDRAMs is chosen to reflect the worst case hot spot on the hottest memory silicon die. The hottest MCDRAM die is expected to be either interior downstream device; the upper middle device is chosen in [Figure 6-1](#) and [Figure 6-2](#).

Design and validation of a thermal solution which properly cools all the components in a MCP drives the need to measure the IHS case temperature above the worst-case location for each different type of device.

The processor will generally exhibit higher temperatures on the IHS at the locations coinciding with the processor and MCDRAM die. The IHS has a heat spreading effect. The temperature delta between silicon die hot spots and the IHS geometric center vary depending on the total dissipated power and the power distribution between the processor and MCDRAM die.



Figure 6-1. Processor Package Thermocouple Locations, Top view



The processor and MCDRAM T_{CASE} value will be influenced by the other powered devices integrated on the MCP. This relationship is described in the following equations:

$$T_{CASE_CPU} = T_{LA} + \Psi_{CC} * P_{CPU} + \Psi_{CM} * P_{MCDRAM} + \Psi_{CF} * P_{Fabric}$$

$$T_{CASE_MCDRAM} = T_{LA} + \Psi_{MC} * P_{CPU} + \Psi_{MM} * P_{MCDRAM} + \Psi_{MF} * P_{Fabric}$$

Table 6-3. Processor T_{CASE} Influence Parameters

Parameter	Description	Reference Solution Expected Value
T _{case_CPU}	Temperature on the IHS surface above the processor hot spot	Calculated
T _{case_MCDRAM}	Temperature on the IHS surface above the MCDRAM hot spot	Calculated
T _{LA}	Temperature of the local ambient air at the heatsink inlet	< 40 °C
P _{CPU}	Power dissipated by the processor	Workload Dependent ¹
P _{MCDRAM}	Power dissipated by MCDRAMs	Workload Dependent ¹
P _{FABRIC}	Power dissipated by the fabric controller (processor with fabric only)	Workload Dependent ¹
Ψ _{CC}	Thermal resistance: IHS processor hot spot due to its own power	0.212 °C/W
Ψ _{CM}	Thermal resistance: IHS processor hot spot due to MCDRAM power	0.134 °C/W
Ψ _{CF}	Thermal resistance: IHS processor hot spot due to fabric power	0.140 °C/W
Ψ _{MC}	Thermal resistance: IHS MCDRAM hot spot due to processor power	0.147 °C/W
Ψ _{MM}	Thermal resistance: IHS MCDRAM hot spot due to its own power	0.177 °C/W
Ψ _{MF}	Thermal resistance: IHS MCDRAM hot spot due to fabric power	0.196 °C/W

Note: 1. Though the constituent device powers may vary with workload, the combined powers must add up to be less than or equal to the Thermal Design Power (TDP).

The processor and MCDRAM power varies dramatically by workload and they do not achieve their maximum allowable values concurrently. Thus, a processor-centric workload maximizes processor power while typically drawing lower MCDRAM power. Conversely, a memory centric workload maximizes MCDRAM power while requiring concurrently a processor power lower than that of the processor centric workload. This is very important to consider when analyzing, designing and testing T_{CASE} thermal solutions.

A couple of processor with fabric examples are provided to illustrate these relationships, with values representing the Intel reference thermal solution:

Example 1: Processor T_{CASE} based on a hypothetical processor centric type workload.

$$T_{CASE_CPU} = T_{LA} + \Psi_{CC} * P_{CPU} + \Psi_{CM} * P_{MCDRAM} + \Psi_{CF} * P_{Fabric}$$

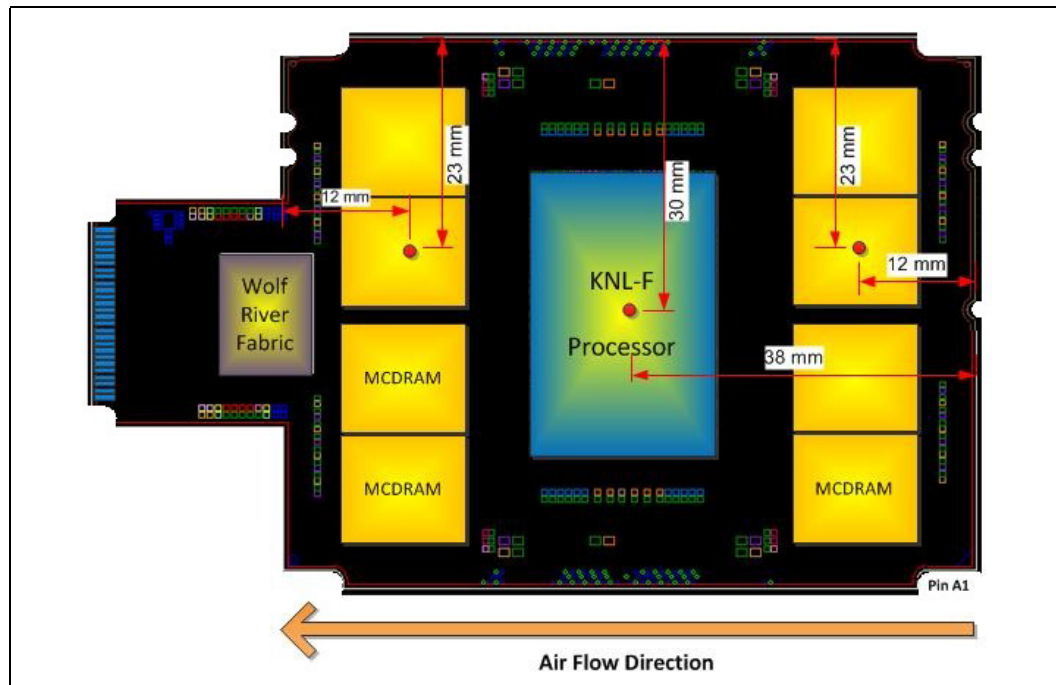
$$= 40 + (0.212) * (185) + (0.134) * (30) + (0.140) * (15) = 85 \text{ }^{\circ}\text{C}$$

Example 2: MCDRAM T_{CASE} based on a hypothetical memory centric type workload.

$$T_{CASE_MCDRAM} = T_{LA} + \Psi_{MC} * P_{CPU} + \Psi_{MM} * P_{MCDRAM} + \Psi_{MF} * P_{Fabric}$$

$$= 40 + (0.147) * (147) + (0.177) * (68) + (0.196) * (15) = 75 \text{ }^{\circ}\text{C}$$

Figure 6-2. Processor with Fabric T_{CASE} Measurement Locations.



Notice, the processor with fabric is not symmetric with respect to the airflow direction. In the previous figure the Fabric die is downstream from the processor and MCDRAM die and thus preheated by the air flowing across these die. The orientation of the package impacts the processor thermal performance.

Finally, it is well known that thermal resistance has a strong dependence on system thermal design parameters such as volumetric airflow. The reference design thermal resistivity dependence on volumetric airflow is illustrated in [Figure 6-3](#).

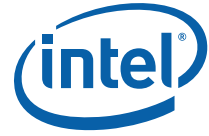
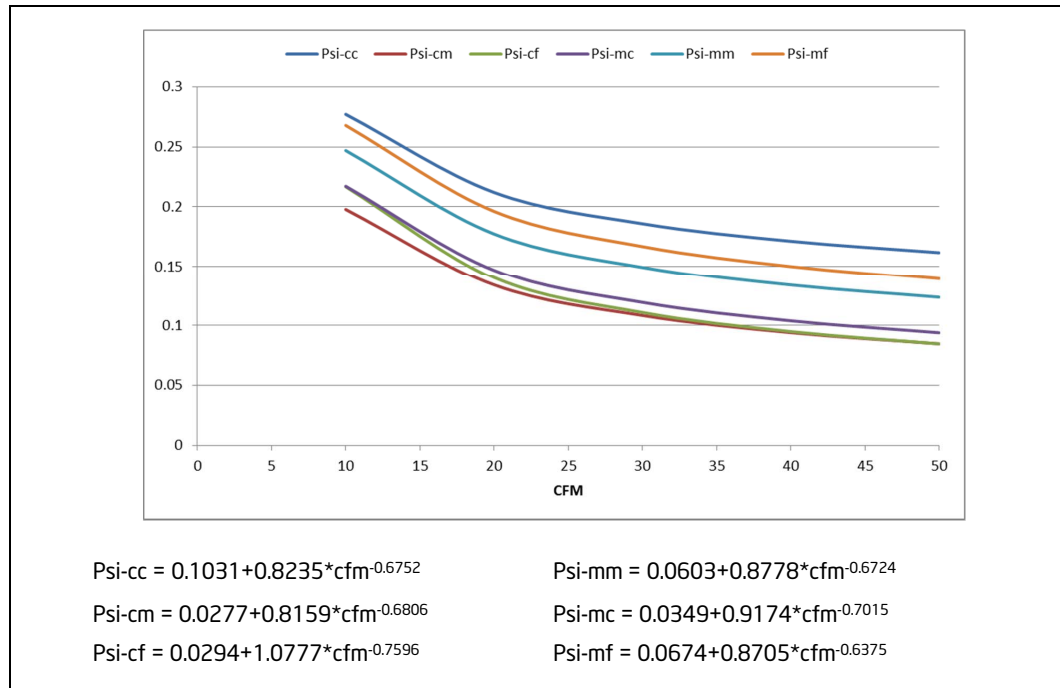


Figure 6-3. Psi Curves for the Reference Thermal Solution (Mean+3 Sigma)



6.1.3 Socket Maximum Temperature

The power dissipated within the socket is a function of the current at the pin level and the effective pin resistance. To ensure socket long term reliability, Intel defines socket maximum temperature using a via on the underside of the main board. Exceeding the temperature guidance may result in socket body deformation, or increases in thermal and electrical resistance which can cause a thermal runaway and eventual electrical failure. The guidance for socket maximum temperature is listed below:

- Via temperature under socket must be <95 °C.
- The specific via used for temperature measurement is located on the bottom of the motherboard between pins BN6 and BJ6.
- The socket maximum temperature is defined at Thermal Design Current (TDC). In addition, the heatsink performance targets and boundary conditions must be met to limit power and thermal dissipation through the socket.

To measure via temperature:

- Drill a hole through the back plate corresponding to the location of pins BN6 and BJ6.
- Thread a T-type thermocouple (36 - 40 gauge) through the hole and glue it into the specific measurement via on the underside of the motherboard.
- Once the glue dries, reinstall the back plate and measure the temperature.



6.1.4 Storage Conditions Specifications

Environmental storage condition limits define the temperature and relative humidity limits to which the device is exposed while being stored in a moisture barrier bag. The specified storage conditions are for component level prior to board installation.

Table 6-4 specifies absolute maximum and minimum storage temperature limits which represent the maximum or minimum device condition beyond which damage, latent or otherwise, may occur. The table also specifies sustained storage temperature, relative humidity, and time-duration limits. These limits specify the maximum or minimum device storage conditions for a sustained period of time. At conditions outside sustained limits, but within absolute maximum and minimum ratings, quality, and reliability may be affected.

Table 6-4. Storage Condition Ratings

Symbol	Parameter	Min.	Max.	Unit
$T_{\text{sustained storage}}$	A prolonged or extended period of time; typically associated with sustained storage conditions. Unopened bag, includes 6 months storage time by customer.	0	30	months
$T_{\text{short term storage}}$	A short period of time (in shipping media).	0	72	hours
$T_{\text{absolute storage}}$	The minimum/maximum device storage temperature beyond which damage (latent or otherwise) may occur when subjected to for any length of time.	-25	125	°C
$T_{\text{sustained storage}}$	The minimum/maximum device storage temperature for a sustained period of time.	-5	40	°C
$T_{\text{short term storage}}$	The ambient storage temperature (in shipping media) for a short period of time.	-20	85	°C
$RH_{\text{sustained storage}}$	The maximum device storage relative humidity for a sustained period of time.	60% @ 24		°C

6.1.5 Reference Design Thermal Interface Material (TIM)

Applying thermal interface material between the processor IHS and the heatsink base will improve the heat transfer between the IHS and the heatsink. Honeywell* PCM45F material is selected for use with the Intel reference heatsink design.

The recommended size ensures adequate coverage at the interface between the processor IHS and heatsink pedestal.

Table 6-5. TIM Specification

Parameter	Value	Unit	Notes
TIM Size	47 x 70 x 0.25	mm	Dimensions apply to Honeywell* PCM45F p/n: H38442
PCM45F Activation Load	340	N	Load required to meet min. TIM pressure (15 psi)

Refer to the TIM manufacturer’s guidelines for specifications and handling instructions.



6.1.6 Reference Thermal Solution Performance Targets

Table 6-6 provides thermal boundary conditions and performance targets for the processor. These values serve as guidance for designing a processor compatible thermal solution. Heatsink design compliance can be determined with thermocouples and TTVs.

Table 6-6. Reference Heatsink Boundary Conditions and Performance Targets

Parameter	Processor	Processor with Fabric	Notes
TDP	215W	230W	
T _{LA} (max)	40 °C		1
System height (form factor)	1U		2
Heatsink volumetric	Overall: 80 x 107 x 27 mm (W x L x H)		3
Heatsink Technology	Cu base with Al fins		

Notes:

1. Local ambient temperature of the air entering the heatsink.
2. Reference system configuration. 1U = 1.75 inches.
3. Dimensions of reference heatsink do not include socket, processor, or other retention assembly components.

6.2 Thermal Design and Management Guidelines

6.2.1 System Thermal Environmental Conditions

6.2.1.1 Ambient Temperature

The temperature of the inlet air entering the processor heatsink module is referenced in this document as the local ambient temperature (T_{LA}). This is not a system requirement, rather simply the local ambient temperature upstream from the processor. It is measured from the air upstream and in close vicinity to the processor heatsink module. For other cooling systems, the ambient temperature is measured from the inlet air to the cooling device.

6.2.1.2 Airflow

Airflow should be provided by a system fan or blower in order to cool the processor package. See the recommended airflow rate for the reference heatsink in Table 6-7.

Table 6-7. Thermal Solution Performance Design Targets and Environment

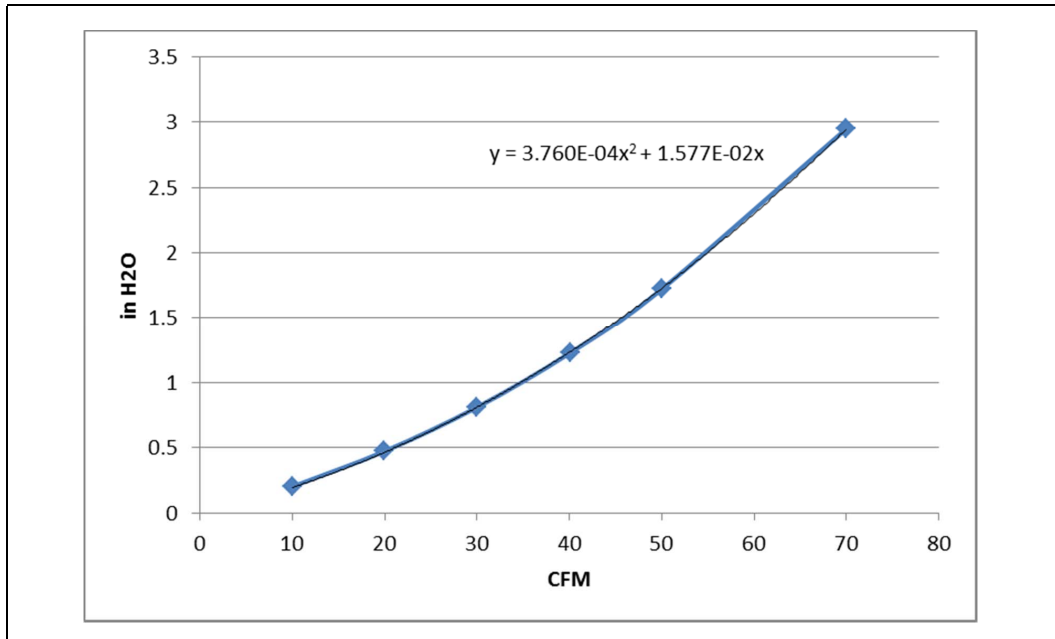
Parameter	Maximum	Unit	Notes
T _{LA}	40	°C	This is the temperature at the processor cooling devices
Pressure Drop	137 (0.55)	Pa (inch H ₂ O)	Total pressure drop across the processor cooling devices
Altitude	Sea-level		Thermal solution optimized for performance at sea-level. De-rate at higher altitudes.
Airflow	9.44 (20)	l/s (CFM)	Airflow through the heatsink fins

Note: Thermal boundary conditions are applied in establishing the processor heatsink cooling solution.

6.2.1.3 Pressure Drop

Figure 6-4 illustrates the relationship of pressure drop to volumetric air flow for the reference thermal solution. Table 6-7 provides the expected value for the pressure drop at the recommended airflow through a reference heatsink. This ensures cooling requirements for the system components downstream from the processor are met while ensuring the processor thermal targets are met.

Figure 6-4. Reference Heatsink Pressure Drop Curve



6.2.2 Thermal Solution Performance Characterization

The following equations can be used to calculate the thermal resistances. Refer to Table 6-3 for definitions.

Power only the CPU, no power to the MCDRAMs or fabric:

$$\Psi_{cc} = (T_{case_CPU} - T_{LA}) / P_{CPU}$$

$$\Psi_{mc} = (T_{case_MCDRAM} - T_{LA}) / P_{CPU}$$

Power only the MCDRAMs, no power to the CPU or fabric:

$$\Psi_{cm} = (T_{case_CPU} - T_{LA}) / P_{MCDRAM}$$

$$\Psi_{mm} = (T_{case_MCDRAM} - T_{LA}) / P_{MCDRAM}$$

Power only the fabric, no power to the CPU or MCDRAMs:

$$\Psi_{cf} = (T_{case_CPU} - T_{LA}) / P_{Fabric}$$

$$\Psi_{mf} = (T_{case_MCDRAM} - T_{LA}) / P_{Fabric}$$



6.2.3 Thermal Test Vehicle (TTV) Correction Factors

Intel offers thermal test vehicles to assist engineers developing and testing thermal/mechanical solutions for LGA3647-1 socket-compatible systems. TTVs are designed to mimic the thermal load of the actual die on the MCP under various work usage scenarios. The TTV can be used for platforms with and without fabric by simply turning the fabric die heater on or off.

Correction factors are provided for the processors to correlate the TTV heaters to the silicon die when analyzing heatsink characterization data.

$$T_{Case_CPU_Product} = T_{Case_CPU_TTV} + CF_{CPU} * (P_{CPU} + P_{MCDRAM} + P_{Fabric})$$

$$T_{Case_MCDRAM_Product} = T_{Case_MCDRAM_TTV} + CF_{MCDRAM} * (P_{CPU} + P_{MCDRAM} + P_{Fabric})$$

TTV to Product Correction Factors	
CF_{CPU}	CF_{MCDRAM}
0.0006 C/W	-0.004 C/W

Processor correction factors are subject to change over time. Contact your Intel Xeon Phi thermal representative if you have questions.

6.2.4 Thermal Management Guidelines

Processor thermal solution, heatsink and/or cold-plate, design must comply with T_{CASE} targets. Thermal solution design compliance can be determined with thermocouple and TTV as with previous processors.

Systems that do not monitor the processor temperature by monitoring the DTS (Digital Thermal Sensor) output must ensure processor cooling solution is capable of meeting the processor based T_{CASE} specifications. In some situations, implementation of DTS-based thermal solutions can reduce average fan power and improve acoustics as compared to the T_{CASE} based targets alone.

When all cores are active, a properly design thermal solution will be able to meet the processor thermal specification. When all cores are not active or when Intel® Turbo Boost Technology is active, attempting to comply with the DTS based thermal specification may drive system fans to increased speed. In such situations, the T_{CASE} temperature will be below the T_{CASE} based thermal profile by design.

6.2.4.1 Processor Absolute Temperatures

Intel does not test any third-party software that reports absolute processor temperature. As such, Intel cannot recommend the use of software that claims this capability. Since there is part-to-part variation in the Thermal Control Circuit (TCC) activation temperature, use of software that reports absolute temperature can be misleading.

6.2.4.2 Fan Speed Control

Fan Speed Control (FSC) methods are commonly used to reduce system-level acoustic noise in server designs. Fan speed is one of the key parameters that determines the amount of airflow provided to the thermal solution. Additionally, airflow is proportional to a thermal solution’s performance, which consequently determines the T_{CASE} of the processor at a given power level. Because the T_{CASE} of a processor is an important parameter in determining the long-term reliability of a processor, the FSC implemented



in a system directly correlates to the processor's ability to meet thermal targets. For this purpose, the parameter called T_{CONTROL} , is to be used in FSC designs to ensure that the long-term reliability of the processor is met while keeping the system-level acoustic noise down.

When DTS values are less than T_{CONTROL} , the thermal target can be ignored. The DTS value is a relative temperature to PROCHOT which is the maximum allowable temperature before the thermal control circuit is activated. In this region, the DTS value can be utilized to not only ensure specification compliance but also to optimize FSC resulting in the lowest possible fan power and acoustics under any operating condition. When DTS goes above T_{CONTROL} , fan speed must increase to bring the sensor temperature below T_{CONTROL} or to ensure compliance with the T_{CASE} profile.

The PECI temperature reading from the processor can be compared to this T_{CONTROL} value. An FSC scheme can be implemented without compromising the long-term reliability of the processor. The PECI command for DTS is GetTemp(). Through use of a sign bit, the value returned from PECI is negative. The PECI command for T_{CONTROL} is RdPkgConfig(), Temperature Target Read, 15:8. The value returned from PECI, while unsigned (positive), is negative by definition.

There are many different ways of implementing FSC; including methods based on processor ambient temperature, processor DTS, or a combination of the two. If FSC is based only on the processor ambient temperature, low acoustic targets can be achieved under low ambient temperature conditions. However, the acoustics cannot be optimized based on the behavior of the processor temperature. If FSC is based only on the DTS, sustained temperatures above T_{CONTROL} drive fans to maximum RPM. If FSC is based both on the ambient and DTS, then ambient temperature can be used to scale the fan RPM controlled by the DTS logic. This would result in an optimal acoustic performance. Regardless of which scheme is employed, system designers must ensure the T_{CASE} specification is met under all operational conditions.

6.2.4.3 Tcontrol Relief

Intel may choose to provide T_{CONTROL} relief near product launch, T_{CONTROL} values closer to 0, as compared to the factory configured T_{CONTROL} values. However, there are no such plans at this time.

6.2.4.4 Thermal Excursion Power

Under fan failure or other anomalous thermal excursions, processor temperature (either T_{CASE} or DTS) may exceed the thermal target for a duration totaling less than 360 hours per year without affecting long term reliability (life) of the processor. For more typical thermal excursions, the thermal monitor is expected to control the processor temperature by reducing the processor power level. These conditions should not allow the processor to exceed the temperature at which the Thermal Control Circuit (TCC) activation initially occurred.

Under more severe anomalous thermal excursions when the processor temperature cannot be controlled at or below thermal profile by TCC activation, then data integrity is not assured. At some higher thresholds, THERMTRIP_N will enable a shut down in an attempt to prevent permanent damage to the processor.

Thermal test vehicles (TTVs) may be used to check anomalous thermal excursion compliance. TTVs can be used to test and ensure the processor T_{CASE} value does not exceed $T_{\text{CASE_MAX}}$ at the anomalous power level for the condition of interest, such as fan failure.



A Quality and Reliability Requirements

A.1 Thermal/Mechanical Solution Stress Test

Intel evaluates reliability performance based on the use conditions (operating environment) of the end product by using acceleration models.

The use condition environment definitions provided in the tables below are based on speculative use condition assumptions, and are provided as examples only.

Based on the system enabling boundary condition, the solder ball temperature can vary and needs to be comprehended for reliability assessment.

Table A-1. Example Thermal Stress Test: Use Condition Environment Definitions

Use Environment	Speculative Stress Condition	Example Use Condition	Example 7 yr. Stress Equivalent	Example 10 yr. Stress Equivalent	Purpose/Failure Mechanism
Slow small internal gradient changes due to external ambient (temperature cycle or externally heated) Fast, large gradient on/off to max operating temperature (power cycle or internally heated including power save features)	Temperature Cycle	DT = 35 - 44 °C (solder joint)	550-930 cycles Temp Cycle (-25 °C to 100 °C)	780-1345 cycles Temp Cycle (-25 °C to 100 °C)	Solder joint fatigue, via barrel cracking, and Thermal Interface Material (TIM) separation/disbond under thermal mechanical stresses
High ambient moisture during low-power state (operating voltage)	THB/HAST	T = 25 - 30 °C 85% RH (ambient)	110-220 hrs at 110 °C and 85% RH	145-240 hrs at 110 °C and 85% RH	Corrosion and material migration induced by moisture/temperature
High Operating temperature and short duration high temperature exposures	Bake	T = 95 - 105 °C (contact)	700 - 2500 hrs at 125 °C	800 - 3300 hrs at 125 °C	Creep-induced failure mechanisms, for example contact relaxation, solder ball creep, and thermal TIM degradation

Material used will not have deformation or degradation in a temperature life test.



Table A-2. Example Mechanical Stress Test: Use Condition Environment Definitions

Use Environment	Speculative Stress Condition		Purpose/Failure Mechanism	
Shipping and Handling	<u>Mechanical Shock</u> <ul style="list-style-type: none"> System-level Unpackaged test Trapezoidal waveform 25 g velocity change is based on packaged weight. Change in velocity is based upon a 0.5 coefficient of restitution. 		<u>12 drops total</u> <ul style="list-style-type: none"> 2 drops per each of 3 perpendicular axes + and - directions 	Mechanical-induced brittle solder joint failures and TIM separation/disbond
	Product Weight (lbs) < 20 lbs 20 to > 40 40 to > 80 80 to < 100 100 to < 120 ≥120	Non-palletized Product Velocity Change (in/sec) 250 225 205 175 145 125		
	<u>Random Vibration</u> <ul style="list-style-type: none"> System-level Unpackaged test 5 Hz to 500 Hz <ul style="list-style-type: none"> 0.001 g²/Hz @ 5Hz, ramping to 0.01 g²/Hz @20 Hz; constant value of 0.01 g²/Hz from 20 to 500 Hz Random control limit tolerance is ± 3 dB Power Spectral Density (PSD) Profile: 2.20 g RMS 		<u>per system total</u> <ul style="list-style-type: none"> 10 min/axis 3 axes 	Example mechanisms include cyclic mechanical fatigue stress and TIM separation/disbond

Note: Need to pass customer visual, thermal, mechanical, and electrical requirements.

A.1.1 Customer Environmental Reliability Testing

The conditions of the tests outlined here may differ from the customers’ system requirements. Board/system level requirements are to be identified and performed by customers planning on using the Intel reference thermal/mechanical solution.

A.1.2 Socket Durability Test

The socket must withstand 30 mating cycles. Test per EIA-364, test procedure 09. Measure contact resistance when mated in 1st and 30th cycles. The package must be removed at the end of each de-actuation cycle and reinserted into the socket.

A.1.3 Intel Reference Component Validation

Intel tests reference components individually and as an assembly on mechanical test boards and assesses performance to the envelopes specified in previous sections by varying boundary conditions.

While component validation shows a reference design is tenable for a limited range of conditions, customers need to assess their specific boundary conditions and perform reliability testing based on their use conditions.

Intel reference components are also used in board functional tests to assess performance for specific conditions.



A.2 Ecological Requirement

General requirements: Materials used in this product comply with Intel's *Environmental Product Content Specification for Suppliers and Outsourced Manufacturers*.

Materials should be resistant to fungal growth. Examples of non-resistant materials include cellulose materials, animal- and vegetable-based adhesives, grease, oils, and many hydrocarbons. Synthetic materials such as PVC formulations, certain polyurethane compositions (for example, polyester and some polyethers), plastics which contain organic fillers of laminating materials, paints, and varnishes also are susceptible to fungal growth. If materials are not fungal growth resistant, then MIL-STD-810E, Method 508.4 must be performed to determine material performance. Cadmium should not be used in the painting or plating of the socket. CFCs and HFCs should not be used in manufacturing the socket.

Any plastic component exceeding 25 grams must be recyclable per the European Blue Angel recycling standards.

Supplier is responsible for complying with industry standards regarding environmental care as well as with the specific standards required per supplier's region. More specifically, supplier is responsible for compliance with the European regulations related to restrictions on the use of Lead and Bromine containing flame-retardants. Legislation varies by geography, European Union (RoHS/WEEE), China, California, and so forth.

The following definitions apply to the use of the terms lead-free, Pb-free, and Restriction of Hazardous Substances (RoHS) compliant.

Halogen flame retardant free (HFR-Free) PCB: Current guidance for the socket pad layout supports FR4 and HFR-Free designs. In future revisions of this document, Intel may provide guidance on the mechanical impact to using a HFR-free laminate in the PCB. This will be limited to workstations.

Lead-free and Pb-free: Lead has not been intentionally added, but lead may still exist as an impurity below 1000 ppm.

RoHS compliant: Lead and other materials banned in RoHS Directive are either (1) below all applicable substance thresholds as proposed by the EU or (2) an approved/pending exemption applies.

Note: RoHS implementation details are not fully defined and may change.

Additional requirements: Cadmium should not be used in painting or plating. No Quaternary salt electrolytic capacitors should be used. Examples of prohibited caps are: United Chemi-Con* type: LXF, LXY, LXZ. No brominated plastics should be used. Also, plastics heavier than 25 g must be labeled per ISO 10469 and may not contain halogenated flame retardant compounds.

Chemical Restrictions:

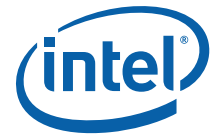
The components must be "halogen-free," that is, they are assembled without the intentional use of halogen in the raw materials and these elements are not intentionally present in the end product.

- IEC 61249-2-21
 - 900 ppm maximum chlorine
 - 900 ppm maximum bromine
 - 1500 ppm maximum total halogens



- IPC-4101B
 - 900 ppm maximum chlorine
 - 900 ppm maximum bromine
 - 1500 ppm maximum total halogens

It is **required** that the production version of the socket, the Processor Heatsink Module (PHM) including the Thermal Interface Material (TIM) and the processor mechanical retention assembly be RoHS compliant, by using 100% lead-free technology. RoHS reference source is http://ec.europa.eu/environment/waste/rohs_eee/events_rohs3_en.htm.



B Supplier Listing

Third-party suppliers are enabled to ensure that reference thermal and mechanical components are available.

B.1 Intel Enabled Supplier Information

This chapter contains supplier details including contact information for the socket, heatsink, TIM and other retention components in future revisions.

- Supplier content is provided by Intel as a convenience to its customers. Intel does not make any representations or warranties whatsoever regarding the quality, reliability, functionality, or compatibility of these devices.
- All Part Numbers (P/N) listed are in prototype phase and have not been verified to meet performance targets or quality and reliability requirements and are subject to change.
- Supplier information provided in the table was deemed accurate when this document was released.
- Customers planning on using the Intel reference design should contact the suppliers for the latest information on their product(s).
- Customers must evaluate performance against their own product requirements.



Table B-1. Intel Xeon Phi Processor Platform Thermal/Mechanical Assembly Part Information

Component	Description	Supplier P/N	Supplier Contact Info
Heatsink	1U Heatsink Assembly; Cu - Al Reference Heatsink, washers, nuts and collars. Intel P/N Vendor P/N	Delta*	DELTA ELECTRONICS, INC. Stephanie Liu Thermal Management Product BU (FMBG) Stephanie.Liu@Delta.com.tw +886-3-359-1968 #2086 Delta Products Corp Jason Tsai, Portland, Oregon jason.fs.tsai@deltaww.com +1-971-205-7074
		H37264-009 DHS-B10780-15	
Thermal Interface Material	Thermal Interface Material PCM45F 70x47x0.25 Intel P/N Vendor P/N	Honeywell*	Honeywell International, Inc. Connie Smiriglio (Account Manager) Connie.smiriglio@honeywell.com +1-845-627-2750 Hyo Xi (Technical) Hyo.xi@honeywell.com 430 Li Bing Rd, Zhangjiang Hi-Tech Park, Pudong, SH Shanghai, 31, 201203, China +86-21-28943106
		H38442-001 099079	
Processor Heatsink Loading Module (PHLM) Vendor Contact Information for <ul style="list-style-type: none"> Processor Carriers Bolster Plate Assemblies Back Plate Assemblies Socket-P Dust Covers 		Foxconn*	Foxconn Interconnect Technology Inc. 1347 N Alma School Rd Ste 230 Chandler, Arizona USA 85224-5947 Albert Terhune al.terhune@fit-foxconn.com +1-480-963-3392
		Lotes*	Lotes Guangzhou Co., Ltd. No. 526 North of Jinling Road Nansha Economic & Technological Development Zone, Guangzhou, 511458 China. Cathy Yang cathy@lotes.com.cn +86-20-84686519
Processor Carrier	Plastic processor carrier. Intel P/N Lotes P/N Foxconn P/N	H53249-003 AZIF0079-P002C* WNMEL00-82N01-EH	
Processor with Fabric Carrier	Plastic processor carrier. Intel P/N Lotes P/N Foxconn P/N	H53248-003 AZIF0080-P002C* WNMEL00-83N01-EH	


Table B-1. Intel Xeon Phi Processor Platform Thermal/Mechanical Assembly Part Information

Component	Description	Supplier P/N	Supplier Contact Info
Bolster Plate Assembly	Bolster plate, posts, leaf spring assembly and insulator. Intel P/N Lotes P/N Foxconn P/N	H77470-008 AZIF0085-P002C* WNMEL60-80N05-EH	
Back Plate Assembly	Back plate, threaded posts and insulator Intel P/N Lotes P/N Foxconn P/N	H77469-002 AHSK0009-P002C* PT44P12-4801	
Dust Cover	Skt-P plastic handling cover Intel P/N Lotes P/N Foxconn P/N	H77975-005 AZIF0084-P002C* WNMEL00-81N00-EH	
Bolster Plate with Dust Cover Assembly	Bolster plate, posts, leaf spring assembly and insulator, Skt-P plastic handling cover Intel P/N Lotes P/N Foxconn P/N	H78747-008 AZIF0086-P002C* PT44L12-4811	
Bolster Plate, Back Plate and Dust Cover Assembly	Bolster plate, posts, leaf spring assembly and insulator, back plate, threaded posts, insulator and Skt-P plastic handling cover Intel P/N Foxconn P/N	NA WNMEA66-81N02-EH	



Table B-1. Intel Xeon Phi Processor Platform Thermal/Mechanical Assembly Part Information

Component	Description	Supplier P/N	Supplier Contact Info
Socket-P1 3647 LGA3647-1	Processor Socket (Intel CAD Number J36228)	Foxconn*	Foxconn Interconnect Technologies (FIT) Foxconn NWInG, Oregon Eric Ling eric.ling@fit-foxconn.com +1-971-506-6441
	30 μ-inch Gold Contacts Right Side P/N Left Side P/N	Intel: J34315-001; Foxconn: PE36473-11NK3-1H Intel: J34315-002; Foxconn: PE36473-11NK4-1H	
	15 μ-inch Gold Contacts Right Side P/N Left Side P/N	Intel: H37600-202; Foxconn: PE36473-11NK1-1H Intel: H37600-203; Foxconn: PE36473-11NK2-1H	
		Tyco*	Tyco Electronics (TE) Connectivity Ellen Liang ellen.yh.liang@te.com +886-2-2171-5261
	30 μ-inch Gold Contacts Right Side P/N Left Side P/N	Intel: J34319-001; Tyco: 2-2129710-8 Intel: J34319-002; Tyco: 2-2129710-7	
	15 μ-inch Gold Contacts Right Side P/N Left Side P/N	Intel: J65188-001; Tyco: 2-2129710-4 Intel: J65188-002; Tyco: 2-2129710-3	



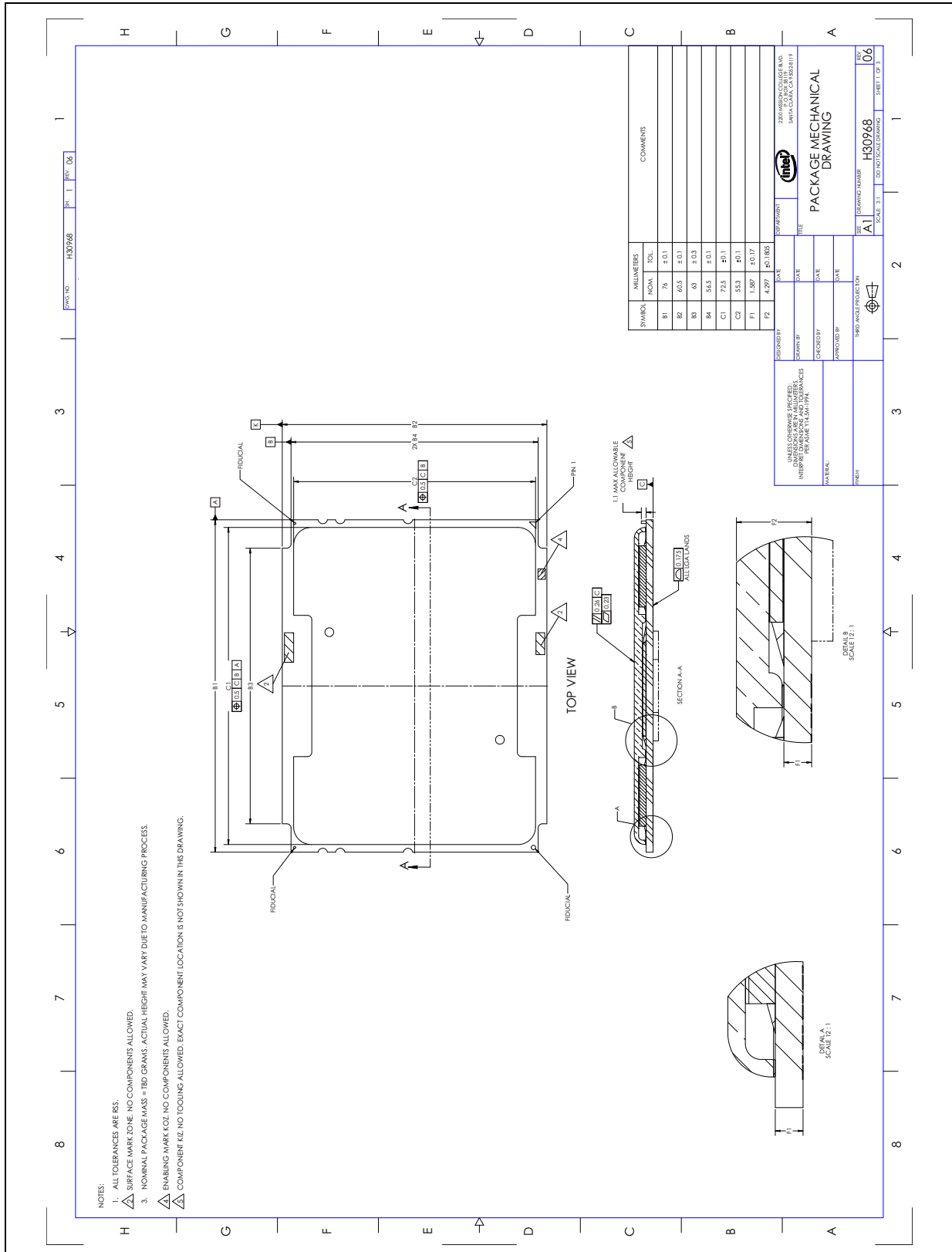
C Processor Package Mechanical Drawings

Table C-1 lists the processor Package Mechanical Drawings (PMD) included in this appendix.

Table C-1. Processor Package Drawing List

Drawing Description	Figure Number
Processor PMD (Sheet 1 of 2)	Figure C-1
Processor PMD (Sheet 2 of 2)	Figure C-2
Processor with Fabric PMD (Sheet 1 of 2)	Figure C-3
Processor with Fabric PMD (Sheet 2 of 2)	Figure C-4

Figure C-1. Processor PMD (Sheet 1 of 2)



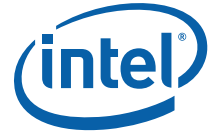


Figure C-2. Processor PMD (Sheet 2 of 2)

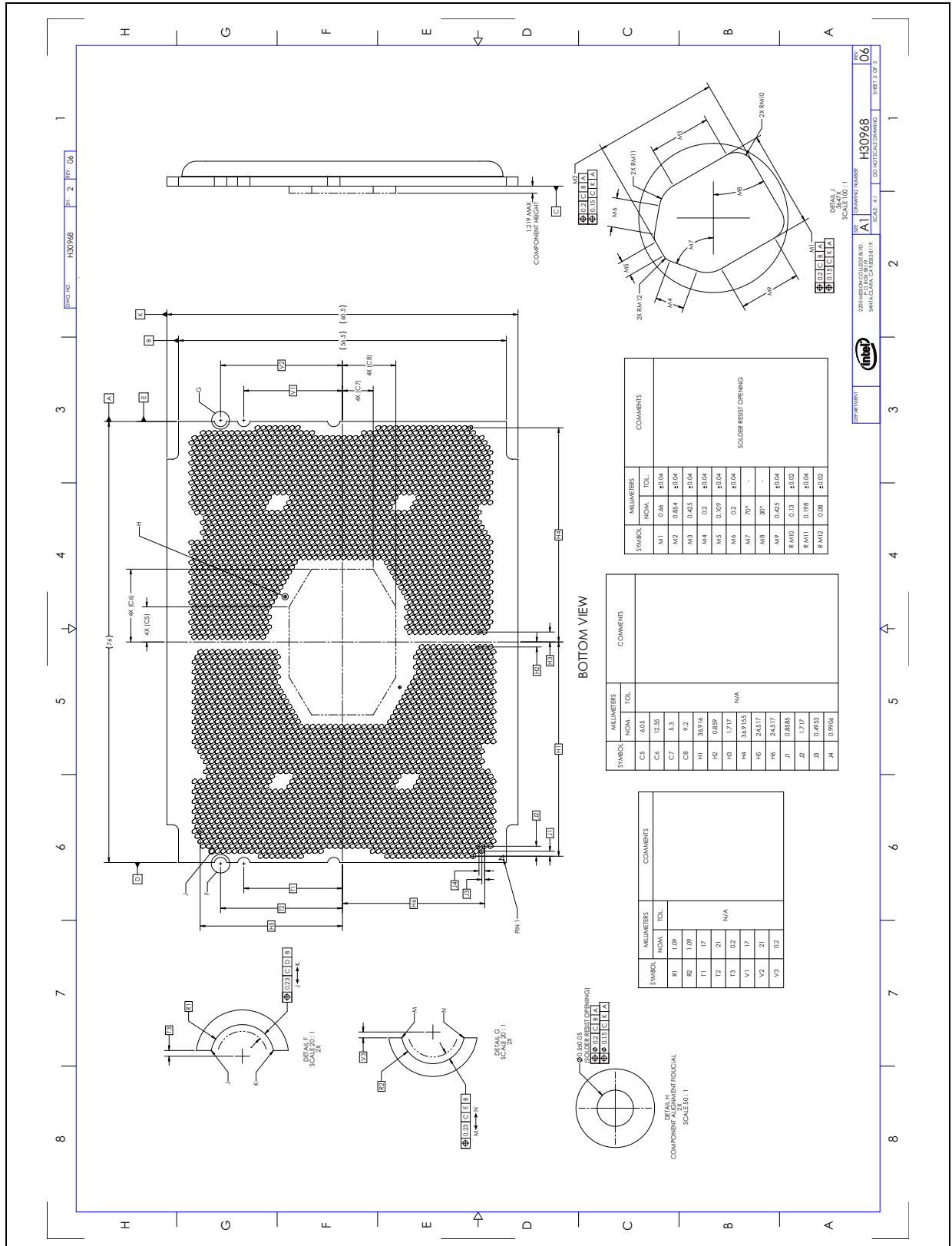
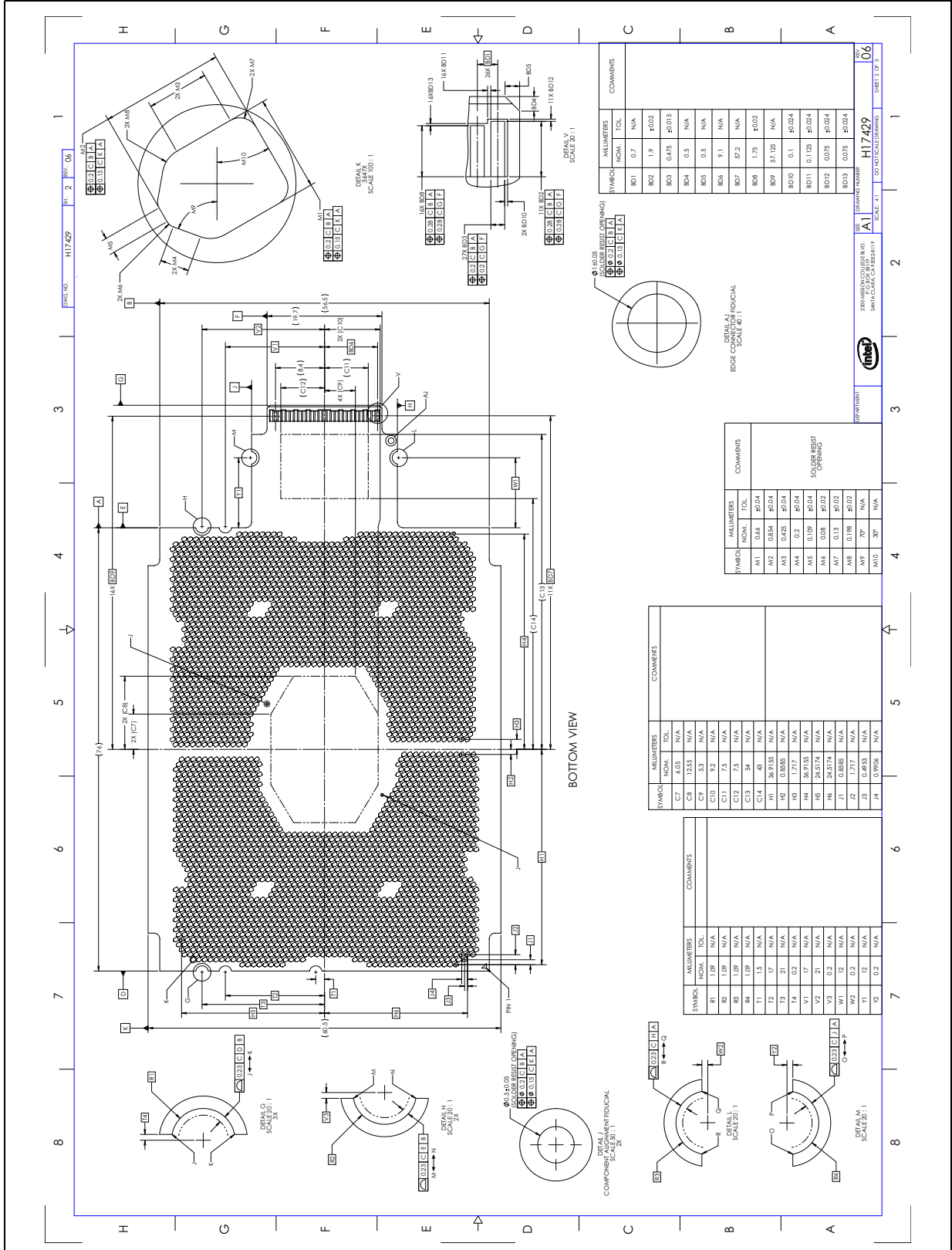




Figure C-4. Processor with Fabric PMD (Sheet 2 of 2)





D LGA3647-1 Socket-P1 Mechanical Drawings

Table D-1 lists the socket drawings included in this appendix.

Table D-1. Socket Drawing List

Drawing Description	Figure Number
Socket Mechanical Drawing (Sheet 1 of 4)	Figure D-1
Socket Mechanical Drawing (Sheet 2 of 4)	Figure D-2
Socket Mechanical Drawing (Sheet 3 of 4)	Figure D-3
Socket Mechanical Drawing (Sheet 4 of 4)	Figure D-4

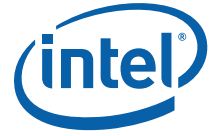


Figure D-1. Socket Mechanical Drawing (Sheet 1 of 4)

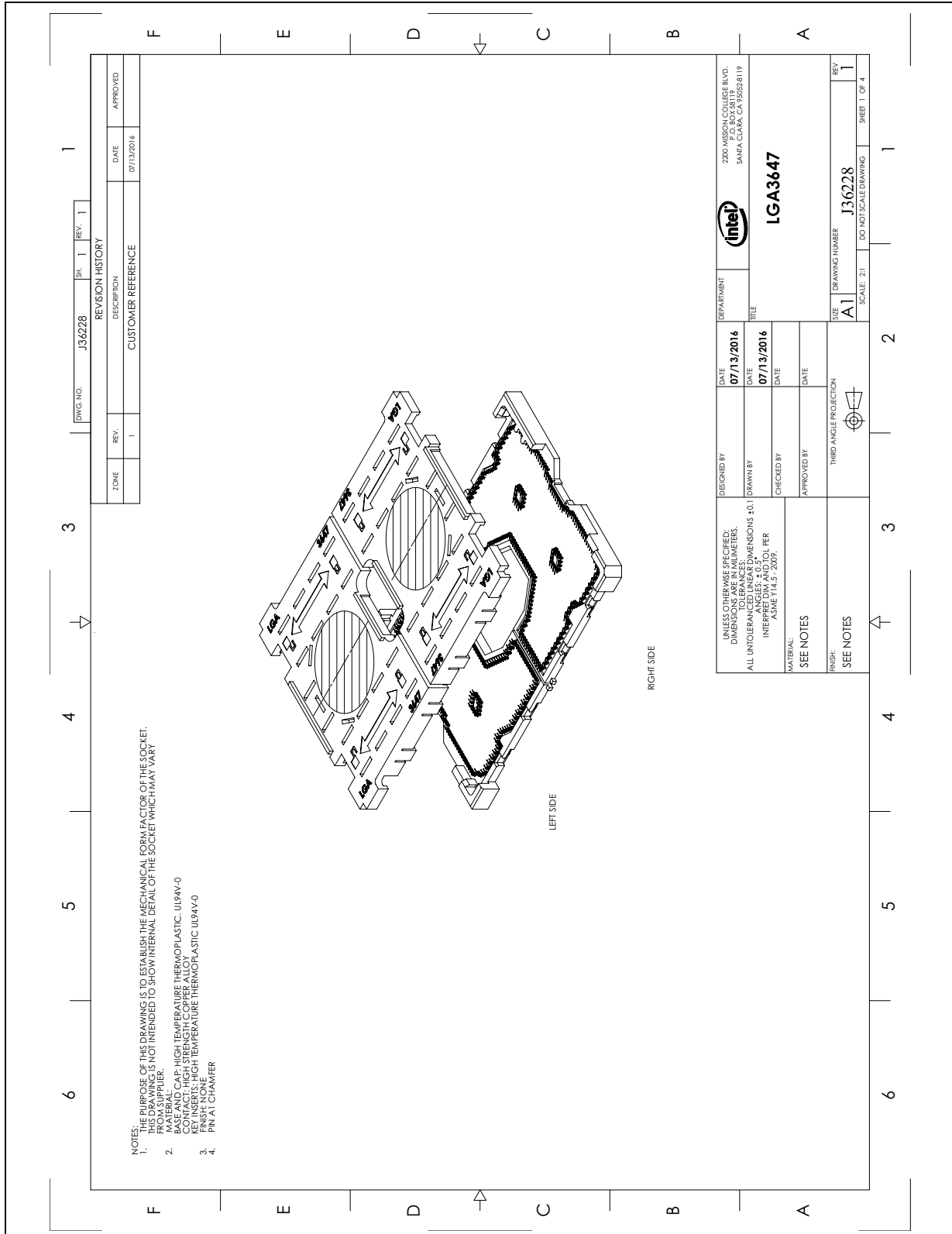
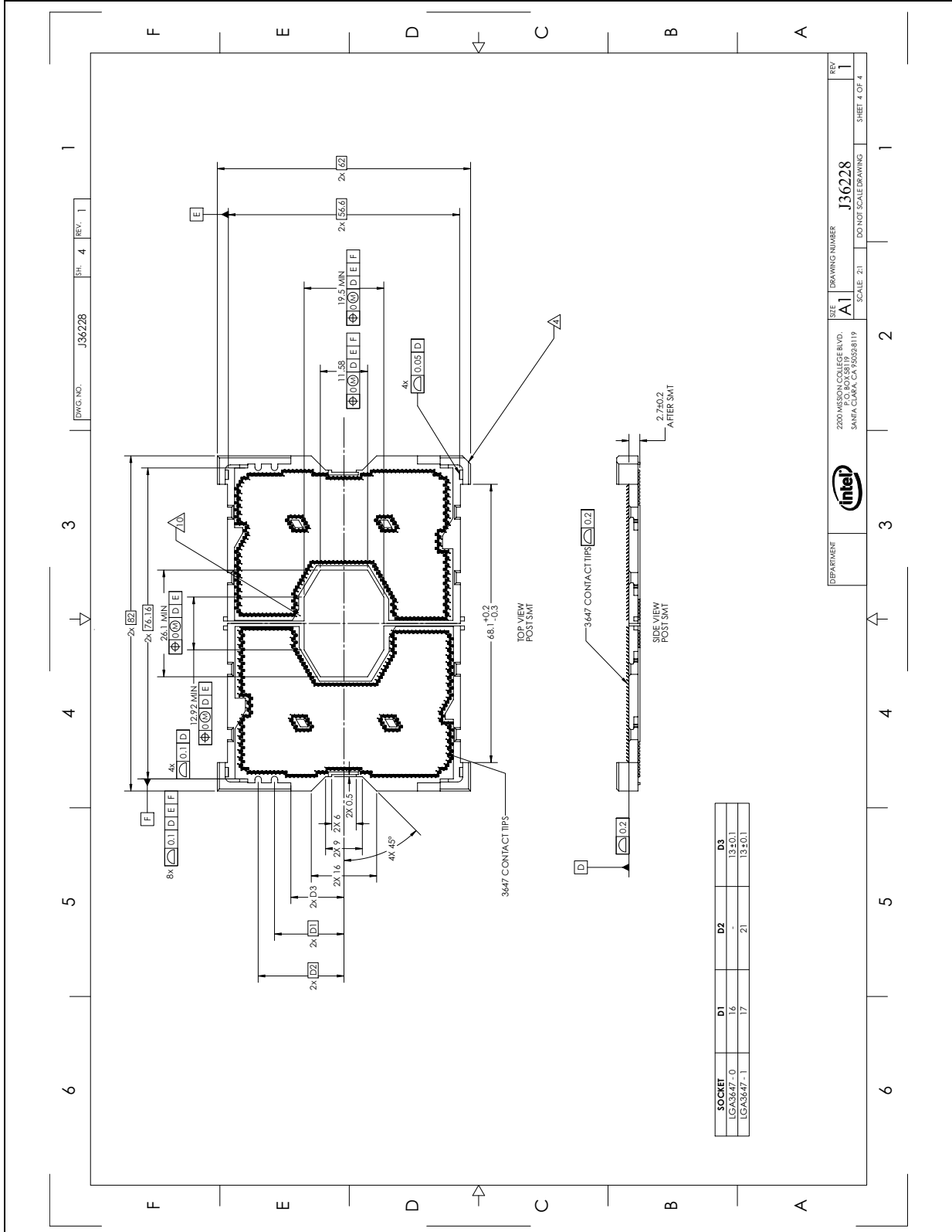




Figure D-4. Socket Mechanical Drawing (Sheet 4 of 4)



DEPARTMENT	INTEL
FILE	A1
DRAWING NUMBER	J36228
SCALE	2:1
DO NOT SCALE DRAWING	
SHEET	4 OF 4



E Retention Assembly Mechanical Drawings

Table E-1 lists the mechanical drawings included in this appendix.

Table E-1. Mechanical Drawing List (Sheet 1 of 2)

Description	Figure
Backplate Assembly, 1/3	Figure E-1
Backplate Assembly, 2/3	Figure E-2
Backplate Assembly, 3/3	Figure E-3
Bolster Plate Assembly and Dust Cover	Figure E-4
Bolster Plate Assembly, 1/2	Figure E-5
Bolster Plate Assembly, 2/2	Figure E-6
Heatsink Module Clip (non-Fabric), 1/2	Figure E-7
Heatsink Module Clip (non-Fabric), 2/2	Figure E-8
Heatsink Module Clip (Fabric), 1/2	Figure E-9
Heatsink Module Clip (Fabric), 2/2	Figure E-10
Backplate	Figure E-11
Backplate Insulator	Figure E-12
Back Plate, M3 Stud	Figure E-13
Bolster Plate, 1/2	Figure E-14
Bolster Plate, 2/2	Figure E-15
Bolster Plate, Insulator	Figure E-16
Bolster Plate, Small Guide Post	Figure E-17
Bolster Plate, Large Guide Post	Figure E-18
Bolster Plate, LEC Guide Pin	Figure E-19
Bolster Plate, Corner Standoff	Figure E-20
Bolster Plate, Spring Assembly	Figure E-21
Bolster Plate, Spring	Figure E-22
Bolster Plate, Spring Stud, M4	Figure E-23
Bolster Plate, Spring Rivet	Figure E-24
Bolster Plate, M3 Captive Nut	Figure E-25
Bolster Plate, M3 Captive Nut Collar	Figure E-26
Socket-P, Dust Cover, 1/2	Figure E-27
Socket-P, Dust Cover, 2/2	Figure E-28
1U Heatsink Assembly, 1/2 (Reference Only)	Figure E-29
1U Heatsink Assembly, 2/2 (Reference Only)	Figure E-30
1U Heatsink, 1/2 (Reference Only)	Figure E-31
1U Heatsink, 2/2 (Reference Only)	Figure E-32
1U Heatsink, Label (Reference Only)	Figure E-33



Table E-1. Mechanical Drawing List (Sheet 2 of 2)

1U Heatsink, PCM45F TIM (Reference Only)	Figure E-34
1U Heatsink, Nut, M4, 1/2 (Reference Only)	Figure E-35
1U Heatsink, Nut, M4, 2/2 (Reference Only)	Figure E-36
1U Heatsink, Nut Collar (Reference Only)	Figure E-37
1U Heatsink, Delrin* Washer (Reference Only)	Figure E-38

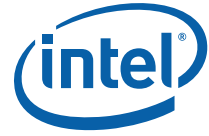


Figure E-1. Backplate Assembly, 1/3

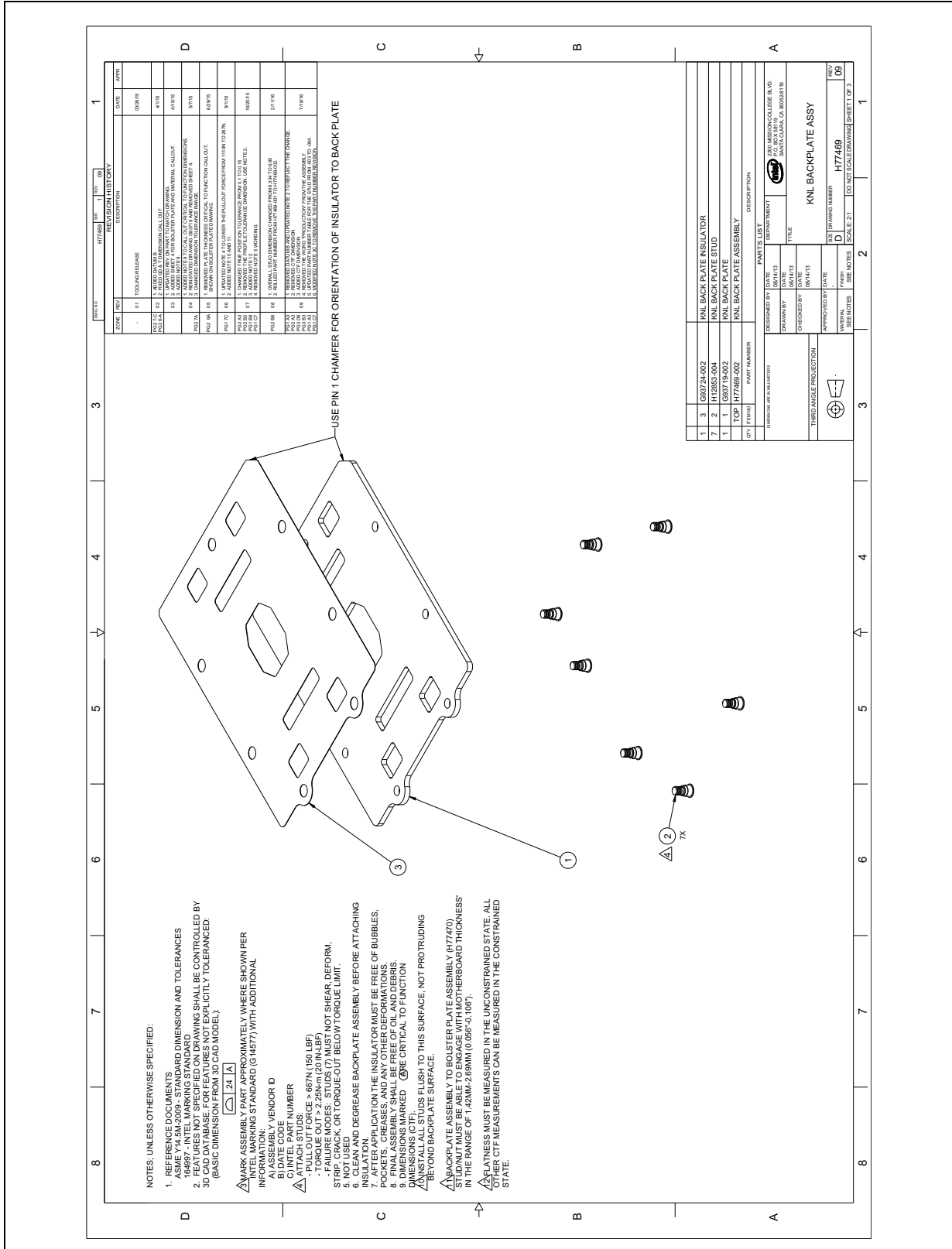


Figure E-2. Backplate Assembly, 2/3

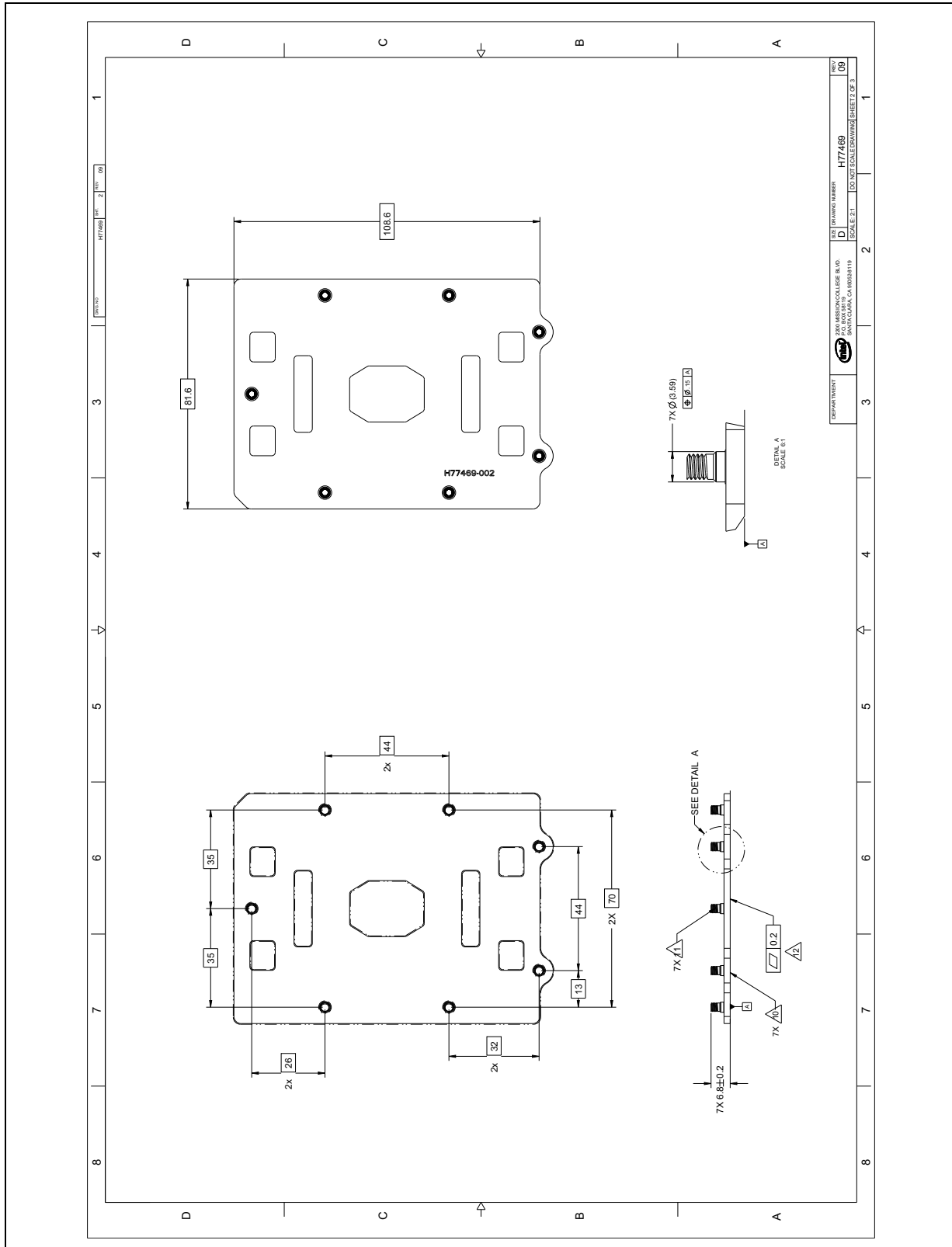




Figure E-3. Backplate Assembly, 3/3

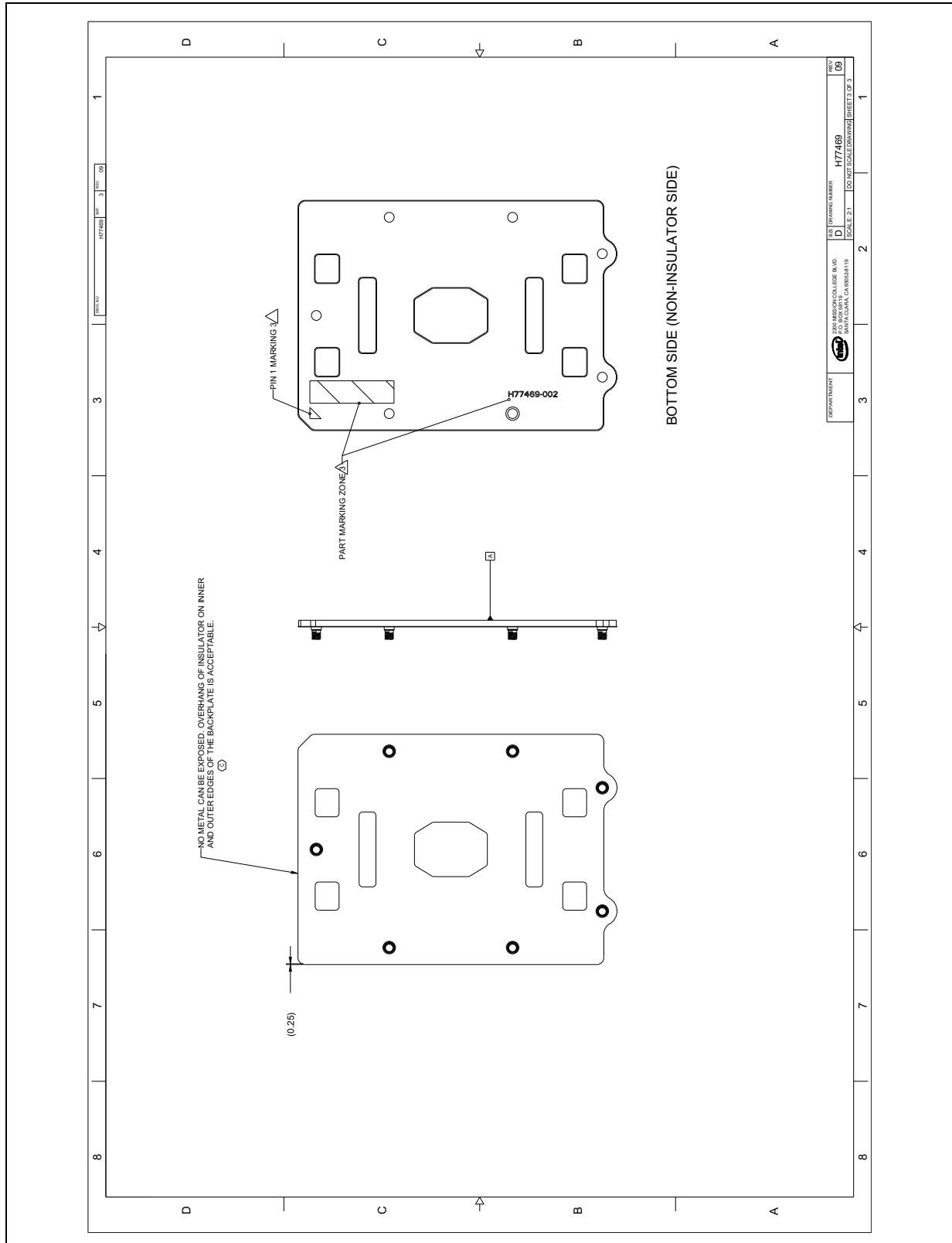


Figure E-4. Bolster Plate Assembly and Dust Cover

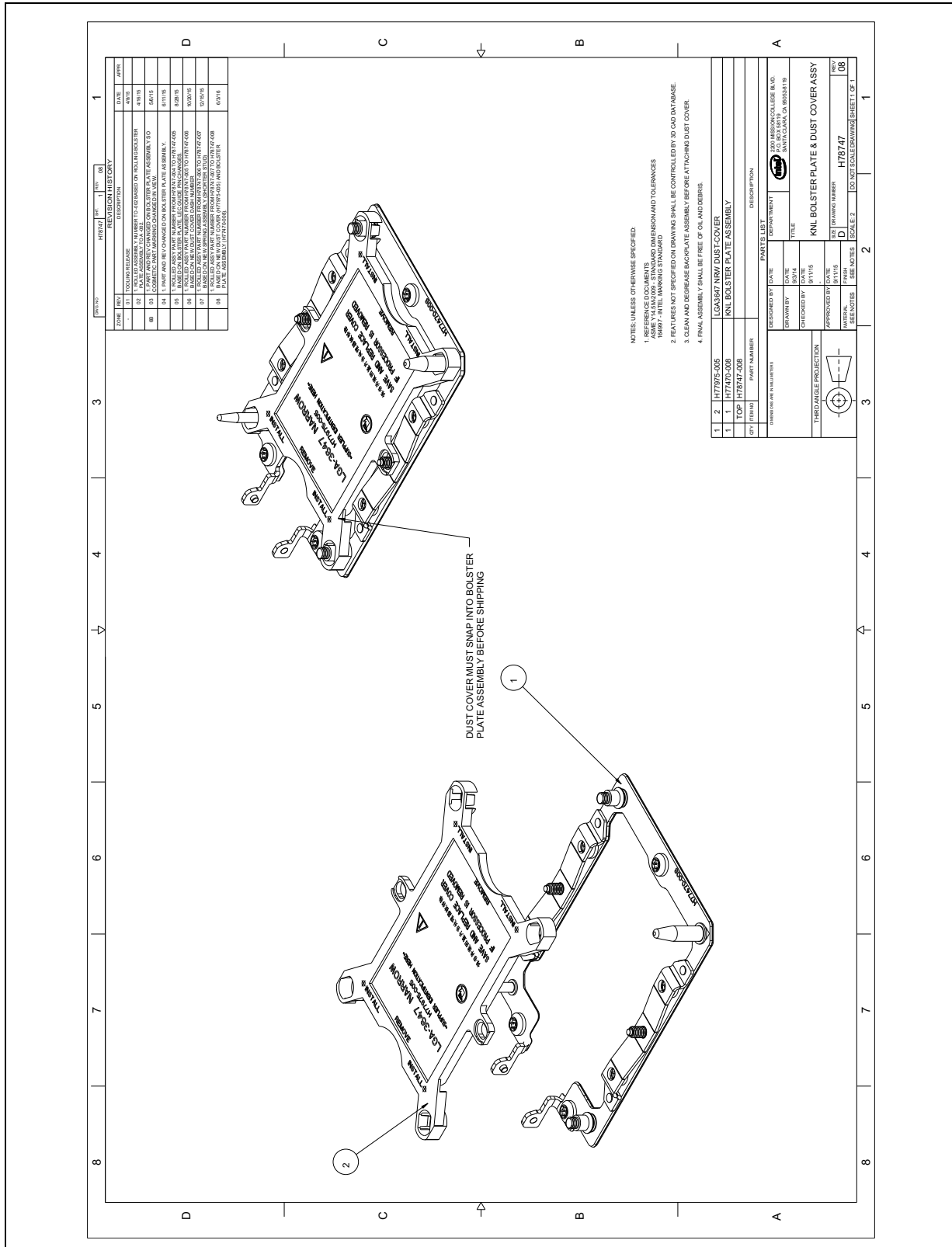




Figure E-5. Bolster Plate Assembly, 1/2

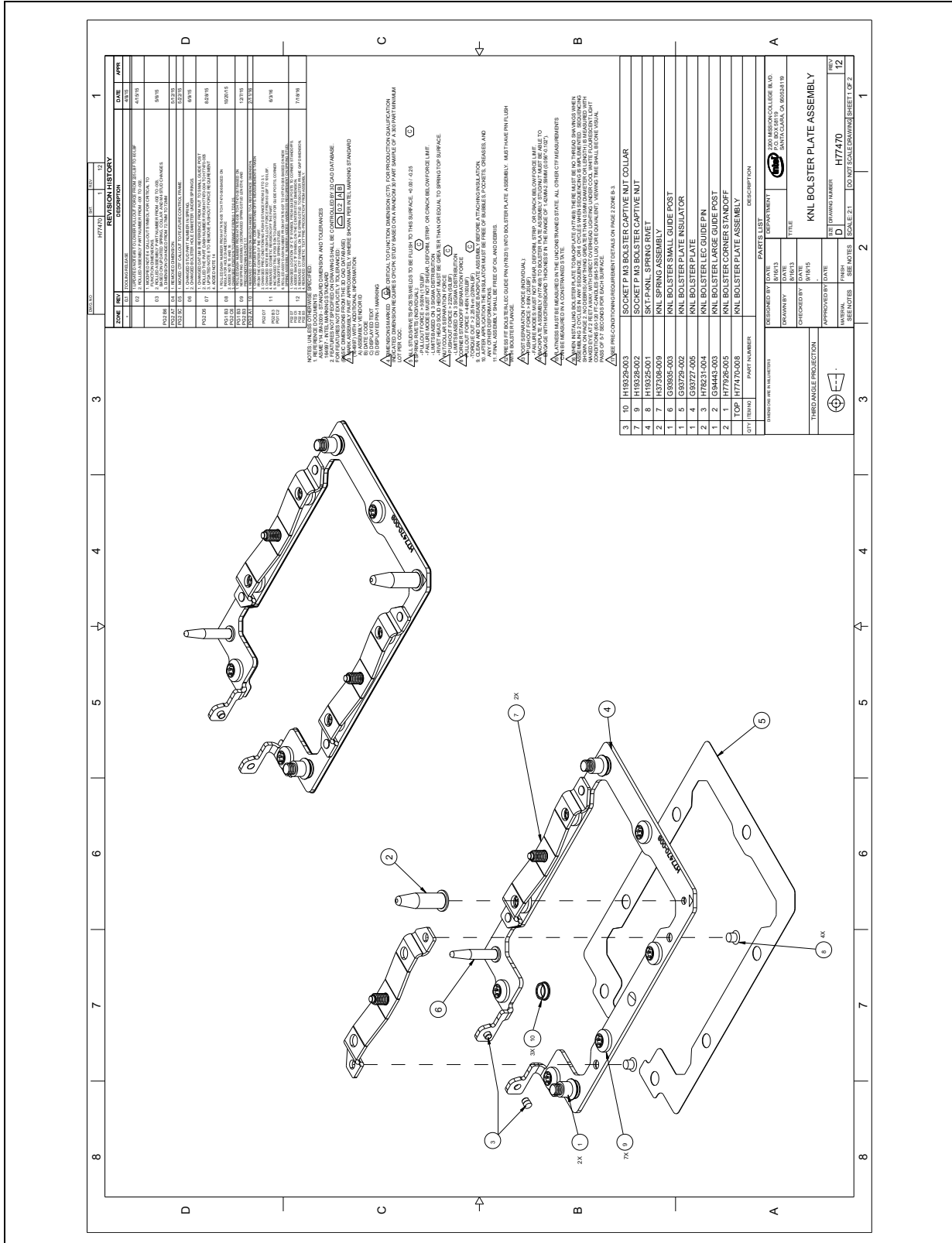
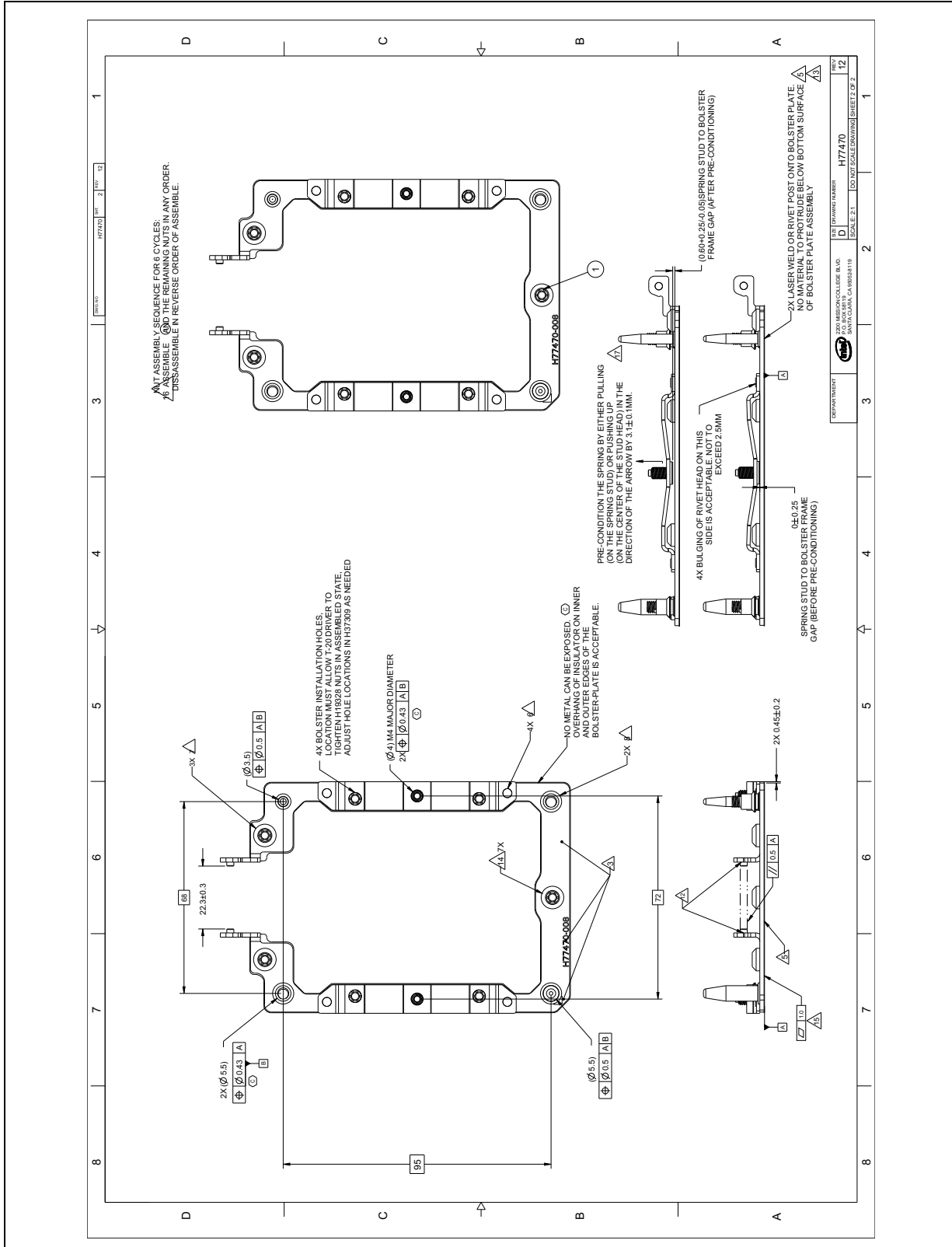


Figure E-6. Bolster Plate Assembly, 2/2



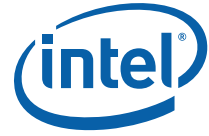


Figure E-7. Heatsink Module Clip (non-Fabric), 1/2

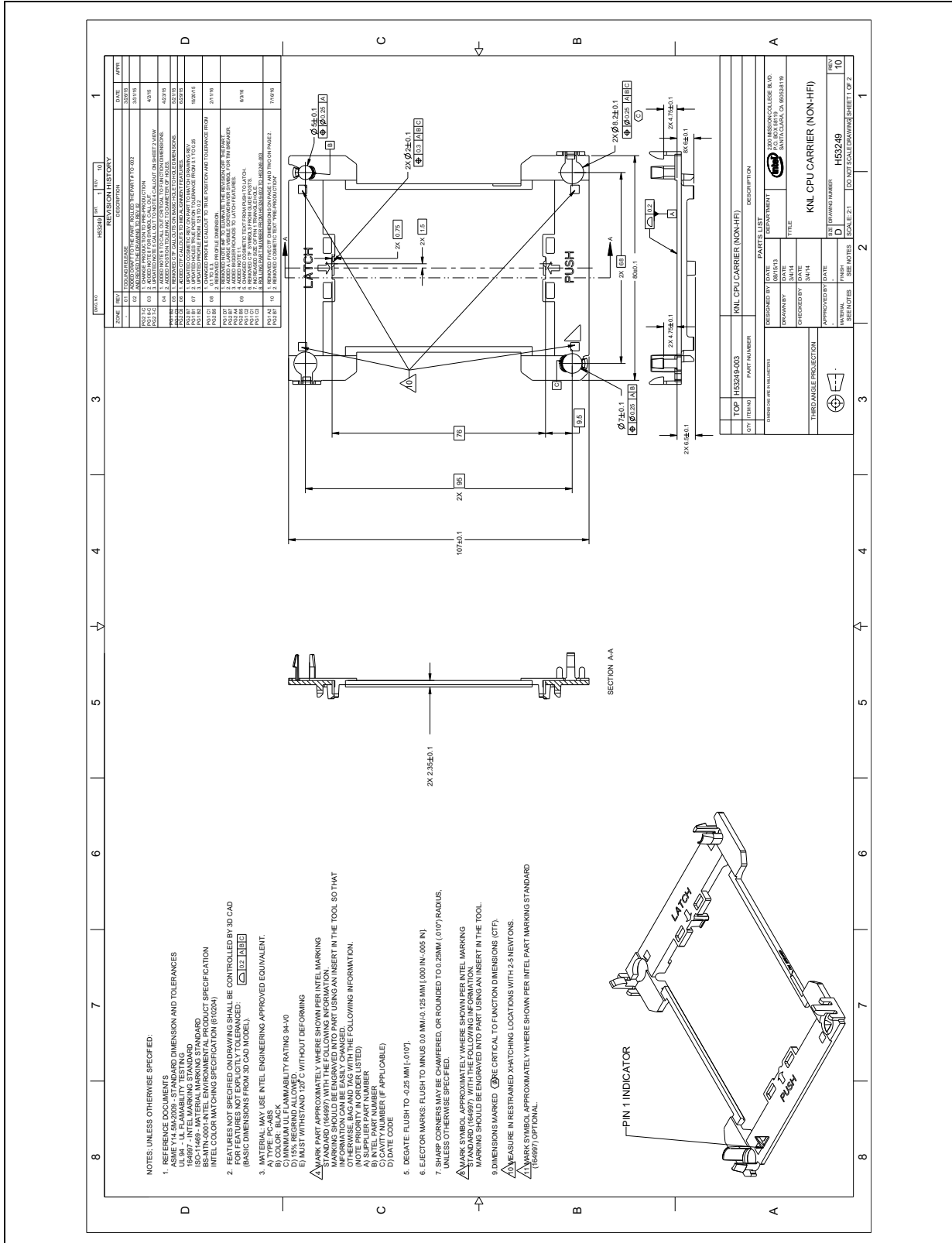


Figure E-8. Heatsink Module Clip (non-Fabric), 2/2

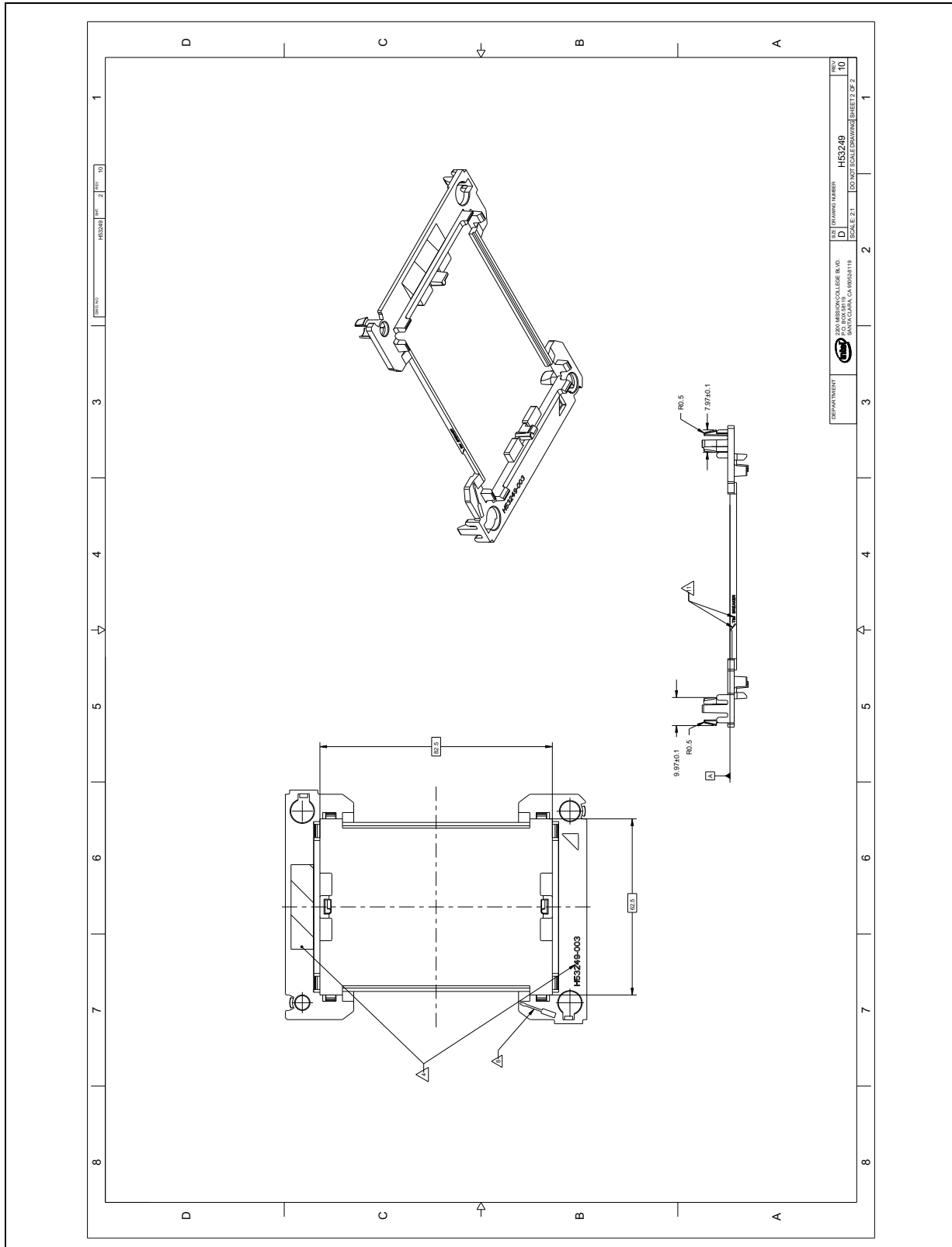


Figure E-9. Heatsink Module Clip (Fabric), 1/2

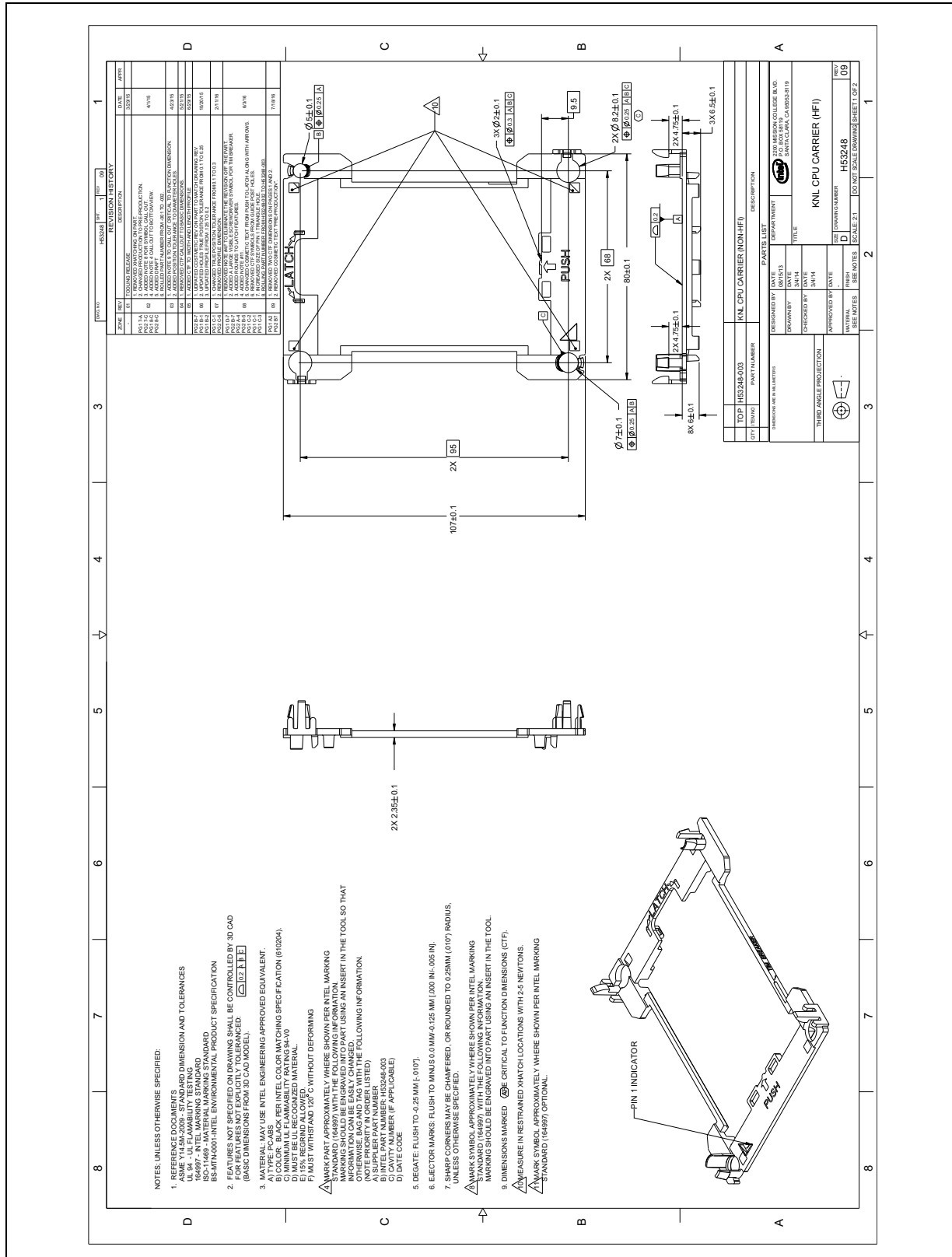


Figure E-10. Heatsink Module Clip (Fabric), 2/2

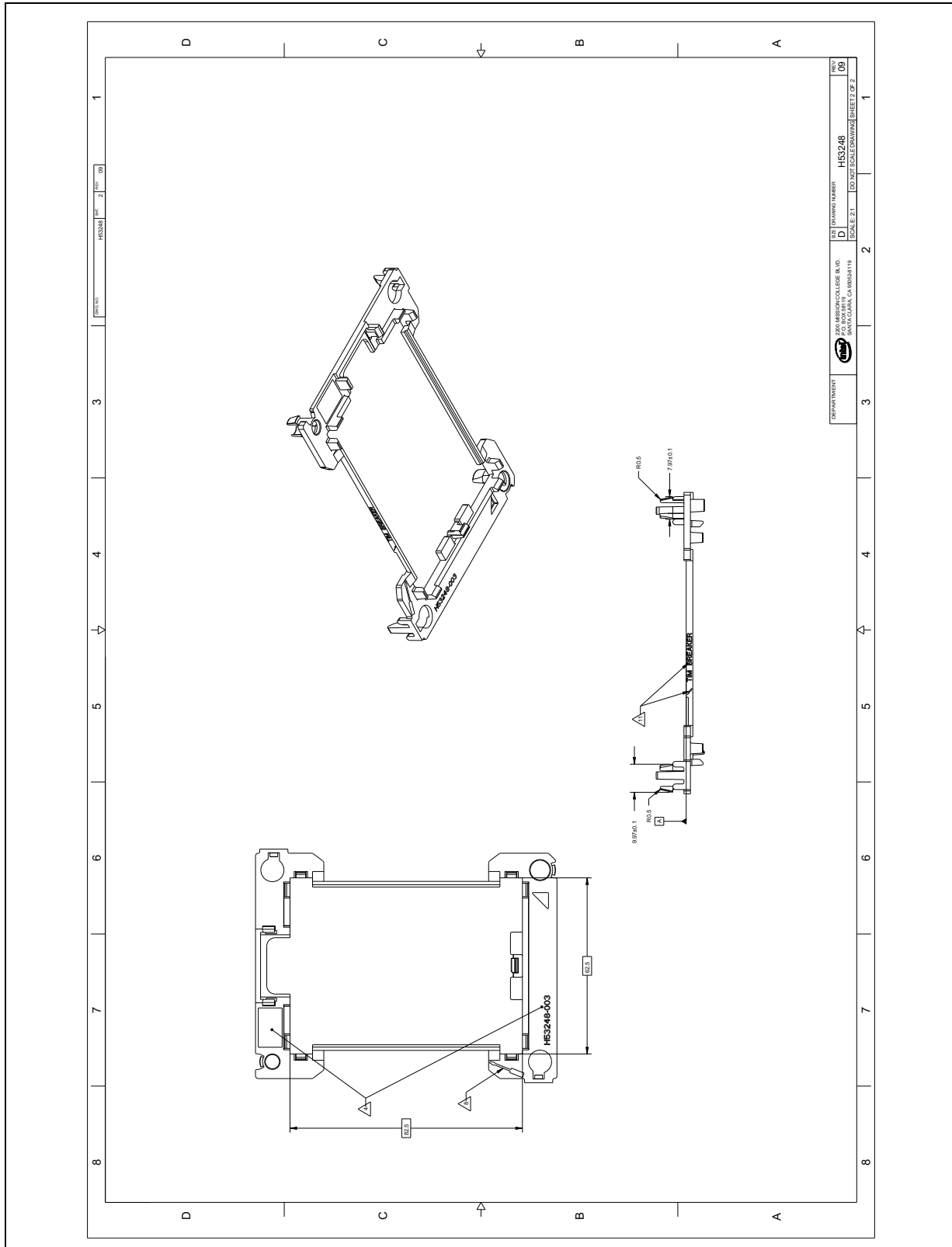


Figure E-11. Backplate

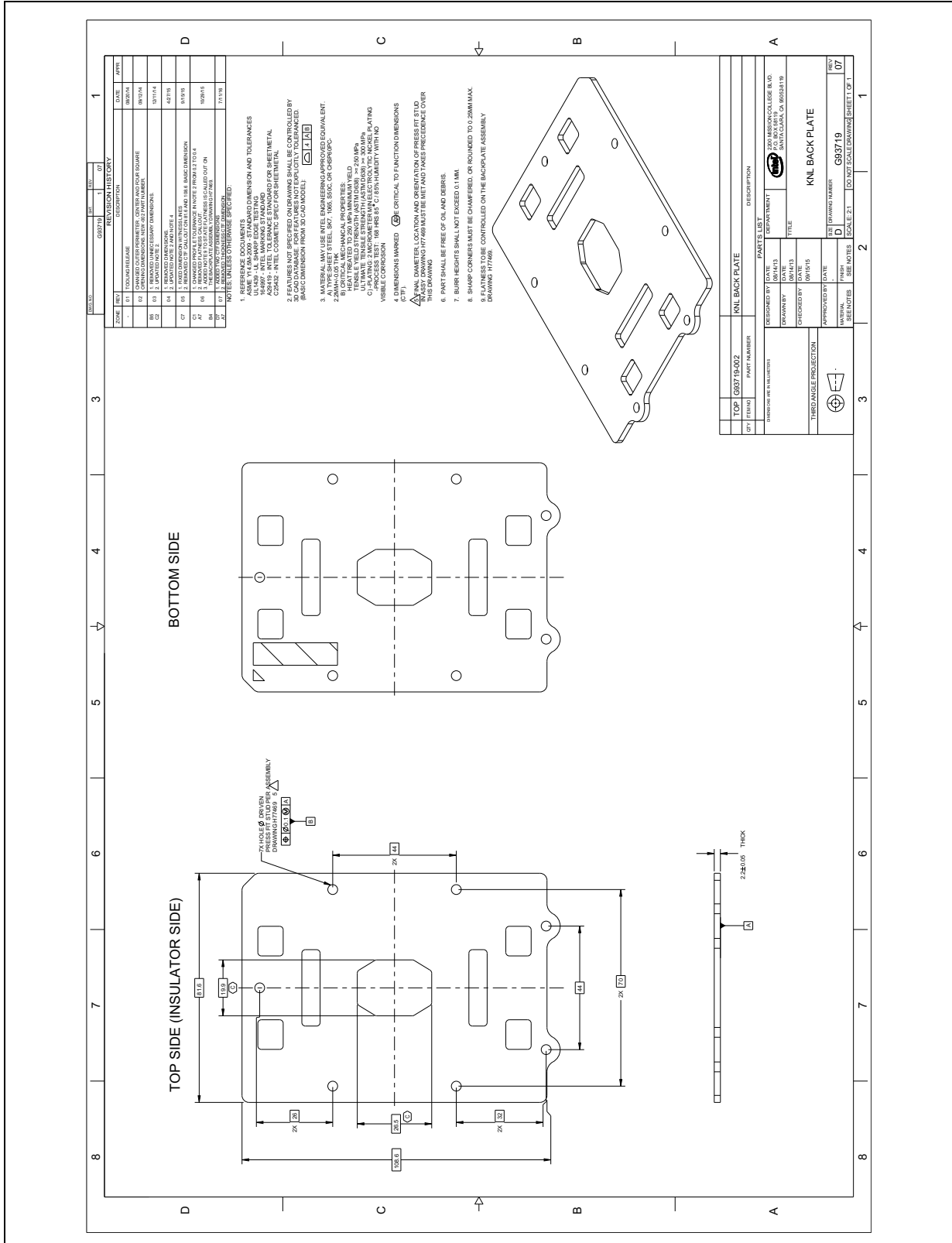


Figure E-12. Backplate Insulator

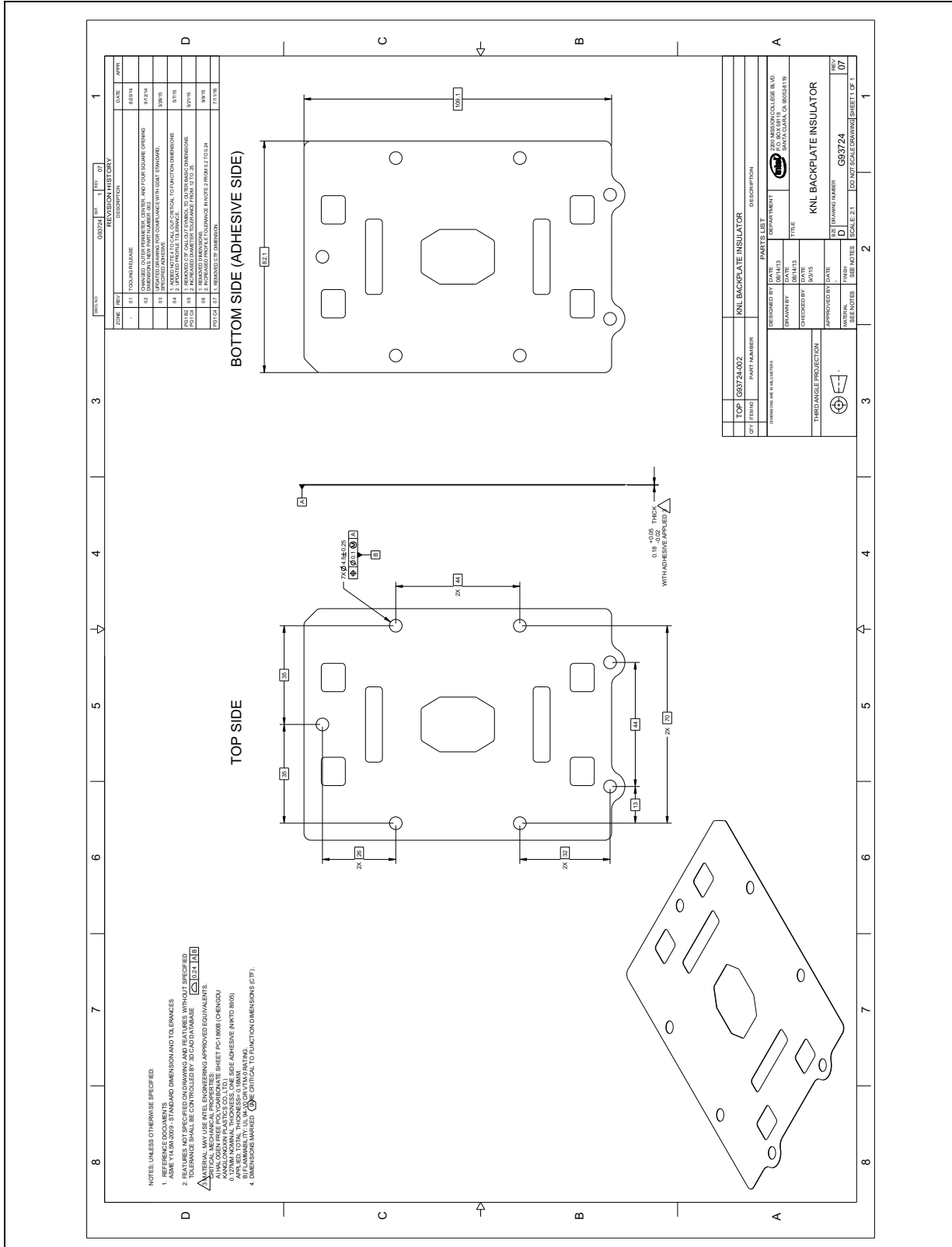




Figure E-13. Back Plate, M3 Stud

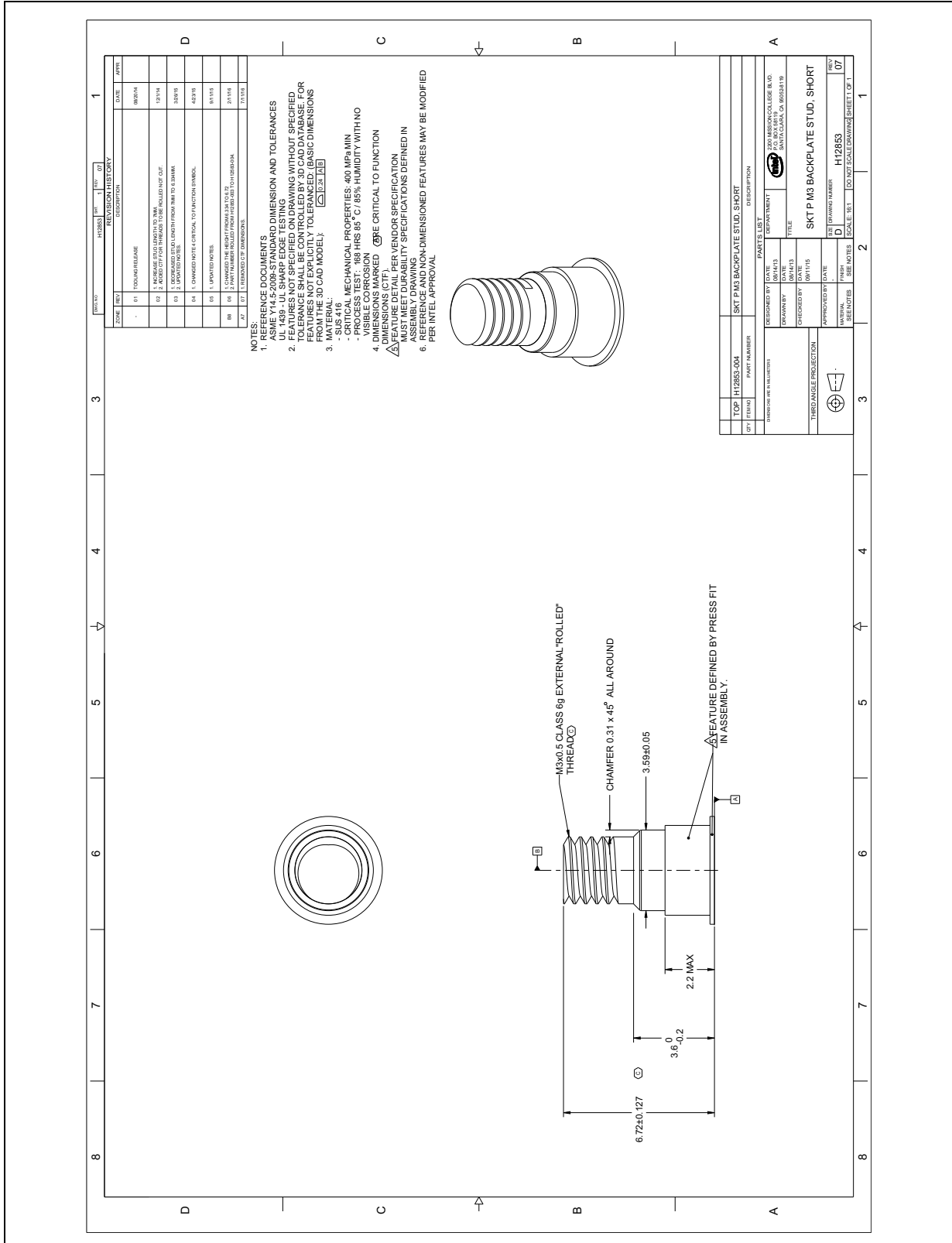
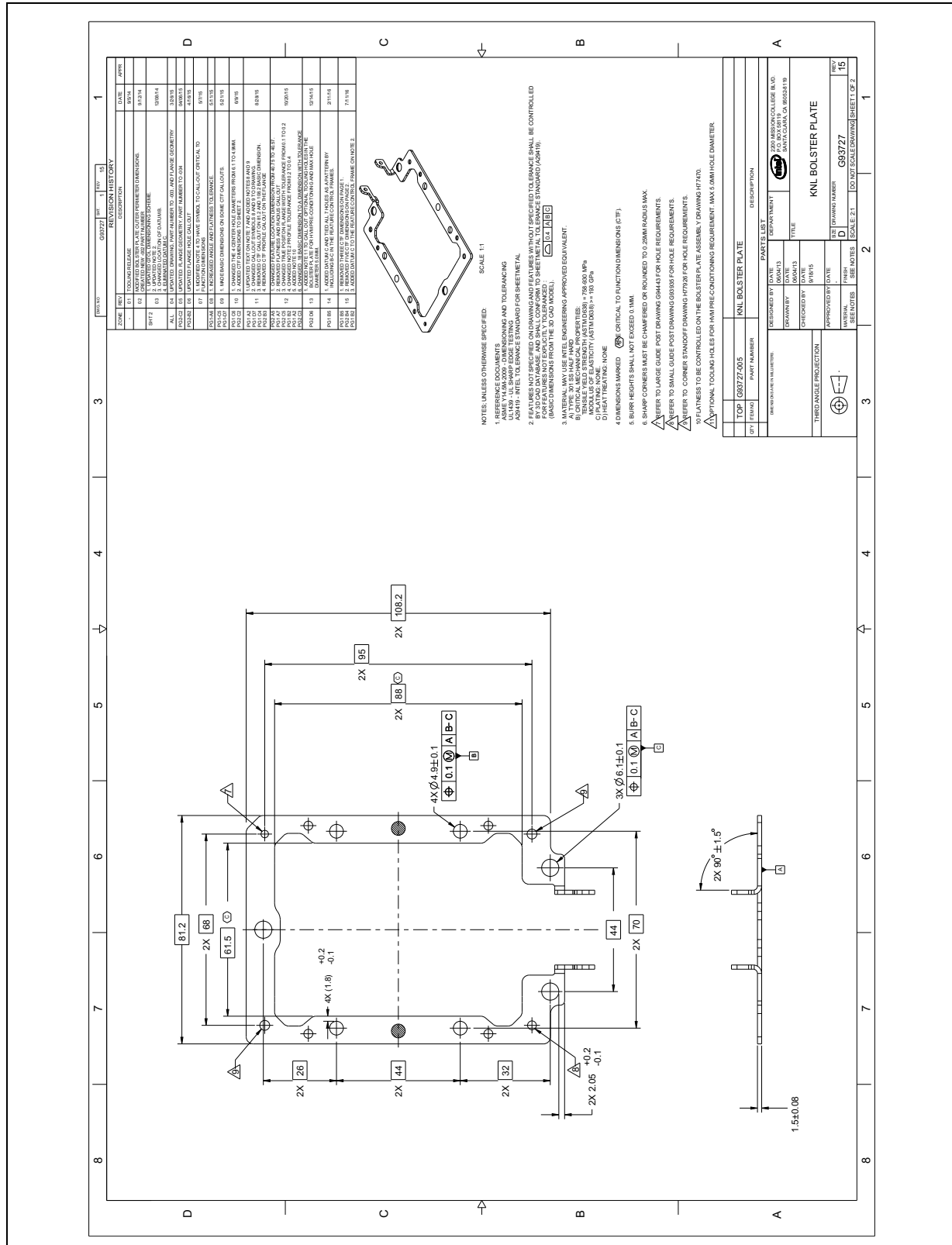


Figure E-14. Bolster Plate, 1/2



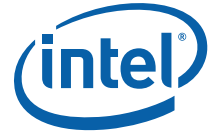


Figure E-15. Bolster Plate, 2/2

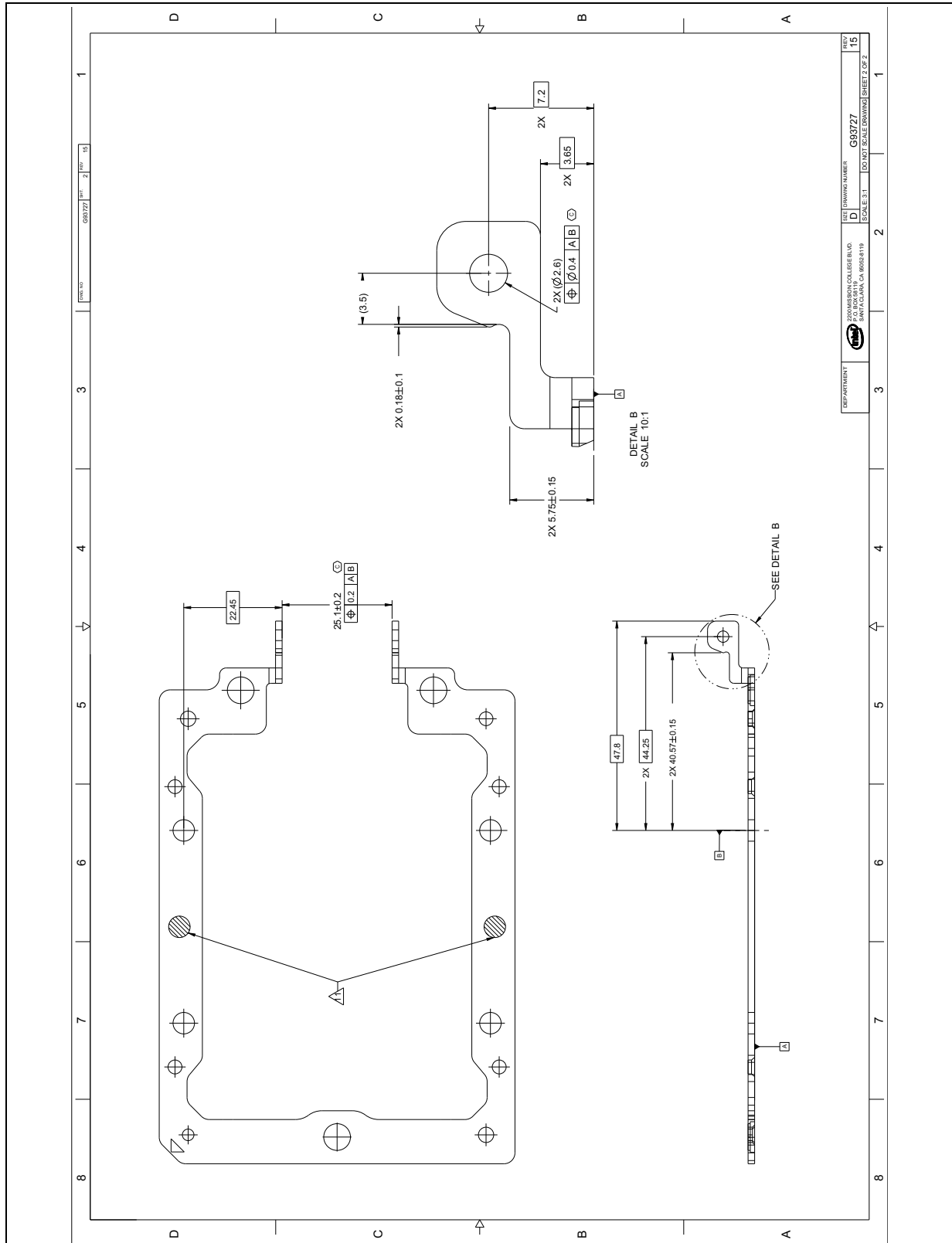
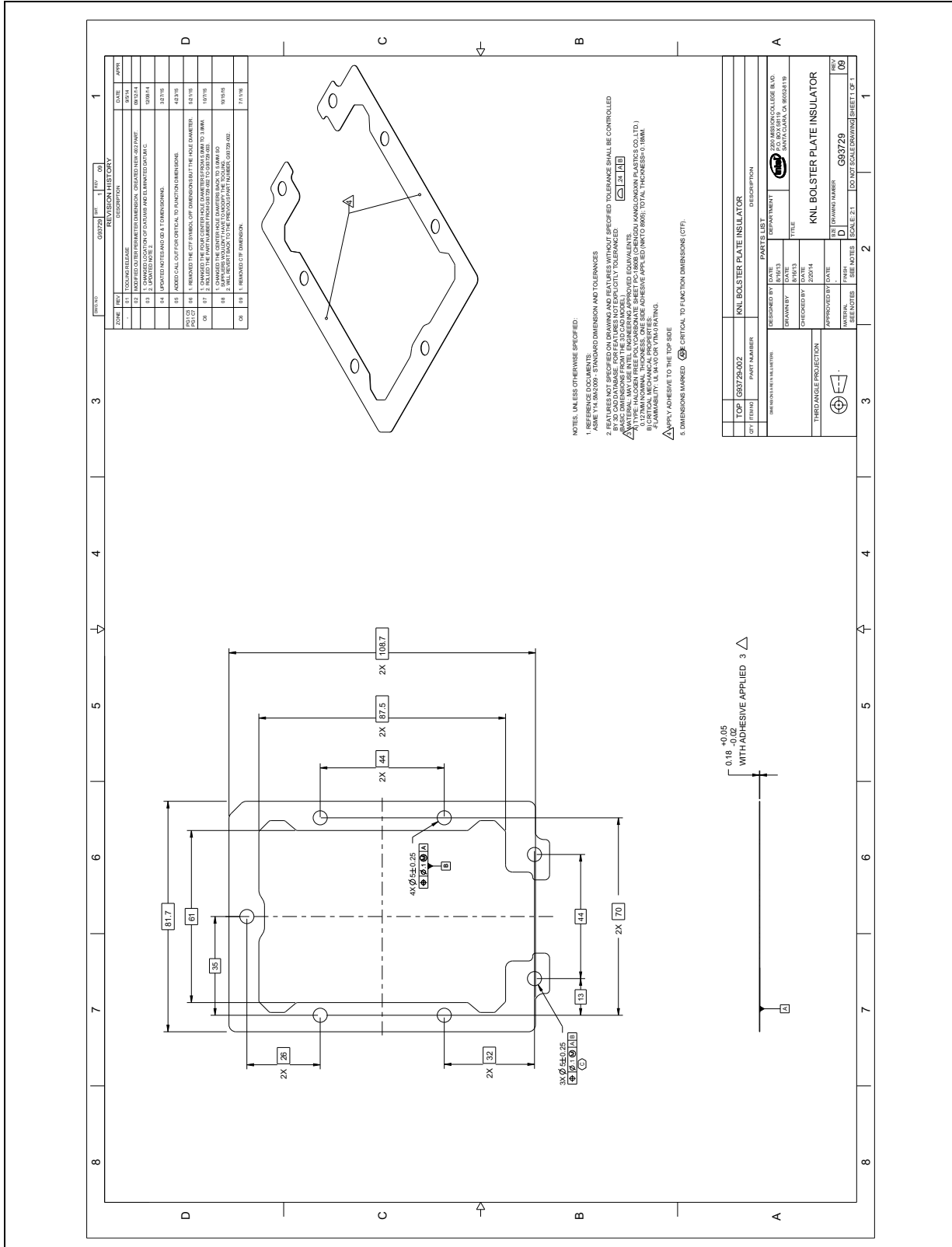


Figure E-16. Bolster Plate, Insulator



DATE	REV	DESCRIPTION	BY	APPV
03/27/04	1	ISSUE		
04/23/04	2	ISSUE		

ZONE	REV	DESCRIPTION
1	1	ISSUE
2	2	ISSUE
3	3	ISSUE
4	4	ISSUE
5	5	ISSUE
6	6	ISSUE
7	7	ISSUE
8	8	ISSUE
9	9	ISSUE
10	10	ISSUE

- NOTES: UNLESS OTHERWISE SPECIFIED:
1. REFERENCE DOCUMENTS:
ASME Y14.5M-2004: STANDARD DIMENSION AND TOLERANCES
 2. FEATURES NOT SPECIFIED ON DRAWING AND FEATURES WITHOUT SPECIFIED TOLERANCE SHALL BE CONTROLLED BY THE DIMENSIONS FROM THE 3D CAD MODEL.
 3. DIMENSIONS FROM THE 3D CAD MODEL SHALL BE PRECEDENT TO DIMENSIONS FROM THIS DRAWING.
 4. TYPE: HALCON FREELY CONFORMABLE SHEET POLYIMIDE (KANGJONSON PLASTICS CO., LTD.)
 5. DIMENSIONAL TOLERANCES: ONE SIDE ADHESIVE APPLIED (NKTD 8805); TOTAL THICKNESS: 0.10MM
 6. FLAMMABILITY: UL 94V0 OR EQUIVANT.
 7. APPLY ADHESIVE TO THE TOP SIDE.
 8. DIMENSIONS MARKED \ominus : CRITICAL TO FUNCTION DIMENSIONS (CTF).

TOP PART NUMBER	DESCRIPTION
GS8729-022	KNL BOLSTER PLATE INSULATOR

DESIGNED BY	DATE	DESIGN CHECKED BY	DATE

CHECKED BY	DATE	APPROVED BY	DATE

REVISION	DESCRIPTION
D	ISSUE
E	ISSUE
F	ISSUE
G	ISSUE
H	ISSUE
I	ISSUE
J	ISSUE
K	ISSUE
L	ISSUE
M	ISSUE
N	ISSUE
O	ISSUE
P	ISSUE
Q	ISSUE
R	ISSUE
S	ISSUE
T	ISSUE
U	ISSUE
V	ISSUE
W	ISSUE
X	ISSUE
Y	ISSUE
Z	ISSUE

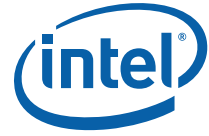


Figure E-17. Bolster Plate, Small Guide Post

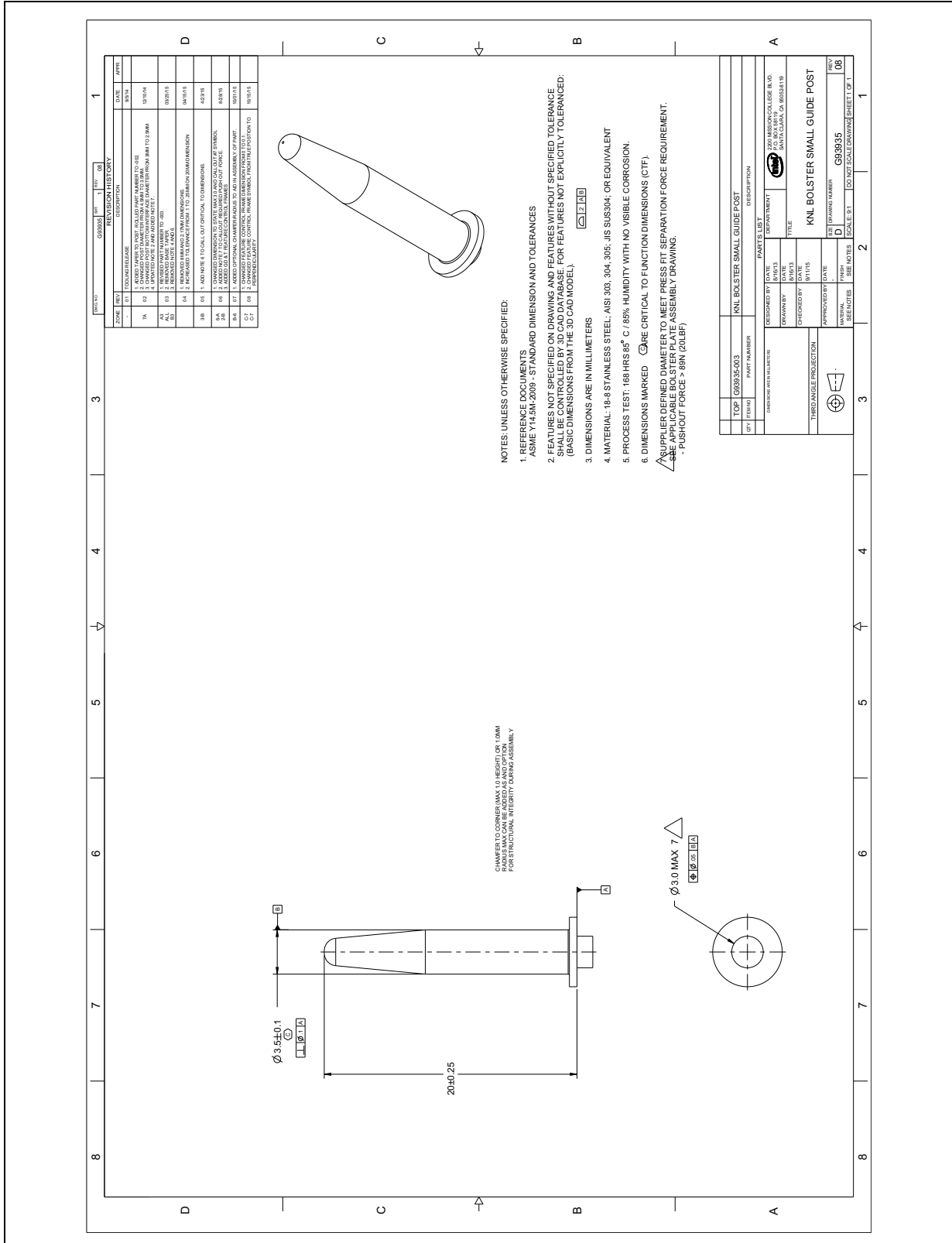
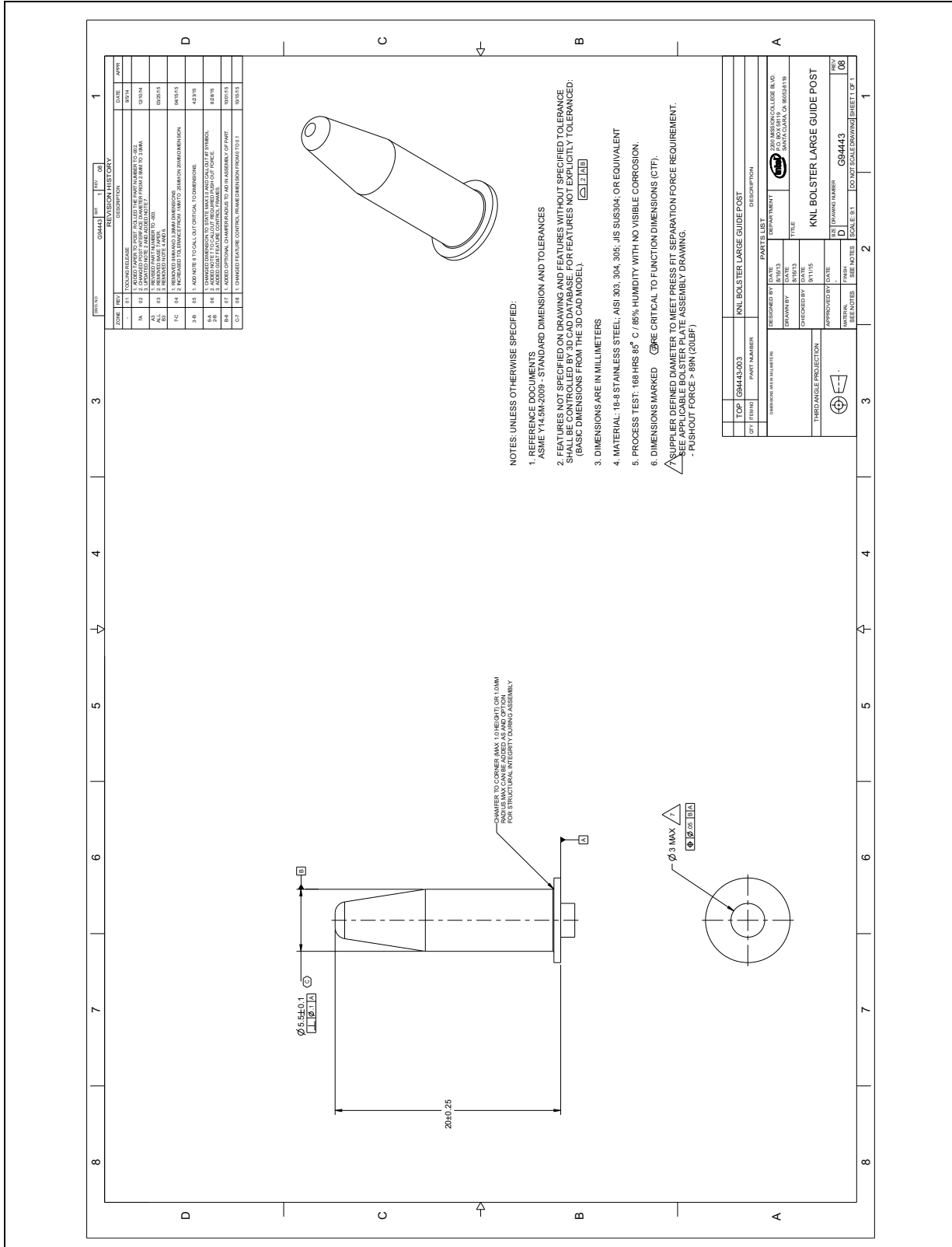


Figure E-18. Bolster Plate, Large Guide Post



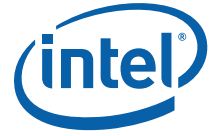


Figure E-19. Bolster Plate, LEC Guide Pin

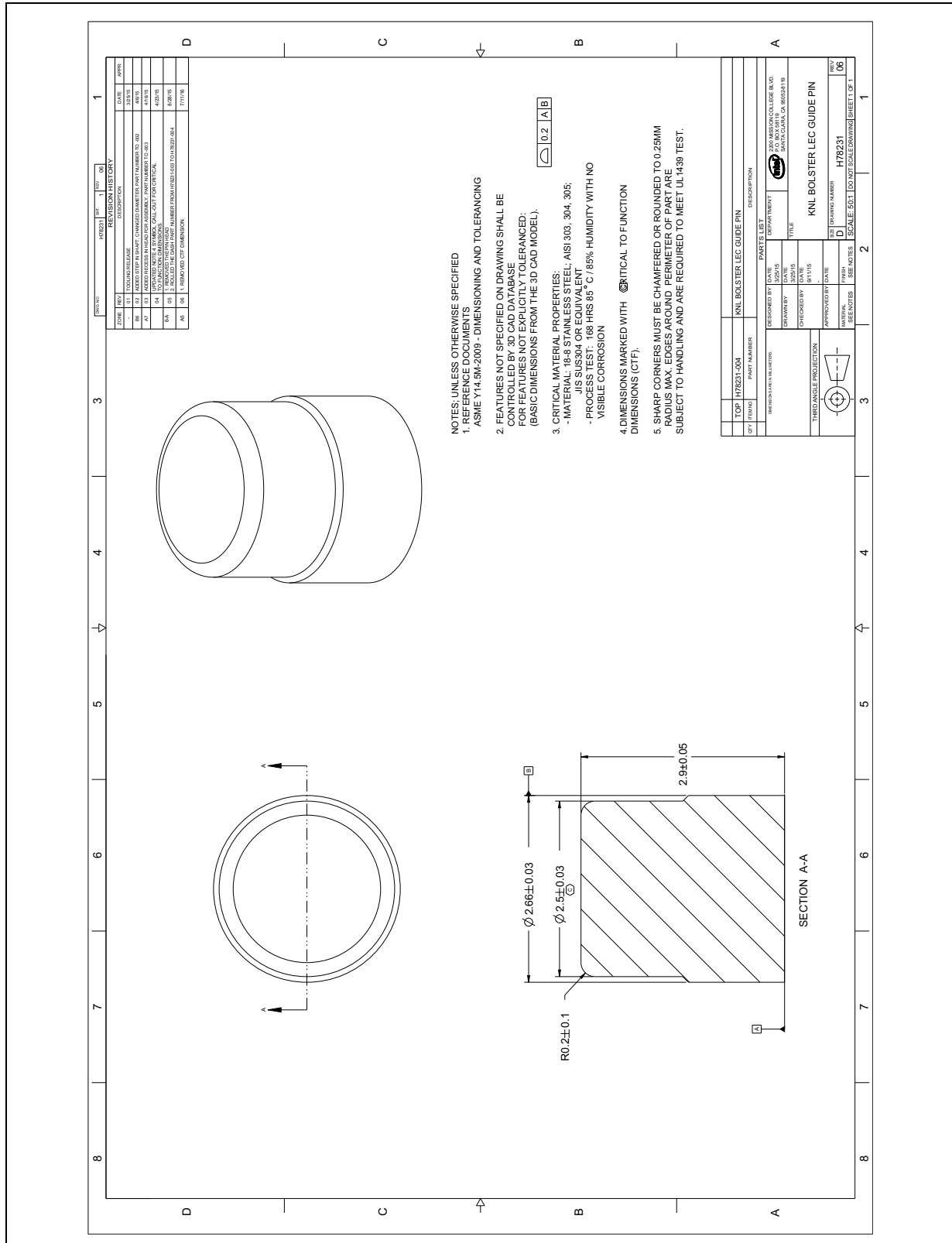


Figure E-20. Bolster Plate, Corner Standoff

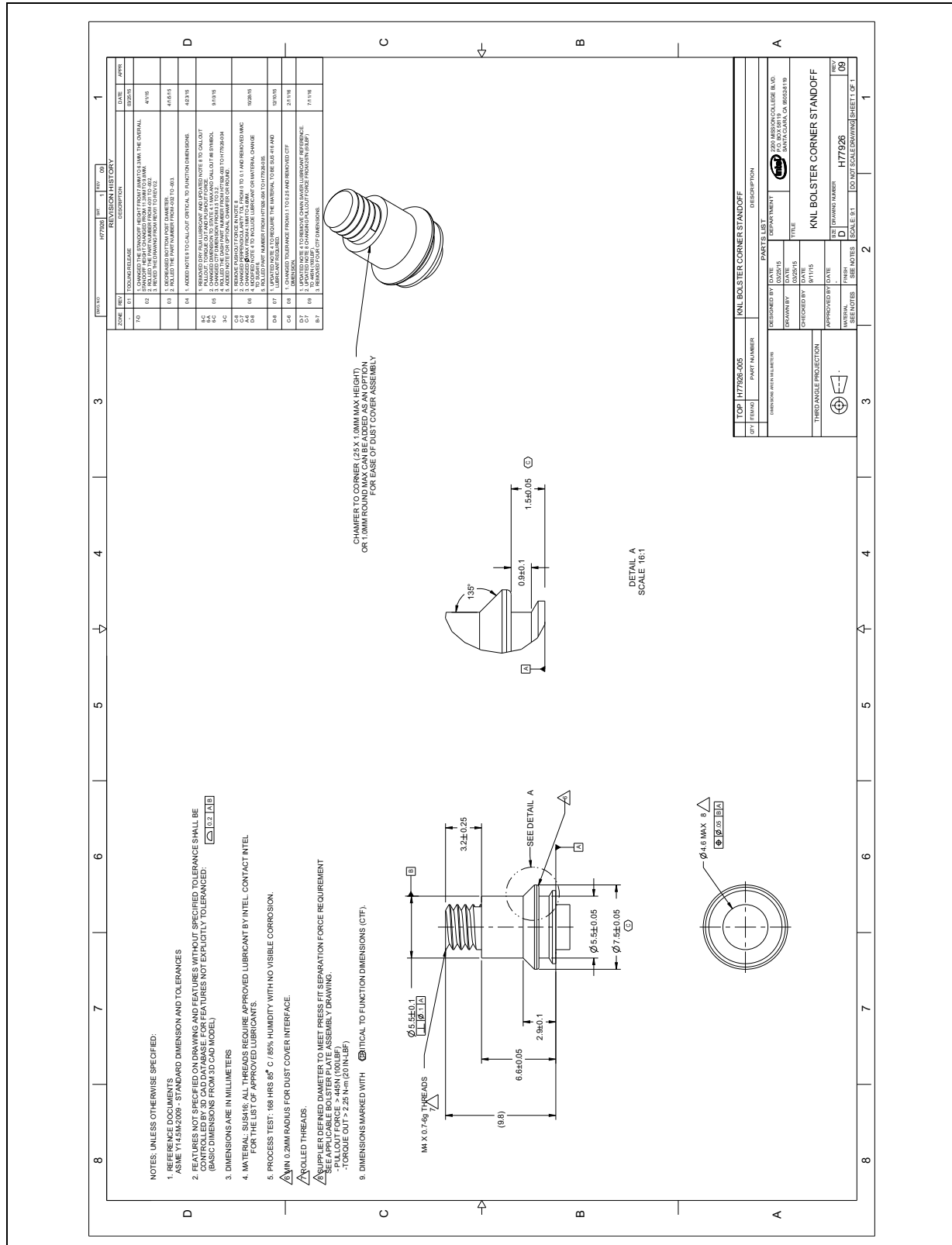


Figure E-21. Bolster Plate, Spring Assembly

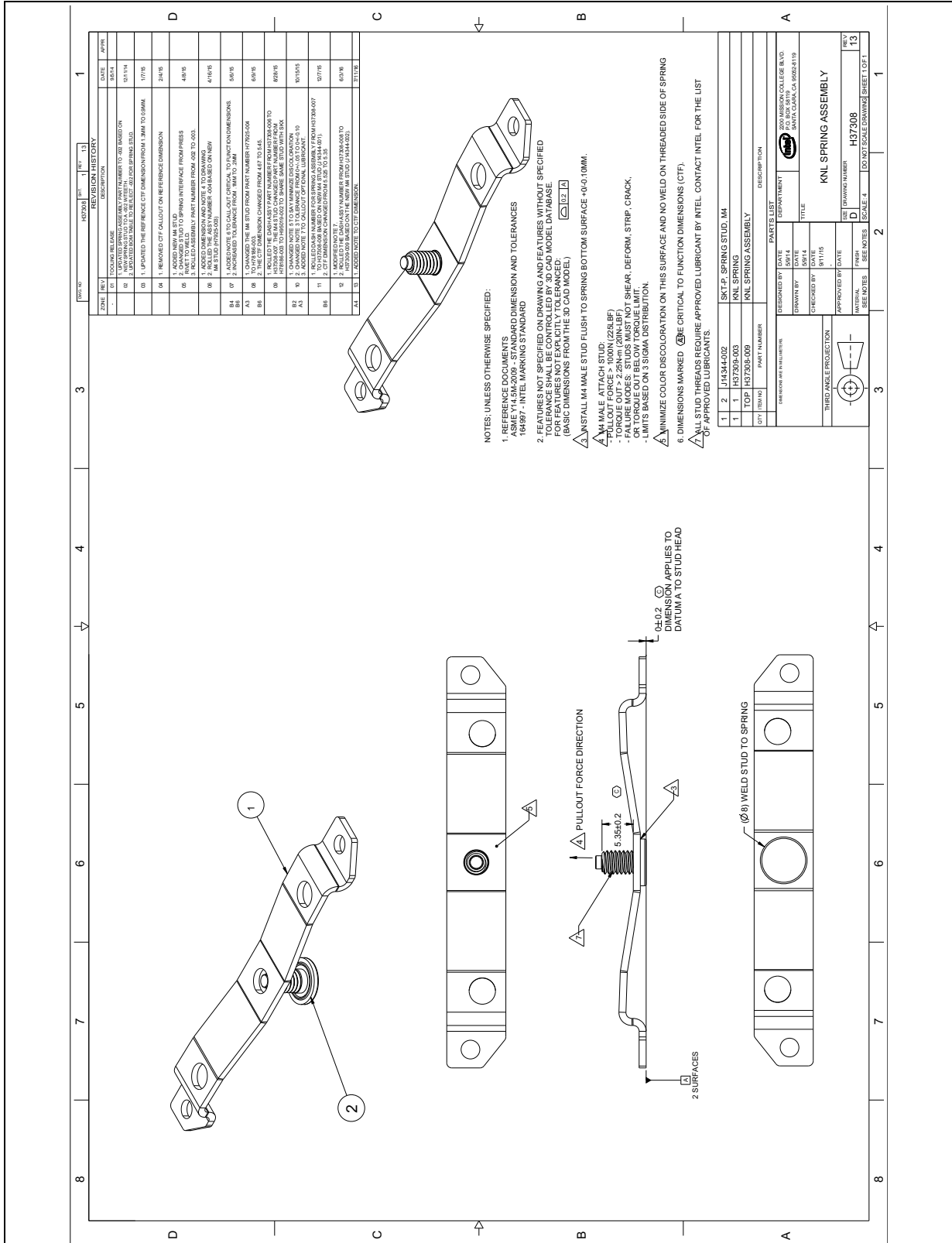
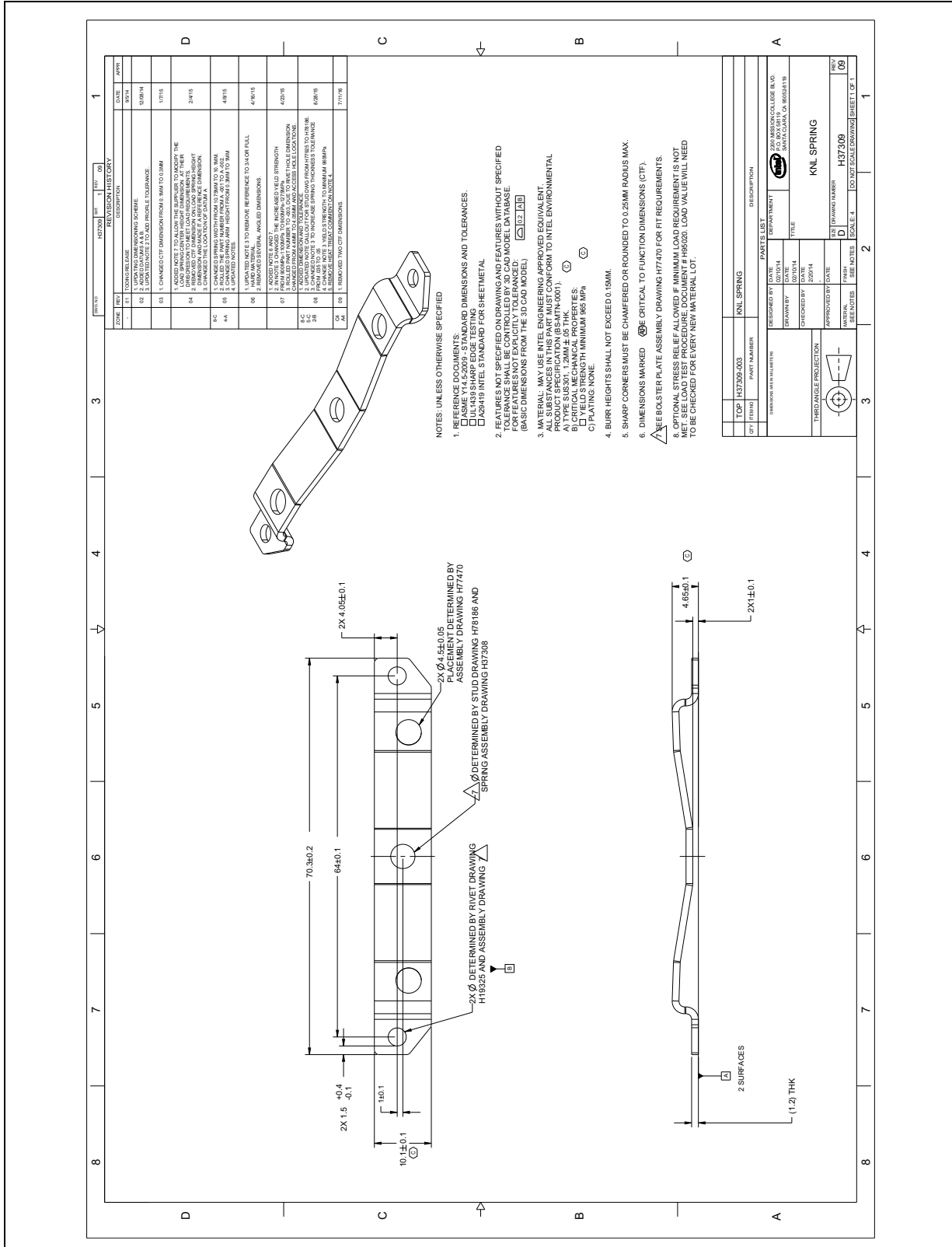


Figure E-22. Bolster Plate, Spring



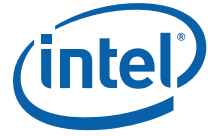


Figure E-23. Bolster Plate, Spring Stud, M4

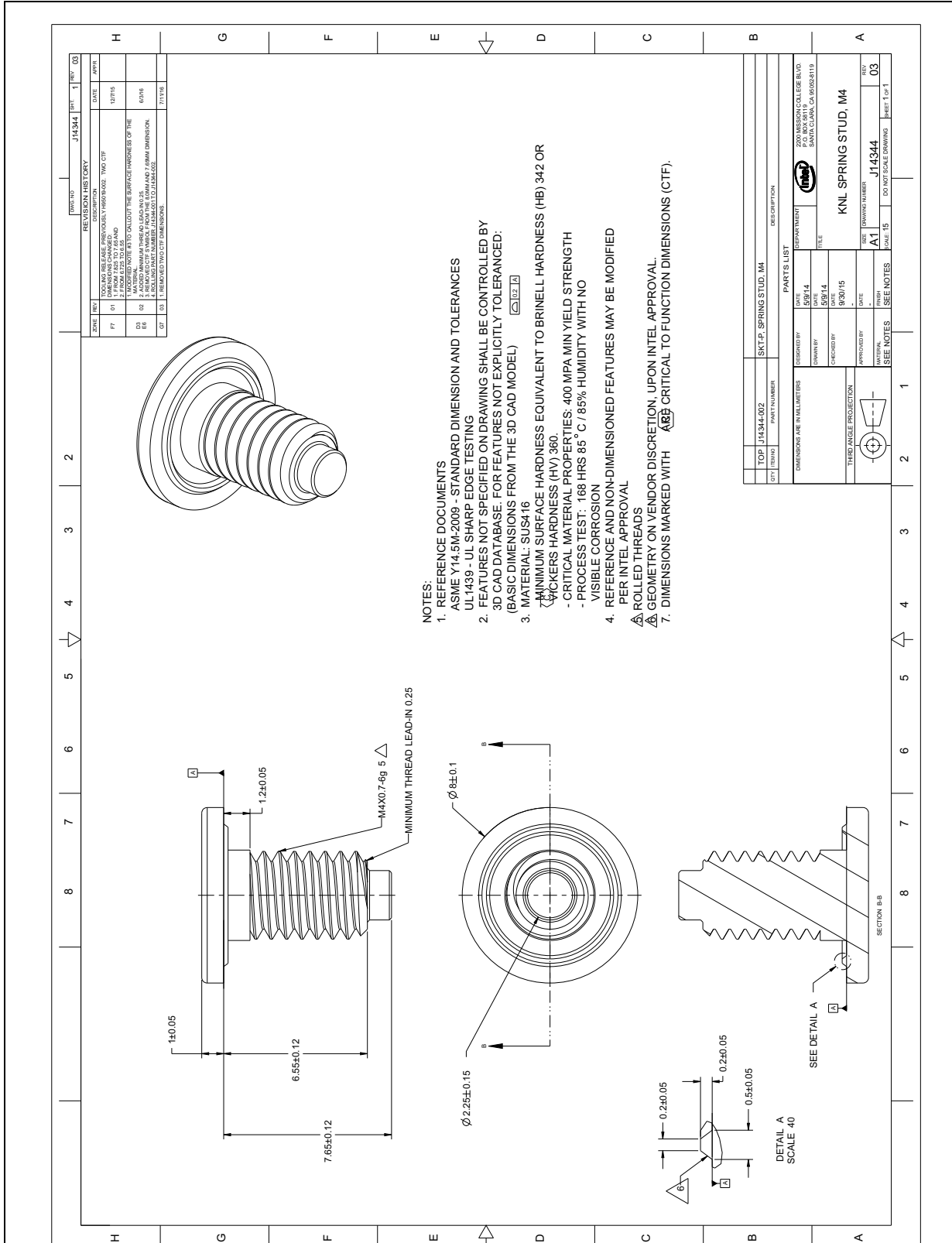
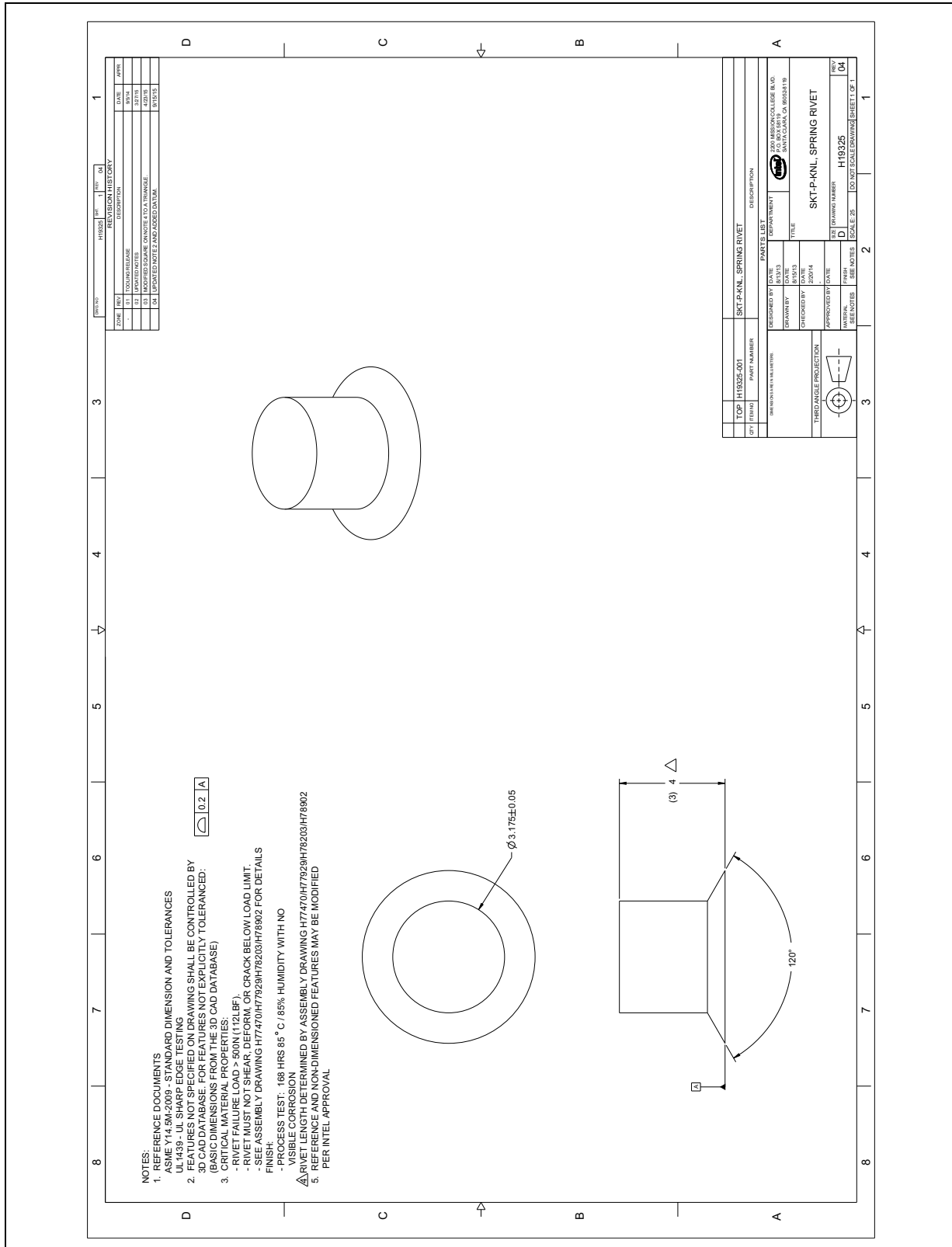


Figure E-24. Bolster Plate, Spring Rivet



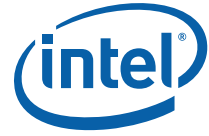


Figure E-25. Bolster Plate, M3 Captive Nut

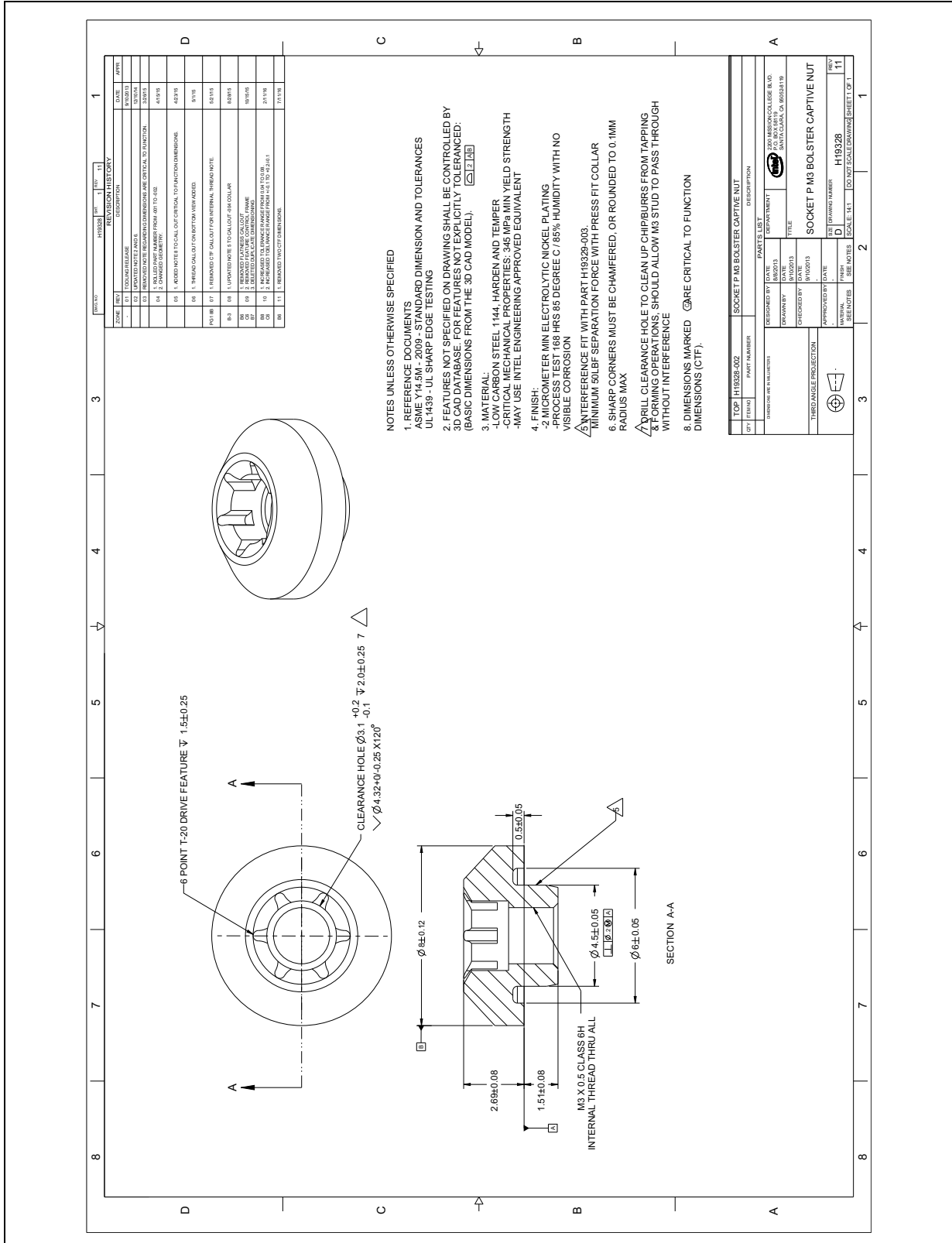
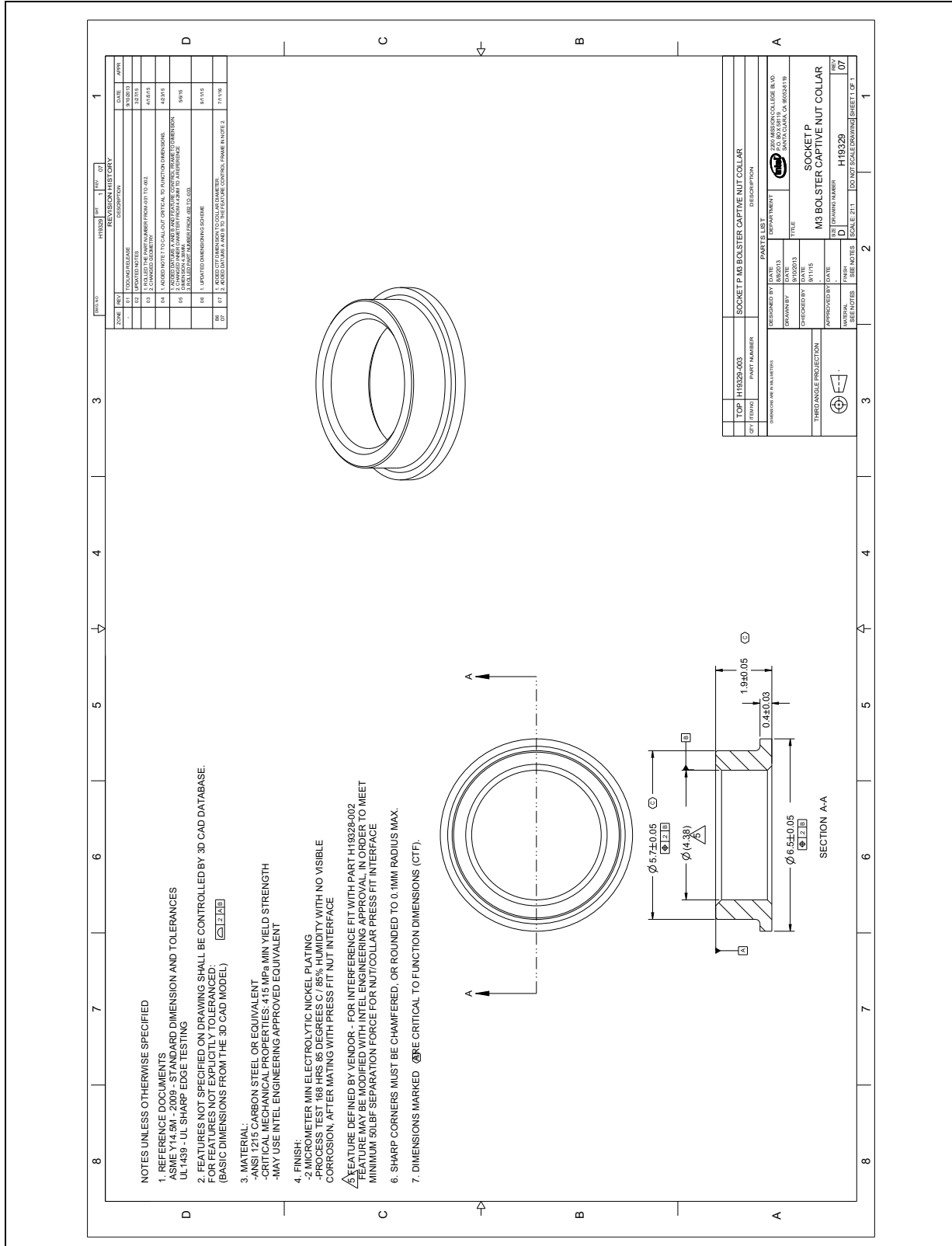


Figure E-26. Bolster Plate, M3 Captive Nut Collar



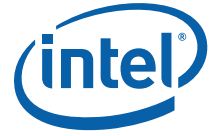


Figure E-27. Socket-P, Dust Cover, 1/2

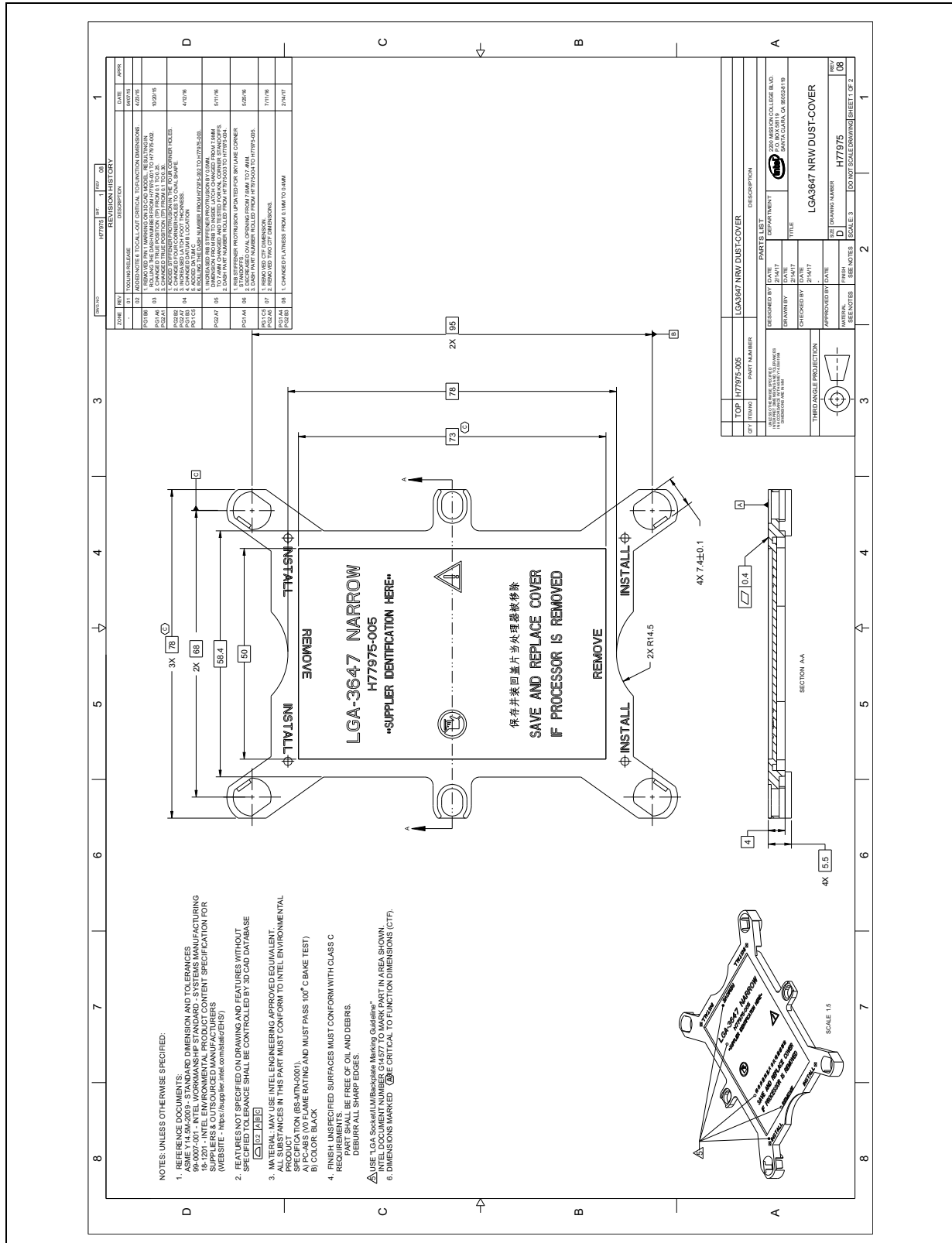
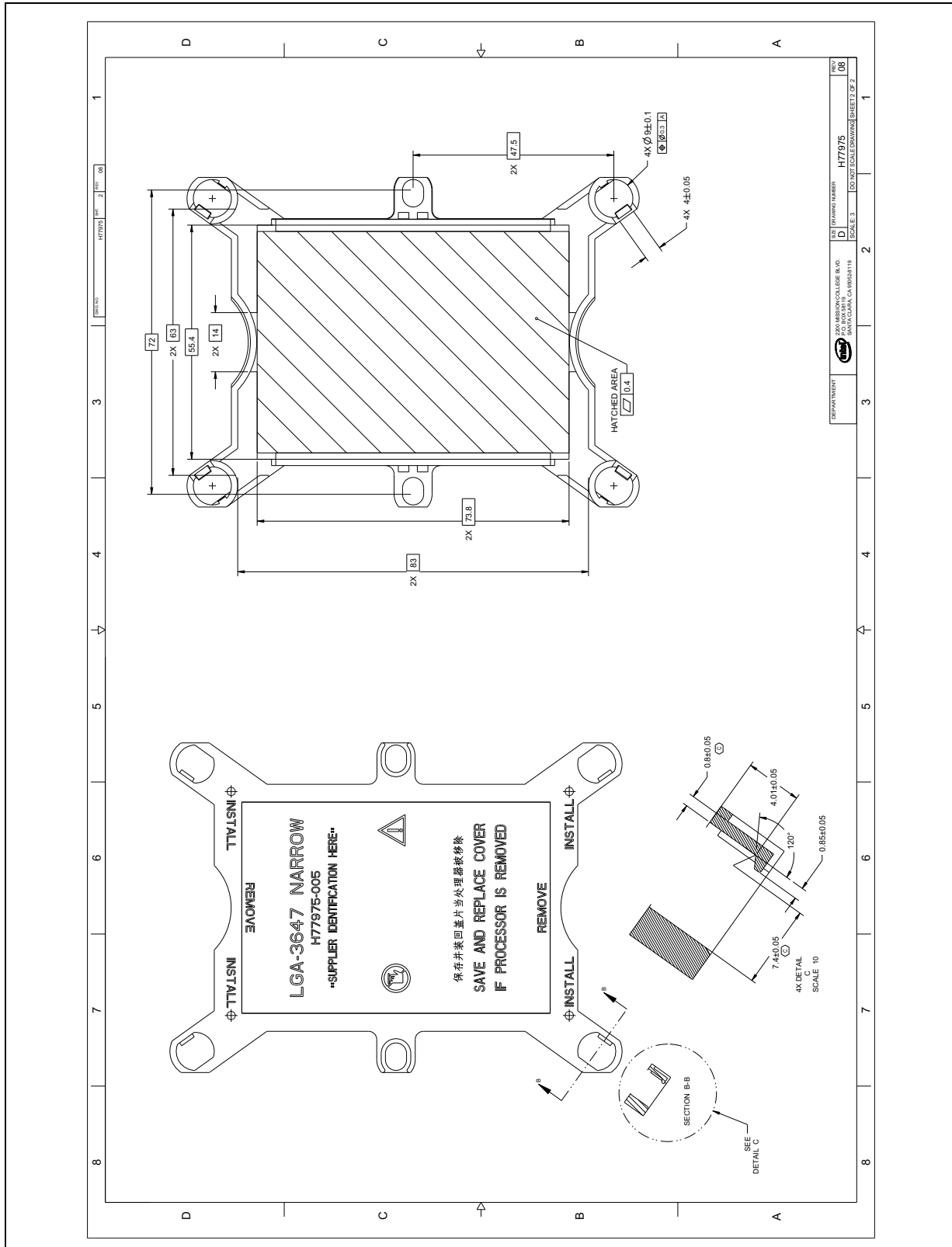




Figure E-28. Socket-P, Dust Cover, 2/2



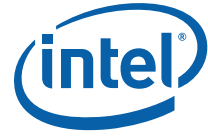


Figure E-29. 1U Heatsink Assembly, 1/2 (Reference Only)

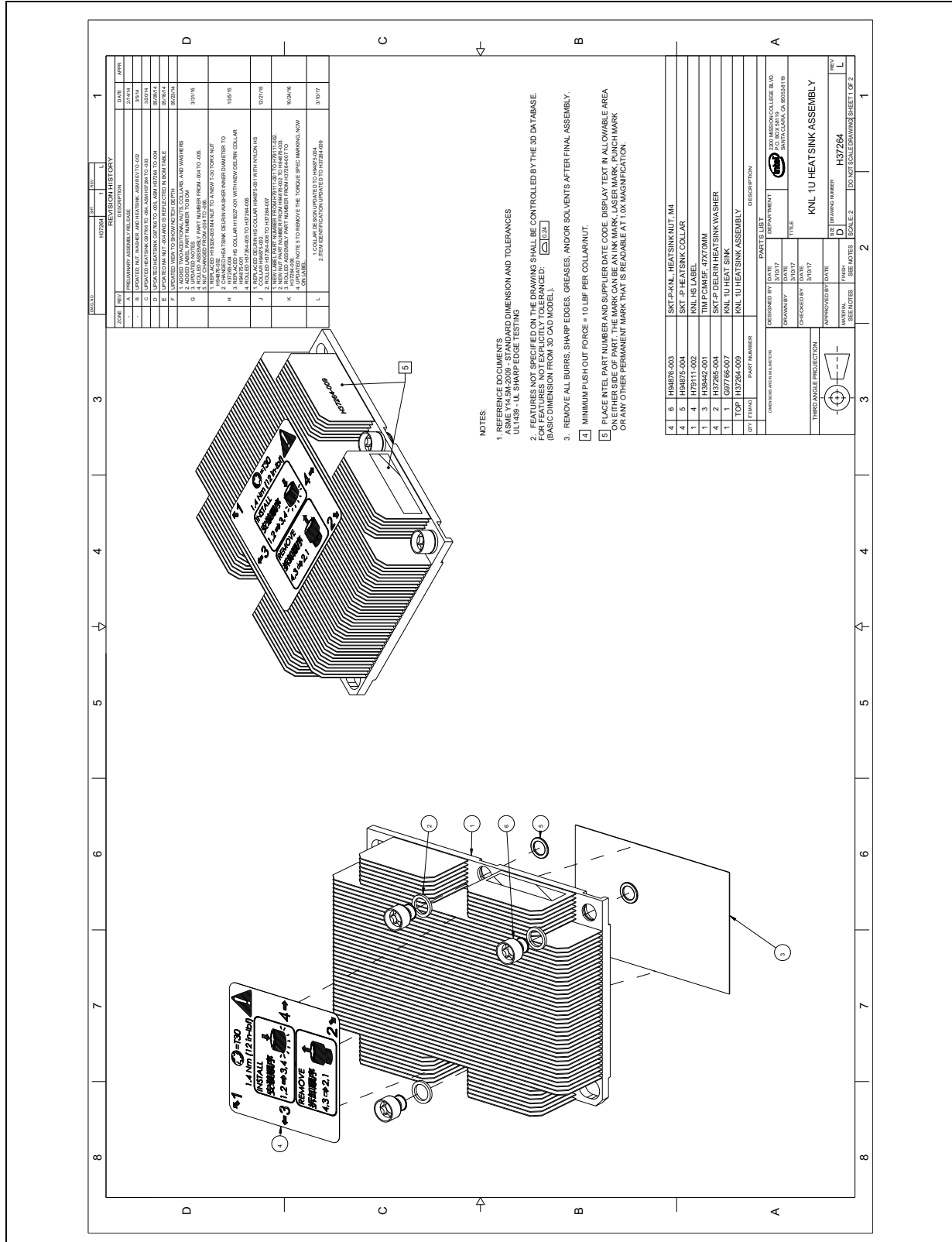


Figure E-30. 1U Heatsink Assembly, 2/2 (Reference Only)

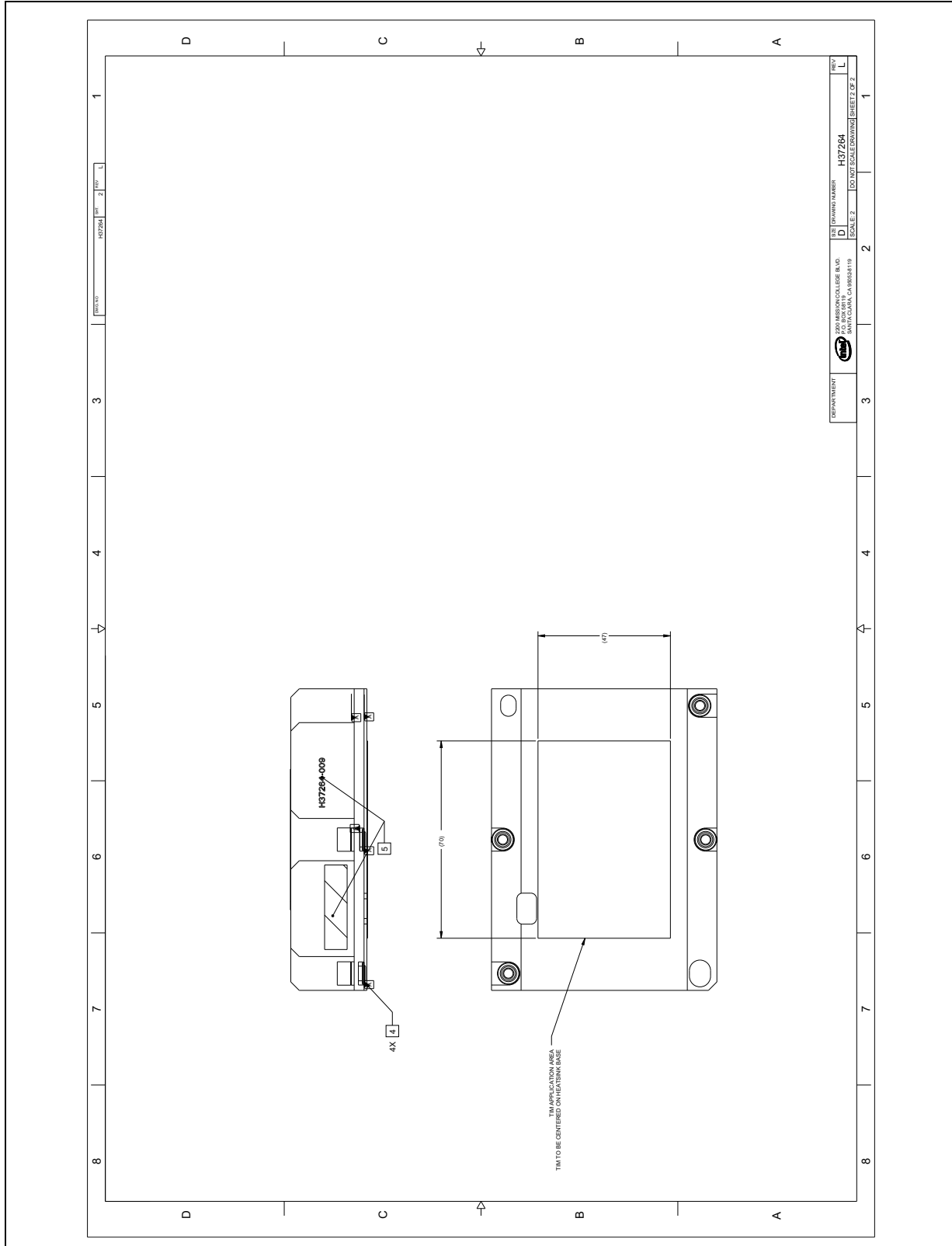


Figure E-31. 1U Heatsink, 1/2 (Reference Only)

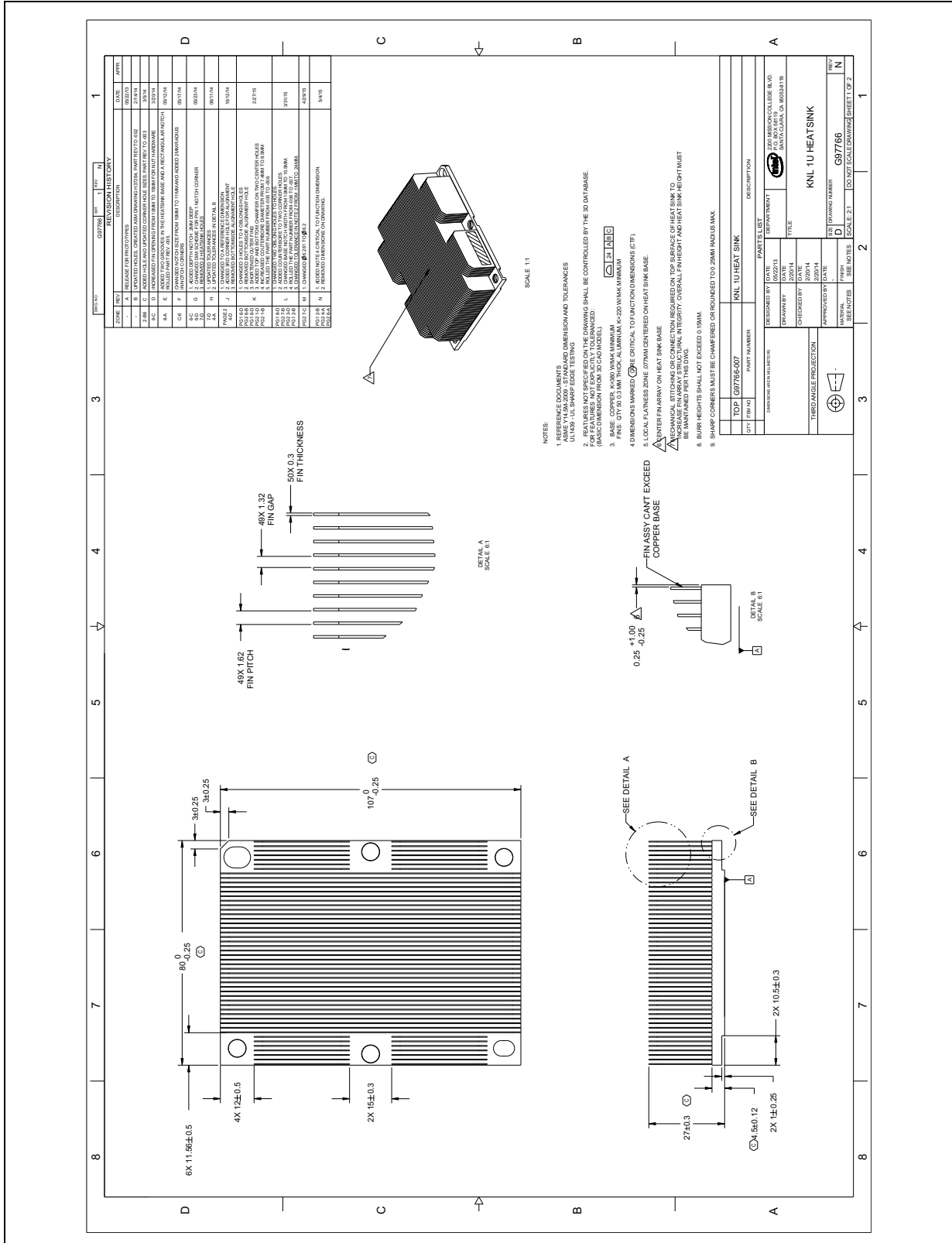
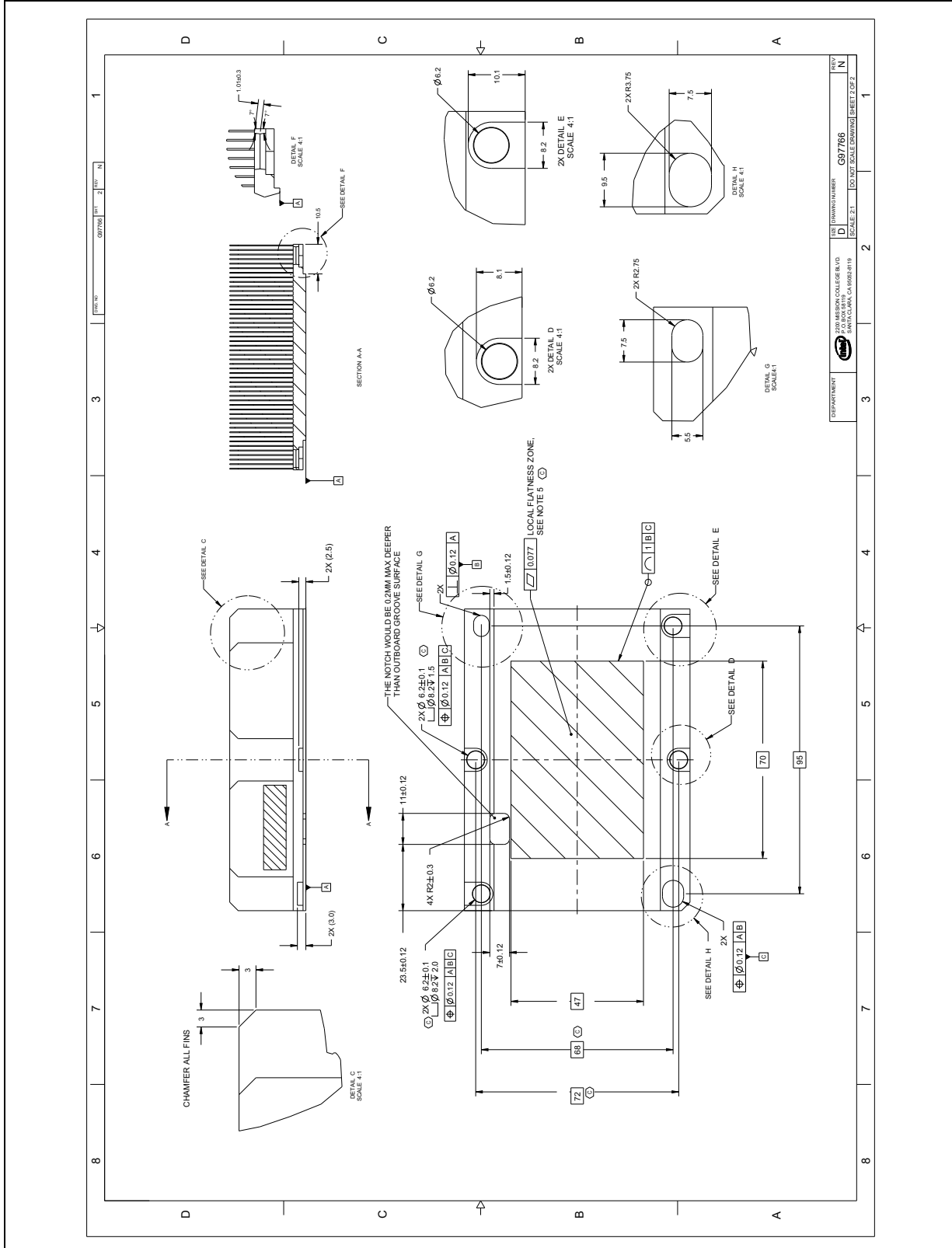




Figure E-32. 1U Heatsink, 2/2 (Reference Only)



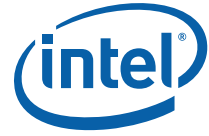


Figure E-33. 1U Heatsink, Label (Reference Only)

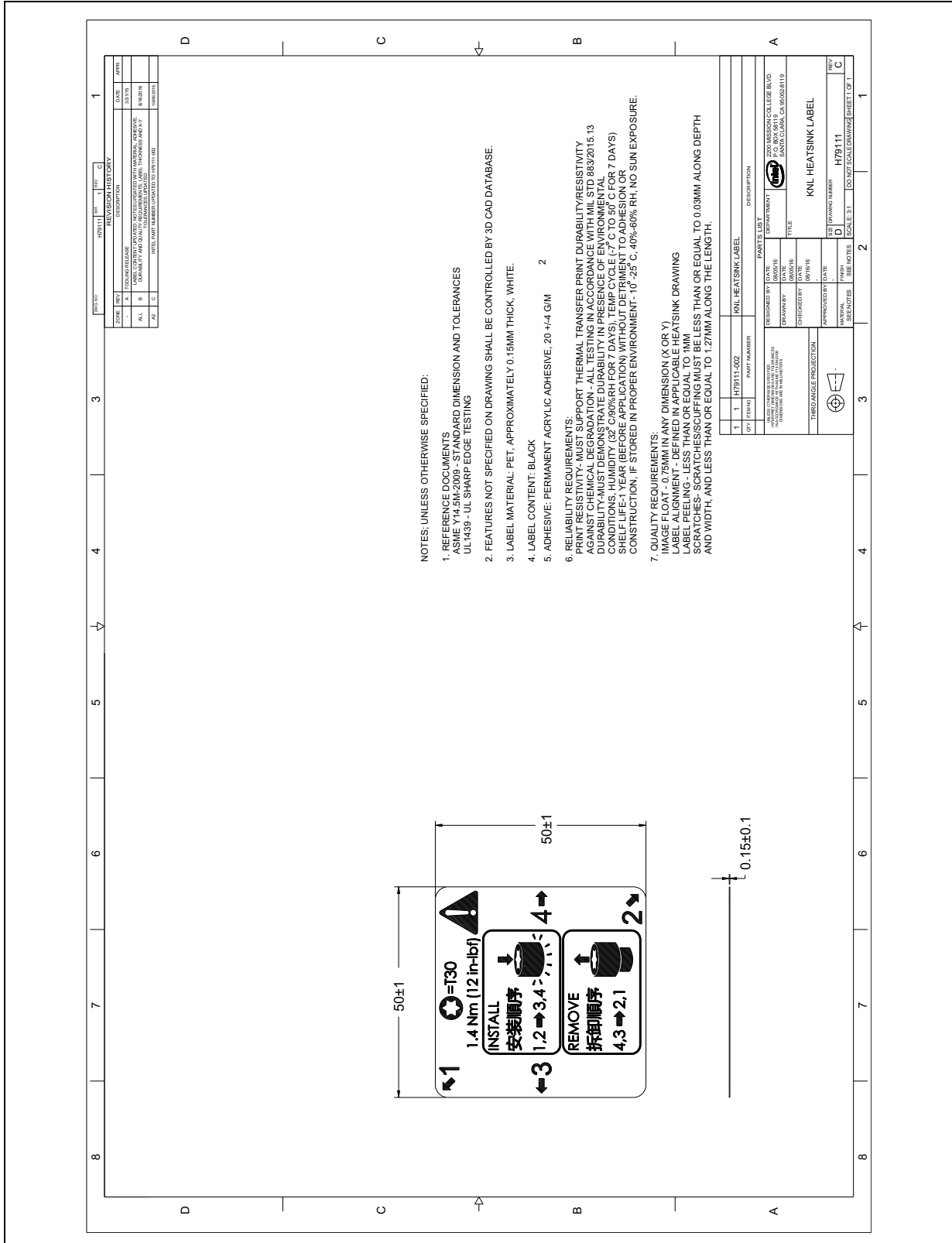




Figure E-34. 1U Heatsink, PCM45F TIM (Reference Only)

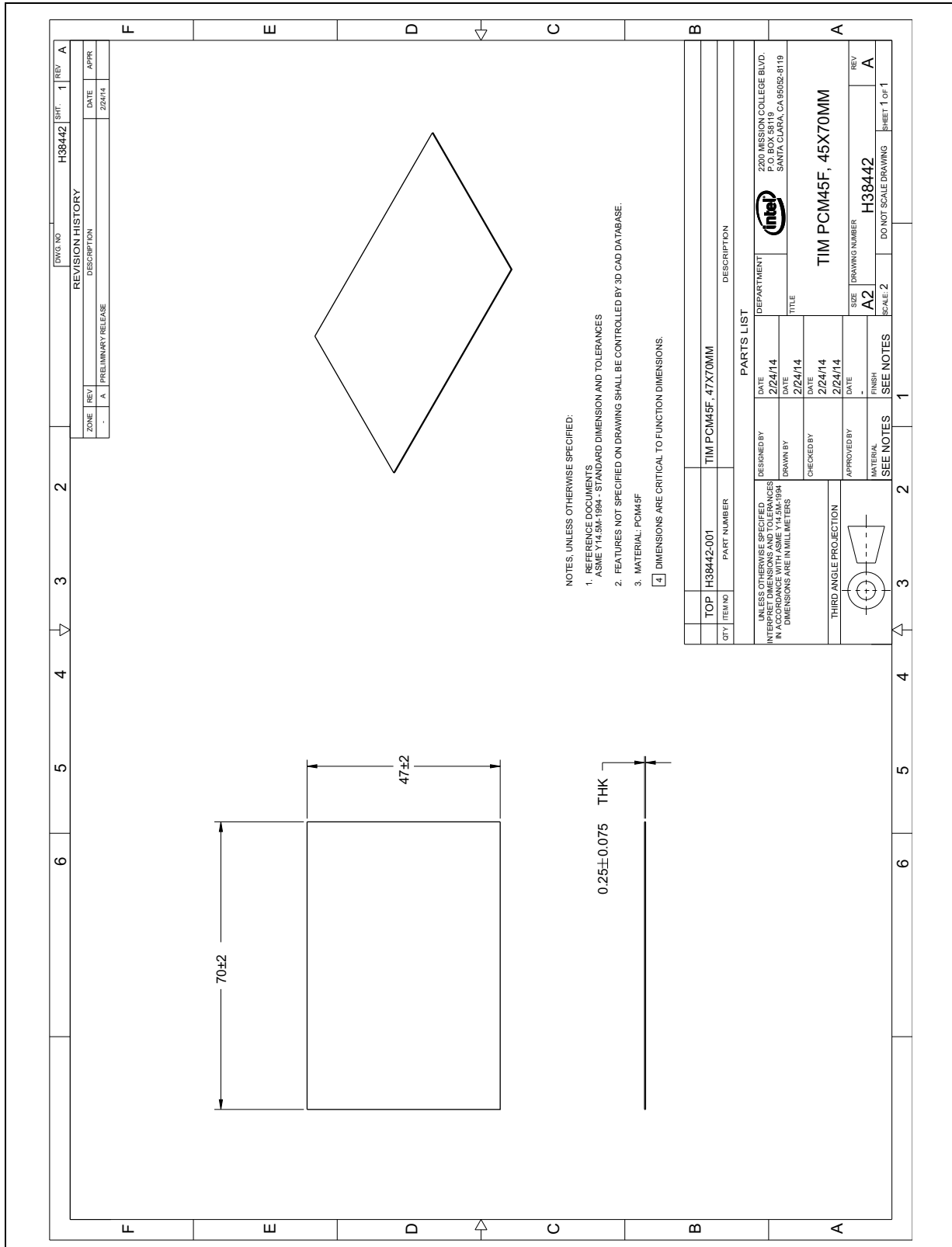




Figure E-36. 1U Heatsink, Nut, M4, 2/2 (Reference Only)

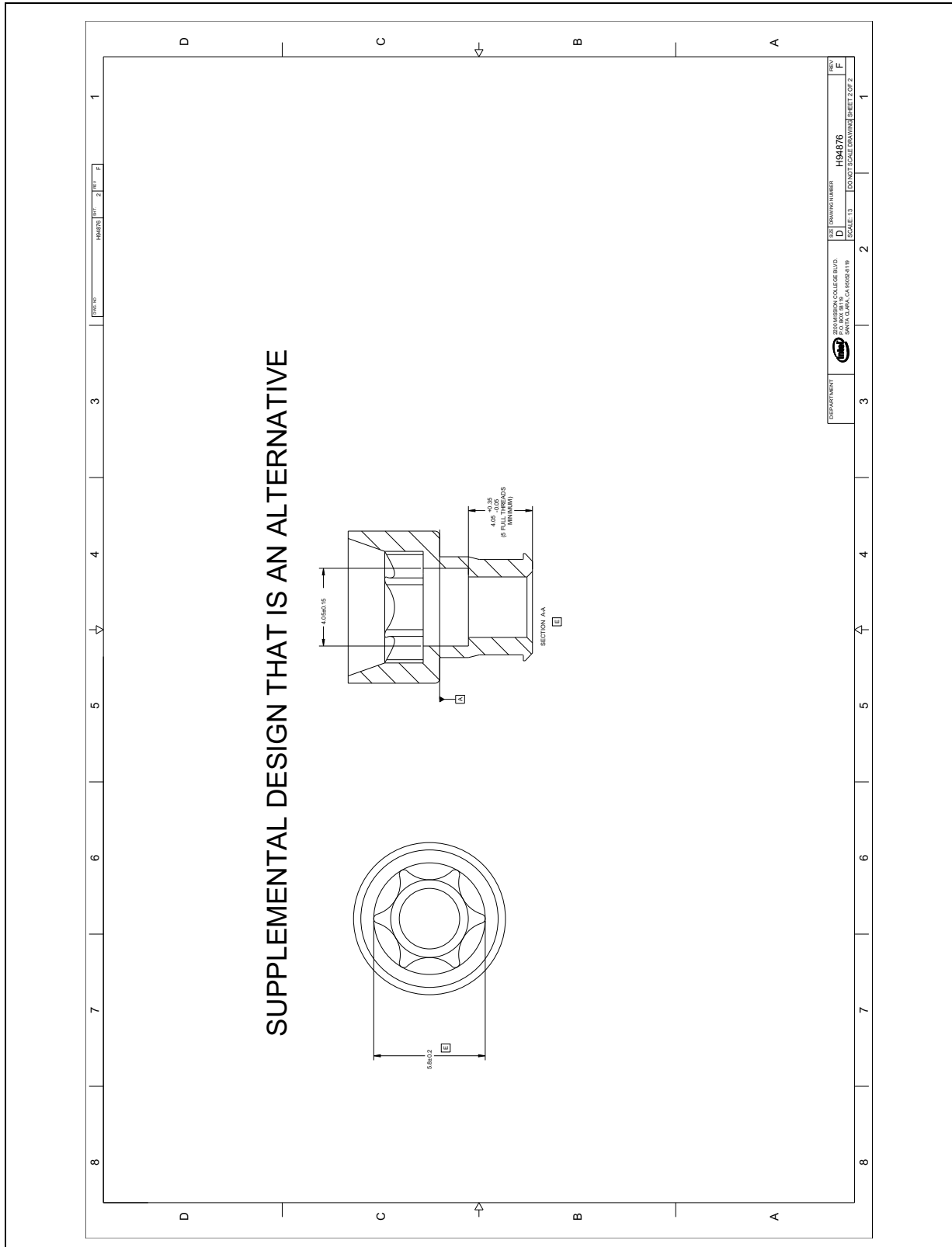




Figure E-37. 1U Heatsink, Nut Collar (Reference Only)

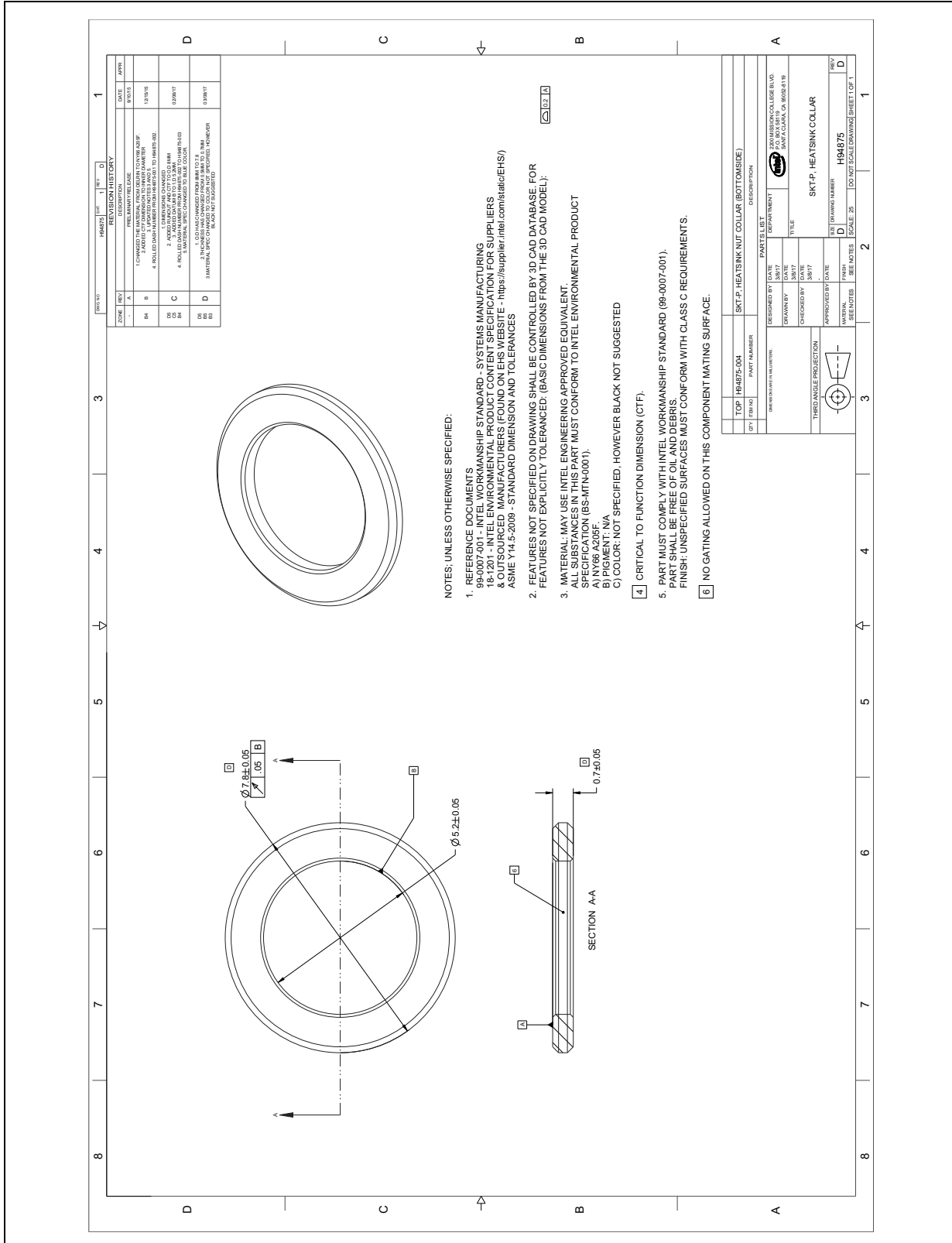
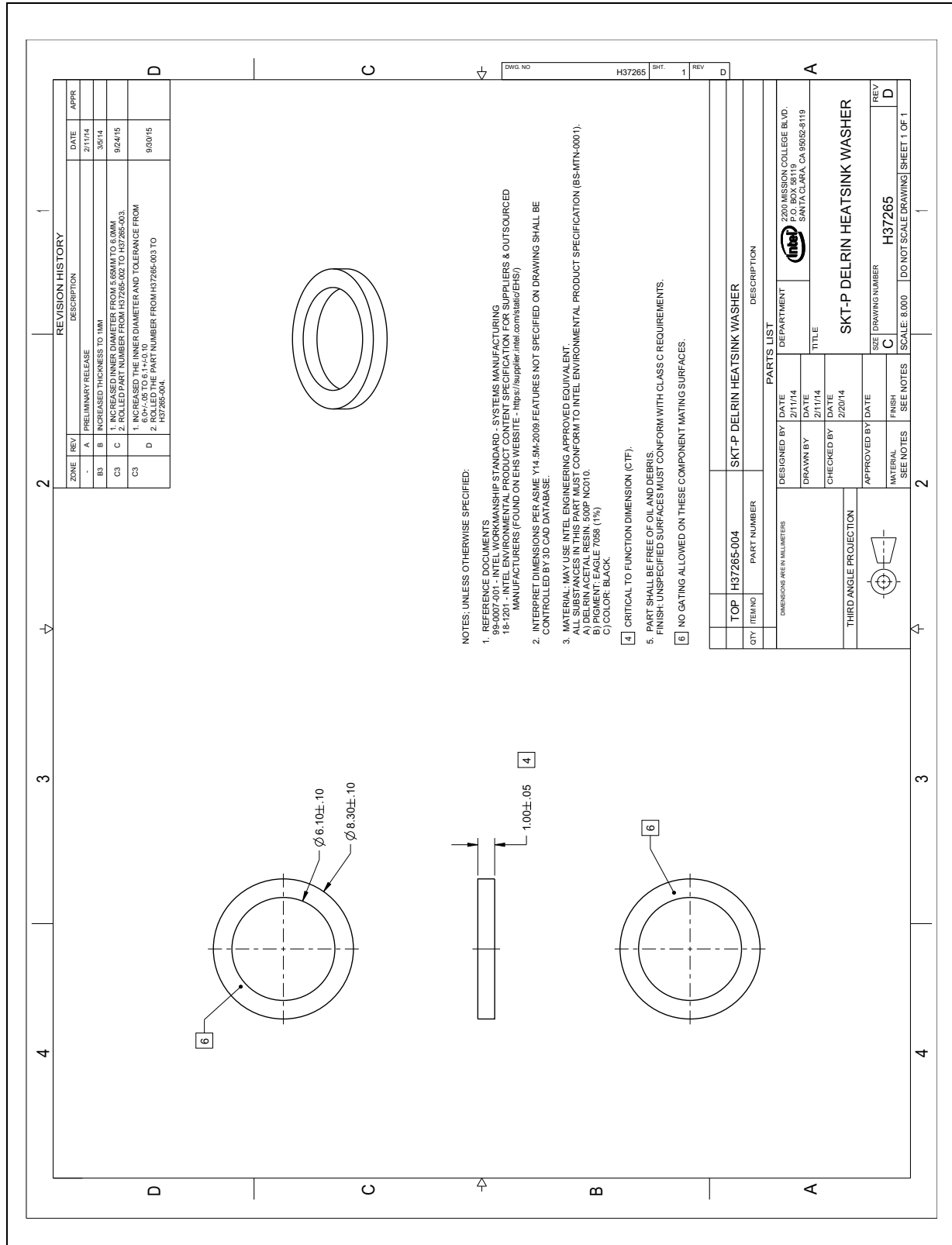


Figure E-38. 1U Heatsink, Delrin* Washer (Reference Only)





F Mechanical KOZs

F.1 Main Board Mechanical KOZs

Processor Heatsink Module (PHM) Keep-Out Zones are included in this appendix. [Table F-1](#) lists the mechanical drawings included in this appendix.

Table F-1. Mechanical Keep-Out Zone Drawing List

Description	Figure
Processor Heatsink Module Topside Keep-Out Zone	Figure F-1
Processor Heatsink Module Mounting Holes Keep-Out Zone	Figure F-2
Processor Heatsink Module Backplate Keep-Out Zone	Figure F-3

Figure F-2. Processor Heatsink Module Mounting Holes Keep-Out Zone

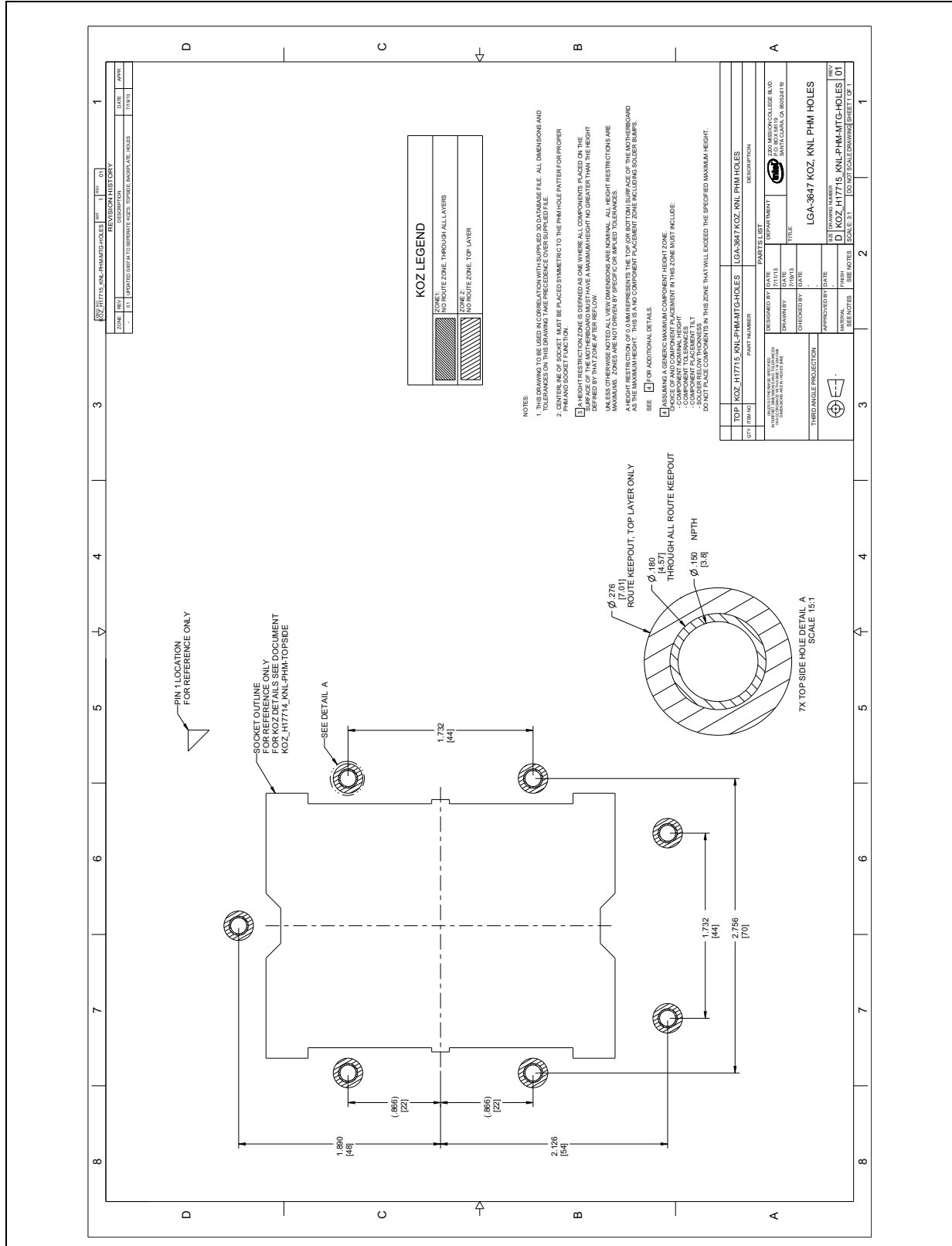


Figure F-3. Processor Heatsink Module Backplate Keep-Out Zone

