Loihi – a brief introduction

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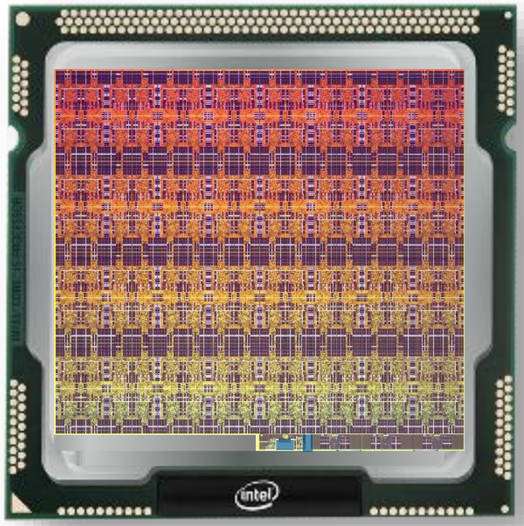
Loihi at a Glance



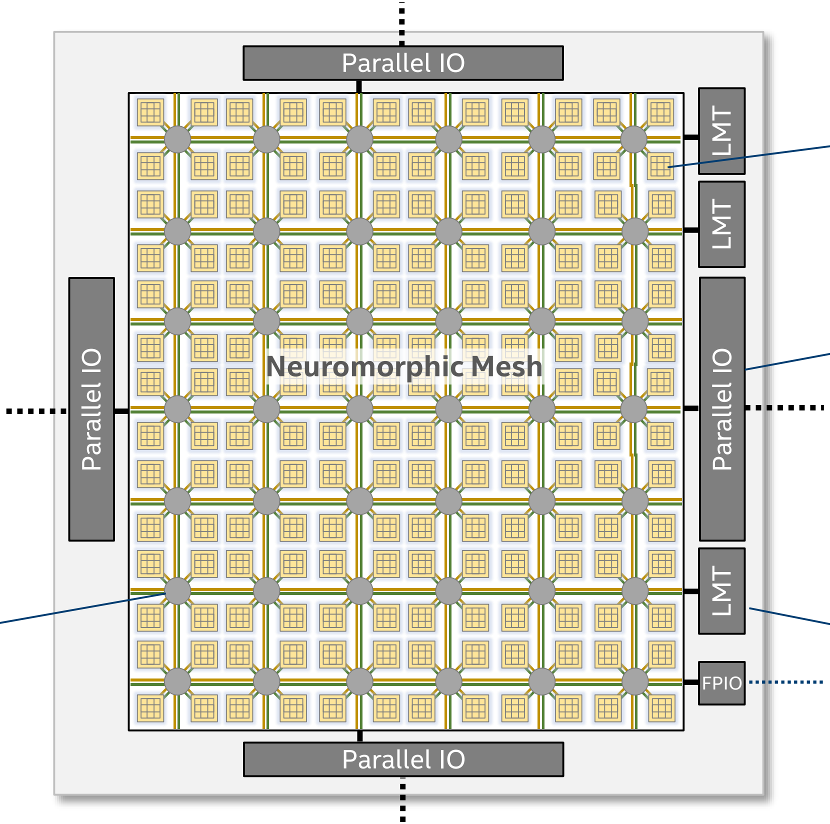
**Integrated
Memory + Compute
Neuromorphic Architecture**

Key Properties

- 128 neuromorphic cores supporting up to 128k neurons and 128M synapses with an **advanced SNN feature set**.
- **Scalable on-chip learning** capabilities to support a range of learning paradigms (unsupervised, supervised, reinforcement-based, and others)
- Supports **highly complex neural network topologies** (up to 2000-way fan-out between neurons)
- Fully digital **asynchronous** implementation
- Fabricated in Intel's **14nm FinFET process** technology

Chip Architecture

Technology:	14nm
Die Area:	64 mm^2
Core area:	0.41 mm^2
NmC cores:	128 cores
x86 cores:	3 LMT cores
Max # neurons:	128K neurons
Max # synapses:	128M synapses
Transistors:	2.07 billion



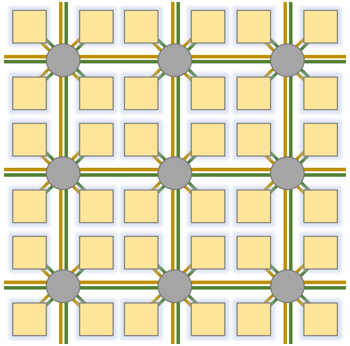
Neuromorphic core
- LIF neuron model
- Programmable learning
- 128 KB synaptic memory
- Up to 1,024 neurons
- Asynchronous design

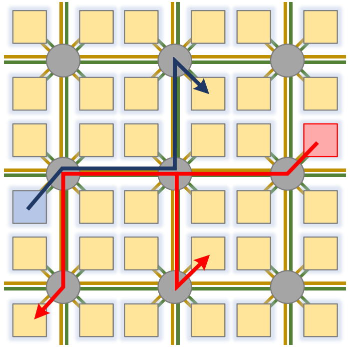
Parallel off-chip interfaces
- Two-phase asynchronous
- Single-ended signaling
- 100-200 MB/s BW

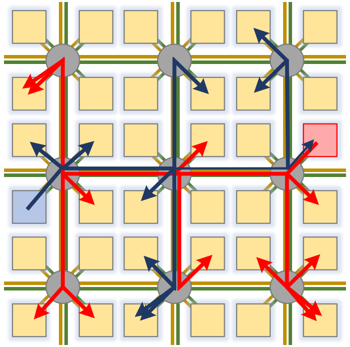
Low-overhead NoC fabric
- 8x16-core 2D mesh
- Scalable to 1000's cores
- Dimension order routed
- Two physical fabrics
- 8 GB/s per hop

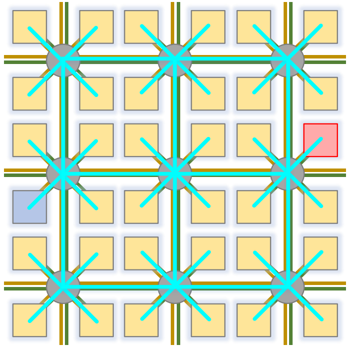
Embedded x86 processors
- Efficient spike-based communication with neuromorphic cores
- Data encoding/decoding
- Network configuration
- Synchronous design

Mesh Operation









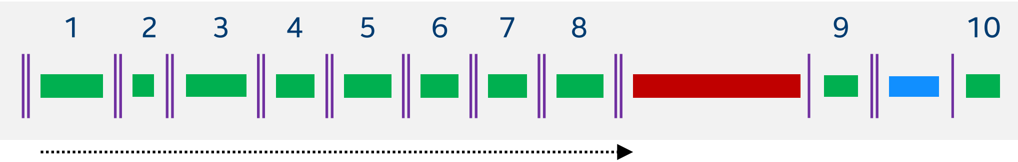
Time step T begins.

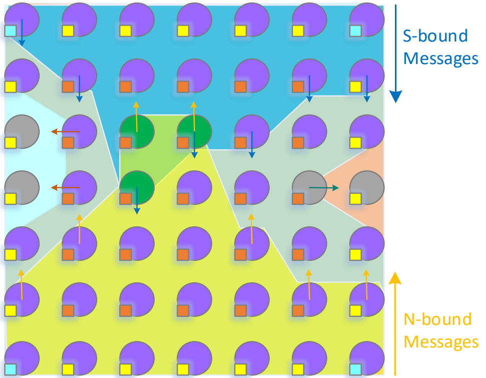
Cores update dynamic neuron state and evaluate firing thresholds

Above-threshold neurons send spike messages to fanout cores

(Two neuron firings shown.)

All neurons that fire in time T route their spike messages to all destination cores.





Neuromorphic Core Architecture

All synaptic connections pooled
128KB shared memory

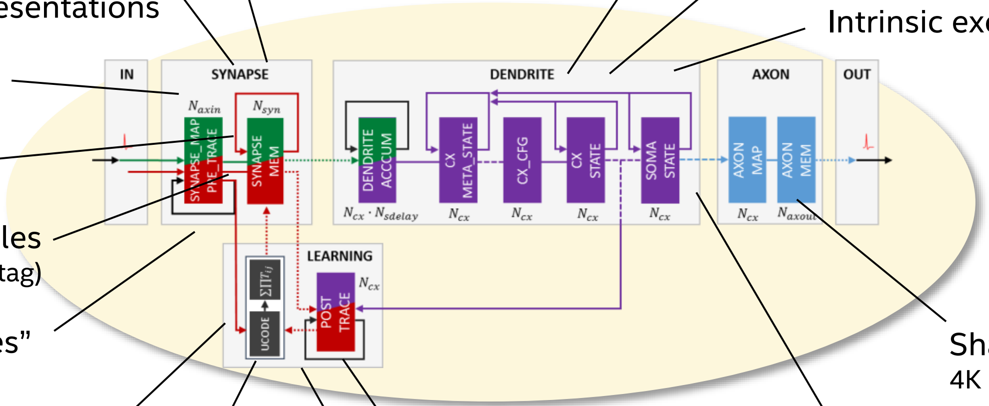
Sparse, *dense*, and *hierarchical*
Synaptic mapping representations

Synaptic delays

Synaptic eligibility traces

Flexible 3-tuple synaptic variables
(1-9b weight, 0-6b delay, 0-8b tag)

Graded “reward spikes”



Discrete time LIF neuron model (CUBA)

Multi-compartment dendritic trees
up to 1K compartments

Intrinsic excitability homeostasis

Shared output routing table
4K axon routes

Axon delays

Refractory delays (+ random)

Flexible synaptic plasticity with microcode-programmable rules

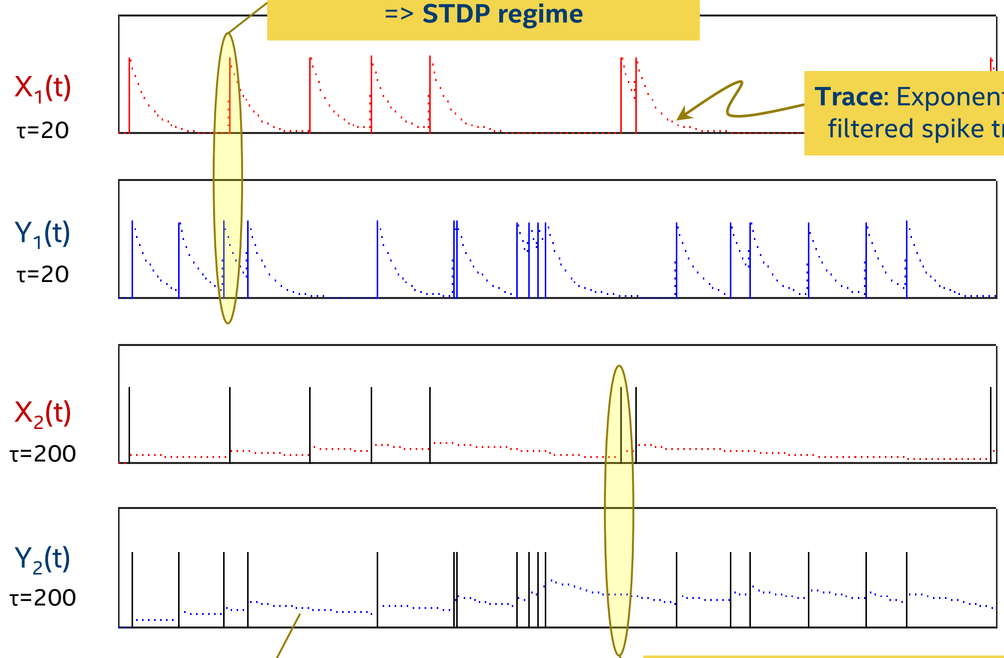
Sum-of-products rule semantics

Filtered spike train traces

Plasticity rules target any synaptic variable

Trace-Based Programmable Learning Rules

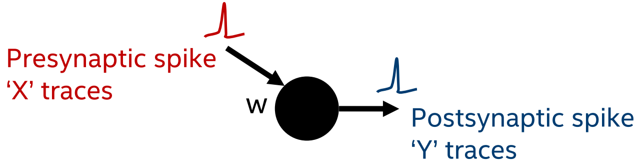
Short time scale trace correlations
=> **STDP regime**



Trace: Exponentially filtered spike train

Traces are **low precision** (7-9b) and may decay **stochastically** for implementation efficiency

Long time scale traces respond to correlations in activity rates



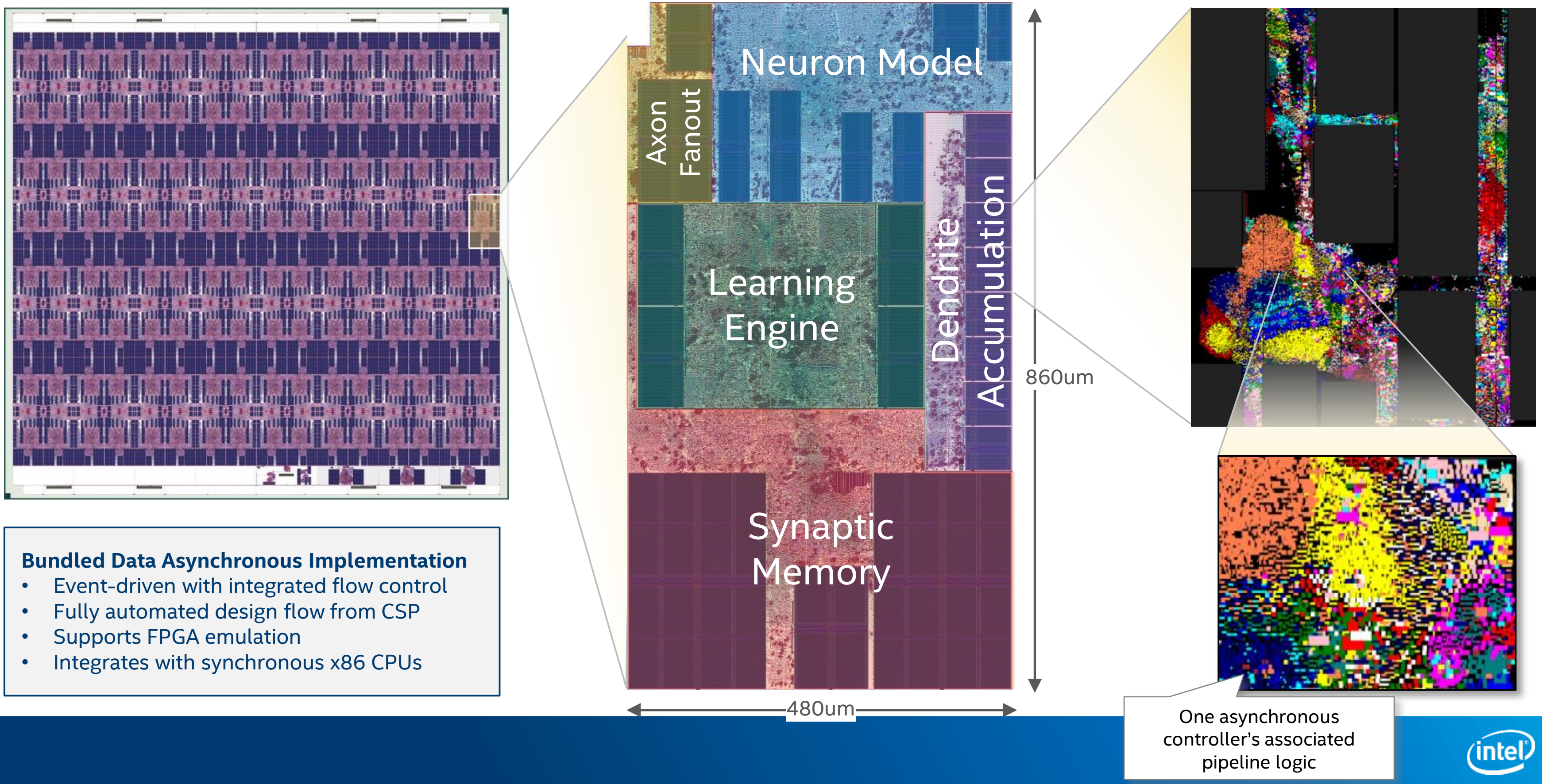
Weight, Delay, and Tag learning rules programmed as **sum-of-product equations**

$$w' = w + \sum_{i=1}^{N_P} S_i \prod_{j=1}^{n_i} (V_{i,j} + C_{i,j})$$

Synaptic Variables
Wgt, Delay, Tag
(variable precision)

Variable Dependencies
X_0, Y_0, X_1, Y_1, X_2, Y_2,
Wgt, Delay, Tag, etc.

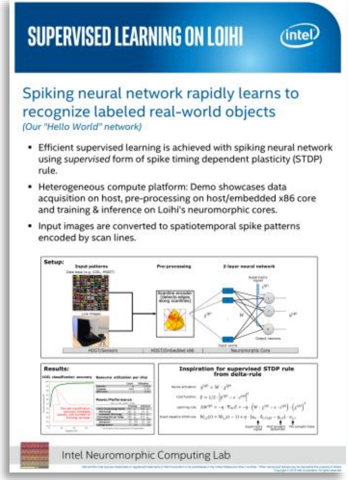
Physical Implementation

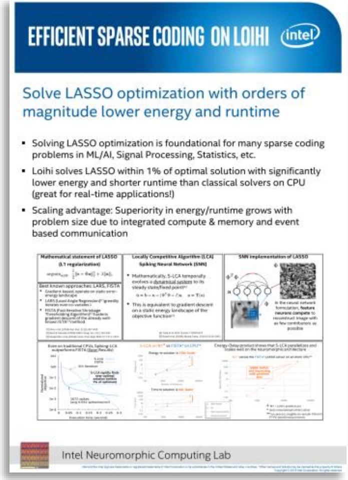


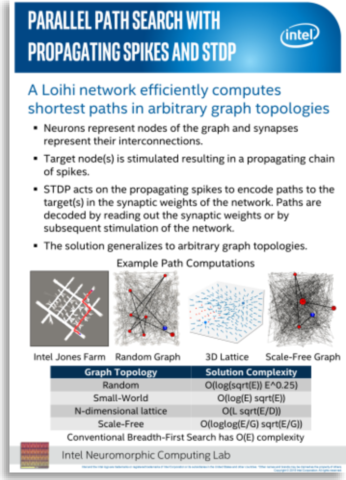
Bundled Data Asynchronous Implementation

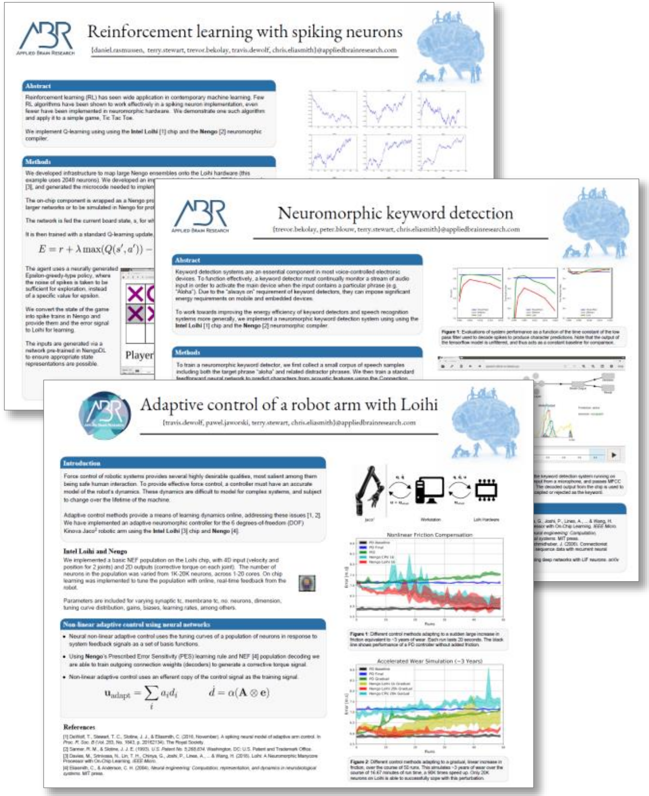
- Event-driven with integrated flow control
- Fully automated design flow from CSP
- Supports FPGA emulation
- Integrates with synchronous x86 CPUs

Application Results









More to come – Thursday morning
Also see our posters and demos for more

M. Davies *et al*., “Loihi: A Neuromorphic Manycore Processor with On-Chip Learning,” in *IEEE Micro*, vol. 38, no. 1, pp. 82-99, January/February 2018

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