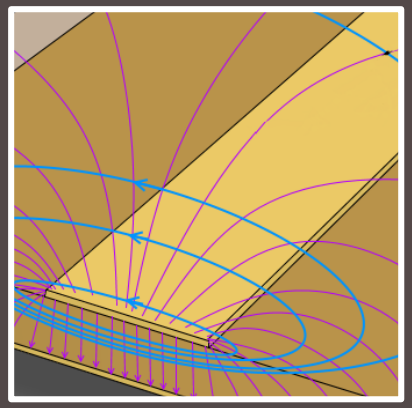
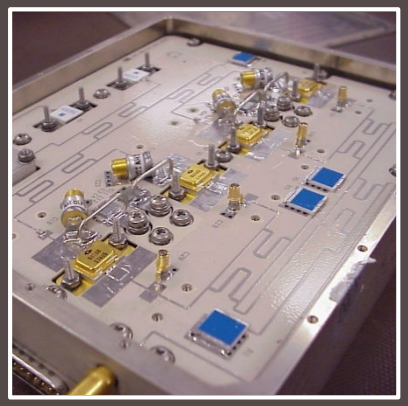


Analog, RF and EMC Considerations in Printed Wiring Board (PWB) Design



James Colotti
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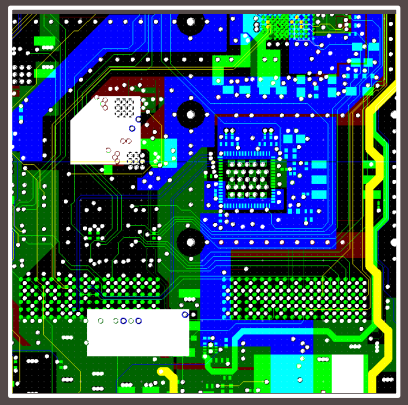
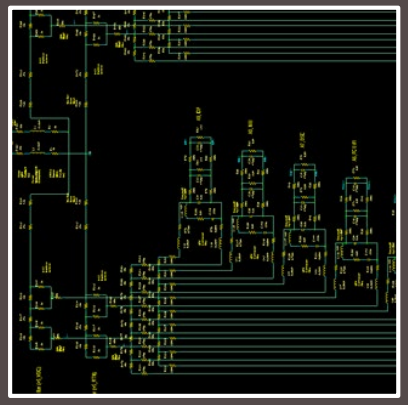
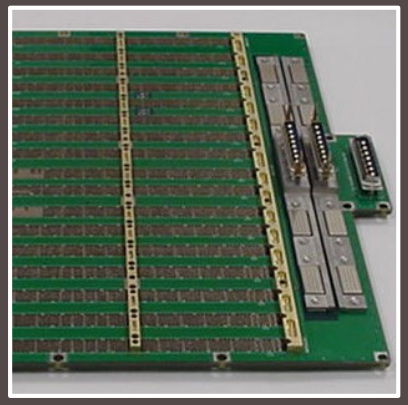


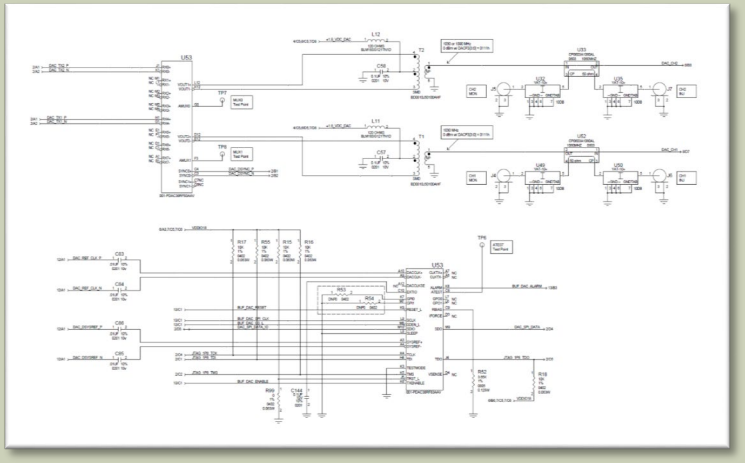




Introduction

Overview

- Printed Wiring Board (PWB)
  - Also known as Printed Circuit Board (PCB)
  - Provides a means of interconnecting various electronic components
  - Provides a mounting platform for these components
  - In some cases, provides a path for thermal management
- When designing electronic circuits, physical properties of the PWB interconnects are often put aside
  - Series Inductance
  - Shunt Capacitance
  - Propagation Delay and Dispersion
  - Dielectric Loss & Resistivity
  - DC Resistance and I^2R Losses
  - Skin Depth
  - Voltage Breakdown
  - Coupling



PWB Focus Areas for Various Circuit Types

- As technology migrates to extremes, PWB characteristics must be taken into account

Circuit Types	Potential Focus Areas
High Speed Digital or Fast t_r and t_f Digital	Dielectric constant and loss, resistive loss, dispersion, impedance matching, propagation delay
RF	Dielectric constant and loss, resistive loss, dispersion, impedance matching
High Current	Resistance (I^2R losses and regulation), thermal management
High Voltage	Dielectric breakdown, clearances, creepage distances, trace geometries (to reduce HV gradients), partial discharge (voids)
Critical Analog	Trace/pad inductance, capacitance
High Impedance	Dielectric resistivity, coupling

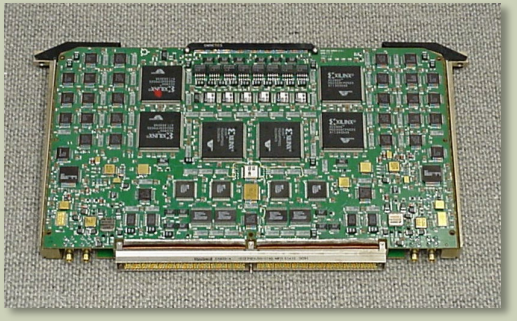
Other Considerations

- Low Size Weight & Power (SWaP) Footprints (e.g. avionics, consumer electronics)
- Electromagnetic Environment of the Circuit Card Assembly (CCA)
- Escape routing on high I/O count, fine pitch packages (e.g. 1.0 mm, 0.8 mm and 0.5 mm BGAs)
- PWB design often involves collaboration among multiple disciplines
  - Electrical
  - Mechanical/Thermal
  - Manufacturing
  - Design/Drafting
  - PWB Supplier
  - Program Management (cost, schedule)

PWB Construction

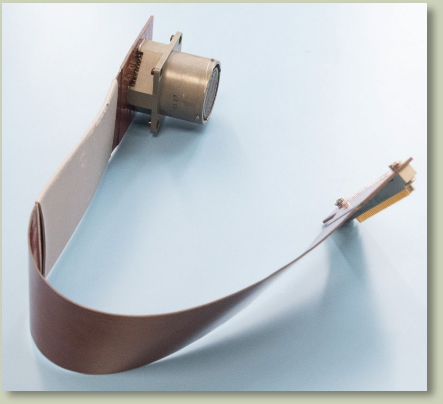
Wide variety of construction options.

PWB/CCA Examples

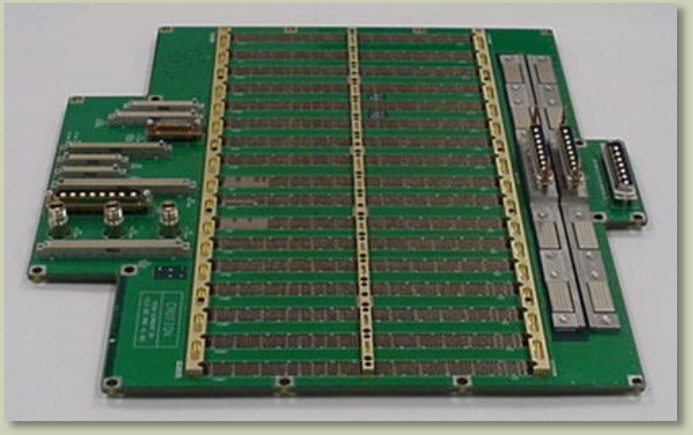


Aramid/Polyimide,
10 Layer
Dual Digitizer/Demodulator

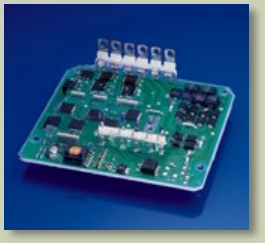
Flex, 4 Layer
Signal Distribution



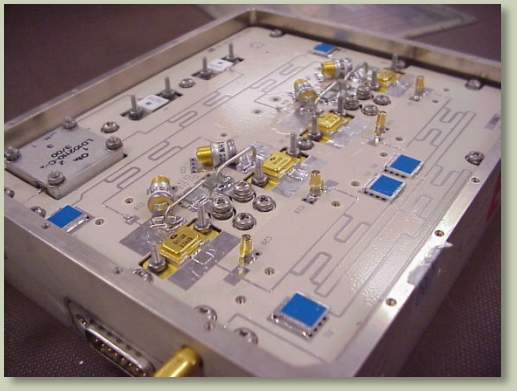
FR-4 Laminate, 24 Layer
Radar Signal Processor Backplane



High Thermal Conductivity
Laminate, 4 Layer
Servo Amplifier



Metal Core, RT/duroid
6010LM, 2 Layer
RF Power Amplifier



Types of Rigid PWB

- Type 1: Rigid, One Layer
- Type 2: Rigid, Two Layer
- Type 3: Rigid, Multi Layer, w/o blind or buried vias
- Type 4: Rigid, Multi Layer, w/ blind and/or buried vias
- Type 5: Rigid, Metal Core, w/o blind or buried vias
- Type 6: Rigid, Metal Core, w/ blind and/or buried vias

(Per IPC-2222 standard, section 1.6.1)

Types of Flex PWB

- Type 1: Flex, One Layer
- Type 2: Flex, Two Layer
- Type 3: Flex, Multi Layer
- Type 4: Multilayer rigid and flexible material combinations containing three or more conductive layers with plated-through holes
- Type 5: Flex or rigid-flex containing two or more conductive layers without plated-through holes

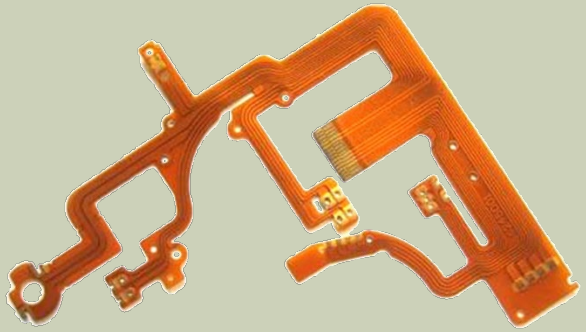
(Per IPC-2223 Standard, section 1.2.1)

Footnotes on Flex PWBs

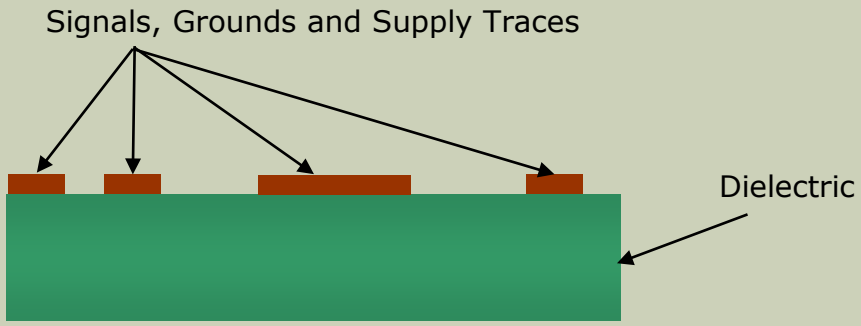
- Used as alternative to a wiring harness
- Many similarities to rigid PWBs
- Typically higher development cost than harness
- Typically cheaper than harness in production
- Improved repeatability
- Typically much less real estate needed

Wire Harness Example

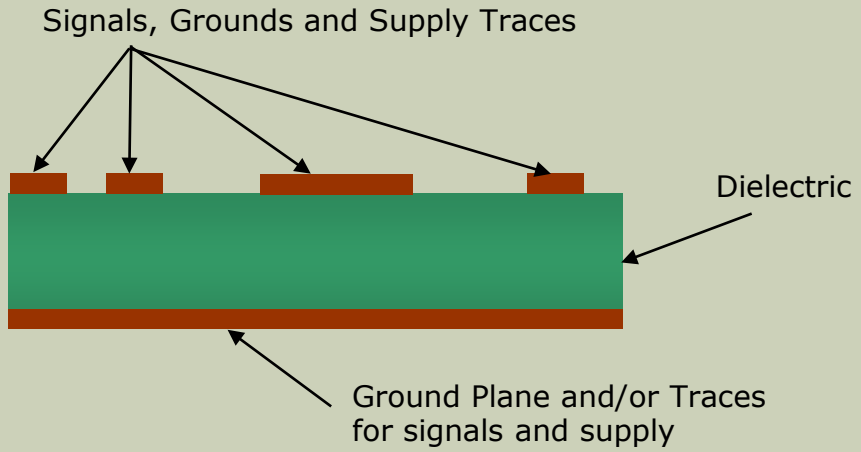
Flex PWB Example



PWB Stack-Ups (1 and 2 Layer)



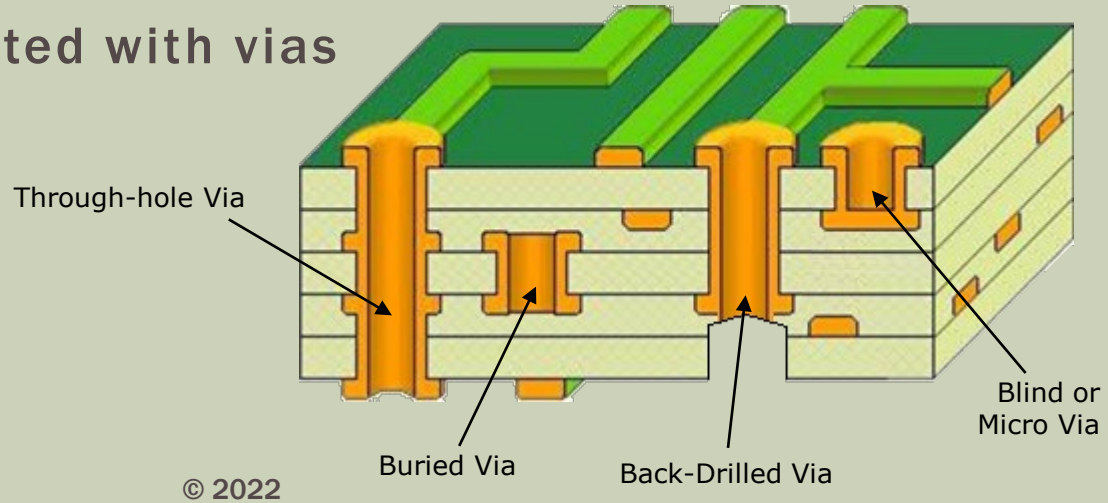
- One Sided
  - Least expensive (assuming no plated through holes)
  - Applicable to straightforward circuits
  - Difficult to control EMI without external shielding
  - Difficult to control impedance



- Two Sided
  - Inexpensive
  - Applicable to more complex circuits
  - EMI can be mitigated by use of a ground plane
  - Impedance control is simplified by use of a ground plane

Multi-Layer PWBs

- More routing resources for signals, power and ground (reference plane)
- Option for dedicating layer(s) to ground
  - Forms reference planes for signals
  - Mitigates EMI Control
  - Simpler impedance control
- Option for dedicating layer(s) to Supply Rail(s)
  - Low ESL/ESR power distribution
- Layers are interconnected with vias
  - Through-hole vias
  - Buried vias
  - Blind vias
  - Micro vias
  - Back-Drilled via



Vias

- Needed to interconnect layers
  - Introduce discontinuities
  - “Choke-off” routing
  - Perforate Ground/Supply Planes
  - Ground vias can aid in signal integrity
- Traditionally implemented with Plated Through Holes (PTHs)
  - Most disruptive as they impact all layers, and are the longest via type
  - Typically not suitable for use under high density components (e.g. 0.8 mm pitch BGAs) because of pad size
- Blind, Buried or Micro Vias
  - Less disruptive as they impact fewer layers
  - Aid in escape routing of high density components (e.g. BGAs)
  - Additional processing cost can be offset by reduction in layers

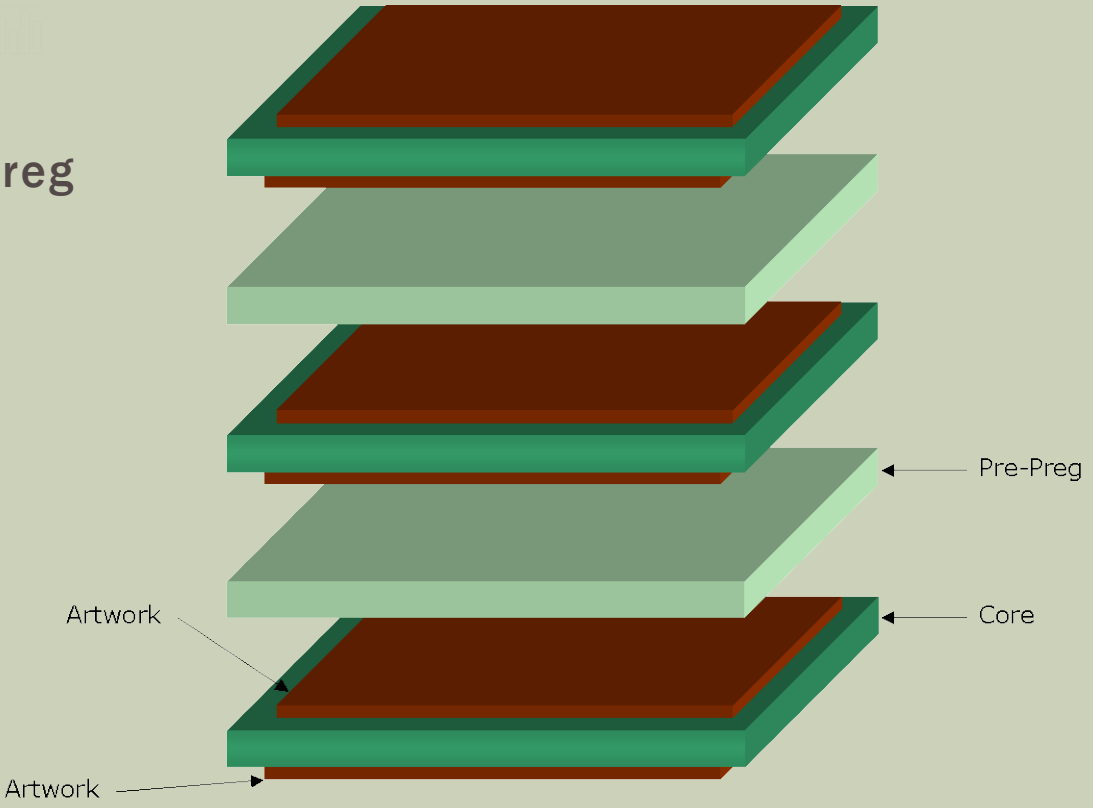
Via Parameters

Via Dia	10			12			15			25		
Pad Dia	22			24			27			37		
Anti-Pad Dia	30			32			35			45		
	R	L	C	R	L	C	R	L	C	R	L	C
Length: 60 Planes: 5	1.55	0.78	0.48	1.25	0.74	0.53	0.97	0.68	0.60	0.57	0.53	0.83
Length: 90 Planes: 7	2.3	1.33	0.66	1.88	1.24	0.69	1.45	1.15	0.78	0.85	0.92	1.08

Notes:
1. R in mΩ , L in nH, C in pF
2. Dimensions are in mils.
3. Planes are evenly spaced.
4. Via inductance can be approximated by: $L = 5.08h\left[ln\left(\frac{4h}{d}\right) - 0.75\right]$ (h and d are in inches, L is in nH)

Exploded View of Multi-Layer PWB

- Core Construction
  - As shown
- Foil Construction
  - Reverse core and pre-preg

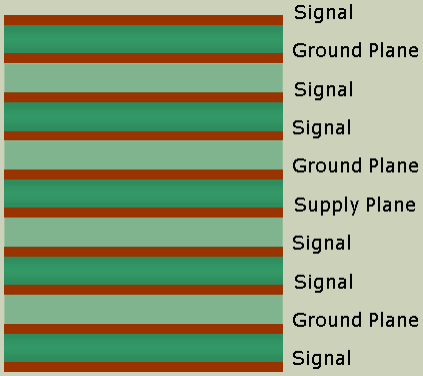


Multi-Layer Stack-Up Examples

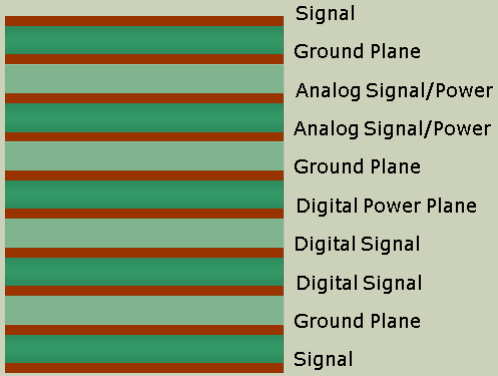
- **PWB Example #1**
  Simple High Speed Digital Application
  - Six Layers
  - Moderate Density
  - Two Microstrip Routing Layers
  - Two Buried Microstrip Routing Layers
  - Single Supply Plane

Note: For all examples, consider ground and power pours on all unused areas, especially on outer layers as density and vias allow.

- **PWB Example #2**
  Moderate High Speed Digital Application
  - Ten Layers
  - High Density
  - Two Microstrip Routing Layers
  - Four Asymmetrical Stripline Routing Layers
  - Single Supply Plane



- **PWB Example #3**
  Mixed Analog/RF/Digital Application
  - Ten Layers
  - Moderate Density
  - Two Microstrip Routing Layers
  - Four Asymmetrical Stripline Routing Layers
  - Single Digital Supply Plane
  - Analog supplies on inner layers



PWB Stack-Up Guidelines

- Maximize symmetry to simply manufacturing and to mitigate warping
- Even number of layers preferred by PWB manufacturers
- Asymmetrical stripline has higher routing efficiency than symmetrical stripline
- Supply planes can be used as reference planes for controlled Z (but not preferred for analog or RF)
- Ideally, supply planes should be run adjacent to ground planes with a thin dialectic separation
- Signals on adjacent layers should be run orthogonally
  - Minimizes coupling between lines

PWB Materials

Wide variety of options available for laminates, conductor thickness, finish and conductor material.

PWB Material and Metal Options

- Dozens of dielectric material suppliers to chose from:
  - Arlon
  - Bergquist
  - Isola
  - Panasonic
  - Park Nelco
  - Rogers
  - Taconic
  - Numerous others
- Several standard dielectric thickness options
- Metal Options
  - Virtually all PWBs use copper as the conductor material but other materials (such as aluminum) can also be used
  - Wide variety of copper thickness options available
- Two copper plating options
  - Rolled
  - Electro-Deposited (multiple variants)

Electrical Considerations in Selecting Dielectric (Laminate) Material

- Permittivity
  - Typically expressed relative to free space (ε_r)
  - The more stable, the better
  - Lower values may be more suitable for high layer counts
  - Higher values may be more suitable for some RF structures
- Loss
  - Typically expressed as loss tangent (tanδ)
  - The lower, the better
  - Becomes more of an issue at higher frequencies
- Moisture Absorption
  - The lower, the better
  - Can effect dielectric constant and loss tangent
  - Can be mitigated with conformal coating
- Voltage Breakdown
  - The higher, the better
  - Typically not an issue, except in high voltage applications
- Resistivity
  - Typically expressed in MΩ for surface resistivity and MΩ-cm for volume resistivity
  - The higher, the better
  - Typically not an issue, except in low leakage, high impedance and/or HV applications

Mechanical Considerations in Selecting Dielectric (Laminate) Material

- Peel Strength
  - The higher, the better
- Flammability Rating
  - UL Standards
- Glass Transition Temperature (Tg)
- Thermal Conductivity
  - Typically PWB material is considered a thermal insulator
  - Some laminates are available with enhanced thermal conductivity
  - Planes & vias contribute to thermal conductivity
- Coefficient of Expansion
  - XY matching to components, solder joint stress (LCC)
  - Z axis expansion, via stress
- Weight (density)
- Flexibility
  - Very low Flexural Modulus materials might require extensive support to prevent component damage
  - Very low Flexural Modulus materials might require extensive support to prevent PWB damage (cracking)

PWB Material Examples

Material	Dielectric Constant (ε_r)	Loss Tangent ($\tan\delta$)	Notes
FR-4, Woven Glass/Epoxy	4.7 (1 MHz) 4.3 (1 GHz)	0.030 (1 MHz) 0.020 (1 GHz)	Inexpensive, available, unstable ε_r, high loss
N7000-1 Polyimide Park-Nelco	3.9 (2.5 GHz) 3.8 (10 GHz)	0.015 (2.5 GHz) 0.016 (10 GHz)	High T_g (260 °C)
CLTE Arlon	2.94 (10 GHz)	0.0025 (10 GHz)	Stable ε_r, low loss
RT6010LM Rogers	10.2 (10 GHz)	0.002 (10 GHz)	High ε_r, high loss
RO4350B Rogers	3.48 (10 GHz)	0.004 (10 GHz)	Stable ε_r, low loss, processing is similar to FR4
RT6002 Rogers	2.94 (10 GHz)	0.0012 (10 GHz)	Stable and accurate ε_r, low loss

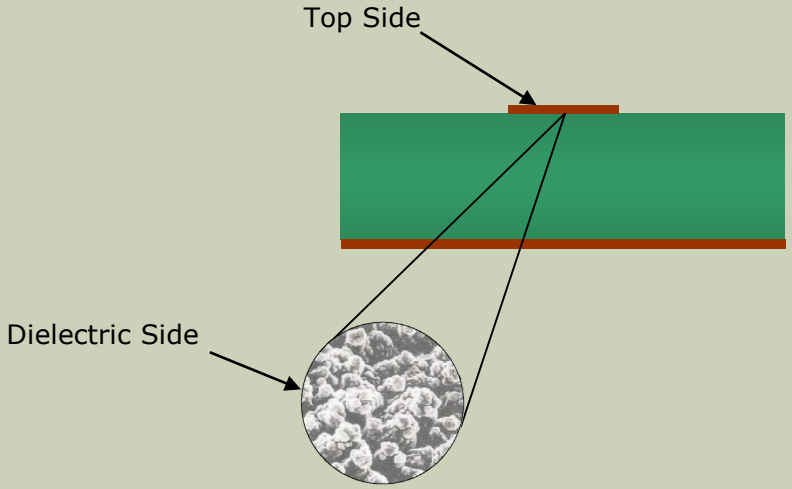
Dielectric, Common Thickness

- Core Material (depending on material type)
  - 0.002, 0.003, 0.004, 0.005, 0.006, 0.007, 0.008, 0.009”
  - 0.010, 0.012, 0.014, 0.015, 0.018, 0.020, 0.031”
  - Typically RF laminates have fewer thickness options
  - Some laminates (e.g. FR-4) are available in 0.5 mil increments
- Pre-Preg (depending on material type)
  - 0.002, 0.003, 0.004, 0.005, 0.008”
  - Pre-preg can be stacked to some extent for thicker layers
- Use standard thickness in designing stack-up
- Work with anticipated PWB vendor(s) when designing stack-up and selecting material especially on complex PWB designs

Copper Options

Common Thickness Options

Weight	Thickness
0.25 oz	0.4 mil (9 μm)
0.5 oz	0.7 mil (18 μm)
1.0 oz	1.4 mil (35 μm)
2.0 oz	2.8 mil (70 μm)

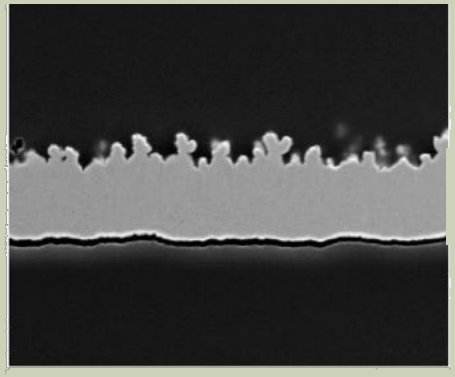


Plating Options

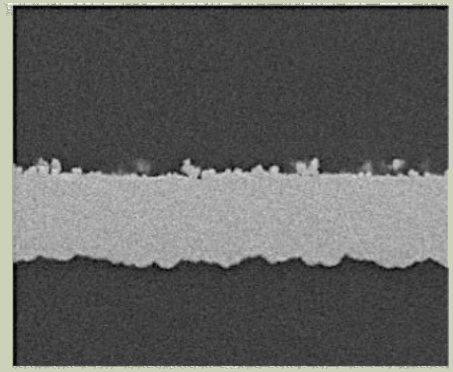
Option	Top Side Surface Roughness	Dielectric Side Surface Roughness	Notes
Rolled	0.3 μm (12 μ")	0.4 μm (16 μ")	Typically lower loss at high frequency (>1 GHz) than ED variants. This option is typically available on Teflon based laminates. Useful in flex circuits.
Electro Deposited	0.4-2.0 μm (16-79 μ")	0.5-3.5 μm (20-138 μ")	In general, ED is less prone to pealing. Roughness depends on copper thickness and specific type of ED process (Standard, Reverse Treated, VLP, HVLP).

Surface Roughness for Various Finishes

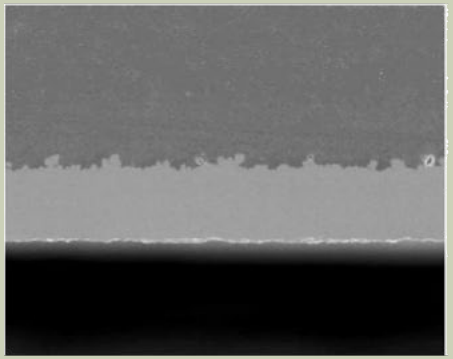
- All foils below are 18 µm (0.7 mils or 0.5 oz)



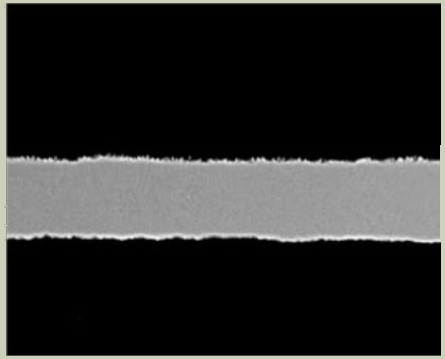
Standard
Electro Deposited



RTF
Electro Deposited



VLP
Electro Deposited



VLP-2
Electro Deposited

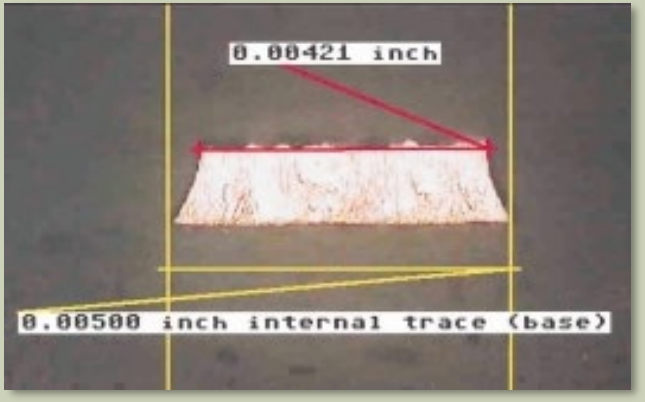
Courtesy TTM

Considerations in Selecting Copper Thickness & Plating

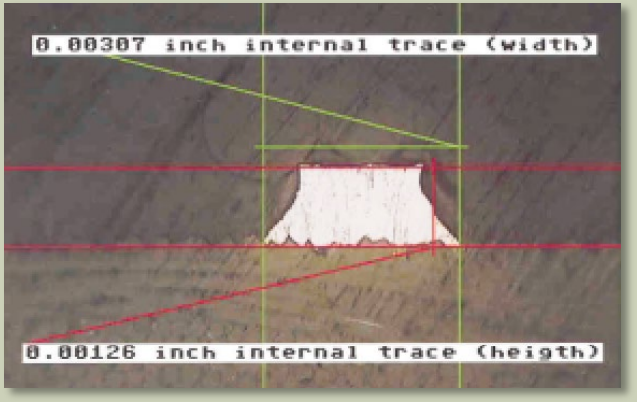
- Power
  - Current capacity
  - Temperature rise (due to i^2R heating)
  - Trace failure due to short
  - Voltage drop (supply voltage regulation)
- Signal Loss
  - Thicker/wider lines reduce resistive loss
  - Higher surface roughness increases loss (>1 GHz)
- Etch Factor

Etch Factor Geometry

- Actual trace shape is trapezoidal
- Thinner copper produces more precise geometries with narrow line widths
- For traces >5 mils, 1 oz or thinner is acceptable
- For traces <5 mils, 0.5 oz or thinner copper should be used
- Guidelines are fabricator and application dependent



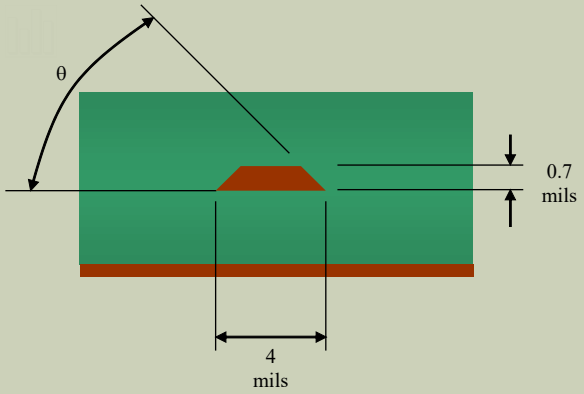
0.005” Trace on 1 oz Copper



0.003” Trace on 1 oz Copper

Etch Factor Effects

- Critical in some RF applications
  - Directional Couplers, Interdigital Filters
- Critical in some narrow line width geometries
  - Significantly effects current capacity of trace
  - Significantly effects trace resistance and loss
- In many applications, effects on Z_0, L, C can be ignored (Buried Microstrip Example)

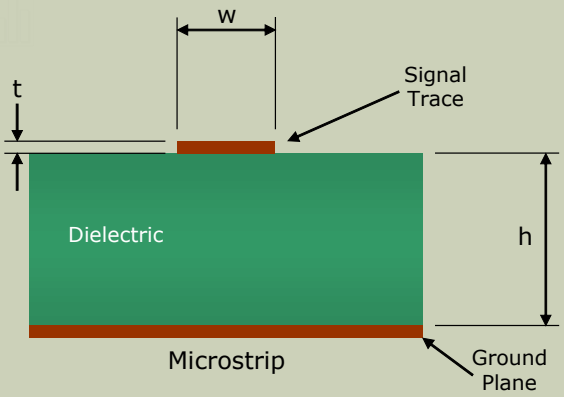


θ (°)	L (nH/in)	C (pF/in)	Z_0 (Ω)
90	8.5	3.4	50.0
79	8.6	3.3	50.7
72	8.6	3.3	51.0
60	8.7	3.3	51.5
45	8.8	3.2	52.2

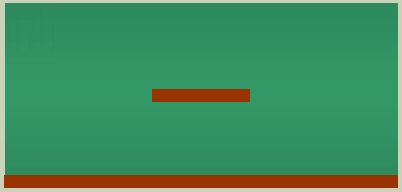
Signal Distribution and Signal Integrity (SI)

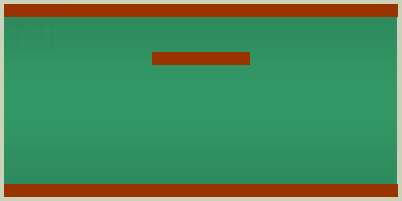
SI is a set of measures to ensure the quality of an electrical signal.

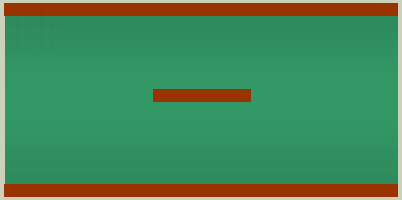
Single Ended Structure Examples



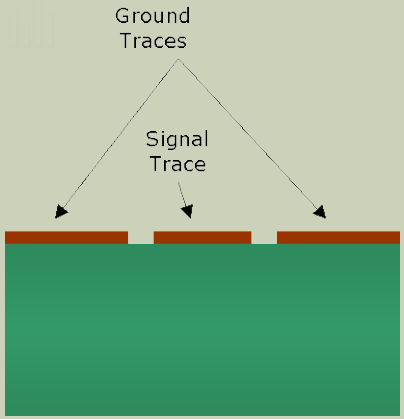
Microstrip


Buried Microstrip


Asymmetrical Stripline

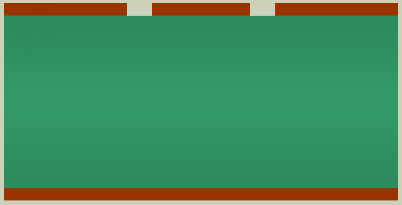

Symmetrical Stripline

Single Ended Structure Examples (continued)

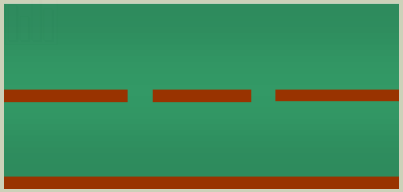


Surface Coplanar Waveguide

Embedded Coplanar
Waveguide



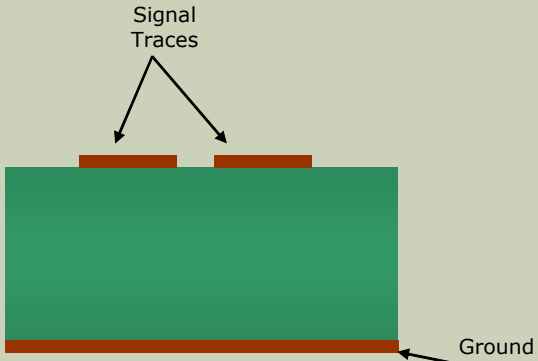
Surface Coplanar Waveguide
with Ground Plane



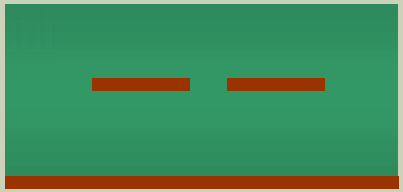
Embedded Coplanar
Waveguide with Ground Plane

Differential Structure Examples

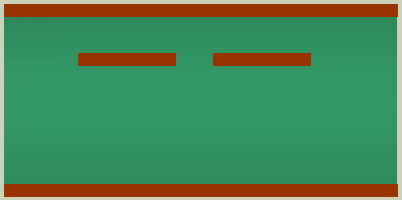
Edge Coupled



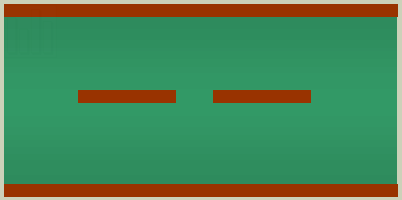
Edge-Coupled Microstrip



Edge-Coupled Imbedded Microstrip



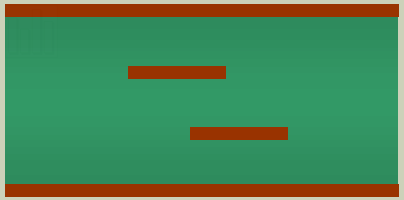
Edge-Coupled Asymmetrical Stripline



Edge-Coupled Symmetrical Stripline

Broadside Coupled

Broadside-Coupled Stripline



Offset Broadside-Coupled Stripline

Trace Parameters

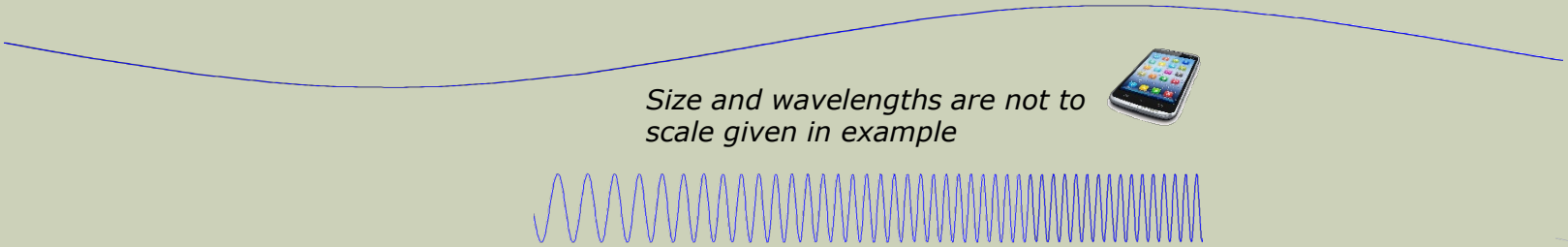
	10 mil trace	20 mil trace	100 mil trace
Capacitance	2.2 pF/in	3.3pF/in	11.6pF/in
Inductance	9.9 nH/in	7.2 nH/in	2.4 nH/in

Notes:
1. Trace is 1 oz electrodeposited copper, microstrip.
2. FR-4 dielectric, ε_r = 4.5, h = 10 mils.

When are traces consider transmission lines and when are they considered lumped elements?

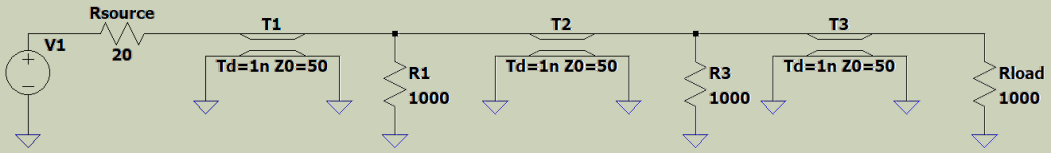
PWB Traces: Transmission Lines or Lumped Elements? (Frequency Domain Viewpoint)

- At low frequencies, traces are treated as lumped elements
  - Signal voltages are essentially at the same potential at any point on the PWB
  - e.g. 6x12 cm cell phone, wavelength of 20 kHz audio is 15 km
- High frequencies, traces are treated as transmission lines
  - Signal wavelength is close to (or smaller than) the physical PWB size
  - Signal voltage is no longer uniform across PWB
  - PWB traces must be viewed as transmission lines
  - e.g. 6x12 cm cell phone, wavelength of 28 GHz 5G carrier is 11 mm

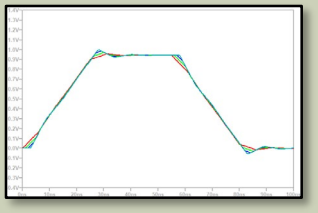


PWB Traces: Transmission Lines or Lumped Elements? (Time Domain Viewpoint)

- When rise and fall times (t_r and t_f) are slow, traces and pads are treated as lumped elements
  - t_r and t_f >> $2t_d$ (t_d is the delay time from source to end of line)
  - Reflected waves are "lost" in the rising and falling edges
  - Impedance matching may be less critical for signal integrity
- Fast rise and fall times, traces are treated as transmission lines
  - t_r and t_f << $2t_d$
  - Impedance matching is more critical for signal integrity
- Example
  - Three cascaded traces, each 1 ns delay ($2t_d$=6 ns)
  - High Z load taps
  - Plots show waveforms at each tap



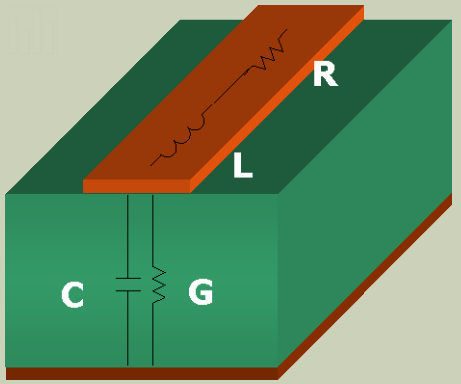
Fast rise and fall times (t_r and t_f = 0.1 ns)



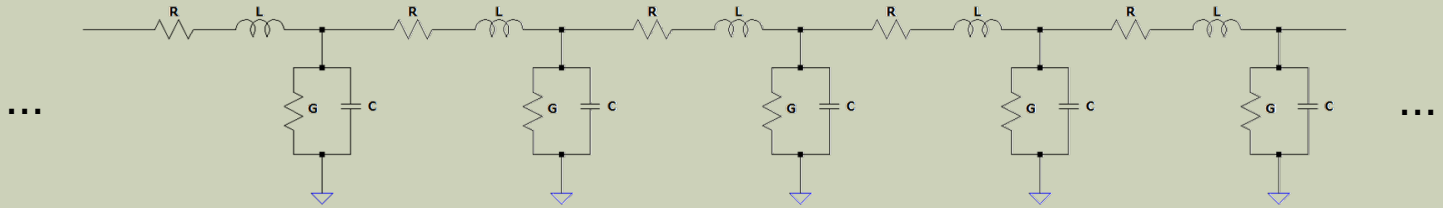
Slow rise and fall times (t_r and t_f = 25 ns)

PWB Traces as Transmission Lines

- PWB trace transmission line model
  - Dielectric Loss (G) per unit length
  - Trace Copper Loss (R) per unit length
  - Trace series inductance (L) per unit length
  - Trace capacitance (C) per unit length



- Schematic representation



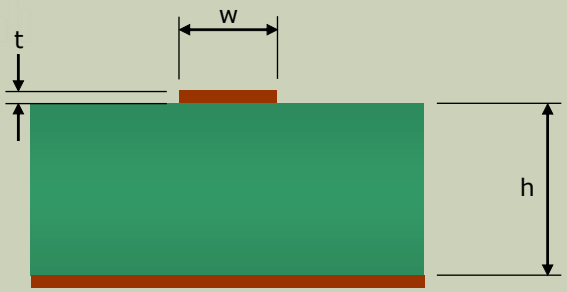
- Characteristic Impedance

$$Z_0 = \sqrt{\frac{R+j\omega L}{G+j\omega C}} \quad or\ when\ R \rightarrow 0\ and\ G \rightarrow 0 \quad Z_0 = \sqrt{\frac{L}{C}}$$

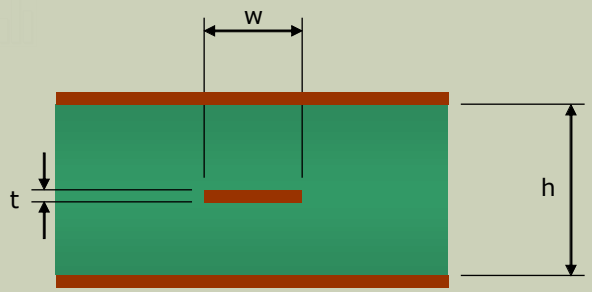
Trace Impedance

- Impedance Determined By
  - Topology (Stripline, Microstrip, Coplanar Waveguide, etc.)
  - Dielectric constant of PWB material (ε_r)
  - Dielectric height (h)
  - Conductor width (w)
  - To a small extend, conductor thickness (t)
- Impedance Control Considerations
  - Delivering max power to load
  - Maintaining signal integrity
  - Prevent excessive driver loading

Stripline & Microstrip Impedance



Micro-Strip



Strip-Line

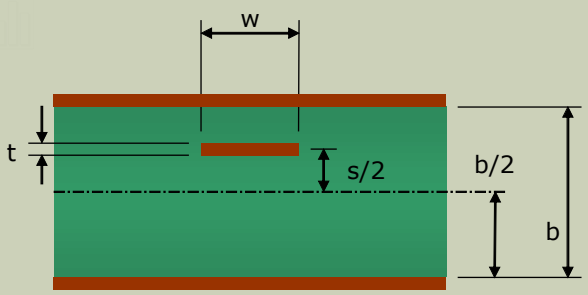
$$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right)$$

when $0.1 < \frac{w}{h} < 2.0$ and $1 < \varepsilon_r < 15$

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln\left(\frac{1.9b}{0.8w + t}\right)$$

when $\frac{w}{h} < 0.35$ and $\frac{t}{h} < 0.25$

Asymmetrical Stripline Impedance



Asymmetrical Strip-Line

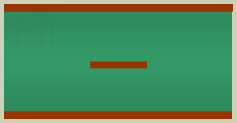
$$Z_0 = \frac{\sqrt{\frac{\mu_0}{\varepsilon_0}}}{2\pi\sqrt{\varepsilon_r}} \cosh^{-1}\left[\sin\left(\frac{\pi(b-s)}{2b}\right)\coth\left(\frac{\pi d_0}{2b}\right)\right]$$

$$d_0 = w\left(0.5008 + 1.0235\left(\frac{t}{w}\right) - 1.0230\left(\frac{t}{w}\right)^2 + 1.1564\left(\frac{t}{w}\right)^3 - 0.4749\left(\frac{t}{w}\right)^4\right)$$

$$\text{when } \frac{w}{b-t} < 0.35$$

Impedance Examples

- Symmetrical Stripline
  50 Ω, 11 mils wide
  (15+15=30 mil dielectric)



- Asymmetrical Stripline
  50 Ω, 9 mils wide
  (10+20=30 mil dielectric)

- Microstrip
  50 Ω Microstrip, 54 mils wide
  (30 mil dielectric)

Notes:

1. Copper: 1 oz, electro-deposited
2. FR4 dielectric constant: 4.50

AC Loss

- AC loss due to three mechanisms
  - Dielectric Loss (loss tangent of PWB material)
  - Conductor Loss (resistive, skin effect, roughness)
  - Radiation Loss (typically negligible portion of loss)
- Loss can be a concern in digital applications
  - High speed
  - Long trace runs
  - and/or fine width lines
- Loss can be a concern in analog/RF applications
  - Gain/loss budgets in RF and IF paths
  - LO distribution loss
  - Video, ADC or DAC scaling

Dielectric and Copper Loss Examples

	FR4			Rogers RO4350B		
Frequency	**Copper Loss**	**Dielectric Loss**	**Total Loss**	**Copper Loss**	**Dielectric Loss**	**Total Loss**
10 MHz	0.005	0.001	0.006	0.005	0.000	0.005
100 MHz	0.017	0.012	0.029	0.017	0.002	0.019
1 GHz	0.068	0.123	0.191	0.070	0.016	0.086
10 GHz	0.309	1.227	1.536	0.322	0.160	0.482

FR4 dielectric loss exceeds copper loss at 1 GHz

The fundamental of a 10 GHz clock will be attenuated by >6 dB over a 4" trace length

Notes:

1. Copper: 1 oz, electrodeposited, 10 mil width, 50 Ohms, stripline
2. FR4 dielectric constant: 4.50, loss tangent 0.025, height 28 mils
3. 4350 dielectric constant: 3.48, loss tangent 0.0037, height 22 mils
4. Loss units are dB/inch

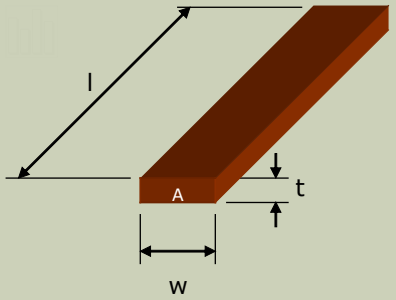
Conductor Loss

- DC Resistance
  - Function of conductivity, length and cross sectional area

$$R_{DC} = \rho\frac{l}{tw} = \rho\frac{l}{A}$$

$$R_{DC} = 0.679\mu\Omega - in\frac{12in}{(0.0014in)(0.010in)} = 0.6\Omega$$

$$R_{DC} = 0.679\mu\Omega - in\frac{12in}{(0.0007in)(0.005in)} = 2.3\Omega$$

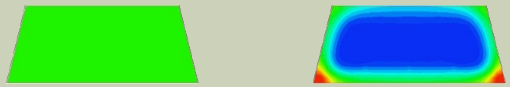


- Skin Depth
  - Function of frequency, conductivity & permeability (copper permeability $\mu_r \approx 1$)
  - Effects AC resistance
  - Defined as point where current density drops to 37% (1/e)
  - Typically can be ignored if t<2δ

$$\delta = \sqrt{\frac{\rho}{\pi f \mu_0 \mu_r}}$$

$$\delta = \sqrt{\frac{0.0172\mu\Omega m}{\pi(10MHz)\left(4\pi x10^{-7}\frac{\Omega s}{m}\right)}} = 21\mu m = 0.8mils$$

$$\delta = \sqrt{\frac{0.0172\mu\Omega m}{\pi(10GHz)\left(4\pi x10^{-7}\frac{\Omega s}{m}\right)}} = 660nm = 0.03mils$$

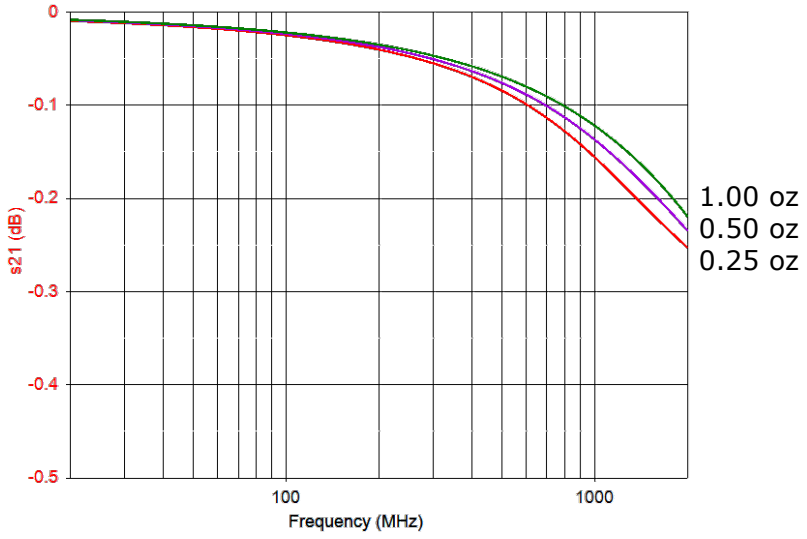


Current Density Distribution at DC

Current Density Distribution at High Freq

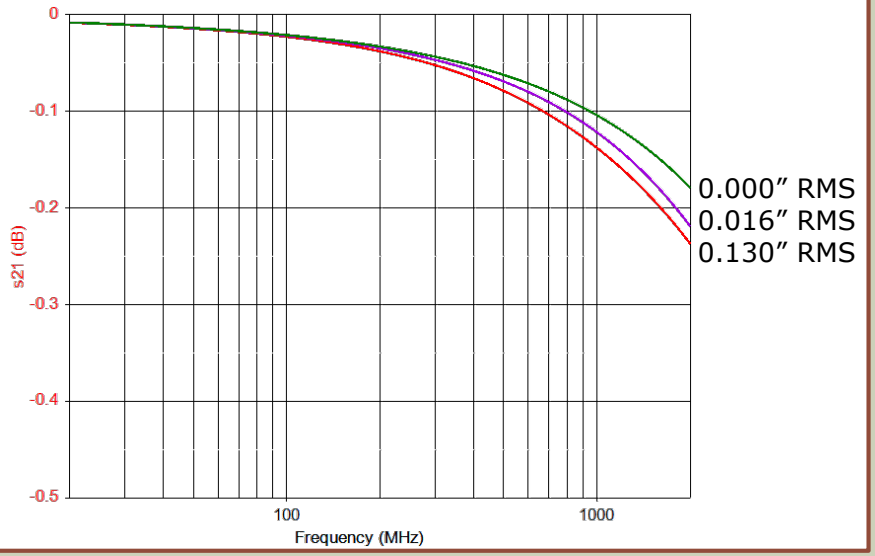
Loss due to Skin Effect & Roughness

Loss per Inch Over Frequency for Various Copper Thickness Values



Stripline
ε_r= 4.6
δ=0.011
h=30 mils
w=10.5 mils
R=0.055″ RMS

Loss per Inch Over Frequency for Various Copper Roughness Values



Stripline
ε_r= 4.6
δ=0.011
h=30 mils
w=10.5 mils
t=1.4 mils

Time Delay

$$t_d = \sqrt{L_0 C_0} = \frac{\sqrt{\varepsilon_{r-effective}}}{c} = 85\sqrt{\varepsilon_{r-effective}} \text{ ps/inch}$$

Where:

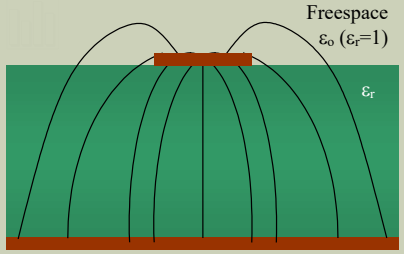
t_d: time delay per unit length

$\varepsilon_{r\text{-effective}}$: Effective Relative Dielectric constant

c: Speed of Light

L_o: Inductance per unit length

C_o: Capacitance per unit length



Microstrip

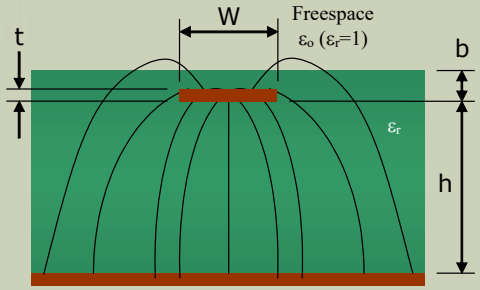
$$\varepsilon_{r-effective} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\frac{1}{\sqrt{1 + \frac{12h}{w}}}\right]$$

when $\frac{w}{h} \geq 1$

FR4 Example

ε_r= 4.5, w = 18 mils, h = 10 mils

t_d = 112 ps/inch

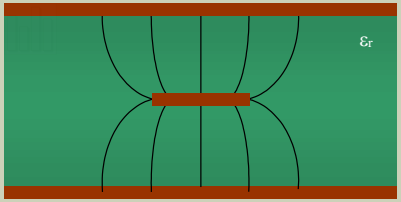


Buried Microstrip

$\varepsilon_{r\text{-effective(microstrip)}} <$

$\varepsilon_{r\text{-effective(buried microstrip)}}$

$< \varepsilon_r$



Stripline

$\varepsilon_{r\text{-effective(stripline)}} = \varepsilon_r$

$$t_d = 85\sqrt{\varepsilon_r} \text{ ps/inch}$$

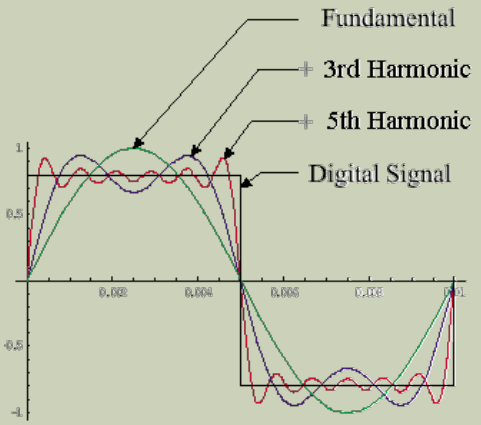
FR4 Example

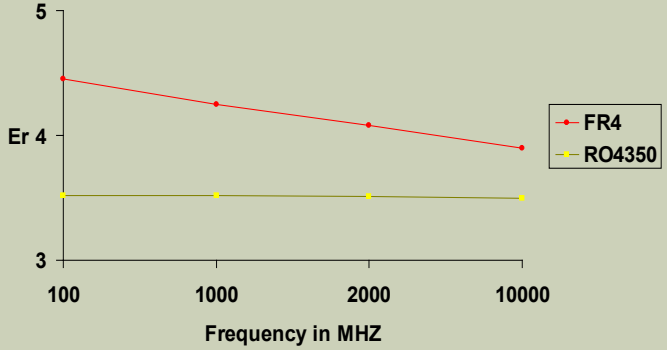
ε_r= 4.5

t_d = 180 ps/inch

Signal Dispersion

- Frequency Dependent Dielectric Constant
  - Propagation velocity is frequency dependent
  - PWB acts as a dispersive medium
- Becomes an issue
  - Long Trace Runs
  - High Speed Data/Clocks
  - Critical Analog
- Constant time delay is necessary to ensure that signals arrive undistorted at the destination
- Issue further exasperated by frequency dependent attenuation

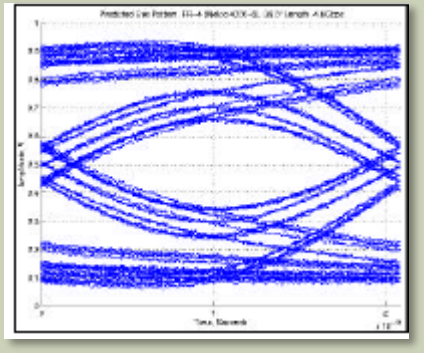




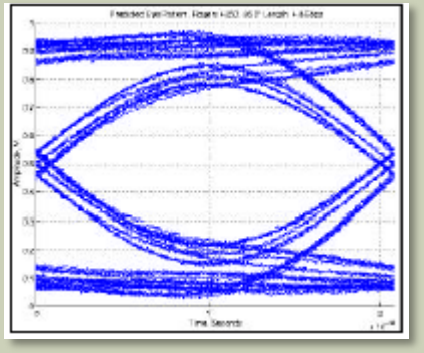
Signal Dispersion Example

- Eye Diagram
  - Provides a visual means to quickly evaluate signal integrity
  - Generated by superimposing successive digital waveforms to create a composite image (i.e. an oscilloscope image with infinite persistence)
- Eye Diagram Example
  - 4.8 Gbps
  - 36” trace length
  - Three different PWB dielectrics

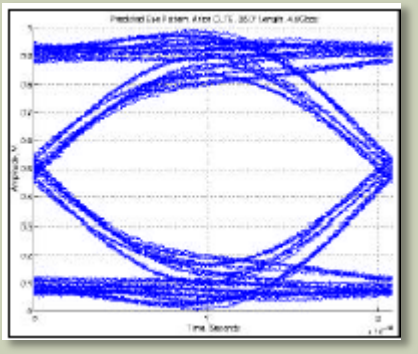
FR4



Rogers 4350

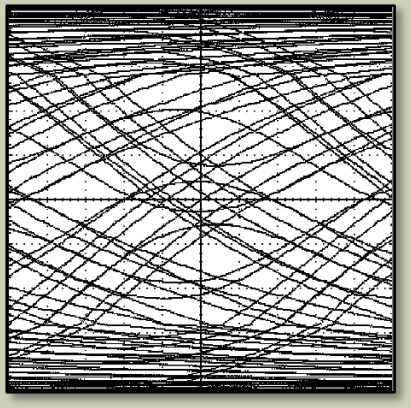


Arlon CLTE



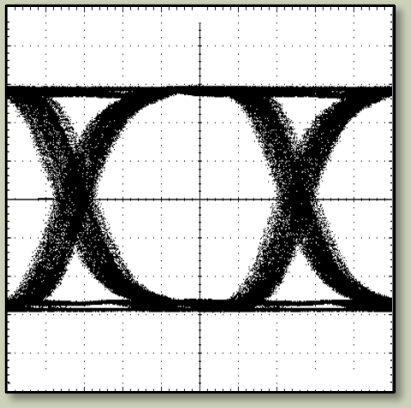
Mitigation of Dispersion and Attenuation

- More Stable Dielectric
- Wider Traces
- Pre-Emphasis Filter at the source
- Equalizer at the destination
  - e.g. Maxim MAX3784 (40” length, 6 mil, FR4, 5 Gbps)



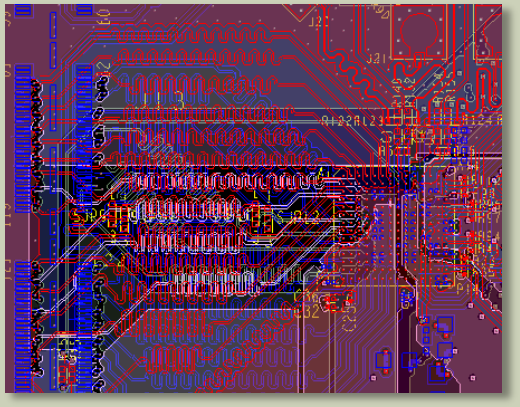
Eye Diagram Before Equalization

Eye Diagram After Equalization



JESD204B

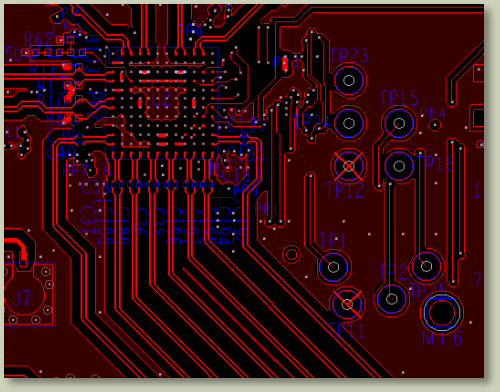
- A standardized serial interface between data converters (ADCs and DACs) and logic devices (FPGAs or ASICs) to reduce the number of I/O between devices
- Accomplished by serializing large amounts of parallel data with 8b/10b Encoding (data rates up to 12.5 Gbps)
- Advantages include
  - Greatly reduced I/O count
  - Reduced number of meandering traces to ensure alignment



32-bit data bus on 4 layers with meandering lines to equalize delay

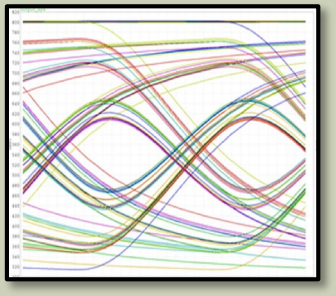
Courtesy TI

JESD204B Implementation using 8 lanes on 1 layer



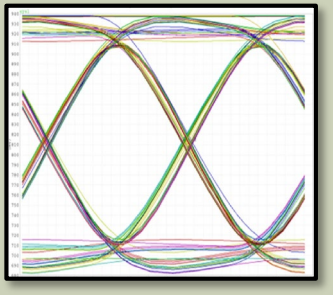
JESD204B Continued

- Example
  - I/Q 16-bit data on two receiver channels sampling at 80 MHz
  - 2 x 16 x 2 x 80 MHz x 10/8 = 6.4 GHz (one serial signal replaces 2 x 16 x 2 = 64)
- JESD204B receiver includes an equalizer to reduce dispersion effects and frequency dependent attenuation both of which are deterministic



Eye Diagram
Before Equalizer

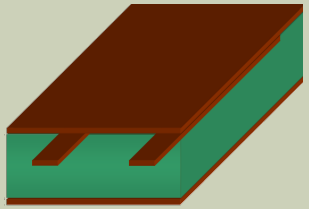
Eye Diagram
After Equalizer



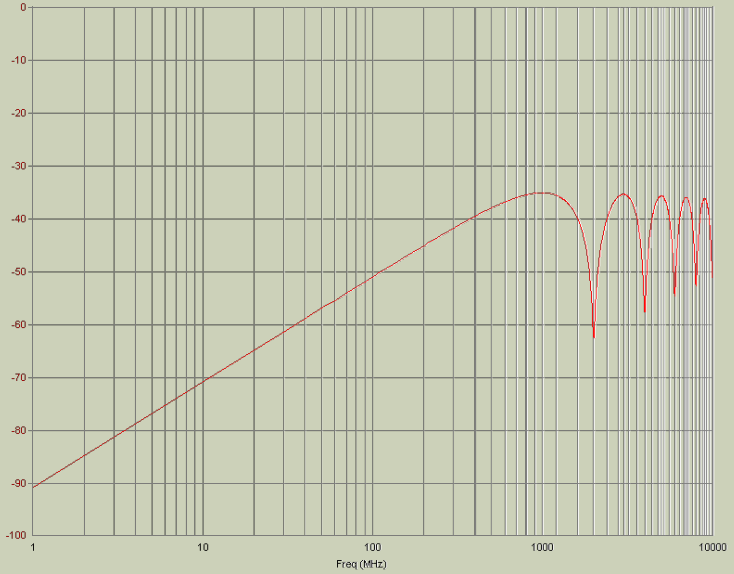
- Relatively easy to achieve high data rates between devices on the same PWB especially on the same side.
  - No vias, minimal discontinuities
- However, the equalizer cannot effectively compensate for impedance discontinuities
  - Care must be taken to ensure a consistent impedance from the JESD204B transmitter to receiver especially in cases where the signals must propagate through multiple connectors

Coupling

- Traces run in close proximity will couple
- Coupling is determined by geometry
  - Trace separation, distance to ground(s) & parallel length
- Most efficient coupling occurs at λ/4
  - For lower frequencies (wavelength longer than λ/4) coupling diminishes with a slope of 20 dB/decade
  - For higher frequencies (wavelength shorter than λ/4) coupling will reach a minimum and maximum every λ/4, with the peak couplings never exceeding that at λ/4.

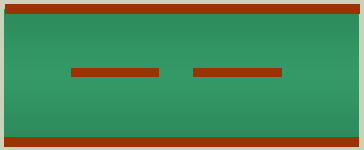


Notes:
1. Material FR4, ε_r = 4.5
2. Parallel length = λ/4 = 1.39″ at 1 GHz
3. t = 1.4 mils
4. h = 30 mils (15 + 15)
5. s = 30 mils
6. w = 11 mils
7. Both lines 50 Ω terminated at both ends



Quarter Wave Coupling/Isolation Examples

- Stripline
  11 mil width
  $\lambda/4 \approx 1.39$”



s	Coupling/Isolation
0.011”	18 dB
0.030”	35 dB

To achieve same level of isolation much greater separation is required with microstrip.

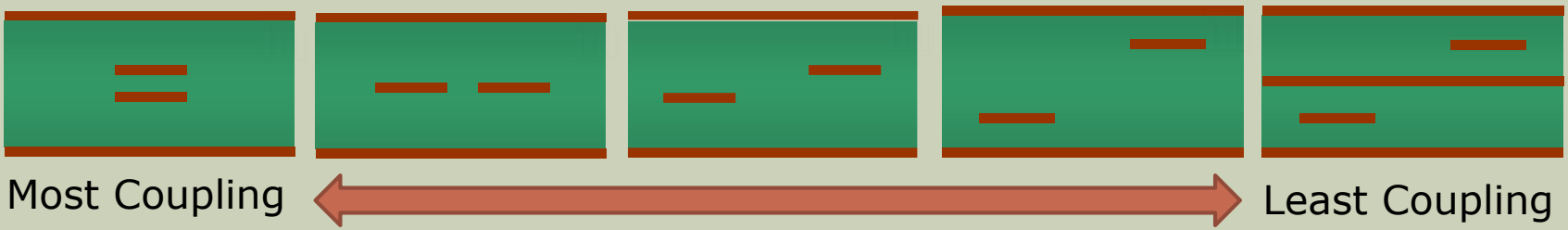
- Microstrip
  54 mil width
  $\lambda/4 \approx 1.60$”

s	Coupling/Isolation
0.030”	18 dB
0.150”	35 dB

In both the above cases, copper is 1 oz electrodeposited, FR4 dielectric (ε_r = 4.50, h = 0.030”) and F = 1.0 GHz.

Mitigation of Coupling

- Separation of traces
- Reduce length of parallel run (to a point, λ dependent)
- On adjacent layers, run traces orthogonally
- Run traces on separate non-adjacent layers
  - Preferably with a ground plane in between
- Run guard trace
  - Ground trace between lines
- Shield (for microstrip)
- Dielectric height allocation

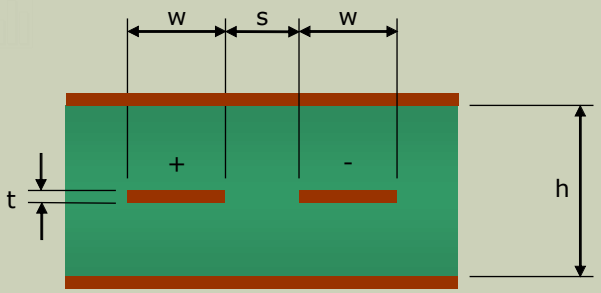


Differential Pairs

- For differential pairs, tight coupling is desired
- Lower cross-talk, lower radiation
- Common mode noise rejection
- Reduces ground reference problems
- Useful in high dynamic range analog applications
  - Log Amplifiers
  - High Resolution ADC/DAC
  - Transducers
- Useful in high speed digital applications
  - Low amplitude clocks
  - Low jitter requirements

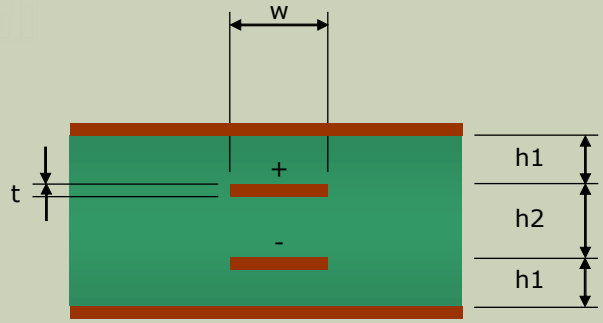
Differential Pair Routing Options

- Geometry and spacing defined by artwork
- High differential impedance easily achievable
- Impedance reduced as “s” is reduced
- As “s” is increased, impedance approaches 2x single ended impedance
- Difficult to rout through fine pitch holes



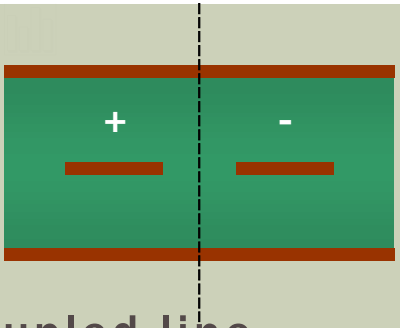
Edge Coupled

- Geometry is effected by layer registration
- Low differential impedance easily achievable
- Easy to route, easy to maintain matched lengths



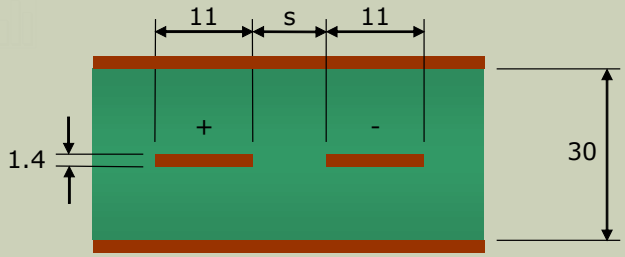
Broadside Coupled

Differential Impedance Definitions



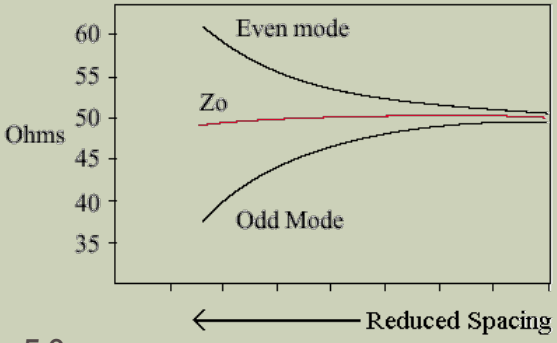
- Single-Ended Impedance (Z_O)
  Impedance on a single line with respect to ground when not coupled to another line
  $Z_0 = \sqrt{Z_{Odd} Z_{Even}}$
- Differential Impedance (Z_{DIF})
  The impedance on one line with respect to the coupled line, when the lines are driven by equal and opposite signals
- Odd Mode Impedance (Z_{Odd})
  Impedance on a single line with respect to ground when the other coupled line is driven by equal and opposite signals ($Z_{DIF} = 2Z_{Odd}$)
- Common Mode Impedance (Z_{CM})
  Impedance of the two lines combined with respect to ground
- Even Mode Impedance (Z_{Even})
  The impedance on one line with respect to ground when the coupled line is driven by an equal and in-phase signal ($Z_{Even} = 2Z_{CM}$)

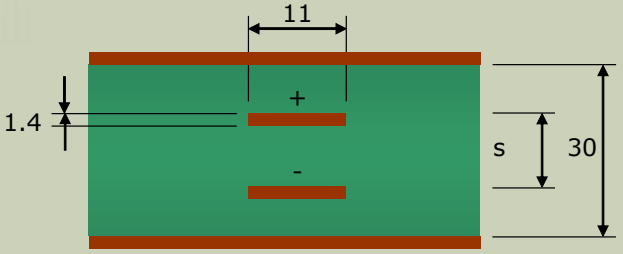
Differential Impedance Examples



Edge Coupled

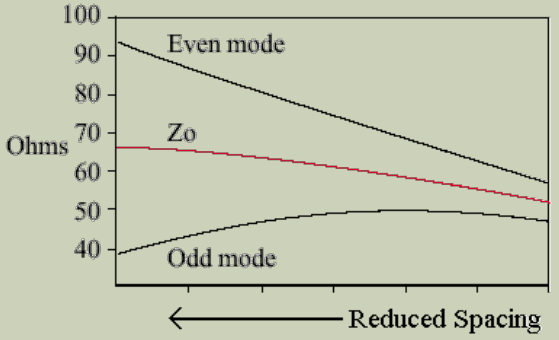
S	Z_{Even}	Z_{Odd}	Z_o	Z_{Diff}
100	49.4	49.4	49.4	98.8
25	50.9	47.9	49.4	95.8
10	56.4	41.9	48.6	83.8





Broadside Coupled

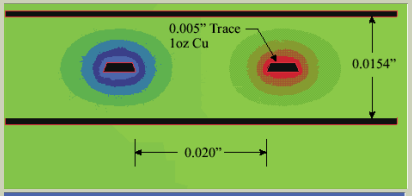
S	Z_{Even}	Z_{Odd}	Z_o	Z_{Diff}
20	41.3	34.7	37.8	69.4
10	68.6	34.7	48.8	69.4

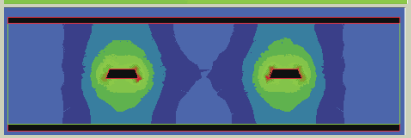


Near Field Stripline Differential Pair

- Lines are far apart
  - Most of electric field is concentrated between ground planes and conductors
  - Little magnetic field interaction
  - Most or all current is returned through the ground plane

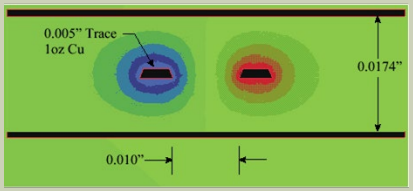
Magnetic Field

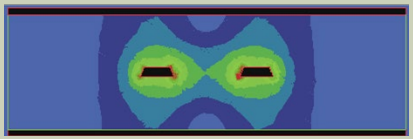


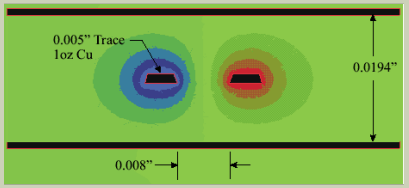


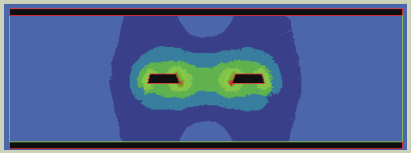
Electric Field

- As the lines are brought closer and/or the ground planes are brought further apart
  - More of the electric field is concentrated between the conductors
  - Less of the field is concentrated between the ground planes and the conductors

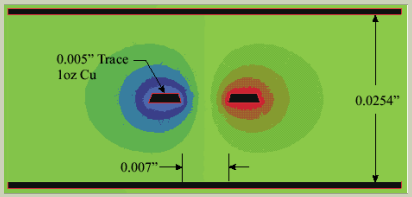


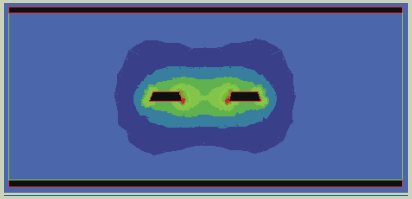




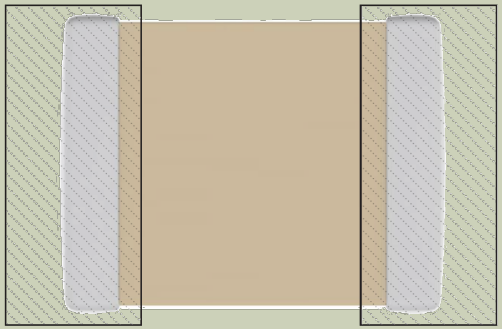


- Lines are very close
  - Most of the electric field is concentrated between the conductors
  - Little return current flows through the ground planes
  - In practice, this can be difficult to achieve on PWBs (because of the high dielectric height, close trace proximity and/or thin lines required)





Pad Parameter Examples

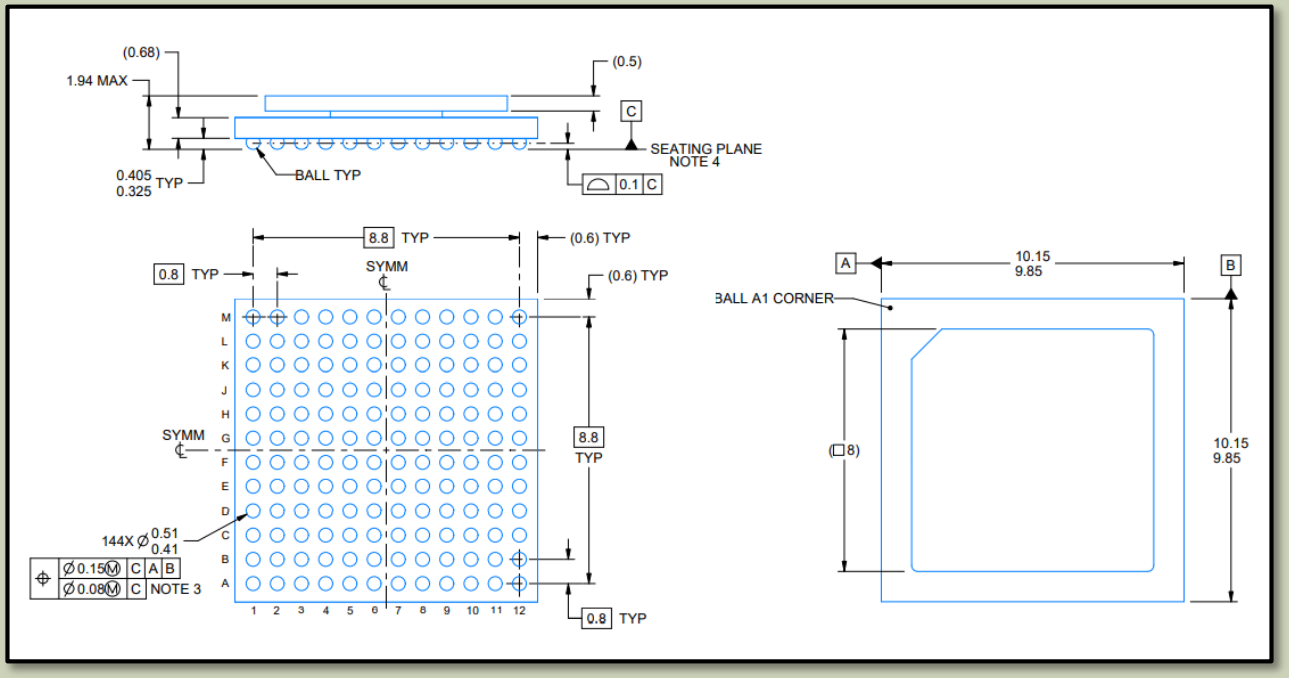


- Pads are typically larger in X and Y dimensions than the component contact areas
- Sensitive applications may require that the pad characteristics be considered
- Land size is in accordance with IPC-7351, Density Level B
- Pad capacitance is based on 1 oz copper, stripline on FR4 (ε_r = 4.50, h = 5mils)

Imperial Size Des	Metric Size Des	Component Size (LxW)	Pad Size (LxW)	Pad Cap (pF)
01005	0402	0.016x0.008 in 0.40x0.20 mm	0.010x0.008 in 0.25x0.20 mm	0.03
0201	0603	0.02x0.01 in 0.60x0.30 mm	0.018x0.017 in 0.46x0.42 mm	0.09
0402	1005	0.04x0.02 in 1.00x0.50 mm	0.024x0.024 in 0.62x0.62 mm	0.15
0603	1608	0.06x0.03 in 1.60x0.80 mm	0.037x0.039 in 0.95x1.00 mm	0.35
0805	2012	0.08x0.05 in 2.00x1.25 mm	0.045x0.057 in 1.15x1.45 mm	0.60
1206	3216	0.12x0.06 in 3.20x1.60 mm	0.045x0.07 in 1.15x1.80 mm	0.74
1210	3225	0.12x0.10 in 3.20x2.50 mm	0.045x0.11 in 1.15x2.70 mm	1.14
1812	4532	0.18x0.12 in 4.50x3.20 mm	0.055x0.14 in 1.40x3.50 mm	1.75
2220	5650	0.22x0.20 in 5.70x5.00 mm	0.059x0.21 in 1.50x5.40 mm	2.80
2225	5664	0.22x0.25 in 5.60x6.40 mm	0.059x0.27 in 1.50x6.80 mm	3.60

Increasing pad capacitance

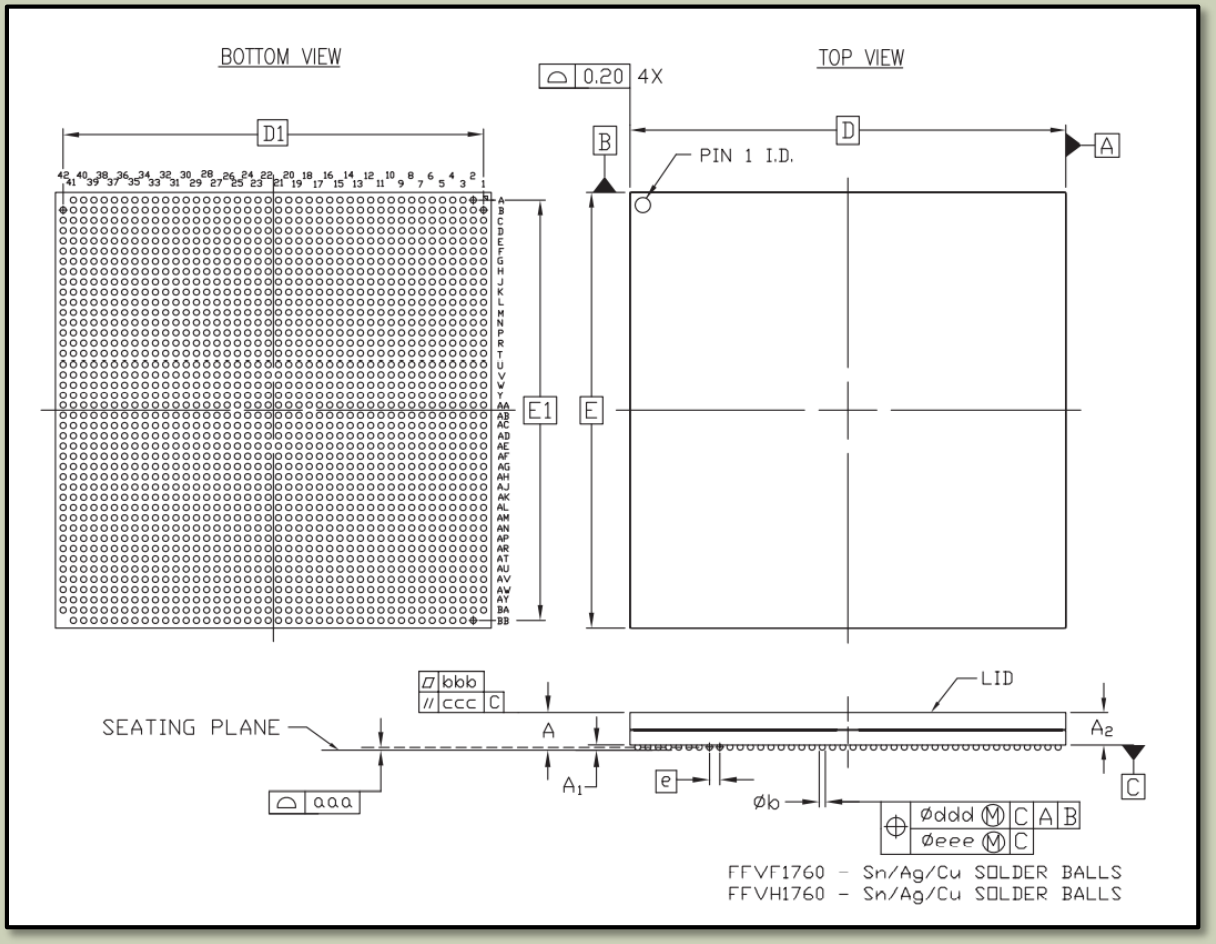
0.8 mm Pitch BGA (FCBGA) Package Example



- DAC38RF83
- 144 contact points
- 0.8 mm (0.031”) pitch
- Overall size is 10.15 mm sq (0.400” square)

Courtesy of TI

1 mm Pitch BGA (FFVH1760) Package Example



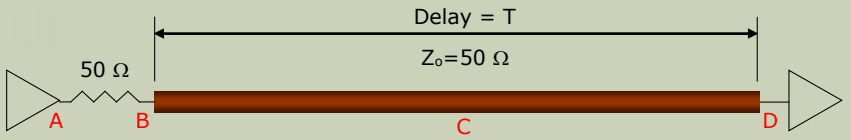
SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.46	3.66	3.86	
A_1	0.40	0.50	0.60	
A_2	2.96	3.16	3.36	
D/E	42.50 BASIC			
D_1/E_1	41.00 BASIC			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	~~	~~	0.20	
bbb	~~	~~	0.10	
ccc	~~	~~	0.10	
ddd	~~	~~	0.25	
eee	~~	~~	0.10	
M	42			2

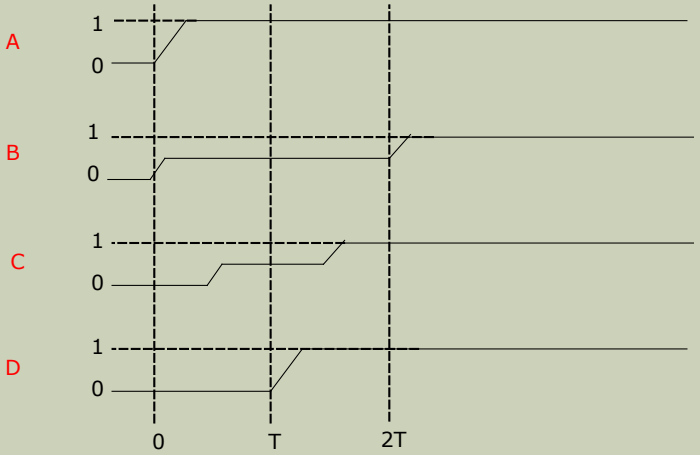
- 1,760 contact points
- 1 mm (0.0394") pitch
- Overall size is 42.5 mm sq (1.673" square)

Courtesy of Xilinx

Source Terminations

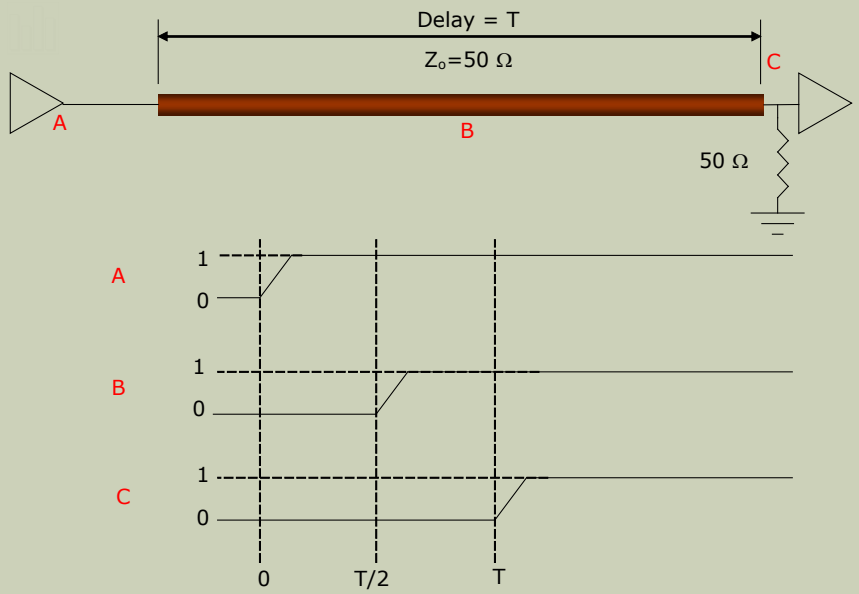
- Reduces peak current demands on the driver
- Driving waveform is halved by the series resistor at the start of propagation (assuming $R_S=Z_0$)
- Driving signal propagates at half amplitude to end of line
- At end reflection coefficient is +1
- Eventually all points reach full amplitude as the reflected wave propagates back to the source





Destination Terminations

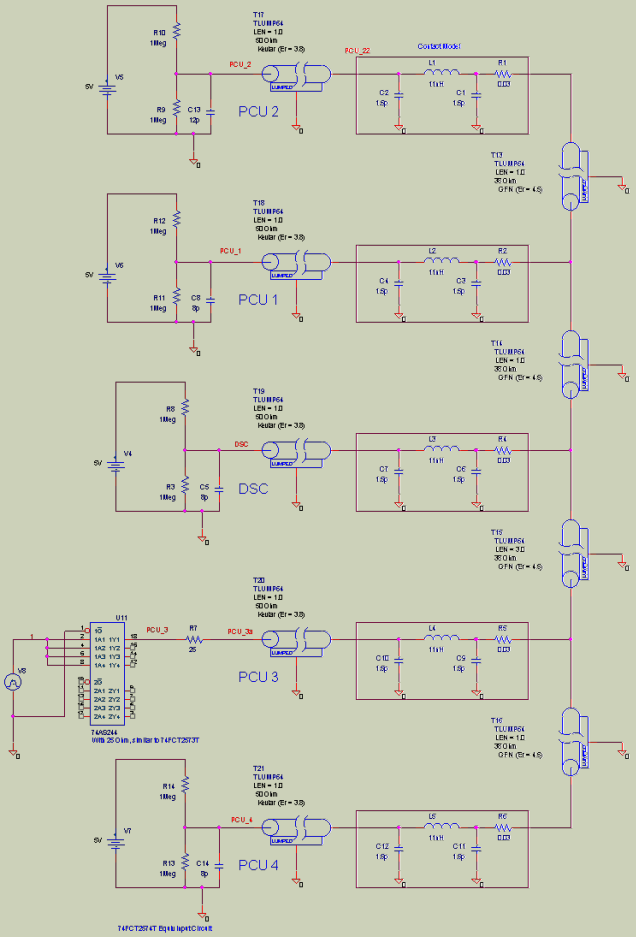
- Driving waveform propagates at full intensity over trace facilitating first-incident switching
- Reflections dampened by end termination
- Received voltage is equal to transmitting voltage at all points (ignoring losses)
- Increased peak current demands on driver



- Steady-state drive current can be reduced by the use of a Thevenin termination

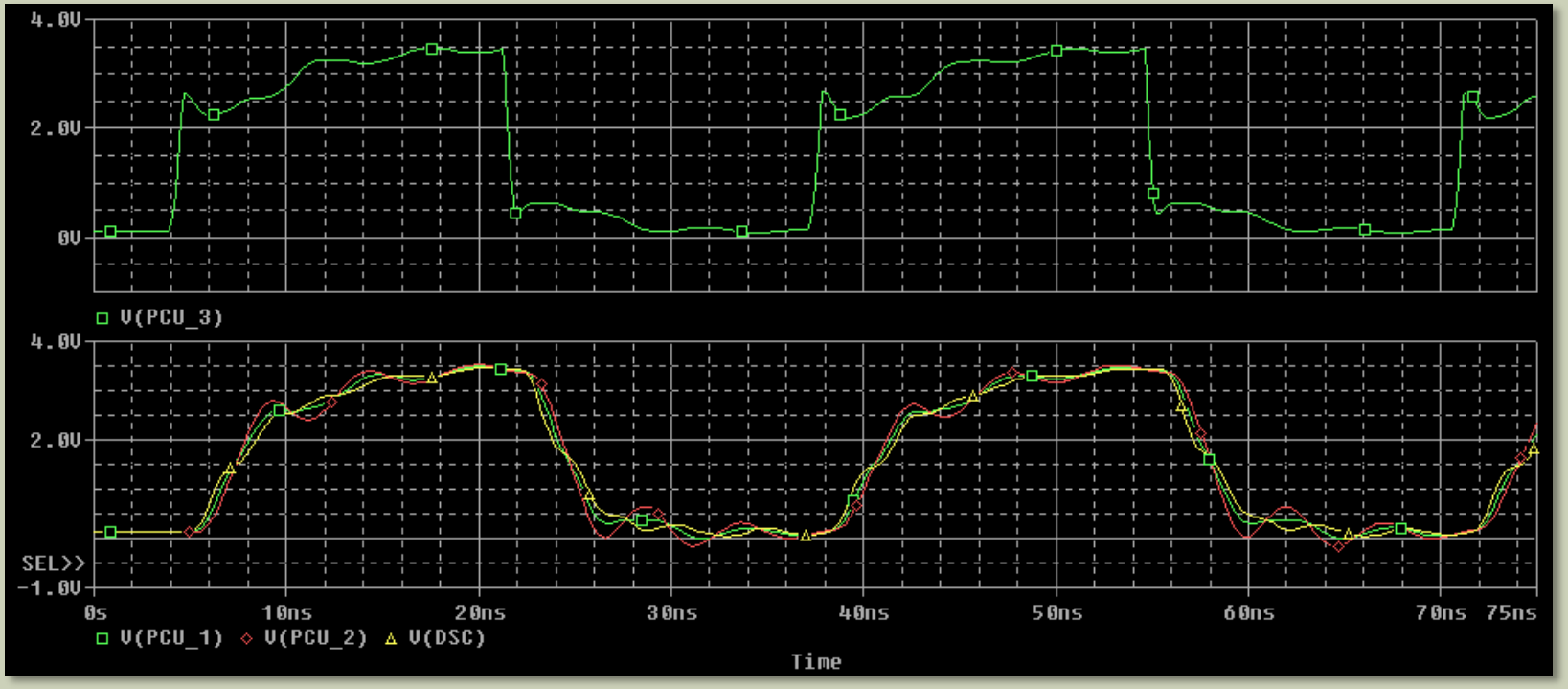
“Intentional” Mismatch Example

- Five selectable sources
- Four destinations
- Modeled signal paths
  - CCA PWB
  - Back Plane PWB
  - Connectors
  - Driver
- Took advantage of relatively slow clock (30 MHz)



“Intentional” Mismatch Example

- Allow reflections to dissipate before clocking data (Clocks distributed point-to-point)



Power Distribution, Power Integrity (PI) and Grounding

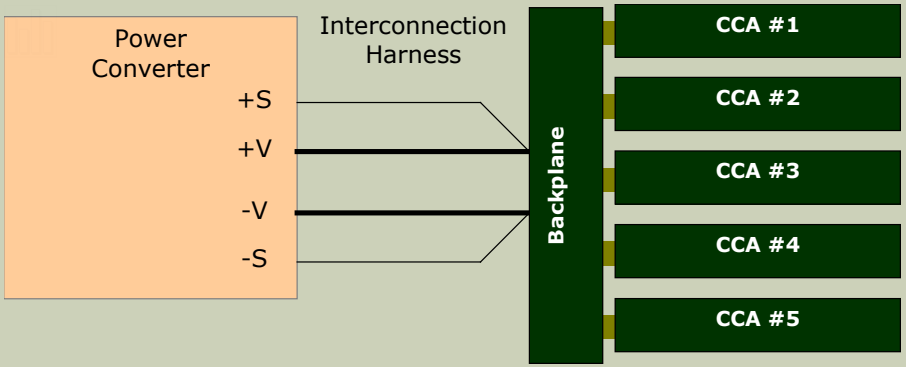
PI is a set of measures to ensure the required voltage and current are distributed from the source to the load(s).

Power Distribution Purpose

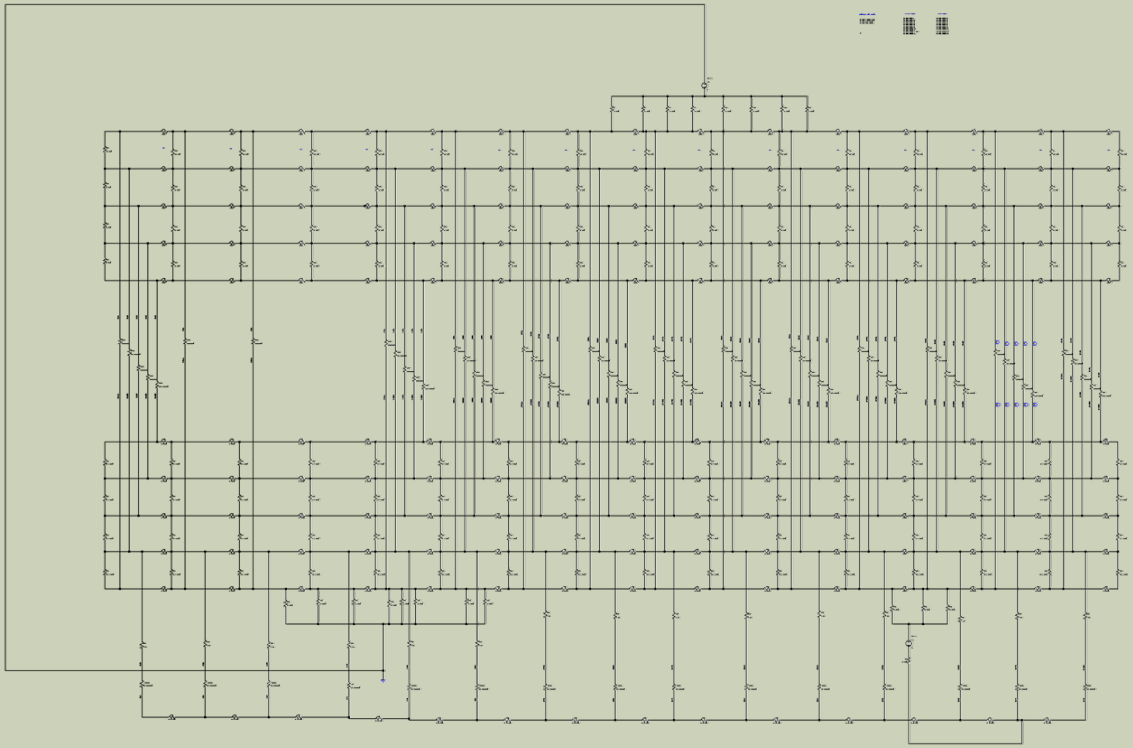
- To distribute the supply voltages necessary to all components within the required regulation
- To provide a reliable reference (ground) for all circuitry
  - Which is also a part of Signal Integrity

Supply Power Loss Budget

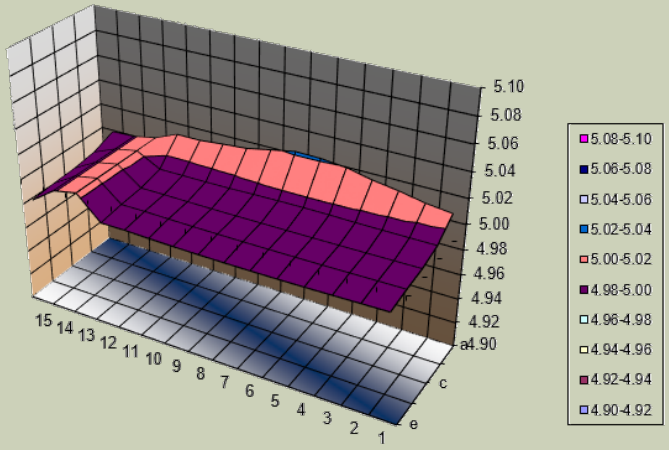
- Distribution loss contributes to supply voltage error delivered to CCA components
- Complete loss budget needs to be established, especially in high power applications
  - Power Supply Voltage Tolerance
  - Harnessing Loss
  - Connector Loss
  - Backplane Loss
  - PWB Loss on CCA
- Remote Sensing
  - Compensate for some losses
  - Location important
  - “Open Sense” protection



Backplane PWB DC Loss Model



Voltage drop across backplane is simulated with PSpice grid model (shown for reference)

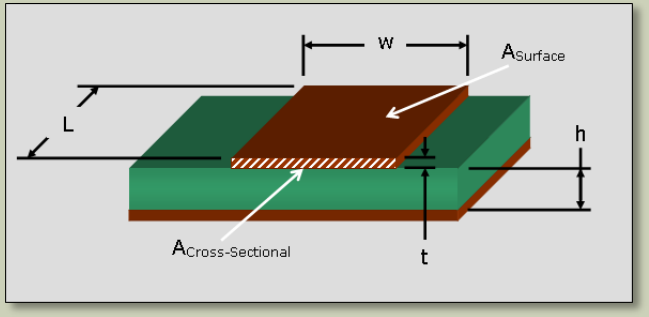


PSpice simulation results showing voltage distribution across backplane

Power Distribution Considerations

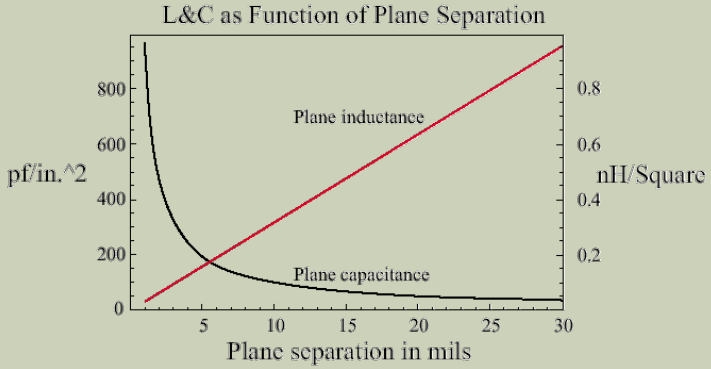
- Dedicated adjacent planes for ground and supply voltage
  - Establishes low inductance distribution
  - Parallel planes create distributed capacitance (which supplement decoupling capacitors)
  - e.g. DuPont HK04M
    - 12 µm (0.5 mil)
    - $\varepsilon_r = 4.0$
    - Yields 240 pF/cm^2
    - By virtue of thin material, distributed inductance is minimized
- Through-holes perforate planes
  - Increases resistance
- Distributing supplies for analog/RF
  - Rout power traces between ground planes

Plane Capacitance, Inductance, Resistance



Inductance

$$L = \mu_0 \mu_r h \frac{l}{w} \qquad \mu_0 = 4\pi x 10^{-7} \frac{H}{m} = 0.32 \frac{nH}{in}$$



Resistance

$$R_{DC} = \rho \frac{l}{tw} = \rho \frac{l}{A} \qquad \rho = 0.0172 \mu\Omega - m = 0.679\ \mu\Omega - in$$

Allowing l=w permits calculation of Resistance per square

$$R_{DC}\ per\ Square = \rho \frac{1}{t} = (0.679 \mu\Omega - in) \frac{1}{0.0014\ in} = 485 \mu\Omega / Square$$

Example is for 1 ounce copper which is 0.0014" thick

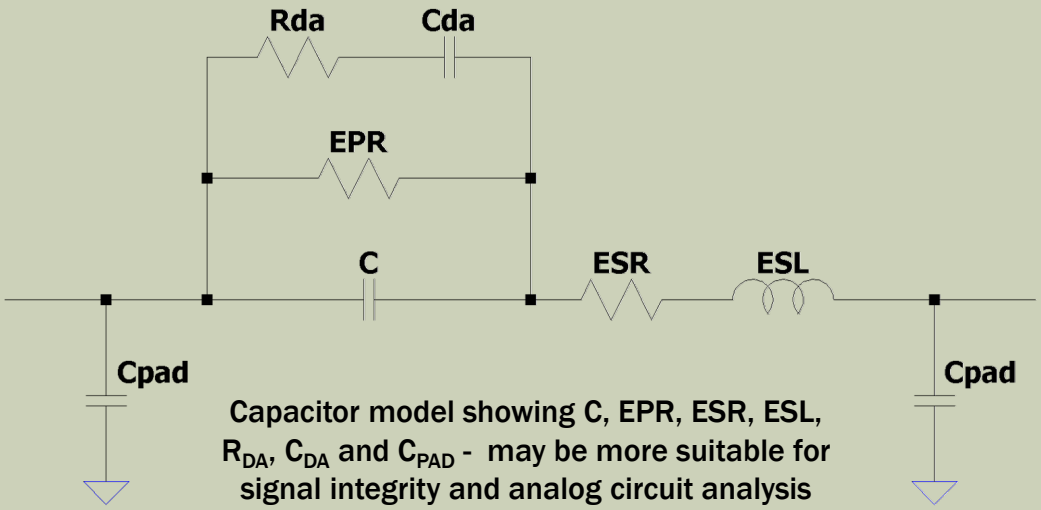
Capacitance

$$C = \varepsilon_0 \varepsilon_r \frac{LW}{h} = \varepsilon_0 \varepsilon_r \frac{A}{h} \qquad \varepsilon_0 = 8.85 x 10^{-12} \frac{F}{m} = 225 x 10^{-15} \frac{F}{in}$$

FR4 Dielectric Thickness (mils)	Plane Inductance (pH/square)	Plane Capacitance (pF/inch²)
8	260	127
4	130	253
2	65	506

Capacitor Model

- Physical capacitors have parasitic elements that limit their ability to stabilize supply lines
- For power integrity, a simplified capacitor model is normally adequate
  - Equivalent series inductance (ESL)
  - Equivalent Series Resistance (ESR)
  - Actual capacitance (C)

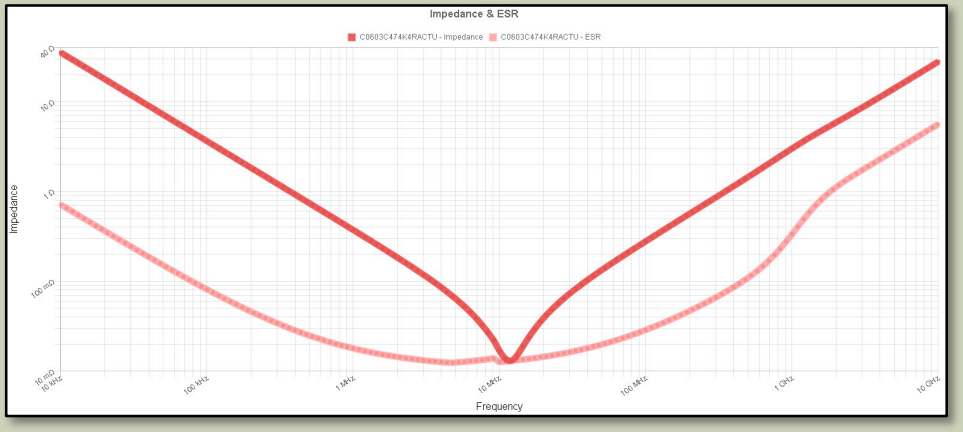


Capacitor model showing C, EPR, ESR, ESL, R_{DA}, C_{DA} and C_{PAD} - may be more suitable for signal integrity and analog circuit analysis

Simplified capacitor model showing C, ESR and ESL is typically adequate for power integrity analysis

Capacitor Parameters

Part Number	Type	Package	Cap (uF)	Voltage (V)	ESL (nH)	ESR (mΩ)	SRF (MHz)
C0603X7S1A104K030BC, TDK	X7S Ceramic	0201	1.0	10	0.06	50	20.0
C0402C104K3RACTU, Kemet	X7R Ceramic	0402	0.10	25	0.2	22	34.8
C0603C474K4RACTU, Kemet	X7R Ceramic	0603	0.47	16	0.4	13	11.6
C0805C224K1RACTU, Kemet	X7R Ceramic	0805	0.22	100	2.3	13	7.1
C1206C225K5RACTU, Kemet	X7R Ceramic	1206	1.0	50	4.0	12	2.5
C1812C475K5RACTU, Kemet	X7R Ceramic	1812	4.7	50	0.7	8	2.7



C0603C474K4RACTU Impedance and ESR vs Frequency (Kemet Capacitor Simulation Tool)

$$f_{SRF} = \frac{1}{2\pi\sqrt{LC}}$$

Self Resonant Frequency

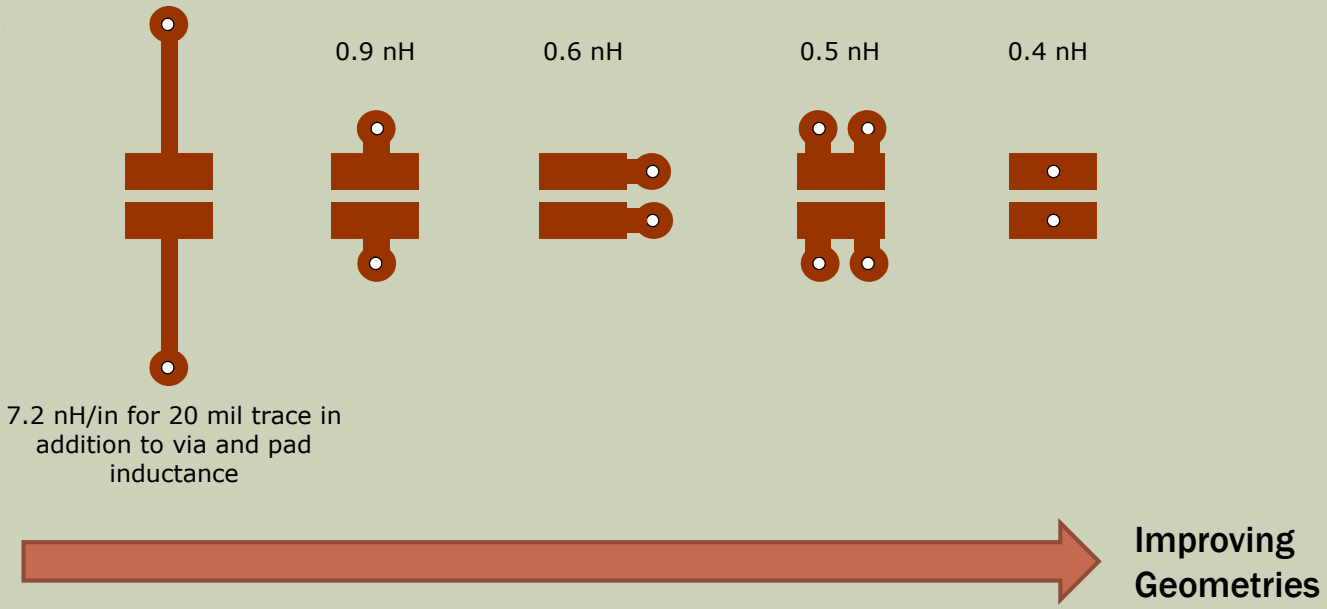
$$Q = \frac{1}{DF} = \frac{X_C}{R} = \frac{1}{2\pi \ f \ C \ R}$$

Quality Factor, Dissipation Factor

Capacitor Parameters (continued)

- Variables that effect parasitic inductance of a capacitor
  - Inductance increases with increasing package height
  - Inductance increases with increasing length
  - Inductance decreases with increasing width
  - Inductance increases with increasing distance between capacitor and ground plane
  - ESL parameter is actual a “Partial Inductance”
- PI Guidelines to minimize parasitic inductance
  - Minimize connection lengths
  - Eliminate or minimize sharing of vias
  - Tend towards using the shortest/lowest/widest package available

Capacitor Mounting Pads

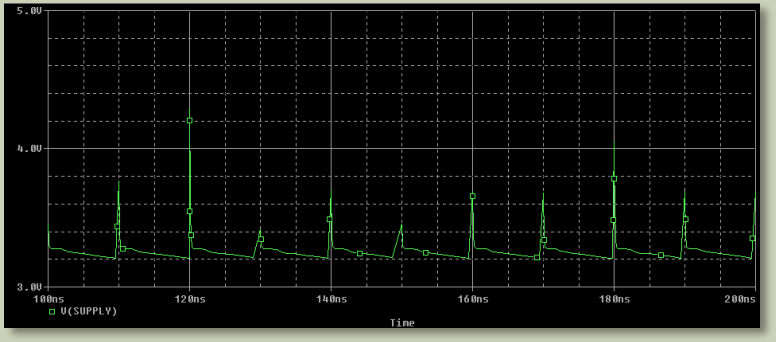


Notes:

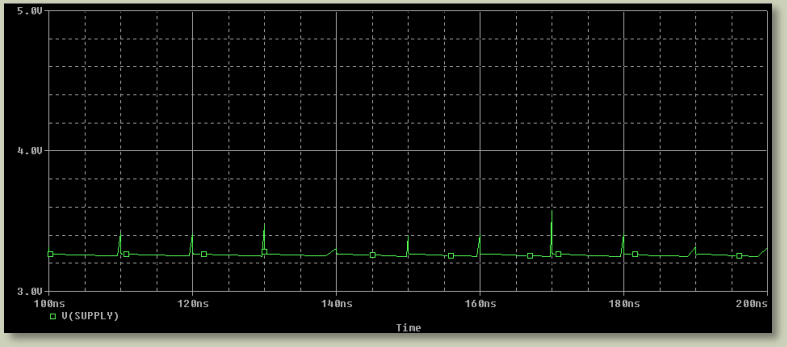
1. Copper: 1 oz, electrodeposited, microstrip
2. FR4 dielectric constant: 4.50, loss tangent 0.025, height 10 mils

Decoupling Examples

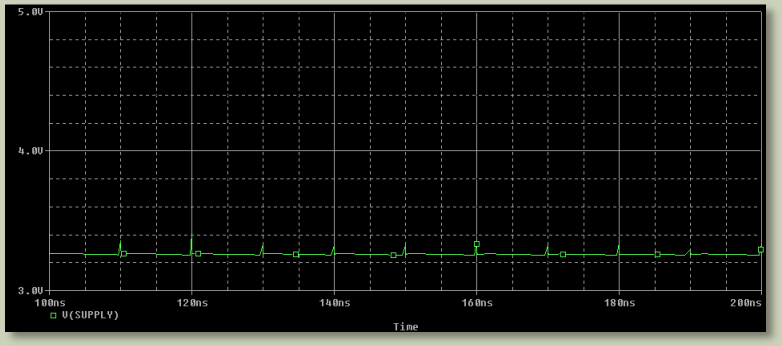
- 100 MHz Logic Device, 100 mA to 150 mA step load change



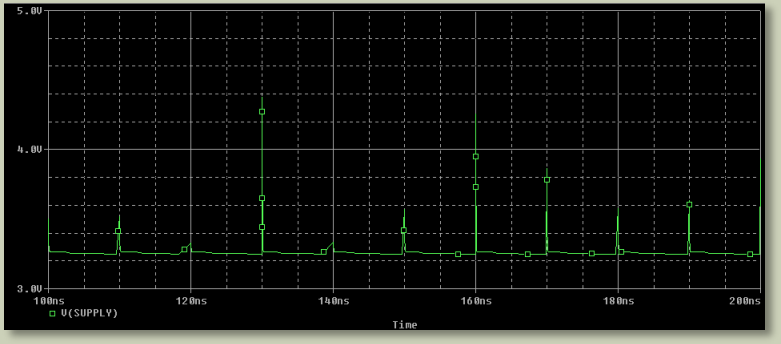
6.8 uF, Ripple: 1 Vpp



6.8 uF + 0.1 uF, Ripple: 0.3 Vpp



6.8 uF + 0.1 uF + 0.01 uF, Ripple: 0.1 Vpp



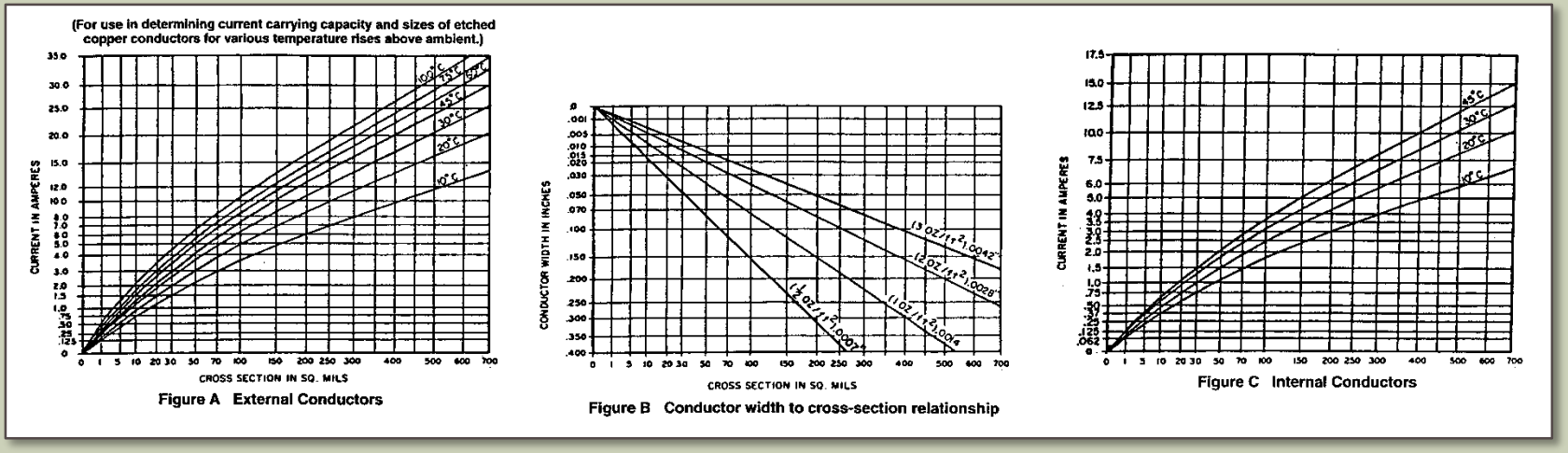
6.8 uF + 0.1 uF + 0.01 uF w/ long traces, Ripple: 1.1 Vpp

Current Carrying Capability of PWB Traces

- Influenced by
  - Trace Cross section (w, t)
  - Position of trace (outer layer, inner layer)
  - Maximum acceptable temperature rise
- IPC-2221, Figure 6-4, can be used as general guideline
- Thermal modeling may be needed in critical applications

Trace Width Example

- Application
  - Inner trace, 1 ounce, maximum fault current is 2 Amps
  - Max CCA temp +90 °C, max PWB temp +150°C, Margin 30 °C
  - Allowable Temp rise = 150–90–30=30°C
- Determine Cross Section from “C” is 56 sq mils
- Determine width from “B” to be 40 mils



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