This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/OJCAS.2022.3174694, IEEE Open Journal of Circuits and Systems

A Stable Digital Impedance Circuit Design Method for Resistive Source Impedances

Christopher G. Daniel Jr., *Student Member, IEEE,* Thomas P. Weldon, *Senior Member, IEEE*

The recent discovery that the input impedance of digital impedance circuits is dependent on the external source impedance requires the development of new design procedures to address the significant complexity of this discovery. These circuits are of particular utility for the implementation of difficult non-Foster impedances such as negative capacitance. Therefore, a new digital impedance circuit design procedure is presented where stable digital filter coefficients are computed to provide desired digital impedance values at two chosen frequencies, given that a stable solution exists. The new design procedure explicitly addresses the aforementioned dependence on the external source impedance for digital impedance circuits with resistive sources. Lastly, simulation results from a negative capacitance design example are compared to the new theory to confirm the efficacy of the new design procedure.

Index Terms—**Digital impedance, mixed-signal circuit stability, non-Foster impedance, source impedance dependence.**

The recent discovery that the input impedance of digital impedance circuits is dependent on the external source impedance requires the development of new design procedures to address the significant complexity of this discovery. These circuits are of particular utility for the implementation of difficult non-Foster impedances such as negative capacitance. Therefore, a new digital impedance circuit design procedure is presented where stable digital filter coefficients are computed to provide desired digital impedance values at two chosen frequencies, given that a stable solution exists. The new design procedure explicitly addresses the aforementioned dependence on the external source impedance for digital impedance circuits with resistive sources. Lastly, simulation results from a negative capacitance design example are compared to the new theory to confirm the efficacy of the new design procedure.

I. Introduction

NON-FOSTER circuits such as negative capacitors offer the potential for increased bandwidth in a variety of applications such as wideband electrically-small antennas, wideband artificial magnetic conductors, wideband acoustic elements, and metamaterials with wideband negative permeability and negative permittivity [1]–[8]. However, the design of stable analog implementations of non-Foster circuits remains challenging, and motivates the consideration of digital implementations of non-Foster impedances [9]–[12].

Digital impedance circuits provide a new alternative approach for the implementation of difficult-to-realize analog impedances, such as negative capacitance and negative inductance [13]. These digital impedance circuits are comprised of an ADC (analog-to-digital converter), a digital filter, and feedback from a DAC (digital-to-analog converter), with the digital filter determining the input port impedance. This digital loop has potential advantages associated with digital systems, such as having digitally-tunable or adaptive circuit parameters which may offer new stabilization approaches.

More recently, we discovered that the input impedance of these digital impedance circuits was dependent on the impedance of the external source driving the circuit when earlier simplified circuit design approximations would fail in certain cases [14]. In particular, the earlier digital impedance design procedures were often ineffective at high frequencies above 20 MHz where the ADC and DAC often have low impdances of 50 ohms. Unfortunately, the analytical result of the digital input impedance when incorporating the dependence on the external source impedance was quite complicated. Nonetheless, we present a new design procedure which does incorporate the discovered dependence on the external source impedance for digital impedance circuits with resistive sources. This novel design procedure will determine the coefficients of the digital filter for a stable digital impedance circuit with desired digital impedance values at two chosen frequencies, given that a solution exists. Note that beyond the present work, the overall design method in and of itself may be useful in solving other related engineering design problems.

In Section II, we first present the theoretical analysis for a source-dependent digital impedance theory in a form which lends itself to the parameterization necessary for the new design procedure. Section III will present the new design procedure for selecting digital filter coefficients to obtain a desired stable digital impedance circuit under the assumption that a solution exists. In Section IV, simulation results from a negative capacitance design example are compared with theoretical results to demonstrate the effectiveness of this new design procedure.

II. Theoretical Analysis

Prior digital impedance design methods used approximations which were useful for the implementation of a digital non-Foster RC circuit in [15]. However, the voltage input ADC used in the microcontroller based system in [15] had very high input resistance, which is not an acceptable assumption in many cases of high-speed ADCs (>20 MHz sampling). Indeed, the earlier approximation-based design procedures often failed when high-speed 50 Ω ADCs and DACs were considered in the analysis. This led to the discovery in [14] that the digital input impedance was dependent on the external source impedance, and is the motivation for the new design procedure below.

C.G. Daniel Jr. is with Stanford University, Stanford, CA.

T.P. Weldon is with the Department of Electrical and Computer Engineering, University of North Carolina at Charlotte, Charlotte, NC, 28223 USA e-mail: tpweldon@uncc.edu.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/OJCAS.2022.3174694, IEEE Open Journal of Circuits and Systems

To begin, consider the digital impedance circuit of Fig. 1 with a source-dependent digital impedance that is analyzed using the Fig. 2 block diagram. In Fig. 2, $V_{in}^{\star}(s)$ is the starred transform of V_{in} [16], and $V_s(s)$ is the Laplace transform of the source voltage. The ADC of Fig. 1 is then replaced by the sampler in Fig. 2, with the sampler output $V_{in}^{\star}(s)$ becoming the starred transform of the input voltage $V_{in}(s)$. The DAC output is formed by passing through the ZOH (zero-order hold) with the transfer function $(1-z^{-1})/s$. The ZOH output in Fig. 2 will also pass through the same time delay $e^{-s\tau}$ as in Fig. 1.

The input voltage from Fig. 2 in the Laplace domain with a general $Z_s(s)$ external source impedance is given as [14]:

$$V_{in}(s) = \left. \frac{\frac{V_s(s)}{Z_s(s)} + \frac{V_{in}^{\star}(s)e^{-s\tau}H(z)(1-z^{-1})/s}{R_{io}+R_{dac}}}{\frac{1}{Z_s(s)} + \frac{1}{R_{adc}} + \frac{1}{R_{io}+R_{dac}}} \right|_{z=e^{sT}}$$

$$= \left. \frac{\frac{V_s(s)}{Z_s(s)} + \frac{V_{in}^{\star}(s)e^{-s\tau}H(z)(1-z^{-1})/s}{R_{io}+R_{dac}}}{\frac{Z_s(s)+R_e}{Z_s(s)R_e}} \right|_{z=e^{sT}}, \quad (1)$$

where T is the sampling period of the ADC and DAC and R_e is the resistance of the parallel combination of R_{adc} with $R_{dac}+R_{io}$. To find $V_{in}^{\star}(s)$, we take the starred transform of both sides of (1) as follows:

$$V_{in}^{\star}(s) = \left(\frac{R_e V_s(s)}{R_e + Z_s(s)} \right)^{\star} + \left. \frac{R_e V_{in}^{\star}(s) H(z)(1-z^{-1})K(z)}{R_{io}+R_{dac}} \right|_{z=e^{sT}}$$

$$= V_s(z)L(z) + \left. \frac{R_e V_{in}^{\star}(s) H(z)(1-z^{-1})K(z)}{R_{io}+R_{dac}} \right|_{z=e^{sT}}, \quad (2)$$

where $([R_e V_s(s)]/[R_e + Z_s(s)])^{\star} \approx V_s(z)L(z)$ for frequencies below $1/(2T)$ of a bandlimited $V_s(s)$ without aliasing, and $L(z)$ is the z-transform of $L(s) = R_e/(Z_s(s)+R_e)$. $K(z)$ is defined as the modified z-transform of:

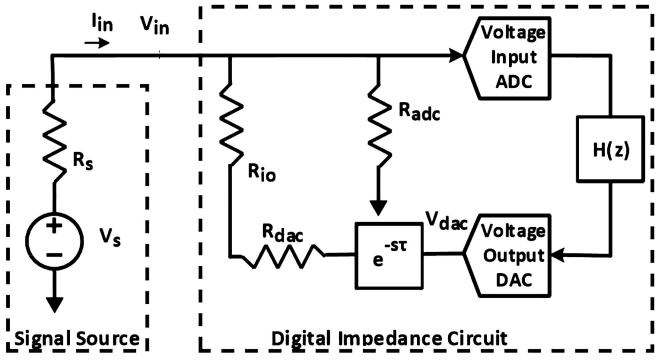

Fig. 1. Block diagram of a Thevenin-form digital impedance circuit driven by an external voltage source $V_s(s)$ and an external source impedance R_s.

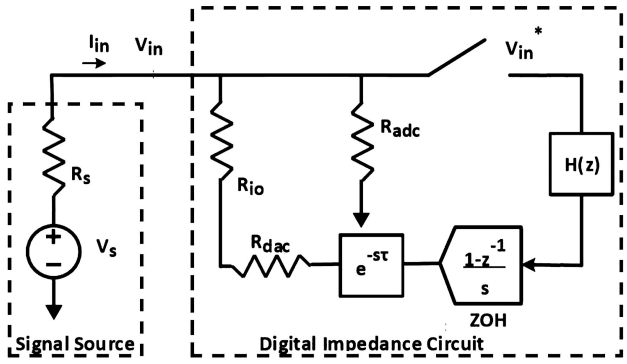

Fig. 2. Analysis block diagram of a Thevenin-form digital discrete-time impedance circuit driven by an external voltage source $V_s(s)$ and an external source resistor R_s with a sampler switch introduced. The ADC acts as a switch and the voltage after the ADC is the starred transform of the input voltage.

$$\frac{Z_s(s)e^{-s\tau}}{s\big(R_e + Z_s(s)\big)}. \quad (3)$$

For resistive sources $Z_s(s) = R_s$, the z-transforms will become $L(z) = R_e/(R_s+R_e)$ and $K(z) = R_s(R_e + R_s)^{-1}(z-1)^{-1}$. The input current is also found by the voltage difference between the source and the input divided by the source resistance:

$$I_{in}(s) = \frac{V_s(s) - V_{in}(s)}{R_s}. \quad (4)$$

To develop a design procedure for the digital filter coefficients in $H(z)$, the extraordinarily complicated equation for the digital impedance $Z_{in}(s)$ given in [14] is rearranged below in a more convenient form for determining stable designs. Using a commercial symbolic solver, the digital input impedance for resistive sources is found to be:

$$Z_{in}(s) = \frac{V_{in}(s)}{I_{in}(s)} = \left. \frac{A(s,z)H(z) + B(s,z)}{C(s,z)H(z) + D(s,z)} \right|_{z=e^{sT}}, \quad (5)$$

where

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/OJCAS.2022.3174694, IEEE Open Journal of Circuits and Systems

$$
\begin{aligned}
A(s,z) &= R_{adc}^2 R_{dac} R_s z - R_{adc}^2 R_{io} R_s - R_{adc}^2 R_{dac} R_s \\
&+ R_{adc}^2 R_{io} R_s z - R_{adc}^2 R_{dac} R_s T s e^{s\tau} \\
&- R_{adc}^2 R_{io} R_s T s e^{s\tau}\big|_{z=e^{sT}}
\end{aligned}
$$

$$
\begin{aligned}
B(s,z) &= R_{adc}^2 R_{dac}^2 T s z e^{s\tau} + R_{adc}^2 R_{io}^2 T s z e^{s\tau} \\
&+ 2R_{adc}^2 R_{dac} R_{io} T s z e^{s\tau} + R_{adc} R_{dac}^2 R_s T s z e^{s\tau} \\
&+ R_{adc}^2 R_{dac} R_s T s z e^{s\tau} + R_{adc} R_{io}^2 R_s T s z e^{s\tau} \\
&+ R_{adc}^2 R_{io} R_s T s z e^{s\tau} \\
&+ 2R_{adc} R_{dac} R_{io} R_s T s z e^{s\tau}\big|_{z=e^{sT}}
\end{aligned}
$$

$$
\begin{aligned}
C(s,z) &= R_{adc}^2 R_{dac} + R_{adc}^2 R_{io} - R_{adc}^2 R_{dac} z \\
&- R_{adc}^2 R_{io} z - R_{adc}^2 R_s T s e^{s\tau} - R_{adc} R_{dac} R_s T s e^{s\tau} \\
&- R_{adc} R_{io} R_s T s e^{s\tau}\big|_{z=e^{sT}}
\end{aligned}
$$

$$
\begin{aligned}
D(s,z) &= R_{adc} R_{dac}^2 T s z e^{s\tau} \\
&+ R_{adc}^2 R_{dac} T s z e^{s\tau} \\
&+ R_{adc} R_{io}^2 T s z e^{s\tau} \\
&+ R_{adc}^2 R_{io} T s z e^{s\tau} \\
&+ R_{adc}^2 R_s T s z e^{s\tau} + R_{dac}^2 R_s T s z e^{s\tau} \\
&+ R_{io}^2 R_s T s z e^{s\tau} + 2R_{adc} R_{dac} R_{io} T s z e^{s\tau} \\
&+ 2R_{adc} R_{dac} R_s T s z e^{s\tau} + 2R_{adc} R_{io} R_s T s z e^{s\tau} \\
&+ 2R_{dac} R_{io} R_s T s z e^{s\tau}\big|_{z=e^{sT}} . \qquad (6)
\end{aligned}
$$

III. Design Procedure

We seek to design a digital filter $H(z)$ in Fig. 2 which will produce a particular desired digital input impedance $Z_{in}(s) = V_{in}(s)/I_{in}(s)$ at two chosen frequencies. In the design procedure, we choose a pole-zero digital filter model for $H(z)$ in the following design equations.

To illustrate the method, we consider two deterministic impedance values at Laplace frequencies s_1 and s_2 which will approximate a negative capacitor frequency response at $Z_{in}(s_1)$ and $Z_{in}(s_2)$. Typically, $Z_{in}(s_1)$ and $Z_{in}(s_2)$ will have a non-zero real and imaginary part to their values. Since $Z_{in}(s_1) = Re\{Z_{in}(s_1)\} + jIm\{Z_{in}(s_1)\}$ and $Z_{in}(s_2) = Re\{Z_{in}(s_2)\} + jIm\{Z_{in}(s_2)\}$, there are effectively four known real and imaginary impedance values which can be used to find a solution in a system of four linear equations to solve for the digital filter coefficients in $H(z)$.

Therefore, a general pole-zero digital filter model with four degrees of freedom combined with the four values $Re\{Z_{in}(s_1)\}$, $Im\{Z_{in}(s_1)\}$, $Re\{Z_{in}(s_2)\}$, $Im\{Z_{in}(s_2)\}$ yields a linear system of four equations with four unknowns and a straightforward solution. For the purpose of illustration, Let

$$
H(z) = \frac{b_0 z + b_1}{z^2 + a_1 z + a_2}, \qquad (7)
$$

then we can solve for a b_0, b_1, a_1, a_2 value since we have four equations with four unknowns. However, such a solution is not necessarily stable.

Nonetheless, a stable solution may still be found by increasing the degrees of freedom in $H(z)$. To allow flexibility for choosing the digital filter coefficients of a pole-zero digital filter model which gives us the desired impedance values for $Z_{in}(s_1)$ and $Z_{in}(s_2)$ with a stable solution, we introduce an underdetermined system of equations for which we dictate $H(z)$ to take the form

$$
H(z) = \frac{b_0 z^2 + b_1 z + b_2}{z^2 + a_1 z + a_2}, \qquad (8)
$$

such that there are fewer equations than unknowns resulting in an infinite amount of solutions for b_0, b_1, b_2, a_1, a_2.

The important question we now address is how to efficiently search the 5-dimensional parameter space for a b_0, b_1, b_2, a_1, a_2 which will produce a stable solution if one exists. To begin, we derive the system of four linear equations which solves for b_0, b_1, b_2, a_1, a_2 by substituting (8) into (5) and then rearranging the equations to get:

$$
\begin{aligned}
&Re((C(s_1,z)Z_{in}(s_1) - A(s_1,z))z^2)b_0 \\
&+ Re((C(s_1,z)Z_{in}(s_1) - A(s_1,z))z)b_1 \\
&+ Re(C(s_1,z)Z_{in}(s_1) - A(s_1,z))b_2 \\
&- Re((B(s_1,z) - D(s_1,z)Z_{in}(s_1))z)a_1 \\
&- Re(B(s_1,z) - D(s_1,z)Z_{in}(s_1))a_2 \\
&= Re((B(s_1,z) - D(s_1,z)Z_{in}(s_1))z^2)\big|_{z=e^{s_1 T}}
\end{aligned}
$$

$$
\begin{aligned}
&Im((C(s_1,z)Z_{in}(s_1) - A(s_1,z))z^2)b_0 \\
&+ Im((C(s_1,z)Z_{in}(s_1) - A(s_1,z))z)b_1 \\
&+ Im(C(s_1,z)Z_{in}(s_1) - A(s_1,z))b_2 \\
&- Im((B(s_1,z) - D(s_1,z)Z_{in}(s_1))z)a_1 \\
&- Im(B(s_1,z) - D(s_1,z)Z_{in}(s_1))a_2 \\
&= Im((B(s_1,z) - D(s_1,z)Z_{in}(s_1))z^2)\big|_{z=e^{s_1 T}}
\end{aligned}
$$

$$
\begin{aligned}
&Re((C(s_2,z)Z_{in}(s_2) - A(s_2,z))z^2)b_0 \\
&+ Re((C(s_2,z)Z_{in}(s_2) - A(s_2,z))z)b_1 \\
&+ Re(C(s_2,z)Z_{in}(s_2) - A(s_2,z))b_2 \\
&- Re((B(s_2,z) - D(s_2,z)Z_{in}(s_2))z)a_1 \\
&- Re(B(s_2,z) - D(s_2,z)Z_{in}(s_2))a_2 \\
&= Re((B(s_2,z) - D(s_2,z)Z_{in}(s_2))z^2)\big|_{z=e^{s_2 T}}
\end{aligned}
$$

$$
\begin{aligned}
&Im((C(s_2,z)Z_{in}(s_2) - A(s_2,z))z^2)b_0 \\
&+ Im((C(s_2,z)Z_{in}(s_2) - A(s_2,z))z)b_1 \\
&+ Im(C(s_2,z)Z_{in}(s_2) - A(s_2,z))b_2 \\
&- Im((B(s_2,z) - D(s_2,z)Z_{in}(s_2))z)a_1 \\
&- Im(B(s_2,z) - D(s_2,z)Z_{in}(s_2))a_2 \\
&= Im((B(s_2,z) - D(s_2,z)Z_{in}(s_2))z^2)\big|_{z=e^{s_2 T}} . \qquad (9)
\end{aligned}
$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/OJCAS.2022.3174694, IEEE Open Journal of Circuits and Systems

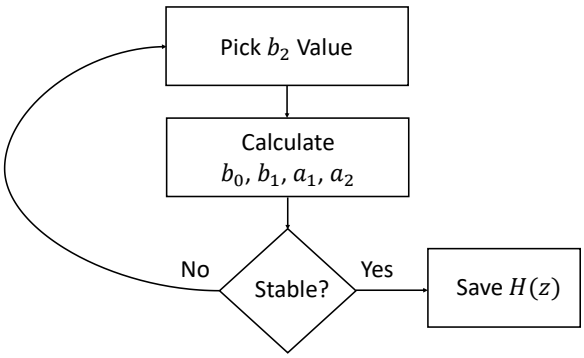

Fig. 3. Flowchart of a proposed search-based design procedure for digital impedance circuits with an external resistive source impedance to determine a stable solution if one exists with the constraint of two desired impedances $Z_{in}(s_1)$ and $Z_{in}(s_2)$ at the frequencies s_1 and s_2.

This system of four linear equations will allow us to choose a free variable from b_0, b_1, b_2, a_1, a_2. A valid choice which allows us to gain the flexibility of choosing digital filter coefficients for a stable solution is to set b_2 as the free variable and to write the parameters b_0, b_1, a_1, a_2 in the linear system of equations in terms of b_2. The motivation for choosing b_2 to become our free variable is as follows. Along the lines of the the stability analysis in [15] for resistive sources, if the Fig. 2 Thevenin source $V_s(s)$ in series with R_s is analyzed as a Norton source $I_s(s) = V_s(s)/R_s$ in parallel with R_s, then

$$\frac{V_{in}(s)}{R_{e2}} = I_s(s) + \frac{V_{in}^{\star}(s)H(z)e^{-s\tau}}{R_{io}+R_{dac}}\frac{(1-z^{-1})}{s}, f \qquad (10)$$

where $1/R_{e2} = 1/R_s + 1/(R_{dac}+R_{io}) + 1/R_{adc}$. Next, by taking the starred transform of both sides where $I_s^{\star}(s) \approx I_s(s)$ for frequencies below $1/(2T)$ of a bandlimited $I_s(s)$ without aliasing and then taking the z-transform of the entire equation, we are left with

$$\frac{V_{in}(z)}{R_{e2}} = I_s(z) + \frac{V_{in}(z)H(z)z^{-1}}{R_{io}+R_{dac}}, \qquad (11)$$

and the transfer function

$$G(z) = \frac{V_{in}(z)}{I_s(z)} = \frac{R_{e2}}{1 - R_{e2}H(z)z^{-1}/(R_{io}+R_{dac})}. \qquad (12)$$

From the denominator of (12), the poles of the system depicted in Fig. 2 must satisfy

$$z = \frac{R_{e2}}{R_{io}+R_{dac}}H(z) = \rho\, H(z), \qquad (13)$$

where $\rho = R_{e2}/(R_{io}+R_{dac})$, and the poles must be inside the unit circle for stability [16]. Now, Substituting (8) into (13) and rearranging the terms gives the following constraint equation for a stable system:

$$\begin{aligned} &z^3 + (a_1 - \rho b_0)z^2 + (a_2 - \rho b_1)z - \rho b_2 = 0 \\ &\quad \text{or} \qquad (z - z_{p1})(z - z_{p2})(z - z_{p3}) = 0 \quad . \end{aligned} \qquad (14)$$

For a stable solution to exist when considering resistive sources, the free variable parameter b_2 must be in the set of real numbers between $-1/\rho$ and $1/\rho$. This is because the constant term of our polynomial in (14) which is $-\rho b_2$ is also equal to the negative of the product of all the poles of our system, such that $-\rho b_2 = -z_{p1}z_{p2}z_{p3}$. Thus, for a stable solution to exist, the magnitude of the product of all the poles must be less than 1 such that

$$|z_{p1}z_{p2}z_{p3}| = |\rho b_2| < 1\,. \qquad (15)$$

Note, there may also be many unstable solutions in the set of real numbers between $b_2 = -1/\rho$ and $b_2 = 1/\rho$ in (15), but if a stable solution exists, then it must meet the criteria of $-1/\rho < b_2 < 1/\rho$ and we can completely disregard searching over the range $b_2 \geq |1/\rho|$ for a stable solution. Therefore, our method proposes a search from $b_2 = -1/\rho$ to $b_2 = 1/\rho$ with a desired numerical precision to determine a stable solution. If a stable solution exists within the desired numerical precision, then a valid b_2 will be found and then the calculations for the parameters b_0, b_1, a_1, a_2 follows from the linear system of equations. If no stable solution is found, either the numerical precision needs to be adjusted when searching b_2 values over the valid range between $b_2 = -1/\rho$ and $b_2 = 1/\rho$ or a stable solution doesn't exist for the system altogether.

The computational complexity of the search space for this proposed design algorithm will be $O(n)$ where n is the length of b_2 values to search over. The flowchart for this proposed design algorithm is shown in Fig. 3. This proposed design algorithm has a significantly reduced search space ($|b_2| \leq |1/\rho|$ rather than $|b_2| < \infty$) and reduced dimensionality (search over one parameter rather than five) from a naive brute force search method over an unconstrained search range for each parameter b_0, b_1, b_2, a_1, a_2.

IV. Results

An example design for a negative capacitance is used to demonstrate the effectiveness of the proposed algorithm. We use scaled parameters for higher operational frequencies from the measured data in Fig. 6 from [14] which includes $R_{adc} = 4700$, $R_{dac} = 1$, $R_{io} = 1000$, with faster sample time $T = 1.25$ ns, and correspondingly shorter latency $\tau = 1.25$ ns. Using our new proposed algorithm for a source resistance of $R_s = 50\ \Omega$ with $Z_{in}(s_1) = -163 + j799$ at $f_1 = 30$ MHz and $Z_{in}(s_2) = -221 + j572$ at $f_2 = 40$ MHz, we found a stable solution with digital filter parameters $b_0 = 13.62$, $b_1 = 12.57$, $b_2 = -21.04$, $a_1 = 2.11$, $a_2 = 2.05$ or

$$H(z) = \frac{13.62z^2 + 12.57z - 21.04}{z^2 + 2.11z + 2.05}, \qquad (16)$$

The design was simulated in the Simulink commercial simulator as shown in Fig. 4, and plotted as the solid curves of Fig. 5, along with circles showing the theoretical $Z_{in}(s)$ from (5). The theoretical poles for this example were stable with $z_{p1} = 0.9957$, $z_{p2} = 0.9957$, and $z_{p3} = 0.9995$. The time-domain simulation confirmed the stability and converged appropriately. The simulated values of $Z_{in}(s_1)$ and $Z_{in}(s_2)$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/OJCAS.2022.3174694, IEEE Open Journal of Circuits and Systems

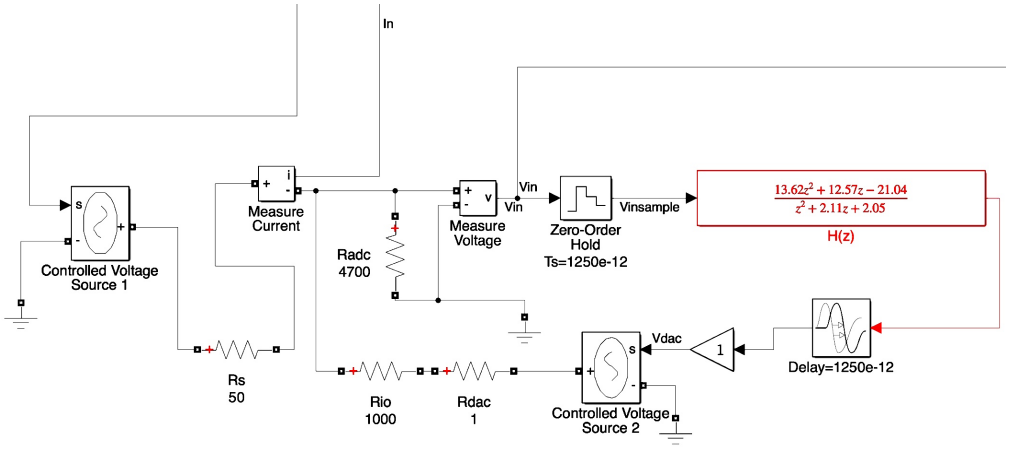

Fig. 4. An example simulink simulation schematic for $H(z) = \frac{13.62z^2+12.57z-21.04}{z^2+2.11z+2.05}$, with R_s, R_{adc}, R_{dac}, and R_{io} shown. Sample time is $T = 1.25$ ns, and latency is $\tau = 1.25$ ns.

were $-153 + j806$ and $-213 + j588$ compared to the theoretical values of $-163 + j799$ and $-221 + j572$ respectively. Therefore, both the real and imaginary parts of the simulated values of $Z_{in}(s_1)$ and $Z_{in}(s_2)$ are very close to matching their theoretical values even on the steepest part of the slope in Fig. 5. We also note that the new design procedure is based on a general source impedance $Z_s(s)$ as seen in (1) – (3), and that the well-controlled resistive source resistance R_s was chosen for a straightforward exposition of the new design procedure. In addition, the digital implementation of $H(z)$ offers the potential for adaptive control of time-varying source impedances that may occur in mobile antennas. Furthermore, applications such as the non-Foster improvement of electrically-small antenna impedance bandwidths from 1% to 5% would suggest choosing design frequencies closer together than the approximate 29% bandwidth of s_1 and s_2 in the example above. Lastly, the maximum frequency in Fig. 5 for the digital impedance circuit is the Nyquist limit of half the ADC and DAC clock frequency $0.5/T = 400$ MHz.

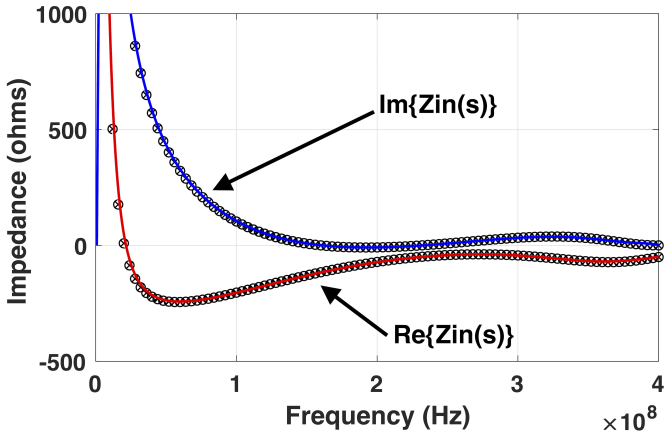

Fig. 5. Digital impedance $Z_{in}(s)$ simulation (solid curves) and theory (points) of a digital non-Foster circuit with parameters $R_{adc} = 4700$, $R_{dac} = 1$, $R_{io} = 1000$, $Rs = 50$, sample time $T = 1.25$ ns, latency $\tau = 1.25$ ns, $Z_{in}(s_1) = -163 + j799$ at $f_1 = 30$ MHz, and $Z_{in}(s_2) = -221 + j572$ at $f_2 = 40$ MHz, with $b_0 = 13.62$, $b_1 = 12.57$, $b_2 = -21.04$, $a_1 = 2.11$, $a_2 = 2.05$. Lower red curve is $Re\{Z_{in}(s)\}$ and upper blue curve is $Im\{Z_{in}(s)\}$.

V. Conclusion

In conclusion, this paper demonstrates a new algorithm for the design of digital impedance circuits which can effectively produce a stable solution, with excellent impedance accuracy at the two design frequencies for a resistive source impedance. The generalization of the Non-Foster digital impedance theoretical analysis opens up new approaches for effective design methods of stable digital impedance circuits. Furthermore, the approach taken in the overall design method in and of itself may be useful in solving other related engineering design problems.

Acknowledgment

This material is based upon work supported by the National Science Foundation under Grant No. 1731675.

References

[1] R. M. Foster, "A reactance theorem," *Bell Syst. Tech. J.*, vol. 3, pp. 259–267, 1924.

[2] M. C. Tang, T. Shi, and R. W. Ziolkowski, "Electrically small, broadside radiating Huygens source antenna augmented with internal non-Foster elements to increase its bandwidth," *IEEE Antennas Wireless Propag. Lett.*, vol. 16, pp. 712–715, 2017.

[3] N. Zhu and R. W. Ziolkowski, "Active metamaterial-inspired broadbandwidth, efficient, electrically small antennas," *IEEE Antennas Wireless Propag. Lett.*, vol. 10, pp. 1582–1585, 2011.

[4] S. E. Sussman-Fort and R. M. Rudish, "Non-Foster impedance matching of electrically-small antennas," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 8, pp. 2230–2241, Aug. 2009.

[5] D. Gregoire, C. White, and J. Colburn, "Wideband artificial magnetic conductors loaded with non–Foster negative inductors," *IEEE Antennas Wireless Propag. Lett.*, vol. 10, pp. 1586–1589, 2011.

[6] A. Nagulu, M. Tymchenko, A. Alù, and H. Krishnaswamy, "Ultra compact, ultra wideband, DC-1GHz CMOS circulator based on quasi-electrostatic wave propagation in commutated switched capacitor networks," in *2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2020, pp. 55–58.

[7] S. Hrabar, "First ten years of active metamaterial structures with "negative" elements," *European Physical Journal Applied Metamaterials*, vol. 5, p. 9, 2018.

[8] S. Hrabar, I. Krois, I. Bonic, and A. Kiricenko, "Negative capacitor paves

the way to ultra-broadband metamaterials," *Appl. Phys. Lett.*, vol. 99, no. 25, p. 254103, 2011.

[9] S. D. Stearns, "Stable band-pass non-Foster circuits," in *2015 IEEE Int. Symp. on Antennas and Propagation USNC/URSI Nat. Radio Science Meeting*, Jul. 2015, pp. 1386–1387.

[10] S. Stearns, "Non-Foster circuits and stability theory," in *2011 IEEE Antennas and Propag. Soc. Int. Symp. (APSURSI)*, Jul. 2011, pp. 1942–1945.

[11] F. Tofigh and R. W. Ziolkowski, "A stable floating non-Foster circuit," in *2020 4th Australian Microwave Symposium (AMS)*, 2020, pp. 1–2.

[12] E. Ugarte-Munoz, S. Hrabar, D. Segovia-Vargas, and A. Kiricenko, "Stability of non-Foster reactive elements for use in active metamaterials and antennas," *IEEE Trans. Antennas Propag.*, vol. 60, no. 7, pp. 3490–3494, Jul. 2012.

[13] T. P. Weldon, P. J. Kehoe, and K. K. Steer, "Bilinear transform approach for wideband digital non-Foster matching of electrically-small antennas," in *2018 IEEE Antennas and Propag. Soc. Int. Symp. (APSURSI)*, Jul. 2018, pp. 945–946.

[14] K. A. Hecht, C. G. Daniel, and T. P. Weldon, "Effect of external source impedance on the input impedance of digital impedance circuits," in *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2020, pp. 1–5.

[15] P. J. Kehoe, K. K. Steer, and T. P. Weldon, "Stability analysis and measurement of RC and RL digital non-Foster circuits with latency," in *IEEE SoutheastCon 2017*, Mar. 2017, pp. 1–4.

[16] C. Phillips and H. Nagle, *Digital Control System Analysis and Design*. Prentice-Hall, 1990.

Christopher G. Daniel Jr. (Student Member, IEEE) received the B.S. degree in computer engineering and physics in 2020 along with the M.S. degree in electrical engineering and applied physics in 2021 from The University of North Carolina at Charlotte. In 2021, he enrolled at Stanford University where he is currently pursing his Ph.D. degree in applied physics. He has previously conducted theoretical research in many different areas of engineering and physics which include digital impedance circuits, non-Foster circuits, age-of-information, quantum computing, quantum optics, quantum cosmology, and quantum gravity. His current research interests are in theoretical engineering and applied physics for quantum technology.

Thomas P. Weldon (Senior Member, IEEE) received the B.S. degree in electrical engineering in 1979 from Penn State, University Park, PA, the M.Eng. in engineering science in 1989 from Penn State, Great Valley, PA, and the Ph.D. in electrical engineering in 1995 from Penn State, University Park, PA. From 1979 to 1982 he designed portable radios at Motorola in Plantation, FL, from 1982 to 1984 he designed custom radio frequency and digital circuits for Alpha Industries (now Skyworks), and from 1984 to 1990 he designed digital signal processing systems, microwave systems, millimeter-wave receivers, and electronic warfare systems while at American Electronic Laboratories (now Cobham Advanced Electronic Solutions). After completing his Ph.D, he joined the Department of Electrical and Computer Engineering at The University of North Carolina at Charlotte in 1995, where he is currently an Associate Professor. He has authored/coauthored more than 80 articles and holds 11 patents. His present research areas are in digital impedance circuits, non-Foster circuits, metamaterials, and applications of antenna theory to gravitational physics.