Conference Report

Report on the Design Automation Conference (DAC 2021)

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Welcome to the 58th Design Automation Conference (DAC). DAC was held at the Moscone Center West, San Francisco, CA, USA, on December 5–9, 2021, and it was great to be back in the beautiful city by the bay for a live event. This year, the DAC Executive Committee experienced many firsts with respect to planning the conference. It was the first DAC to be rescheduled from its normal summer timeframe to December due to COVID-19. It was the first DAC to colocate with both the RISC-V Summit and SEMICON West. And it was the first DAC to go hybrid with both a live and virtual component.

The technical program began each day with a well-attended opening session that includes a keynote. Monday's keynote was given by Jeff Dean, Senior Vice President at Google Research, who provided a history of the growth in AI with a focus on the potential for AI to become an integral part of the solution for several new problems within the electronics and systems industry. Bill Dally, Chief Scientist for Nvidia, presented Tuesday's keynote focused on three trajectories: 1) how GPUs can accelerate EDA; 2) how GPUs enable deep learning; and 3) how deep learning can accelerate or enhance EDA. Wednesday's keynote was given by Joe Costello who currently serves as the Executive Chairman at Arrikto, Metrics, and KWIKBIT. Joe was one of the visionaries in the early years of EDA when he served as the first president and CEO of Cadence Design Systems. His talk was titled "When the Winds of Change Blow, Some People Build Walls and Others Build Windmills" where he offered a simple but powerful message to the EDA community: do not fight a macro trend—ride it. Finally, Thursday's keynote was given by Kurt Keutzer, Professor at the Graduate School in EECS, University of California. Kurt successfully brought the key points from this year's keynotes together while expanding the message on how the EDA community can bring its very sophisticated set of skills, honed by 50 years of keeping up with Moore's law, to the preeminently important problems of optimizing the design and implementation of deep learning models.

Spirits were high from an industry perspective where three invited talks provided an optimistic analysis of today's EDA industry. This included talks from Charles Shi from Needham & Company on Sunday, Joe Sawicki from Siemens EDA on Monday, and Jay Vleeschhouwer from Griffin Securities on Tuesday who predicted an impressive 10% growth for EDA in 2021.

The DAC Pavilion, located on the exhibition floor, provided a packed agenda with a constant flow of traffic. This included the following.

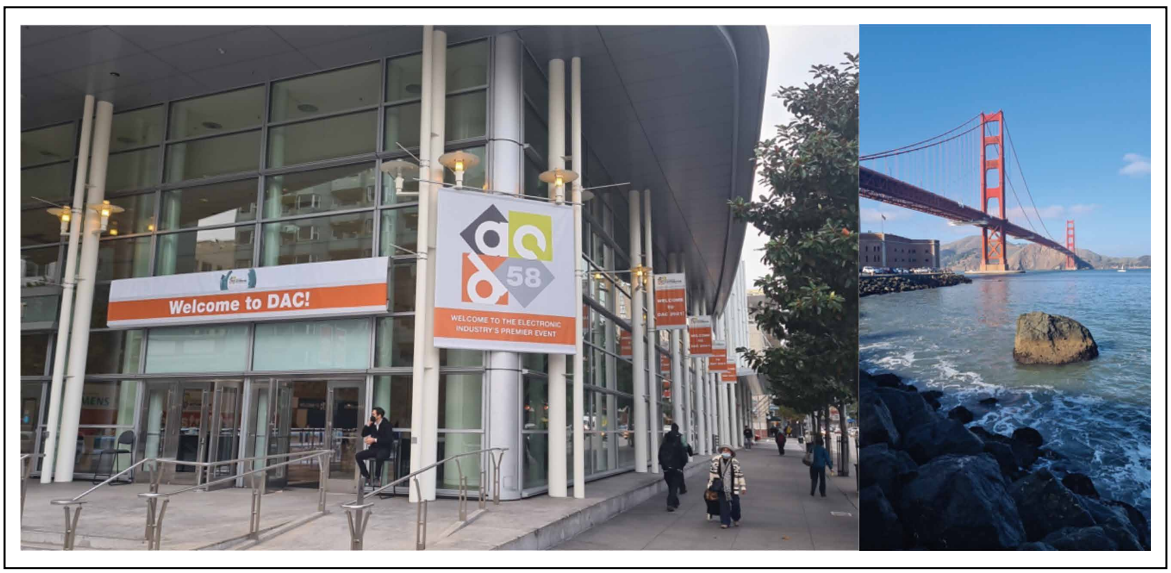
- Three SKYTalks (short keynotes) by William Chappell, CTO Azure Global and Vice President

Digital Object Identifier 10.1109/MDAT.2021.3138609
Date of current version: 9 February 2022.

of Mission Systems at Microsoft; Kailash Gopalakrishnan, IBM Fellow and Senior Manager Accelerator Architectures and Machine Learning; Sam Naffziger, AMD Senior Vice President, Corporate Fellow, and Product Technology Architect.
- Four TechTalks by Serge Leef, DARPA Program Manager, Microsystems Technology Office; Neeraj Kaul, Vice President of Engineering, Digital Design Group, Synopsys; Michael Jackson, Corporate Vice President Research and Development, Cadence Design Systems; Steve Roddy, Vice President, Machine Learning Group at Arm.
- Four Pavilion panels.

DAC 2021 received a total of 914 research paper submissions across six topic areas—autonomous systems, artificial intelligence and machine learning (AI/ML), design, electronic design automation (EDA), embedded systems and software, and security. Although the number of submissions were slightly down from 2020, it was still healthy—with a large number of submissions in the new quantum computing track and significant growth in submissions to the analog design, simulation, verification and test, as well as near-memory and in-memory computing tracks. In keeping with recent trends, the AI/ML and EDA tracks garnered the largest percentage of submissions among all tracks. 40% of the submissions were from North America with another 40% from Asia, and the remaining 20% from Europe, thus reaffirming the fact that DAC remains a premiere international conference with a truly global reach across the worldwide research community. The technical program committee (TPC) consisted of 347 experts along with 62 more serving as subcommittee chairs/co-chairs across the 31 subcommittees spanning 26 tracks. A diverse and inclusive TPC consisting of 12% women, 22% from industry, and 33% from outside North America facilitated a robust paper review and selection process that captured a wide range of reviewer perspectives. Author-flagged and institutional conflicts-of-interest (COIs) were thoroughly checked and strictly enforced to ensure an unbiased selection process of double-blind manuscripts. A virtual paper selection meeting—a first time for DAC—led by subcommittee chair/co-chairs via offline discussions and online live sessions to accommodate the wide-ranging time zones of subcommittee members, resulted in 215 papers being selected—representing a 23% acceptance rate. The average number of reviews per paper was 3.7, with each paper receiving at least three reviews. The selected papers were presented in 45 sessions—with 40% presented in-person at the conference held on December 7–9, 2021, in San Francisco, CA, USA, and the remaining delivered through the on-demand virtual platform to conference registrants who could not attend the conference in person due to the ongoing global pandemic.

The DAC 2021 Best Paper has been awarded to "Gemmini: Enabling Systematic Deep-Learning Architecture Evaluation via Full-Stack Integration," coauthored by a group of researchers from



the University of California at Berkeley jointly with a coauthor from MIT. Congratulations to the Best Paper authors! It is a distinctive award since DAC has only one best paper across all DAC subtopics (around 30). The article was selected out of a total of five candidates. The other four were: "Architecture-Aware Precision Tuning with Multiple Number Representation Systems," "A Resource Binding Approach to Logic Obfuscation," "Distilling Arbitration Logic from Traces Using Machine Learning: A Case Study on NoC," and "DNN-Opt: An RL Inspired Optimization for Analog Circuit Sizing Using Deep Neural Networks."

All of them are marked in the DAC Program as "Best Paper Candidate," which is a distinction on its own. We want to congratulate all authors to their achievements. Our thanks also go to the members of the best paper selection committee, a group of high-profile experts from industry and academia, who have selected these papers in a multistage, multiweek process considering both the printer-ready versions of the respective papers as well as the accompanying video presentations.

We look forward to welcome you at DAC'59 to be held on July 10–14, again in San Francisco! ■

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