

# Modeling Simplification for Thermal Mechanical Analysis of High Density Chip-to-Substrate Connections

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*Finite element modeling (FEM) is an important component in the design of reliable chip-to-substrate connections. However, FEM can quickly become complex as the number of input/output connections increases. Three-dimensional (3D) chip-substrate models are usually simplified where only portions of the chip-substrate structure is considered in order to conserve computer resources and time. Chip symmetry is often used to simplify the models from full-chip structures to quarter or octant models. Recently, an even simpler 3D model, general plane deformation (GPD) slice model, has been used to characterize the properties of the full-chip and local regions on the structures, such as in the structures for solder ball fatigue. In this study, the accuracy of the GPD model is examined by comparing the mechanical behavior of a flip-chip, copper pillar package from various full and partial chip models to that of the GDP model. In addition, it is shown that the GPD model can be further simplified to a half-GPD model by using the symmetry plane in the middle of the slice and choosing the proper boundary conditions. The number of nodes required for each model and the accuracy of the different FEM models are compared. Analysis of the maximum stress in the silicon chip shows that the full-chip model, quarter model, and octant model all convergence to the same result. However, the GPD and half-GPD models, with the previously used boundary conditions, converge to a different stress values from that of the full-chip models. The error in the GPD models for small, 36 I/O package was 4.7% compared to the more complete, full-chip FEM models. The displacement error in the GPD models was more than 50%, compared to the full-chip models, and increased with larger structures. The high displacement error of the GPD models was due to the ordinarily used boundary conditions which neglect the effect from adjacent I/O on the sidewall of the GPD slice. An optimization equation is proposed to account for the spatial variation in the stress on the GPD sidewall. The GPD displacement error was reduced from 50% to 3.3% for the 36 pillar array. [DOI: 10.1115/1.4005289]*

## Introduction

In chip-to-substrate connections, the flip-chip connection has become important in high-performance packages due to its high density and low inductance, compared to wire bonding. Flip-chip normally uses solder as the connecting material, however, it suffers from mechanical fatigue due to the rigid nature of silicon and the substrate, and the mismatch in thermal expansion between the silicon and package. Flip-chip connections using copper pillars with solder caps [1–4] and all-copper pillars [5–7] have been demonstrated recently to improve the performance and reliability [8]. All-copper-connections use high aspect ratio (height-to-width) pillars rather than solder balls [9] and they are simpler to process compared to copper pillars with solder caps. The high aspect ratio is critical for mechanical integrity in copper pillars because they are stiffer than solder. Therefore, the all-copper-connection was selected in this work to investigate the modeling aspects and simplifications in high density flip-chip connections.

Improvements in the chip-to-substrate connection density have been made in recent years so as to enable higher system performance driven by the scaling of transistors. According to the International Technology Roadmap for Semiconductors [8], the maximum package pin count for a high-performance FPGA in 2011 is 5094 with a chip area of 804 mm<sup>2</sup>, which gives a maximum I/O pitch

of 397  $\mu\text{m}$ . As the size and the shape of connections are decreasing and the number of I/O is increasing, the mechanical reliability becomes more important. The stress induced by thermal mismatch between the chip and the substrate can cause mechanical failures, especially within the connections bearing the maximum stress and deformation.

Finite element method (FEM) can be used to characterize, compare, and predict the performance and reliability of the chip-to-substrate connections. Normally, three kinds of three-dimension (3D) models are used in FEM analysis to characterize chip-substrate I/O connections: the total-chip model [10], the quarter-chip model [10–14], and the octant-chip model [15,16]. These 3D models have higher accuracy but require larger degrees of freedom (DOF) and computational facilities than the two dimensional (2D) models [17]. The quarter-chip model and the octant-chip model take advantage of symmetry planes to reduce the computation time and lower the number of DOFs in the model. Thus, the 3D model, especially the octant model, is an attractive approach to capturing the mechanical behavior of chip packages while maintaining high accuracy [13]. However, as packages become ever larger, more efficient models than the octant model are needed. On the one hand, the complex shape of I/O in chip packages creates high thermal stress gradients at the corners of the components. These high gradients require a very high density of mesh elements at these critical corners. On the other hand, the large scale of the chip and the high number of I/O per package require an enormous number of DOF to describe the general performance. Thus, the octant model needs to be simplified while at

Contributed by the Electronic and Photonic Packaging Division of ASME for publication in the JOURNAL OF ELECTRONIC PACKAGING. Manuscript received May 28, 2010; final manuscript received August 24, 2011; published online December 9, 2011. Assoc. Editor: Bongtae Han.

the same time keeping the ability to characterize both the general deformation of the chip and the local stress at the chip corner with high level accuracy.

One of the ways to simplify the 3D model is by coupling models [10,17,18]. The thermal mechanical results are obtained by coupling the general field chip model and the local deformation connection model. In the general field model, connections are simplified into one-dimensional (1D) beams [18,19]. A rigorous equivalent model library was proposed [18] and an original and general optimization methodology was developed to find the simplified and equivalent model [19].

The beam deformation is obtained from the local deformation connection model. In the local deformation model, the connection deformation relates the location of the connections in the chip. The 3D model used for high density connections is built by iterating the results of the local connection model into the general model and loading the expansion results of the general connection into the local model as the boundary conditions. This avoids having to use a massive number of DOF. Accordingly, the computation time is shortened. However, these coupling model methods are too complex for repeated iterations. In addition, the accuracy of the method needs to be improved.

Another way of the simplifying the 3D model is by cutting the octant model into slices. A slice model with three or four I/O was generated to examine the issues within the local connections [13,16,19,20]. This slice model is based on an assumption that the chip is infinitely larger than the size of the pillar. Thus, the local stress can be obtained by using periodic boundary conditions. However, the accuracy of the model cannot be guaranteed and the model cannot express general deformation information. Therefore, a general plane deformation (GPD) slice model originating from the chip center to the edge of the device along the diagonal line of the chip which includes the I/O was put forward recently [6]. This GPD slice model conserves nodes, and the local high-gradient corners can be solved. The general chip deformation can be determined at the same time. However, the accuracy of the GPD model is not evident and the loadings on the side-walls of the slice may not be adequate for making the GPD slice representative of the total-chip.

A second simplification method was used to simplify the octant model to reduce the DOF and computation time while maintaining accuracy of the 3D models. The GPD model was cut in half by using the symmetry boundary condition along the diagonal plane down the center of the slice. In this work, the accuracy of the GPD model and half-GPD has been studied by comparing the maximum thermal mechanical stress and the maximum deformation in the three 3D models with the GPD and half-GPD models. It was found that a large error occurred in the maximum deformation in the GPD models, although only a small error occurred in the maximum stress within the chip. A new, simple method is put forward to optimize the deformation by refining the loading on the side-walls of GPD or half-GPD model. The method was verified even in the case of a large number of I/O. It was found that the half-GPD had the fewest DOFs and computation time. Finally, it was concluded that the half-GPD is the most effective, 3D general field model with the lowest number of DOF while maintaining adequate accuracy.

## Finite Element Model

The major thermal mechanical issue in high density, I/O chip packages relate to the stress caused by thermal cycling of the component and resulting reliability concerns. The mismatch between the thermal expansion of the silicon chip and the substrate can cause bending, deformation, and crack failures. The thermal stress, especially the stress induced in the interface of the silicon chip by the bending connections, needs to be evaluated. In this work, three 3D models: the total-chip model, the quarter-chip, the octant-chip models, and a GPD and half-GPD slice model were compared. The maximum stress at the interface of the chip and

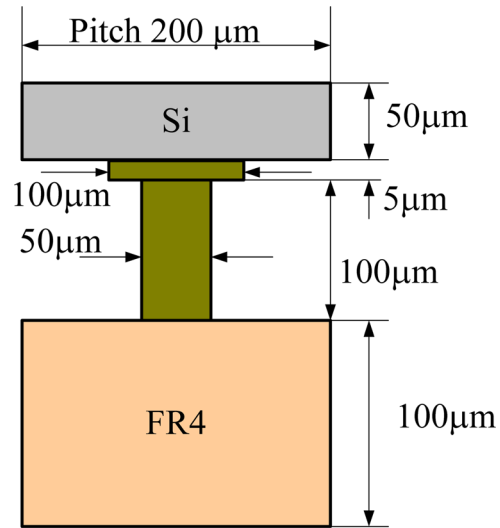


Fig. 1 Specifications of a unit of I/O

the I/O connection and the maximum deformation of the components have been characterized and compared across the five models. The GPD and half-GPD models were optimized by refining the boundary conditions on the slice side-walls.

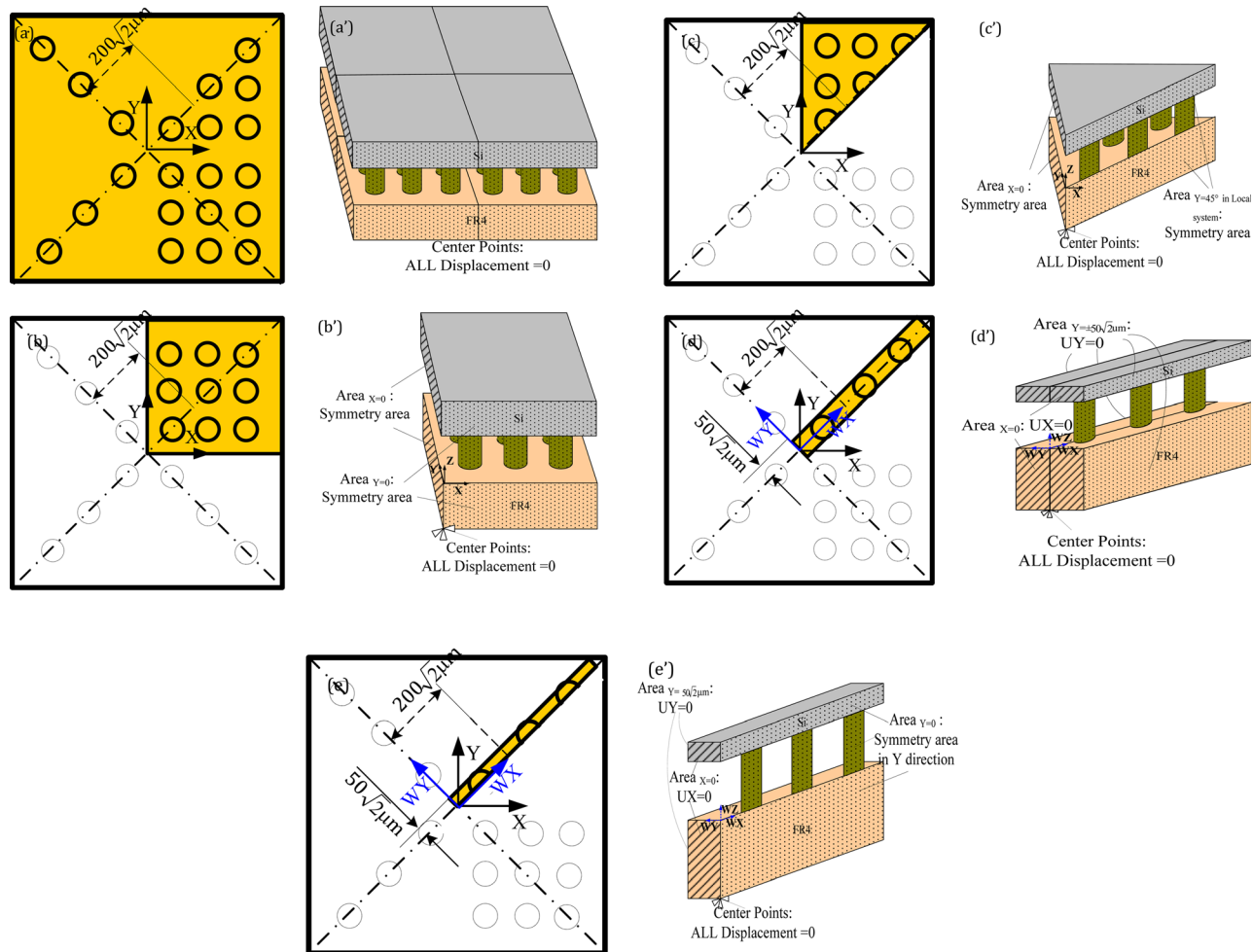
Five 3D models were built to examine a silicon chip on FR4 substrate structure with  $6 \times 6$  all-copper, I/O pillars (36 I/Os). The pitch size of each model was held constant at  $200 \mu\text{m}$ , as shown in Fig. 1. The thickness of the chip, pillars, and substrate was  $50 \mu\text{m}$ ,  $100 \mu\text{m}$ , and  $100 \mu\text{m}$ , respectively. The copper pillar was terminated on a  $5 \mu\text{m}$  thick copper pad on the silicon surface. The copper pad represents the I/O connection to the chip which helps distribute the stress imposed on the chip by the pillars. The linear and nonlinear elastic properties of the materials were used in the models. The silicon and copper were both taken as isotropic materials while the FR4 substrate was anisotropic, as shown in Table 1.

The configuration of the five models and their respective boundary conditions are listed in Fig. 2. There are 36 pillars in the total-chip model, 9 pillars in the quarter model, and 4.5 pillars in the octant model (see Figs. 2(a)–2(c)). The GPD model is a structure extending out from the center of the chip to the corner of the chip and contains 3 pillars as shown in Fig. 2(d). The half-GPD model requires only  $3/2$  pillars to capture the mechanical information of the 36 pillars array, as shown in Fig. 2(e). The pillar pitch along the slice diagonal is  $200\sqrt{2} \mu\text{m}$ , as shown in Fig. 2(d). The width of the slice is  $100\sqrt{2} \mu\text{m}$  for the full GPD model and  $50\sqrt{2} \mu\text{m}$  for the half-slice GPD model.

In the total-chip model, the displacement of the center nodes inside of the circle (radius  $< 40 \mu\text{m}$ ) are fixed at zero in all directions, and the other faces are free to move, as shown in Fig. 2(a'). The nodes are located in the center of the FR4 board at the bottom. The purpose of these boundary conditions is to prevent the model from moving or rotating, while allowing the model to freely expanding in all directions. Fig. 2(b') shows boundary conditions for the quarter model. The displacements of the center nodes inside the circle are fixed at zero in all directions, just as in Fig. 2(a') for the total-chip model. The area of the XZ and YZ

Table 1 Linear thermoelastic properties for materials at  $100^\circ\text{C}$

Material	Tensile modulus, E(GPa)	$\alpha(\text{ppm}/^\circ\text{C})$	Poisson's ratio, $\nu$
Si [21]	140.0	2.8	0.23
Cu [22]	123.8	16.0	0.34
FR4 Board	$E_{XY}: 20.45 E_Z: 1.16$	16.086.5	$\nu_{YZ} \nu_{ZX}: 0.1425 \nu_{XY}: 0.002$



**Fig. 2 Models and relative boundary conditions (a) Total-chip model; (a') Boundary conditions for the total-chip model; (b) Quarter model; (b') Boundary conditions for the quarter model; (c) Octant model; (c') Boundary conditions for the octant model; (d) GPD model; (d') Boundary conditions for the GPD model; (e) Half-GPD model; and (e') Boundary conditions for the half-GPD model**

planes are set to be symmetry areas in each of the normal directions. A schematic diagram of the boundary conditions of the octant model is shown in Fig. 2(c'), where the displacement of the center nodes in the circle are fixed at zero in all directions. In addition, the deformation of the areas defined by the YZ plane ( $X=0$ ) in Cartesian coordinates and the 45 deg YZ plane in cylindrical coordinates in the work plane are both symmetrical in the normal directions to the symmetry planes, respectively. In the GPD and half-GPD model, the boundary conditions are loaded in the work plane (WP). WP is obtained by rotating the coordinates ( $X$  and  $Y$ ) 45 deg counter-clockwise to the coordinates ( $WX$  and  $WY$ ) (see Figs. 2(d) and 2(e)). Labels for the boundary conditions in Figs. 2(d) and 2(d') are the values in the WP. In addition to fixing the center nodes in the side, the area of the ZY plane at  $WX=0$  and the displacement of the sidewalls in the GPD model are assumed to be zero in the  $WY$  direction (see Figs. 2(d) and 2(d')). Thus, the slice is free to expand in the  $X$  and  $Z$  directions under thermal loading. In the half-GPD model, a new symmetry plane is used where  $WY=0$  is defined in normal direction to the  $WX$ - $Z$  plane for the GPD model. The boundary conditions are shown in Fig. 2(e').

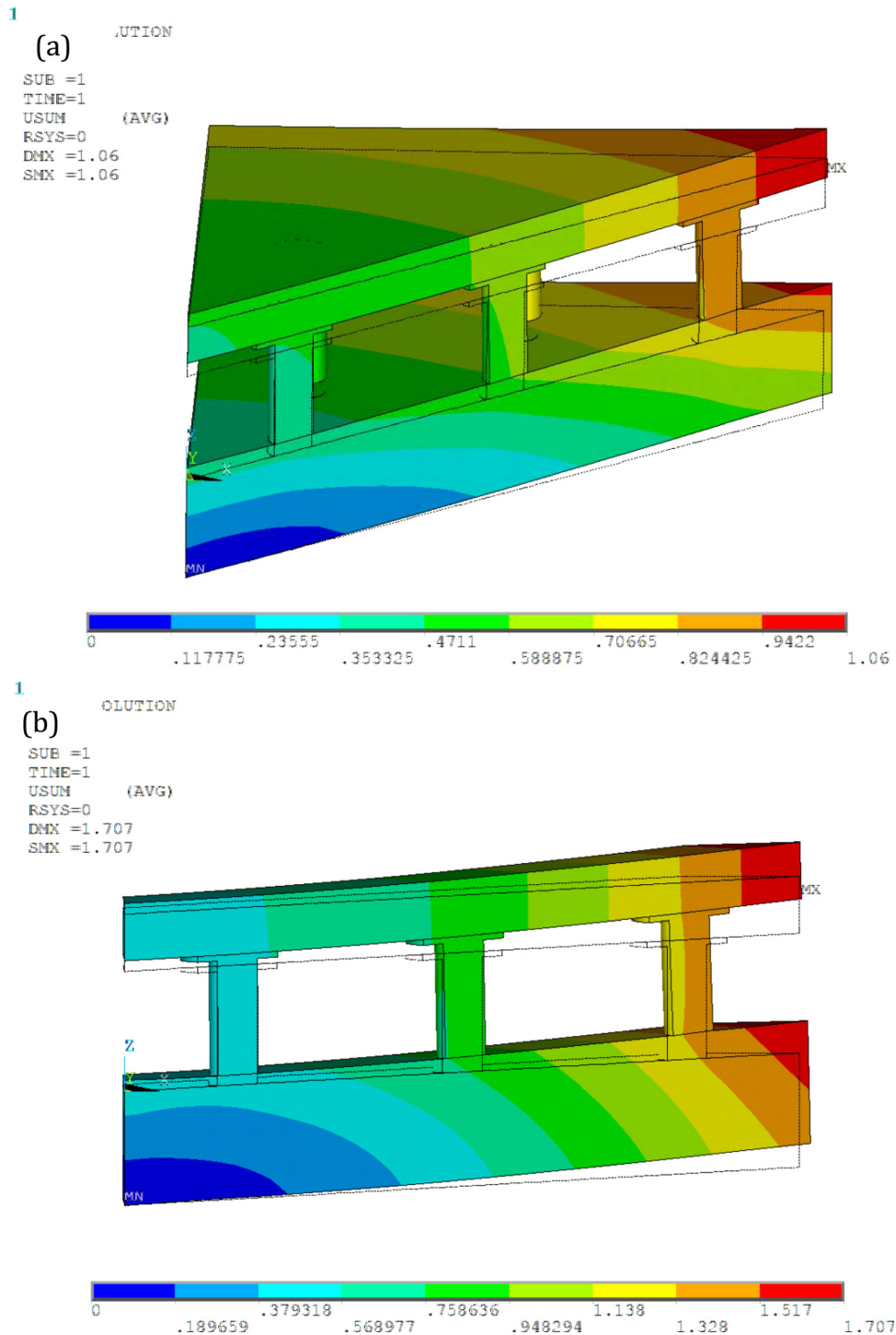
## Results and Discussion

In this modeling, 70 °C was used as the reference temperature because it is the temperature at which the bonding process takes

place. The maximum von Mises stress generated in the silicon chip at 100 °C was investigated and compared for each of the five models.

The FR4 substrate expands a greater amount than the silicon chip at elevated temperature causing the chip to bend upward, especially at the end of the diagonal line. Figs. 3(a) and 4(a) show the vector sum of the displacement (USUM) and Von Mises stress for the nodal contour solutions for the octant model. Figs. 3(b) and 4(b) show the USUM and Von Mises stress for the nodal contour solutions of the half-GPD model. The USUM and the stress distribution of the half-GPD model are similar to that of the full GPD model.

The maximum stress in the silicon chip is important because the stress affects the mechanical reliability of the chip. Figure 5 is a plot of the maximum stress in the chip at 100 °C as a function of the number of nodes used (Solid 45, ANSYS) in each of the five models. The maximum stress converges to 42 MPa when the number of nodes approaches 1,558,070 in the full-chip model, 711,449 in the quarter model, and 357,329 in the octant model. However, the stress converges to a different value, 40 MPa in the GPD and half-GPD model. It required only 443,030 nodes in the GPD model and 141,070 nodes in the half-GPD model for convergence. In terms of computation time, a comparison was made using a workstation with an Intel core2 CPU and 12 GB RAM. The computation time was 25 h for the full-chip model, 5 h for the quarter model, 1 h for the octant model, 30 min for the GPD model, and



**Fig. 3 The vector sum of displacement result of (a) the octant model; and (b) the half-GPD model ( $\mu\text{m}$ )**

10 min for the half-GPD model to obtain mesh element independent results with an error less than 1%, as shown in Fig. 5. In addition to computation time being different, it is particularly curious that the GPD model converges to a lower stress value, 40.2 MPa versus 42.5 MPa. The difference in stress between the GPD models and others is about 4.7% for the 36 pillar device. The difference in the vector sum of displacement between models, as shown in Fig. 3, is quite different.

Table 2 is a list of the vector sum of displacement of the half-GPD model and their optimization, where  $U_o$  is USUM of the half-GPD model before optimization. The difference between USUM of the GPD models compared to the other three models is

61.0% for the 36 I/O device, which is unacceptable. This difference is rarely stated in previous papers using the GPD model.

The source of the difference in stress and USUM between the full/quarter/octant model and the GPD models was considered. Analysis of the boundary conditions in Fig. 2 shows that the critical difference in the GPD model is the loading on the side-walls. In the GPD and half-GPD models, the nonhomogenous effect of the components adjacent to the GPD is ignored. That is, the side-walls of the GPD models are assumed to act like a homogenous, uniform plane whereas the actual effect has spatially varying conditions due to the presence and location of the copper pillars on the chip surface. Therefore, this spatially varying effect of the



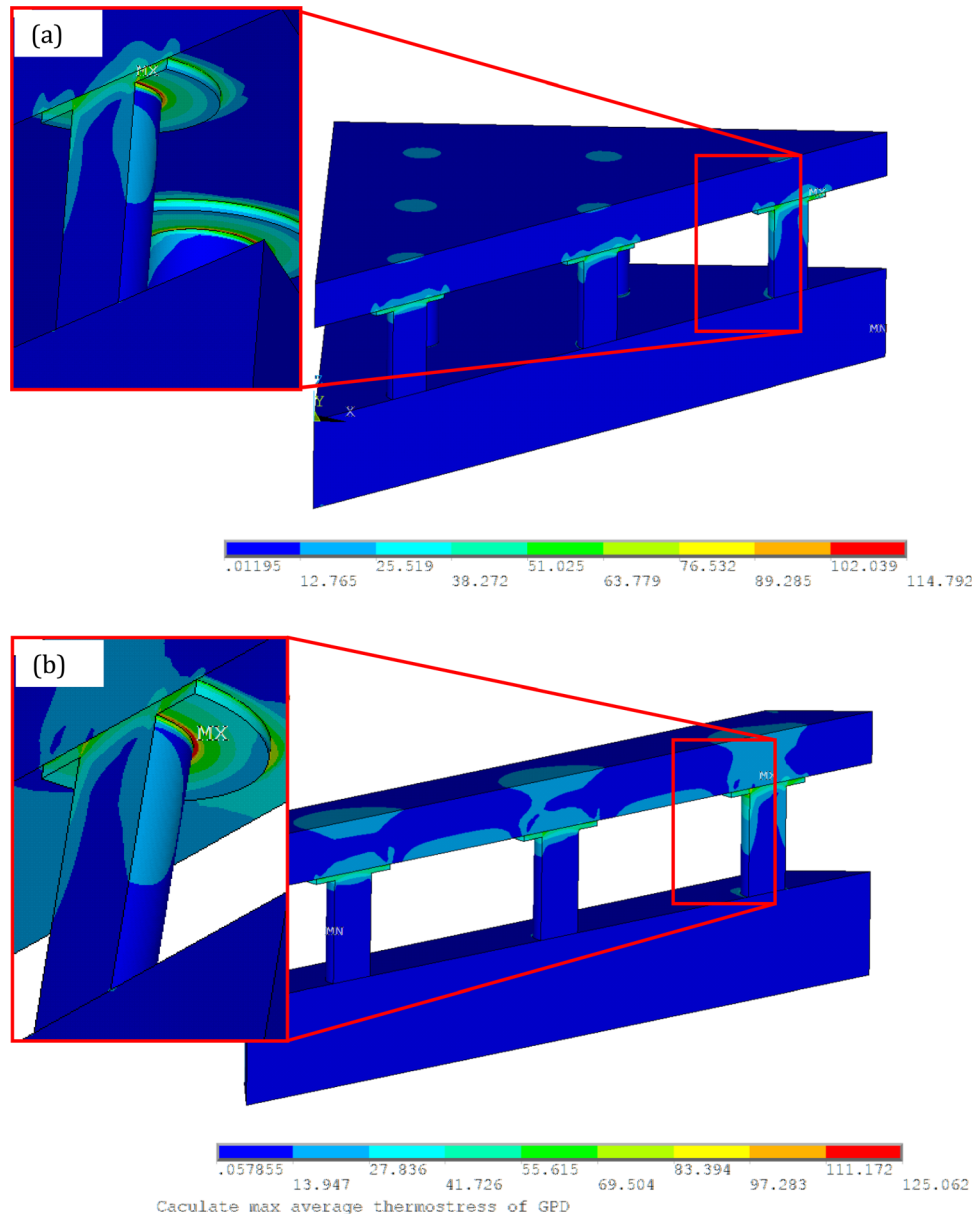


Fig. 4 The Von Mises stress contour plot of (a) the octant model; and (b) the half-GPD model (MPa)

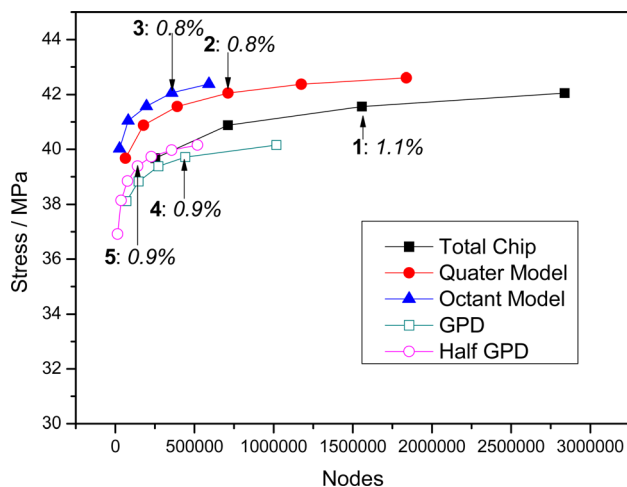


Fig. 5 Element independence curves

adjacent pillars needs to be considered and accounted for. The GPD and half-GPD models have a larger vector sum displacement if the loading is changed by altering the boundary conditions shown in Fig. 2.

USUM of the half-GPD model (Table 2) is  $1.707 \mu\text{m}$  compared to the USUM of the octant model at  $1.060 \mu\text{m}$ . This 61.0% error shows that the general plane deformation assumption does not accurately reflect reality. Moreover, this error becomes more significant and higher in magnitude for higher I/O models. The error in  $U_0$  increased from 61.0% to 96.3% when the number of I/O pillars was increased from 36 to 900.

Analysis of the USUM showed that the difference in value between the half-GPD model and octant model was mainly caused by the difference in component displacement in the Z direction. This means that the structures just outside of the GPD slice, especially those parts neighboring the GPD slice, help to deflect the silicon chip upward or downward. Previously, it was thought that the effect of the material just outside of the GPD was mainly in WY because the components are all free to expand in the Z direction (see Fig. 2(e')). However, each of the pillars is stretched by

**Table 2 Vector sum of displacement in the half-GPD model and the optimization**

I/O scale number	Pillars in GPD model	$U_r$ ( $\mu\text{m}$ )	$U_0$ ( $\mu\text{m}$ )	Error in $U_0$	$U_1$ ( $\mu\text{m}$ )	Error in $U_1$
$6 \times 6$	3	1.060	1.707	61.0%	1.024	3.3%
$12 \times 12$	6	3.231	6.014	86.1%	3.280	1.5%
$18 \times 18$	9	6.928	13.319	92.2%	7.050	1.7%
$30 \times 30$	15	18.791	36.885	96.3%	19.08	1.5%

FR4 substrate and silicon chip to a different extent, as shown in Fig. 6. The neighboring pillars act together to support the pillars in the GPD slice holding the silicon chip to the FR4 substrate. If these neighboring pillars were not included in the GPD model, the restraining force would be lower than that of the full, quarter, or octant model which includes these neighboring pillars. Thus, the USUM of the GPD and half-GPD model is higher than that of the other models. Fortunately, the GPD models can be optimized by considering the neighboring pillars.

The GPD models can be modified to correct for the nonhomogenous loading conditions on the sidewalls by adding a modification to  $U_0$  shown in Eq. (1). The ratio  $(\frac{N}{2N-1})$  is the quotient of the number of pillar in the GPD ( $N$ ) to the sum of the number of pillars in the neighboring region ( $N-1$ )

$$U_1 = \frac{U_0 \times N}{2N - 1} \quad (1)$$

where,  $U_0$  is the maximum USUM for the half-GPD model before optimization,  $U_1$  is the maximum USUM for the half-GPD model after optimization using Eq. (1), and  $N$  is the number of pillars in the GPD or half-GPD model. Without concerning the loading effect from the neighbor pillars, the denominator  $(2N-1)$  reduces to  $N$ , and  $U_1 = U_0$ . The denominator  $(2N-1)$  reflects the fact that the chip and the substrate in the GPD or half-GPD models are stretched by the pillars in the slice and the pillars neighboring the slice. Therefore, the optimized loading on the sidewalls of the GPD slices can be expressed by the denominator of the equation.

It was found that Eq. (1) works even for a higher number of connections. The half-GPD slice models with 3, 6, 9, and 15 pillars were investigated, as shown in Table 2. The approach may also be used for structures with two boards connected by pillars, solder balls or other arrays with the same pitch size.

The USUM of the octant model,  $U_r$ , was taken as a reference value for the displacement so that the results can be compared to the GPD models.  $U_0$  is the USUM of the half-GPD model before optimization. The error associated with it can be expressed as the ratio  $\frac{U_0 - U_r}{U_r}$  by comparing it to the octant model.  $U_1$  is the maxi-

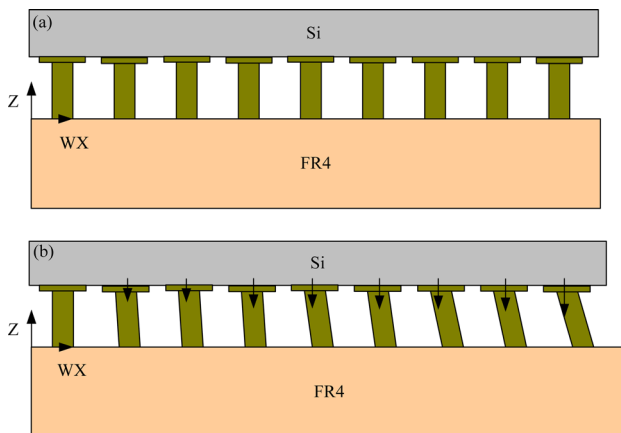
mum USUM of the half-GPD after optimization. The error for it can be expressed as the ratio  $\frac{U_1 - U_r}{U_r}$ . The USUM after optimization,  $U_1$ , shows 3.3% error for the 36 ( $6 \times 6$ ) I/O model, and 1.7% for the 324 I/O model. The effectiveness of Eq. (1) was verified in a higher density, 900 ( $30 \times 30$ ) I/O pillar model. The USUM error after optimization remained about 1.5% for the 900 pillars model. It can also be seen in Table 2 that the error in  $U_0$  approaches 100% in the higher I/O, larger devices. In another words,  $U_1$  approaches half of its uncorrected value, Eq. (1), when  $N$  is large,  $U_1 = \frac{U_0}{2}$ .

At higher loading temperatures, the expansion in the WX direction in Fig. 2(e') of the FR4 substrate is  $\Delta L_{wx}(\text{FR4}) = \alpha_1 \cdot \Delta T$ , where  $\alpha_1$  is the coefficient of thermal expansion (CTE) of the FR4 board. The expansion of the silicon chip in WX direction is  $\Delta L_{wx}(\text{Si}) = \alpha_2 \cdot \Delta T$ , where  $\alpha_2$  is the CTE of silicon. Thus, the copper pillar farthest from the chip center, at the corner of the package is elongated to a new length in the WX direction:  $\Delta L_{wx}(\text{Cu}) = \Delta L_{wx}(\text{FR4}) - \Delta L_{wx}(\text{Si}) = (\alpha_1 - \alpha_2) \cdot \Delta T$ . Thus, the expansion of the copper pillar in the WX direction is much larger than the expansion in the Z direction. The copper pillars in the large GPD slice model are assumed to be beam-like. Therefore, the elongation of the copper pillars in the WZ direction can be

expressed as  $\Delta L_{wz}(\text{Cu}) = \sqrt{H^2 + \Delta L_{wx}^2(\text{Cu})} - H$ , where  $H$  is the length of pillars, because the components in the structure are free to expand in the Z direction. Finally, the average force that the last copper pillar exerts on the chip can be expressed as  $F = \frac{E(\text{Cu})\Delta L_{wz}(\text{Cu})}{H} A$ , where  $A$  is the cross-sectional area of the last pillar and  $E(\text{Cu})$  is the elastic modulus of the copper. The total restraining force on the pillars due to the chip is proportional to the total cross-sectional area of the pillars. If the effect of the neighboring pillars is not considered in GPD modeling, the total area  $\sum^A = N \times A$  is the sum of the cross-section area of the pillars in the GPD slice. The average force can be expressed by  $F = \frac{E(\text{Cu})\Delta L_{wz}(\text{Cu})}{H} \sum^A$ . If the total area ( $\sum^A = (2N-1) \times A$ ) is the sum of the cross-section area of the pillars in the slice and the neighboring pillars, then, the force is  $F' = F \times \frac{2N-1}{N}$ . The restraining force is increased by the factor  $\frac{2N-1}{N}$ . Thus, the deformation decreases by  $\frac{2N-1}{N}$ . This is the basis for Eq. (1) and why it correctly modifies USUM, as shown in Table 2, where  $\frac{U_0}{U_1} = \frac{2N-1}{N}$ .

## Conclusions

Five models were used to compare the mechanical behavior of copper pillar chip-to-substrate structures. As for the maximum stress of the models, the results show that the GPD and the half-GPD models without optimization have a 4.7% difference compared to the results of the total-chip model, quarter model, and octant model in a flip-chip configuration. As for the maximum deformation of the models, the accuracy of the original GPD model was poor because of the erroneous boundary conditions. It was found that the error in the original GPD model was caused by neglecting the effect of the neighboring I/O structures in the GPD slice model. An optimized GPD model was obtained and the results show that the error in the GPD model after optimization was lowered to 1.5%, which is similar to the value obtained in the octant model. A simple equation was used to modify the boundary condition at the side-walls of the GPD slice model. It was also



**Fig. 6 Schematic diagram of deformed half-GPD model under at high temperature**

found that the new GPD model conditions are applicable to a higher number of I/O.

The half-GPD 3D model was significantly faster and required fewer nodes than the total-chip, quarter, or octant models. Moreover, the GPD model provides accurate calculation of the mechanical properties of the composite structure. It was shown that the half-GPD model with optimized boundary conditions at the side-walls can be used in place of the total-chip, quarter, or GPD models. The half-GPD model correction includes accounting for the effect of the neighbor I/O on the GPD slice. The correction,  $U_1 = \frac{U_0 \times N}{2N-1}$ , was used to adjust the displacement and the stress. This model with the refined boundary conditions can be used in thermal stress analysis, general plane deformation description, failures prediction, and life prediction in high density flip-chip package.

## Acknowledgment

The authors gratefully acknowledge the financial support of the Global Research Collaboration of the Semiconductor Research Corporation, Project No. 1883.004. The discussions with C. Hunter Lightsey and Hyo-chol Koo are also gratefully acknowledged.

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