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DIAMOND TRANSISTOR OPA660

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CIRCUIT TECHNOLOGY WITH THE DIAMOND TRANSISTOR OPA660

The monolithic integrated circuit OPA660 uses the Diamond structure to act as an ideal transistor. However, this circuit has the advantage that it avoids the biasing circuits and eliminates the need for an offset voltage compensation network. With this element, peripheral components are reduced to the essential minimum. Using the DC-coupled wideband voltage amplifier and buffer, conventional and new circuit designs of the OPA660 can be compared with each other.

A report in Electronik Industrie 90 (vol. 1, p.70) presented basic explanations, along with a schematic overview of circuits possible with the voltage-controlled current source OPA660. This article is intended to describe the practical circuit design. From the many possible application circuits, this article first examines the basic circuits without external feedback.

DIAMOND TRANSISTOR

Figure 1 illustrates what is probably the simplest DC-coupled voltage amplifier. Several factors in the circuit design are disadvantageous for easy and general application: the input offset voltage which is dependent upon temperature (V_{IO} = –627mV—see Table I), the output offset voltage— also dependent upon the temperature (V_{OO} = + 3V), and the bias current (I_O = 2mA), which flows through the output load resistor (1kΩ). When the offset-free signal voltage V_{IN} appears at the output, it is amplified as desired (G = 2) but is superimposed with bias voltage and current. These DC currents and bias voltages, which are determined by the transistor, are systematically compensated in the following circuit variations. V_{IO} and I_O require that the emitter resistor be divided (743Ω and 1.53kΩ). The signal voltage gain results from:

$$G = \frac{V_{OUT}}{V_{IN}} \approx \frac{1k\Omega}{743\|1.53k\Omega} = 2$$

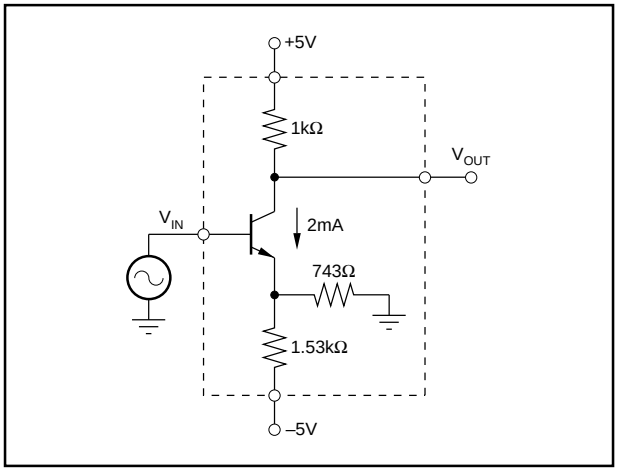

FIGURE 1. DC-Coupled Voltage Amplifier.

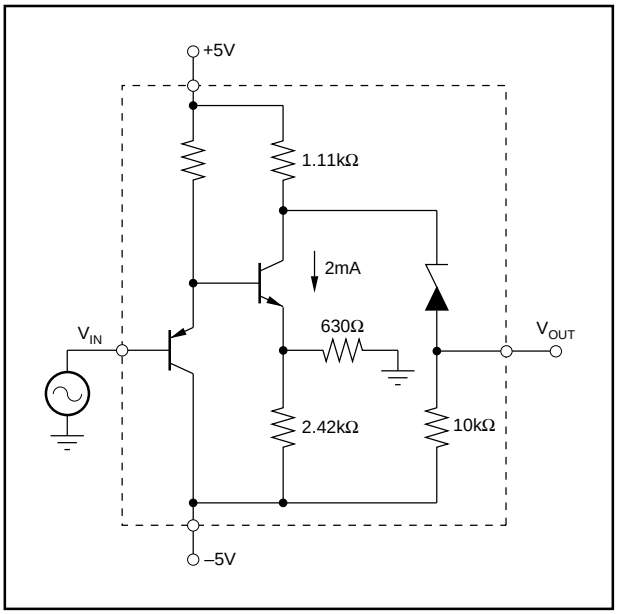

FIGURE 2. Adjustment of V_{IO}.

Further important parameters are summarized in Table I. In Figure 2, V_{IO} is compensated with a previously inserted complementary emitter follower (pnp), while V_{OO} is compensated with a zener diode inserted afterward. I_O still requires division of the emitter resistor (630Ω and 2.42kΩ). The signal gain now results from:

$$G = \frac{V_{OUT}}{V_{IN}} \approx (1.11k\Omega \parallel 10k\Omega)/(630\Omega \parallel 2.42k\Omega) = 2$$

With current sources as shown in Figure 3, the gain determined by the resistors (500Ω and 1kΩ) can be achieved as desired, without bias currents and voltages.

$$G = \frac{V_{OUT}}{V_{IN}} \approx \frac{1k\Omega}{500\Omega} = 2$$

Printed in U.S.A. May, 1993

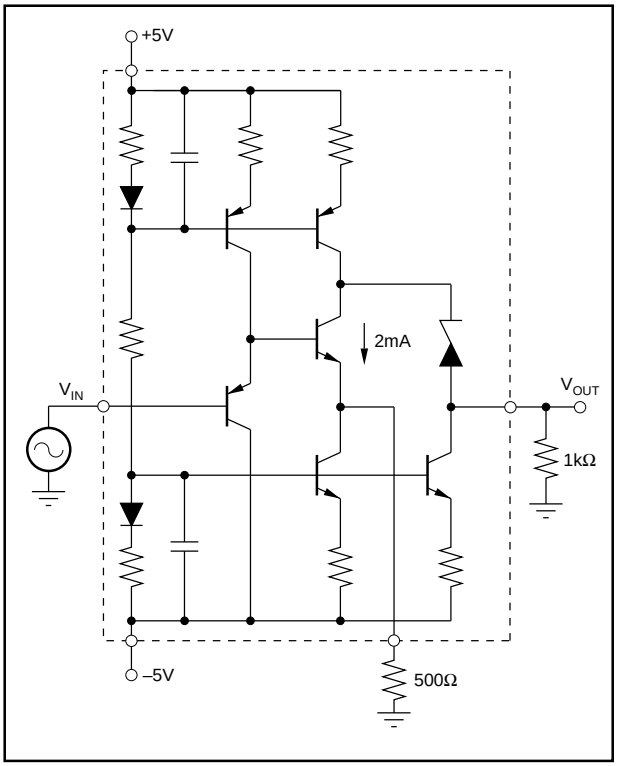

FIGURE 3. Circuit with Constant Current Sources.

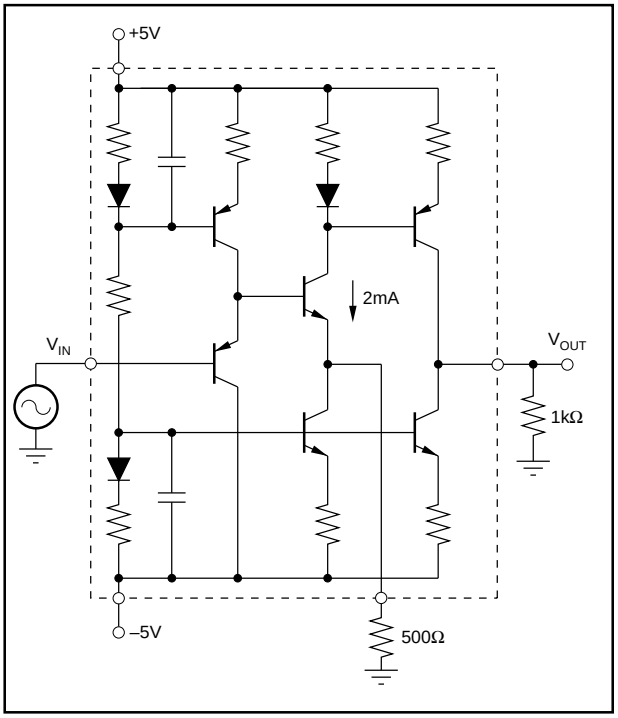

FIGURE 4. Insertion of PNP Current Mirror.

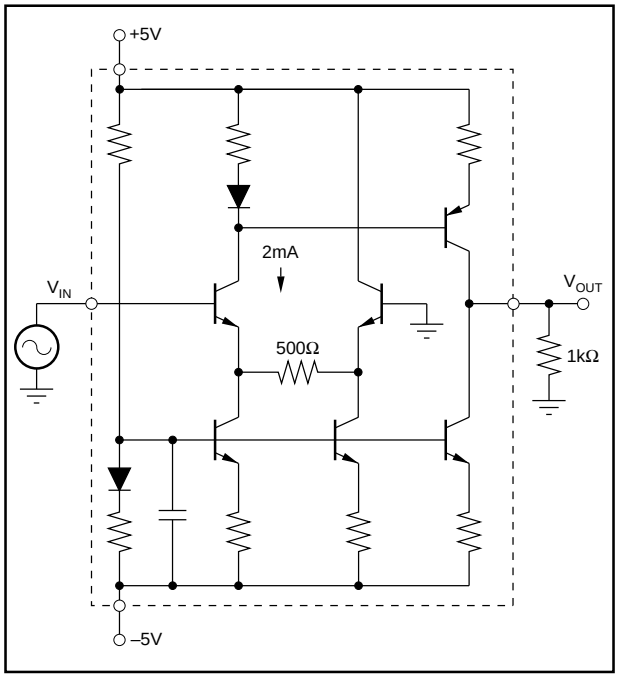

FIGURE 5. Differential Amplifier for Compensation of V_{IO}.

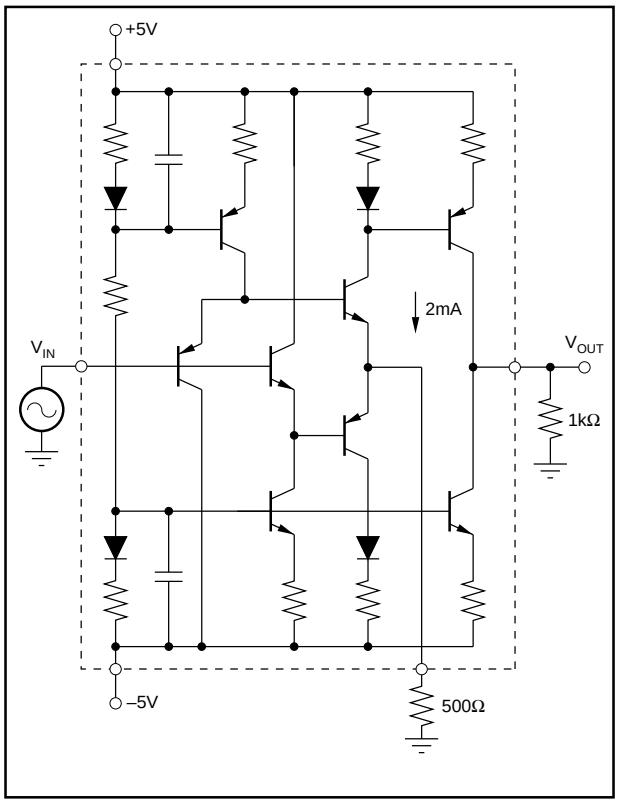

FIGURE 6. Diamond Structure.

Figure 4 shows a variation comparable to Figure 3, in which the V_{OO} is avoided using a current mirror instead of a zener diode. Figure 5 shows how a differential amplifier can be used to compensate the V_{IO} in place of the previously inserted complementary emitter follower. This method has the disadvantage that the emitter resistor (500Ω) is connected on both sides to "hot" adaptors. The previously discussed methods using zener diodes or resistors instead of current sources are also possible here. Figure 6 illustrates the most developed and elegant method with a complementary

symmetric circuit, called “Diamond structure” in laboratory jargon. Ideally, the three signal terminals are free from bias currents and offset voltages. In this case:

$$G = \frac{V_{OUT}}{V_{IN}} \approx \frac{1k\Omega}{500\Omega} = 2$$

The active operating area of the previously discussed circuit designs that are not complementary-symmetric is limited by the polarity of the input signal. For instance, when the signal current as shown in Figure 4 exceeds the quiescent current (I_O = 2mA) through the emitter resistor (500Ω) using a negative input signal, it will load up to a signal limitation. This limitation does not correspond to Figure 6. This circuit looks like a quasi-ideal transistor and is characterized as the Diamond Transistor (DT) in the following. Burr-Brown offers this monolithic integrated circuit under the name OPA660. Figure 7 shows how the DT is used in the DC-coupled voltage amplifier examined here. With the resistor R_Q, the quiescent current I_Q, for example I_Q = 2mA, is adjusted, as is the transconductance gm. Thus the following equation holds:

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{1k\Omega}{500\Omega + \frac{1}{gm}} \approx \frac{1k\Omega}{500\Omega} = 2$$

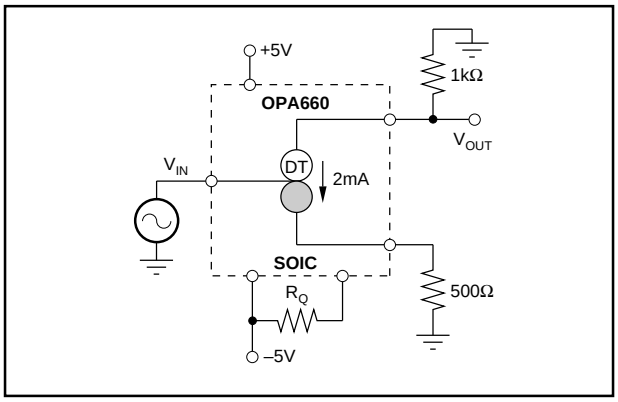

FIGURE 7. Diamond Transistor in a DC-Coupled Voltage Amplifier.

DIAMOND BUFFER

The simplest form of a DC-coupled buffer is the emitter follower as illustrated in Figure 8. The disadvantage of this buffer is that the voltage offset is dependent upon the temperature (V_{IO} = –627mV, see Table II) between the input and output signals, while the ability to handle negative signals depends upon the quiescent current (I_O = 2mA) and load resistor (200Ω). In Figure 9, an additional emitter follower is inserted to compensate the V_{IO}. The next step is shown in Figure 10, in which the pull-up and pull-down resistors are replaced by constant current sources.

As shown in Figure 11, the advantages that can be achieved with a complementary symmetric solution are comparable to those using a Diamond transistor. A comparison of Figures

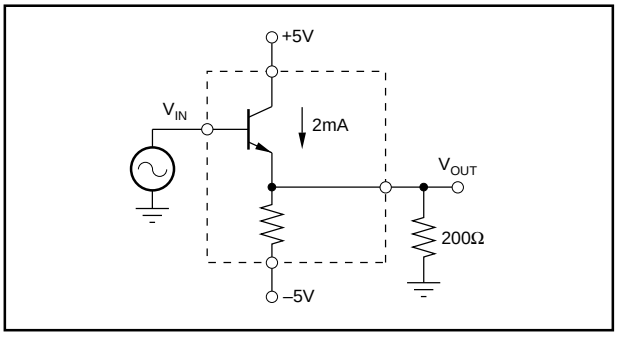

FIGURE 8. DC-Coupled Buffer.

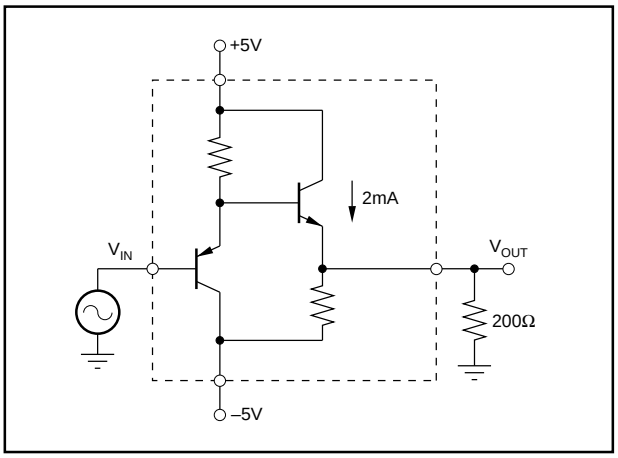

FIGURE 9. Adjustment of V_{IO} with Previously Inserted Complementary Emitter Follower.

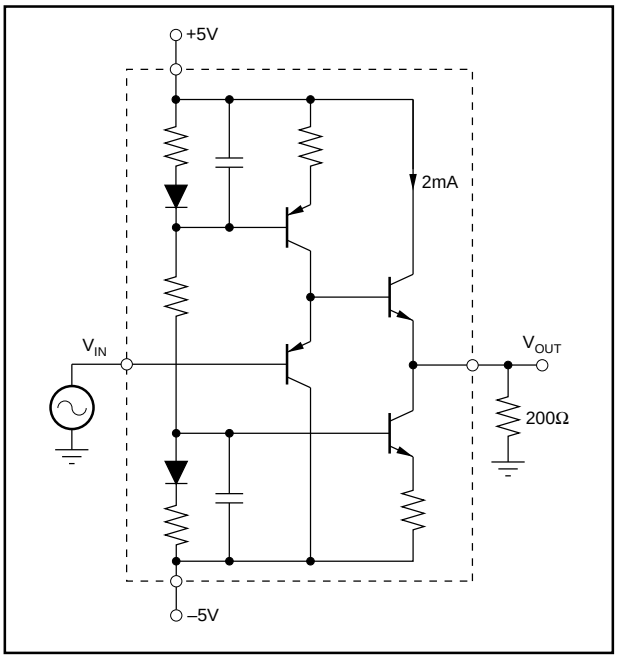

FIGURE 10. The Pull-Up and Pull-Down Resistors are Replaced Here by Constant Current Sources.

11 and 6 demonstrates that Figure 11 is a part of the circuit illustrated in Figure 6. This section, which is also a so-called push-pull buffer design, is used in Figure 12 as a part of the Diamond transistor. The following equation applies:

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{200\Omega}{200\Omega + \frac{1}{gm}} \approx 1$$

The integrated circuit OPA660 contains a complete DT as well as a part of the DT, shown in Figure 11, which is called the Diamond Buffer (DB) and is available in an 8-pin DIL or SOIC package (see Figure 13).

BASIC CIRCUITRY

To give the reader an overview, the previous explanations of the DB and DT are summarized schematically in Figure 14. The common base circuit is also detailed in this presentation to complete the explanations. The signal transmission of the DT is the reverse of that of a normal transistor. The common emitter circuit with the DT does not invert the phase of the input signal, while the common base inverts. In many applications, the high-impedance output with its small output current capability seems to be a disadvantage, as shown in Figures 14b and 14c. In conventional circuits, the emitter follower is inserted afterwards. Figure 15 shows the connection between DT and DB, in which all advantages mentioned here are maintained. The signal-inverting variation as illustrated in Figure 14c has a low-impedance signal input (2). This disadvantage, however, can be avoided by connecting the emitter follower to the low-impedance input as shown in Figure 16. DB and DT form a differential amplifier with current output. This is the well-known function of an operational transconductance amplifier (OTA). The cascaded circuitry made up of two DTs shows similar external effects, as shown in Figure 17.

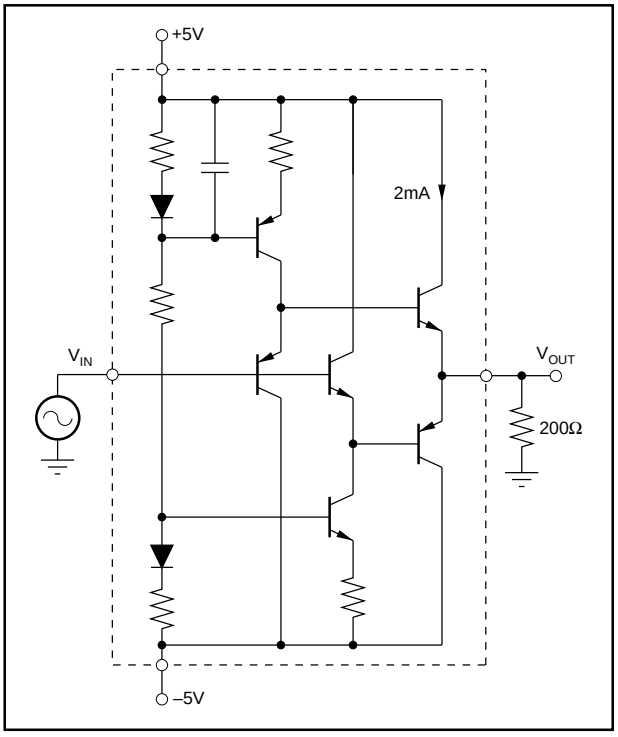

FIGURE 11. Push-Pull Buffer.

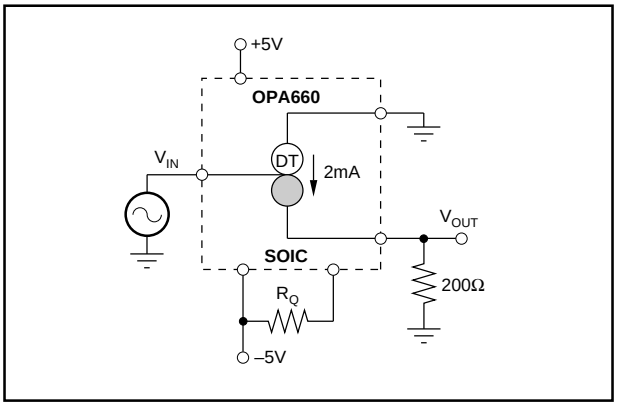

FIGURE 12. Push-Pull Buffer as a Part of the Diamond Transistor.

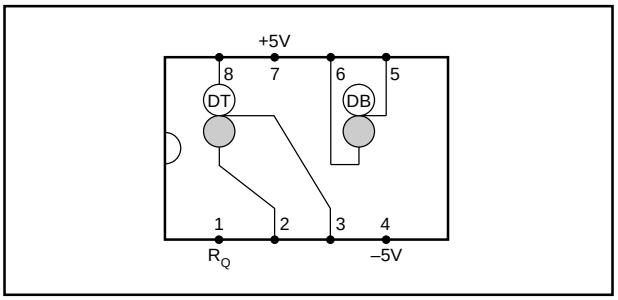

FIGURE 13. The OPA660 is Housed in an 8-Pole DIP or SOIC Package.

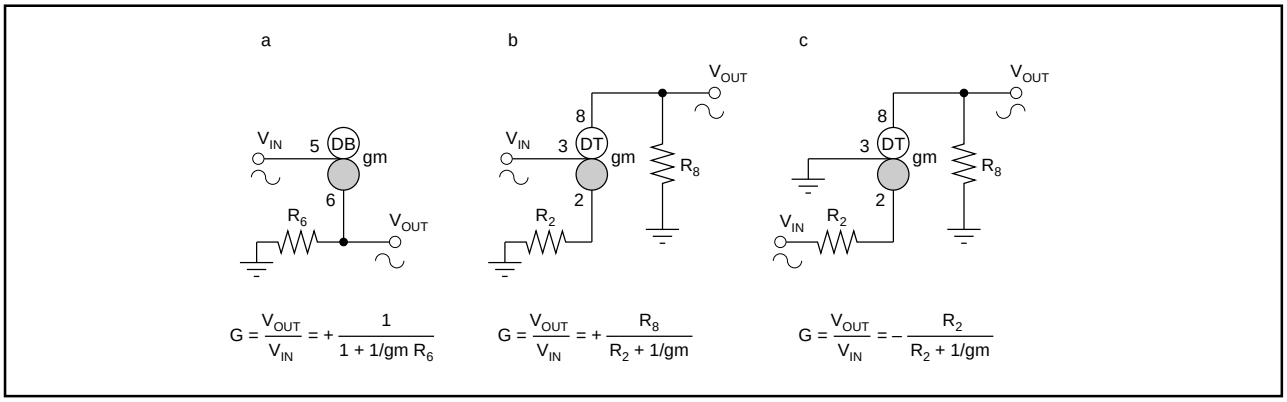

FIGURE 14. DC-Coupling of the Basic Circuits with DB and DT.

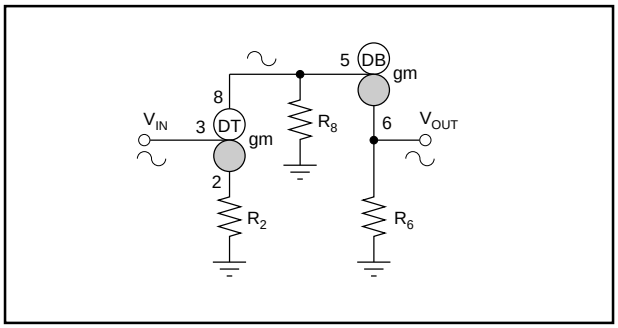

FIGURE 15. DT and DB Inserted Afterwards.

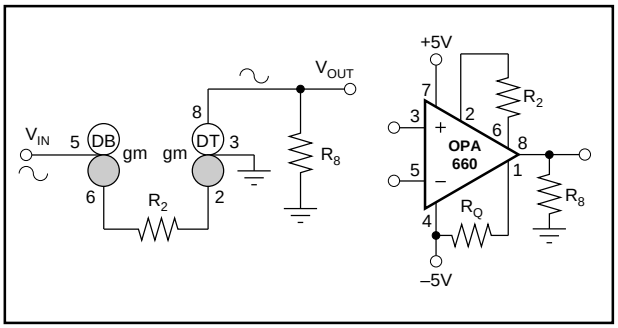

FIGURE 16. Operational Transconductance Amplifier (OTA).

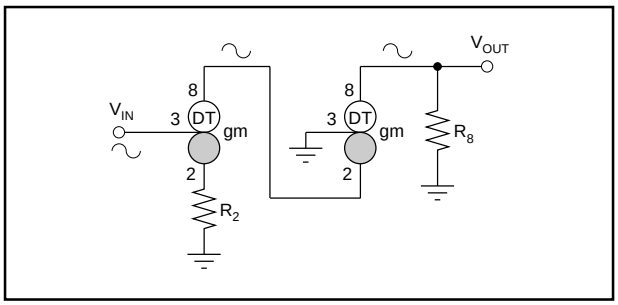

FIGURE 17. Cascaded Diamond Transistors.

SUMMARY

The applications presented here are intended to provide an overview of the versatile applications using DB and DT according to their prototype, the normal transistor. In contrast to the conventional transistor, the DB and DT require practically no circuit interface. The external components are reduced to the necessary functional elements. Looking at the results of Tables I and II, particularly from the DB and DT, one notices that some parameter are not exactly "ideal." Through their hard work, however, design engineers are coming closer and closer to this ideal. In this process, the OPA660 is the first step. Including feedback circuits in the combination of DB and DT results in, among other things, current-feedback and voltage-feedback amplifiers. Schematic examples of these designs are outlined in (1).

		FIGURE							
PARAMETER	**CONDITION**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**UNIT**
Input Offset Voltage	–25°C +27°C +125°C	–722 –627 –445	–19.1 –22.5 –28.4	15.0 18.2 24.2	14.1 17.1 22.9	0 0 0	–1.8 –1.7 –1.3	–13.9 –16.3 –20.1	mV
Input Bias Current	–25°C +27°C +125°C	–14.4 –15.4 –17.4	10.2 10.1 9.8	–11.9 –11.8 –11.6	–12.2 –12.0 –11.8	–15.6 –15.3 –14.8	–8.8 –8.5 –8.0	–2.2 –1.6 –0.9	µA
Output Offset Voltage	–25°C +27°C +125°C	3188 3000 2636	–7.0 –0.7 10.2	47.0 35.5 14.5	–33.1 –34.6 –38.2	-4.7 –0.4 +7.1	2.5 3.4 4.3	40.1 30.0 16.3	mV
Output Bias Current	–25°C +27°C +125°C	1812 2000 2636	2009 2003 1993	18.2 0.6 –31.8	–6.6 –2.5 4.6	–4.7 –0.4 +7.1	–0.9 0.2 1.8	15.6 0 –22.3	µA
Transconductance	–25°C +27°C +125°C	79.1 72.6 65.0	85.0 70.9 53.9	83.5 71.4 56.9	81.6 69.9 55.8	42.0 35.6 27.8	161.3 138.9 111.8	100.1 112.1 120.9	mA/V
DC Gain	+27°C	1.93	1.92	1.92	1.88	1.83	1.90	1.84	V/V
Input Resistance	10kHz	0.065	0.38	3.0	3.0	0.068	1.6	1.4	MΩ
Input Capacitance	10MHz	7.5	2.2	2.1	1.9	3.7	3.8	0.8	pF
Output Resistance	10kHz	(1)	(1)	48	150	153	110	27	kΩ
Output Capacitance	10MHz	3.0	3.6	2.5	8.4	8.4	11.8	2.8	pF
Small Frequency Resp.	0.1Vp-p –3dB	90	65	22	22	22	19	74	MHz
Large Frequency Resp.	2Vp-p	90	65	22	22	22	19	74	MHz
Slew Rate	2Vp-p	220	140	60	70	70	50	300	V/µs
Differential Gain	2Vp-p 5MHz	2.9	2.4	3.2	1.4	2.2	0.2	1.3	%
Differential Phase		1.6	4.0	1.8	2.1	0.9	0.6	0.05	deg
Open-Loop Gain	10kHz	37	37	65	74	69	78	70	dB
Common-Mode Gain	10kHz	6	6	–13	–19	11	–26	–1	dB
Supply Reject. Positive	1Hz	0	–1	–33	–49	48	–45	–52	dB
Supply Reject. Negative	1Hz	–4	–6	–37	–51	56	–46	–38	dB
Quiescent Current	+27°C	2	2	2	2	2	2	2	mA

TABLE I. Important Parameters of the Previously Examined Circuits (numbers correspond to the Figure numbers).

		FIGURE					
PARAMETER	**CONDITION**	**8**	**9**	**10**	**11**	**12**	**UNIT**
Input Offset Voltage	–25°C +27°C +125°C	–717 –627 –453	0.6 0.9 1.8	1.1 1.0 0.6	1.7 1.6 1.2	13.2 15.5 19.2	mV
Input Bias Current	–25°C +27°C +125°C	–11.3 –15.2 –22.2	23.5 23.2 22.5	23.6 23.3 22.7	8.7 8.5 8.0	2.1 1.6 0.9	μA
DC Gain	+27°C	0.922	0.924	0.935	0.966	0.953	V/V
Input Resistance	10kHz	0.023	0.16	1.4	1.1	1.1	MΩ
Input Capacitance	10MHz	6.5	2.3	2.0	3.9	0.8	pF
Output Resistance	10kHz	12.6	12.8	12.9	6.8	8.2	Ω
Small Frequency Resp.	0.1Vp-p	383	193	195	254	850	MHz
Large Frequency Resp.	1Vp-p	315	180	175	234	760	MHz
Slew Rate	1Vp-p	490	310	273	466	1210	V/μs
Differential Gain	1Vp-p 5MHz	5.8	4.7	4.4	1.0	0.71	%
Differential Phase		0.07	0.09	0.014	0.19	0.026	deg.
Supply Reject. Positive	1Hz	–74	–44	–71	–70	–49	dB
Supply Reject. Negative	1Hz	–37	–45	–72	–72	–52	dB
Quiescent Current	+27°C	2	2	2	2	2	mA

TABLE II. Important Parameters of the Previously Examined Circuits.

[1] Lehmann, K; Elektronik Industrie 90, Quasiideale Stromquelle, Vol. 1, p.70.

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