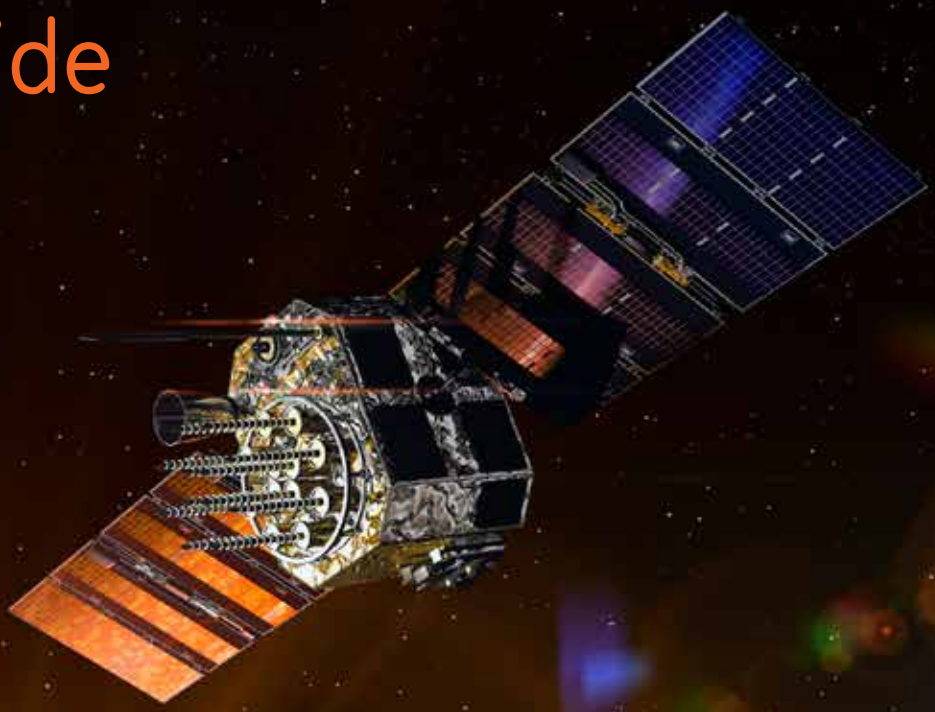
BAE SYSTEMS

Radiation-hardened electronics product guide

Short-form



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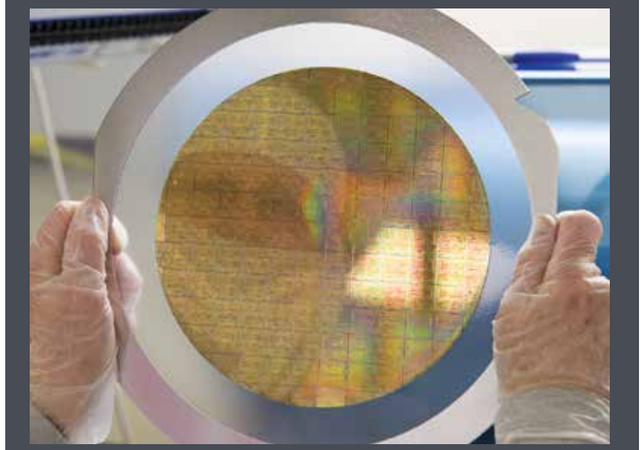


Technology center for radiation-hardened and high-reliability electronics

Overview

BAE Systems is a global defense, security, and aerospace company, delivering a full range of products and services for air, land, and naval forces, as well as advanced electronics, information technology solutions, and customer support services.

The company develops and produces a wide array of radiation-hardened space products, from standard components and single-board computers, to complete system payloads. BAE Systems specializes in a broad domain of radiation-hardened electronics, including application-specific integrated circuits (ASICs), application-specific standard products (ASSPs), microprocessors, memories, Field Programmable Gate Arrays (FPGAs), and single-board computers. With more than 1,000 computers in space, including the 16-bit GVSC1750, the 32-bit RAD6000® CPU, and the RAD750® family of products, BAE Systems' space computers have logged over 10,000 years in orbit.

The Space Products and Processing group in Manassas, Virginia has been providing products and system-level solutions to the commercial, military, and space communities since the early 1980s. Our latest family of Power Architecture® computer products, based on a radiation-hardened version of the 32/64-bit e5500 processor core, includes single-core and multi-core based single board computers, such as the RAD5545® SBC.

Packaging

BAE Systems offers a wide range of wirebond and flip-chip hermetic packages to support space, military, avionics, and commercial ASICs and memories. These include families of ceramic quad flat packs, ceramic column grid arrays, plastic ball grid arrays with glob-top, and stacked and unstacked die in multichip modules.

Testing

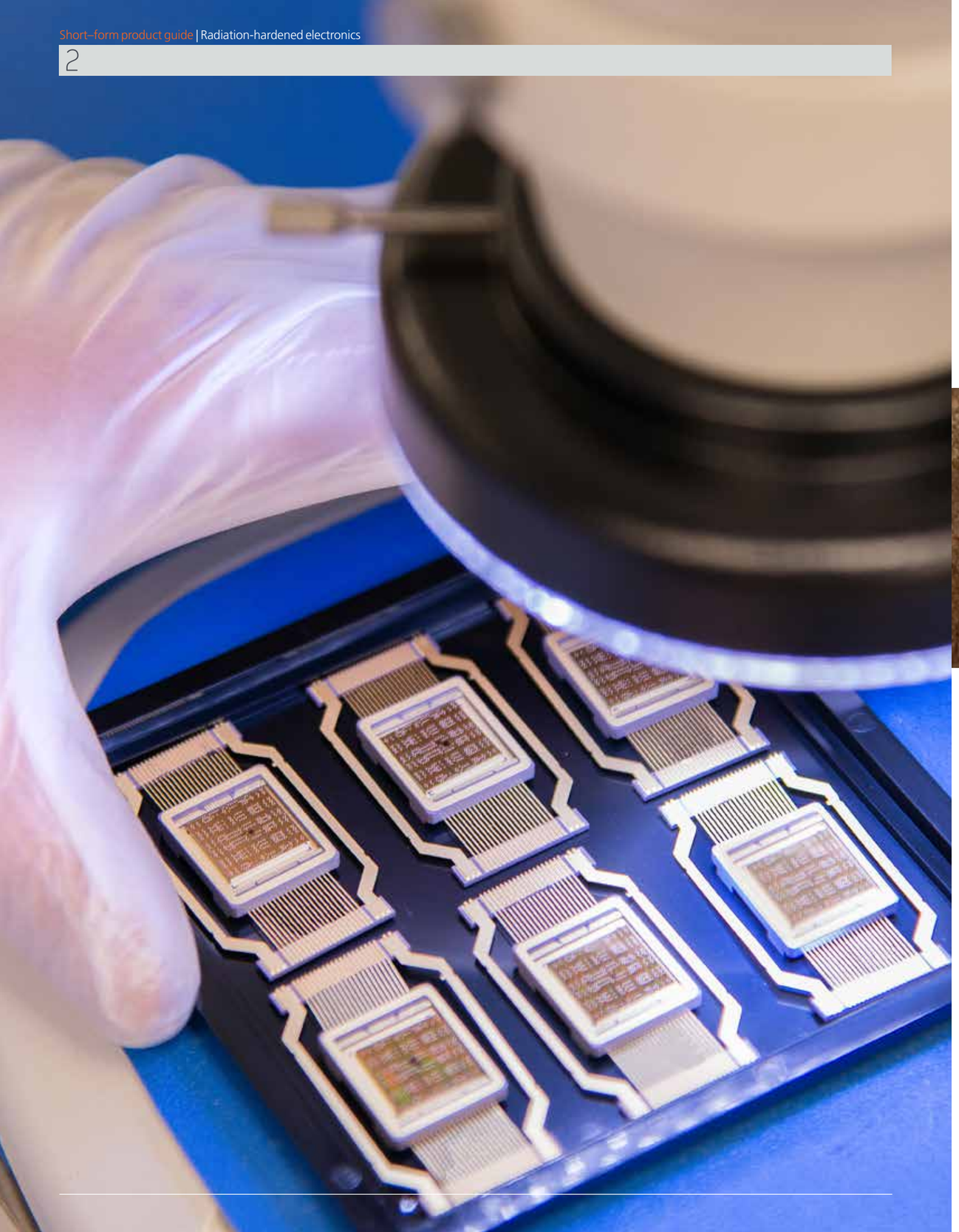
BAE Systems' space test facility provides logic and memory testers for components and flying probe and card testers for circuit card assemblies. The facility has full environmental testing capability for both components and cards, including a J.L. Shepherd Cobalt-60 Gamma source for on-site total-dose testing at military-standard (MIL-STD) dose rates and a thermal vacuum chamber for card test. Failure analysis instruments include photoemission and scanning electron microscopes, and focused-ion beam systems that support process diagnostics and semiconductor repair. Electrical test equipment includes the Advantest V93000 smart scale System-on-chip (SoC) test system with 1024 signals installed and a capacity of up to 4000 signal pins. Speeds as high as 8 Gbps are available.

BAE Systems also has extensive experience developing and performing tests at linear accelerator, flash X-ray, heavy-ion, proton and neutron test facilities.

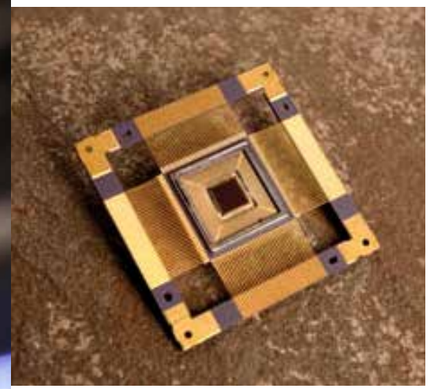
Quality

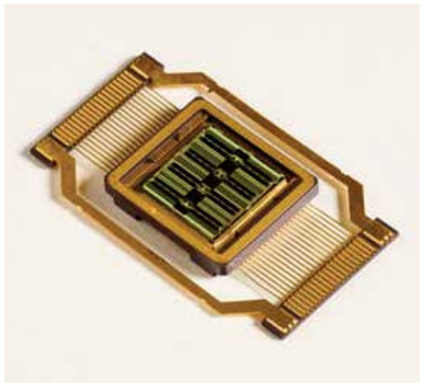
The BAE Systems Manassas and foundry partner fabrication facilities are included in the Defense Logistics Agency (DLA) Qualified Manufacturer List (QML) for production of avionics and radiation-hardened space parts.

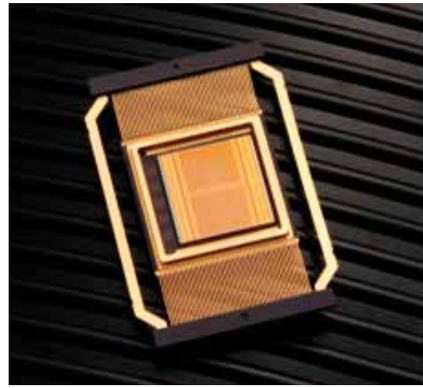
Qualification under the Department of Defense (DoD) QML program involves a rigorous validation process by a panel of government agencies and customers. Qualified manufacturers understand user requirements and technical processes to produce and constantly improve high-quality, reliable integrated circuits and modules. BAE Systems' space product portfolio is certified and qualified to DLA performance specifications MIL-PRF-38535 and MIL-STD-883 for QML Class V and Q, including Radiation Hardness Assurance (RHA) and support for legacy requirements.The facility is accredited as a DoD category 1A trusted source aggregator, covering design, test, packaging, and assembly services. The accreditation expresses the Defense Department's confidence in BAE Systems' ability to deliver trusted microelectronics equipment and services to U.S. government end users.



Standard components



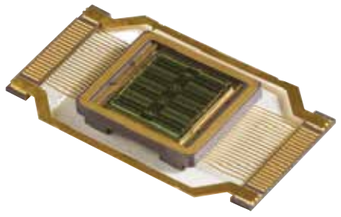


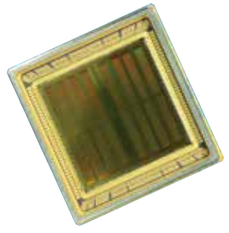


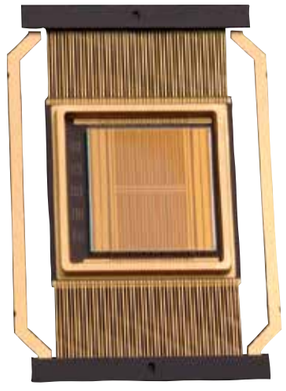
Reliable, radiation-hardened, space-qualified, hermetically-sealed, and military-screened components

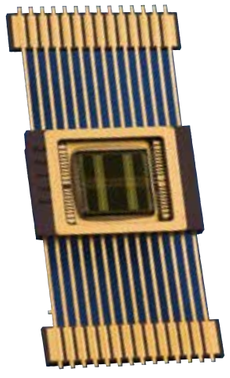
Memory

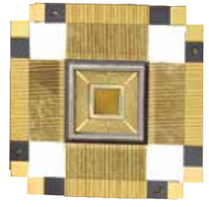
Memory	Part number (P/N)	Description	Configuration	Voltage (V)	Typical access/ clock (ns)	Total-dose (rad[Si])	Single-event upset (upsets/bit-day)	Latch-up immune	Package	Qualified	SMD number
SRAM	251A172	MILLENNIUM	512k x 32	2.5/3.3	12	>100k	<1E-10	Yes	84-lead FP	Internally qualified	N/A
SRAM	251A137	MILLENNIUM	512k x 40	2.5/3.3	12	>100k	<1E-10	Yes	84-lead FP	Internally qualified	N/A
SRAM	8427352	INDEPENDENCE	512k x 32	1.5/3.3	17	>1M	<1E-12	Yes	86-lead FP	Q, V	5962H13235
SRAM	8427352	INDEPENDENCE	512k x 32	1.5/3.3	20	>1M	<1E-12	Yes	86-lead FP	Q, V	5962H13235
SDRAMs	8515862	4-HI STACK	128M x 16	3.3	7	>50k	<1E-9	Yes	54-lead SOP	Internally qualified	N/A
PROM	238A790		32k x 8	3.3 TTL	60	>500k	immune	Yes	28-lead FP	Q,V	5962G02502
PROM	197A807		32k x 8	5.0 CMOS/TTL	27	>200k	immune	Yes	28-lead FP	Q,V	5962R96891
C-RAM	8406746		256k x 8	3.3	Read: 70 Write: 1000	>500k	<1E-11	Yes	40-lead FP	Q, V-pending	5962G08240
C-RAM	8406746		512k x 8	3.3	Read: 70 Write: 1000	>500k	<1E-11	Yes	40-lead FP	Q, V-pending	5962G08241









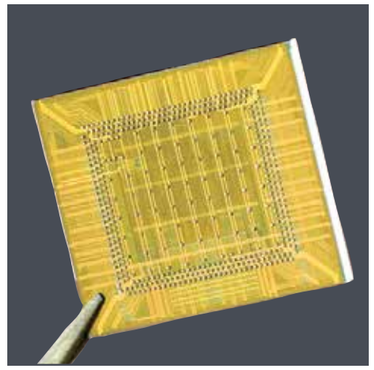


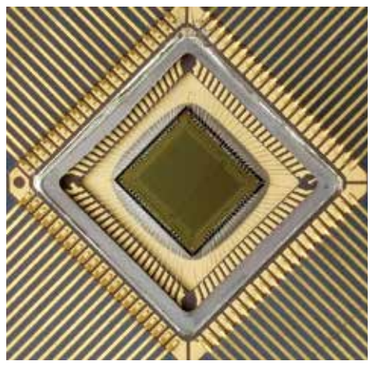
Microprocessors*

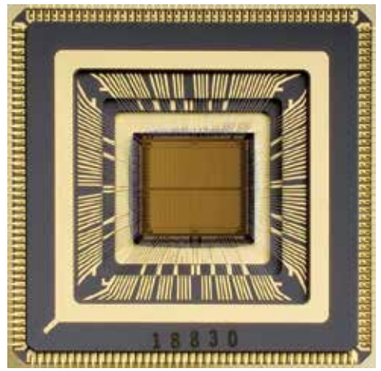
Microprocessors	Part number (P/N)	Speed	Voltage (V)	Total-dose (rad[Si])	Single-event upset errors/bit-day 90% geo (W.C.)	Latch-up immune	Package (CCGA)	Qualified	SMD number
RAD750® V2	8447257	200 MHz	1.9/3.3	>1M	<1.0E-10	Yes	360-pin	Q,V	5962H12229
RAD5545®SoC V1.1	8507255	466MHz	1.8/2.5/3.3	1M	<2E-9	Yes	1752-pin	In-Progress	TBD
RAD5545®SoC V1.2	8556754	466MHz	1.8/2.5/3.3	1M	<2E-9	Yes	1752-pin	In-Progress	TBD
RAD510® SoC	Coming Soon								

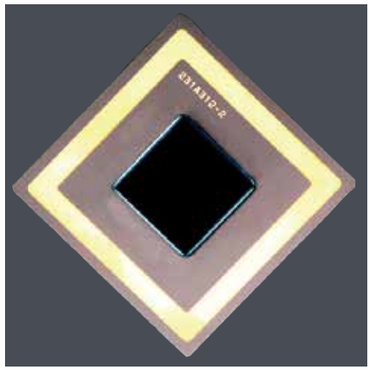
FPGAs

FPGAs	Part number (P/N)	Voltage (V)	Logic cells	Total-dose (rad[Si])	Single-event upset effective LET 90% geo (C-module)	Single-event upset effective LET 90% geo (S-module)	Latch-up immune	Package (CQFP)	Qualified	SMD number
RH1020B	197A805	5	2000	>150k	3.6	120	Yes	84-lead	Q, V	5962R90965
RH1280B	197A806	5	8000	>100k	5.7	1.8	Yes	172-lead	Q, V-pending	5962R92156





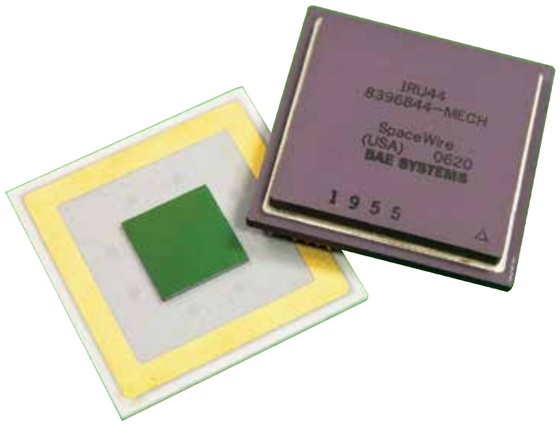


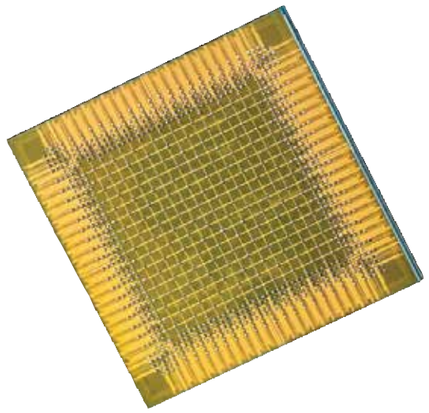


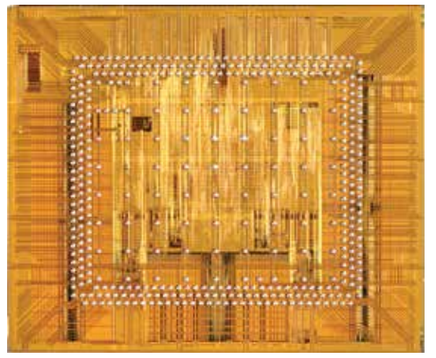
*BAE Systems reserves the right to restrict component sales based on application and volume. Please contact the factory for more information.

ASSP interface components

Interface components	Part number (P/N)	Voltage (V)	Total-dose (rad[Si])	Single-event upset (upsets/bit-day)	Interfaces	Data rates	Embedded microcontroller (MIPs)	Embedded memory	Latch-up immune	Package	Qualified	SMD number
Enhanced PowerPCI	8395188	2.5/3.3	>200k	<1E-10	PCI 2.2, UART, IEEE 1149.1, memory (PROM, EEPROM, SRAM, SDRAM), RAD750/PowerPC, programmable discretes	PCI peak bandwidth (32bit, 33MHz): 132MB/s write, 126MB/s read	4	128 kb	Yes	624 CCGA	Q	5962R08A04
SpaceWire	8396844	2.5/3.3	>200k	< 1E-9	Dual PCI 2.2, UART, IEEE 1149.1, memory (PROM, EEPROM, SRAM, SDRAM), SpaceWire (4-ports with router), programmable discretes	PCI peak bandwidth (32 bit, 33 MHz): 132MB/s write, 126MB/s read SpaceWire bandwidth: 195 Mb/s at 260 MHz	6	256 kb	Yes	624 CCGA	Q	5962R08A03
RADNET™ SpW-EP SpaceWire Endpoint ASSP	8455613	1.5/3.3	>1M	<1E-11	UART, IEEE 1149.1, memory (PROM, EEPROM, C-RAM, SRAM), SpaceWire (1 redundant port with RMAP), programmable discretes, SPI, dual I2C, external FIFO, selectMap	SpaceWire bandwidth: 240 Mb/s at 320 MHz	16	256 kb	Yes	360 CCGA	Internally qualified	Pending





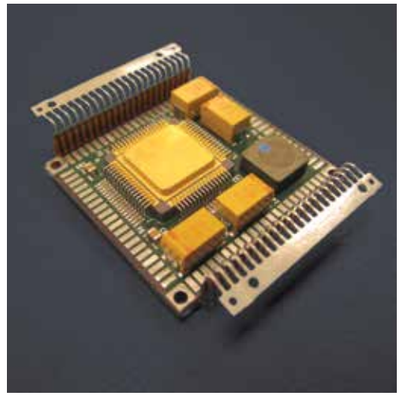


ASSP interface components

Interface components	Part number (P/N)	Voltage (V)	Total-dose (rad[Si])	Single-event upset (upsets/bit-day)	Interfaces	Data rates	Latch-up immune	Package
RADNET™ 1616-XP radiation-hardened serializer/ deserializer crosspoint switch ASSP	8504720	0.95/3.3	1M	<8E-14	16 SerDes receivers with programmable input equalizer and integrated 50 Ohm termination. 16 SerDes drivers with programmable drive level, programmable de-emphasis and integrated 50 Ohm output impedence. I2C up to 1M baud JTAG port	3.125 Gbps	Yes	269CCGA
RADNET™1848-PS radiation-hardened serial RapidIO packet switch ASSP	8544363	0.95/1.8, 2.5 or 3.3	1M	<2E-9	18 serial RapidIO ports across 48 lanes I2C master/slave JTAG slave	3.125 Gbaud/lane	Yes	728CCGA

Power converters

Power converters	Part number (P/N)	Voltage (V) [In]	Voltage (V) [Out]	Latch-up immune	Total-dose	Package	Output current	Qualified
RAD® POL-14P	8522724	3.1 to 5.5 VDC	0.8 V to 85% Input	Yes	100k	84-pin FP	14A single, 22A pair	Qualified
RAD® POL-14S	8522729	3.1 to 5.5 VDC	0.8 V to 85% Input	Yes	100k	44-pin FP	14A	Qualified
RAD® POLDDR-09P	8507027	3.1 to 6 VDC	0.8 V to 85% Input	Yes	100k	44-pin FP	7.5A	Qualified



RAD750® 3U cPCI

RAD750® 6U cPCI

RAD5545® SBC

Notes:

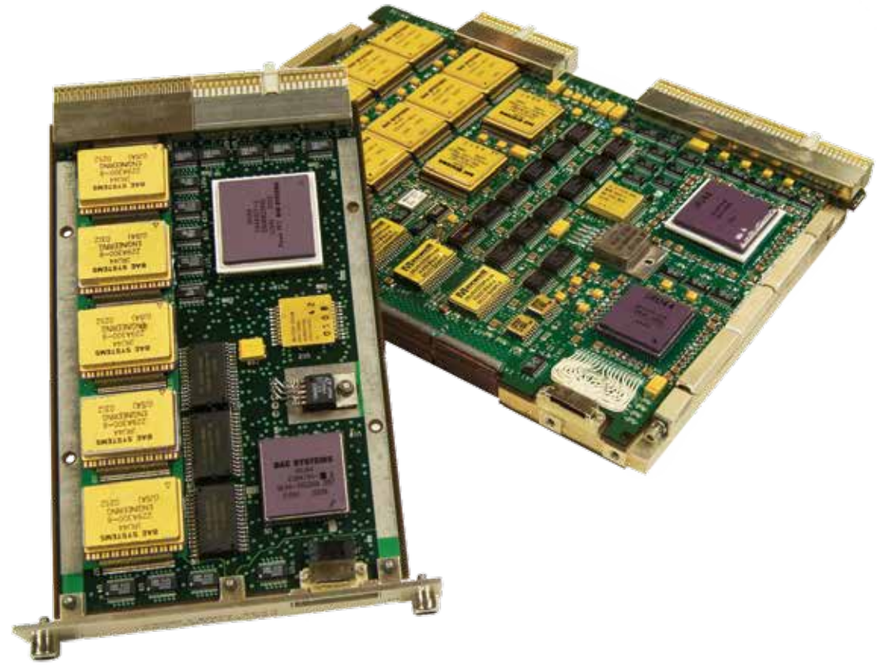
All boards can be customized. For more information, please call the Manassas facility at 571-364-7777.
All boards contain an Embedded Microcontroller (EMC) within their respective Bridge ASICs.
All assemblies will be manufactured to IPC J-STD-001FS

Boards are not to scale

Single-board computer products

Over 1,000 BAE Systems processors on more than 300 satellites with over 10,000 years of space operation

Flexible architecture and a wide range of processing options



RAD750® 3U single-board computers

Product name (PN) (Released, Prelimary, No PDM)		Card format	RAD750® processor version	RAD750® processor (MHz)	Bus speed (MHz)	Supply voltage ±5%	L2 cache	SRAM	SDRAM	EEPROM	SuROM	I/O connector	Test connector	On-card POR	On-card power control EEPROM	SpaceWire	1553
Flight	Prototype																
8515742-1	8516746-1	3U	V2	182	33	3.3	No	No	1 GB	None	64 KB PROM 1 – 256 KB EEPROM 2 – 128 KB EEPROM 4 – 64 KB EEPROM	Hypertronics	37-Pin Micro-D	Yes	No	No	No
8515742-2	8516746-2	3U	V2	182	33	3.3	No	No	1 GB	None	64 KB PROM 1 – 256 KB EEPROM 2 – 128 KB EEPROM 4 – 64 KB EEPROM	Hypertronics	37-Pin Micro-D	No	No	No	No
8515744-1	8516747-1	3U	V3	198	33 or 66	3.3	No	No	1 GB	None	64 KB PROM 1 – 256 KB EEPROM 2 – 128 KB EEPROM 4 – 64 KB EEPROM	Hypertronics	37-Pin Micro-D	Yes	No	No	No
8515744-2	8516747-2	3U	V3	198	33 or 66	3.3	No	No	1 GB	None	64 KB PROM 1 – 256 KB EEPROM 2 – 128 KB EEPROM 4 – 64 KB EEPROM	Hypertronics	37-Pin Micro-D	No	No	No	No
8523313-1 (TOR)	N/A	3U	V3	198	33 or 66	3.3	No	No	1 GB	None	64 KB PROM 1 – 256 KB EEPROM 2 – 128 KB EEPROM 4 – 64 KB EEPROM	Hypertronics	37-Pin Micro-D	Yes	No	No	No

RAD750® 6U single-board computers

Product name (PN)			Card format	RAD750® processor (MHz)	SRAM	Non-volatile Memory (EEPROM or MRAM)	SuROM	Connector	On-card POR	Power control EEPROM
Flight	EDU	Prototype								
Various*	Various*	Various*	6U-160 or 6U-220	116 to 180	8, 12, 16, 20, or 24	4MB	64 KB PROM 64KB PROM (256 KB EEPROM-EDU/PROTO) 256KB PROM (1MB EEPROM-EDU)	Hypertronics or Airborn 300-pin	Available on some versions	Version dependent

*Please contact the factory for more information on ordering and customizing Flight, EDU, and Prototype units.

RAD5545® single-board computers

Product name (PN)			Card format	RAD5545® quad core processor (MHz)	L2/L3 Cache	RAM (DDR3)	Flash	Connector	Daughter card expansion slot	SpaceWire	Serial rapid I/O	Secure boot	Security encryption engine
Flight	EDU	Prototype											
*Please contact the factory for more information on Flight, EDU, and Prototype units.			6U-220	Up to 466 x 4 cores 5.6 GIPS	L2: 512 KB- core L3: 1 MB x 2	Up to 4 GB	Up to 1 GB	SpaceVPX	Yes	16 ports up to 320 MHz (4 ports via expansion slot)	4 ports up to 3.125 Gbaud	Yes	Yes

RAD5545® support products

Product name (PN)	Features	Backplane slots	Integrated power supply output voltage	Other features

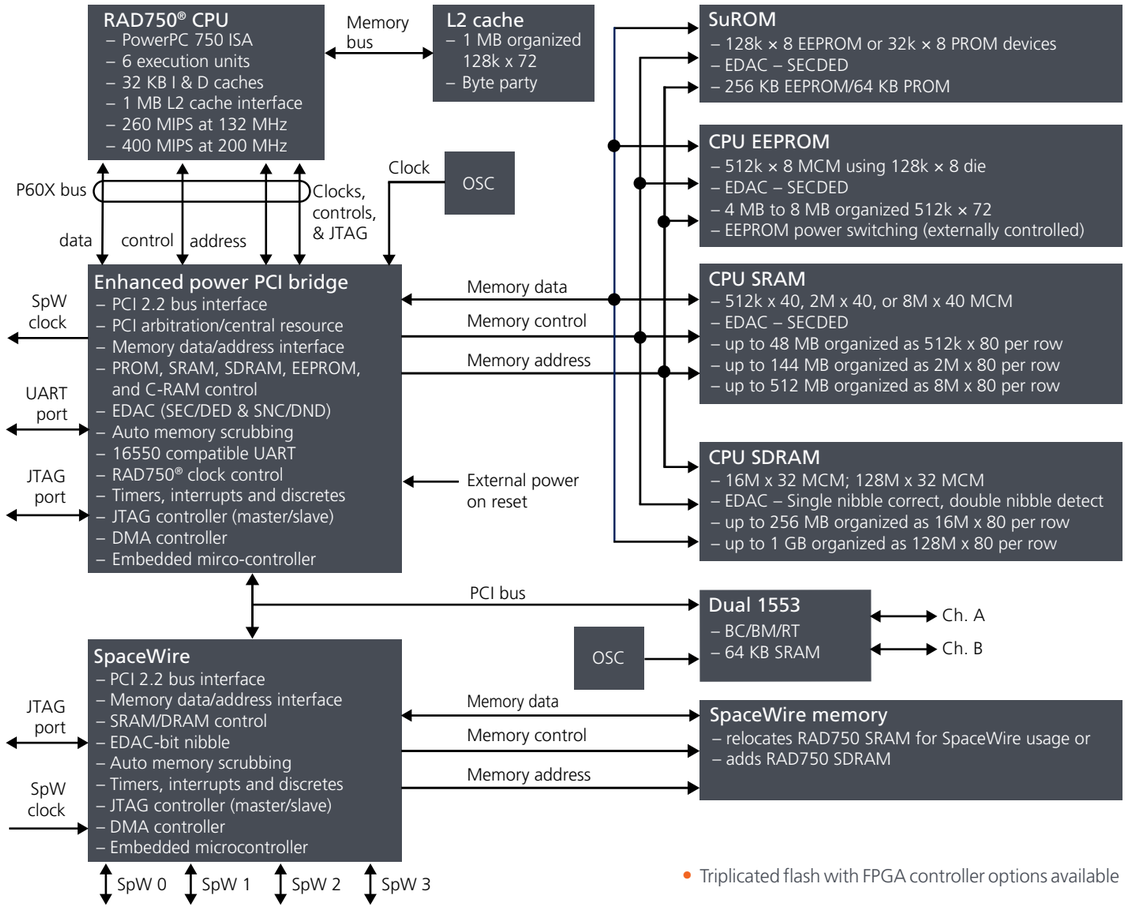
RAD5545® SpaceVPX ELMA Electronics E-Frame Test Chassis	• Commercial VPX test fixture with integrated power supply
	• Customized 5 slot backplane
	• Additional Peripherals available upon request
		• 1 standard cPCI slot
		• 1 customized cPCI slot that supports 6U RAD750 SBCs
		• 3 SpaceVPX slots
		  • 1 customized for SpaceVPX RAD750SBC
		  • 1 VPX slot for RAD5545® SBC
		  • 1 standard VPX slot
			• +5V @40A
			• +3.3V @20A
			• +12V @6A
			• -12V @3A
				• SpaceWire/ethernet adapter
				• JTAG/I2C test probes for debug
				• Pass through VPX connections to backside connectors for access to all backplane I/O and installation of a rear transition module
				• Open access to front panel and FPGA for accessing programming ports and integration with the "orange Box"

Product name (PN)	Processor	Memory	PCI express	Features
RAD5545® P5020 development system (P5020DS)	• P5020, 2.0GHz core with 1333MHz DDR3 data rate • Multiple SysClk inputs for generating various device frequencies	• Dual unbuffered DDR3 240-pin uDIMM modules with ECC (72-bit bus), 4GB memory, 1333MHz data rate • 128MB NOR flash • 1GB NAND flash • SPI-based 128MB flash • SPI-based 128KB EEPROM • SD card interface	• Two x4 express slots • Can support Freescale's XAUI-Riser and SGMIII-PEX-RISER option cards	• FMC SpaceWire card added to support two SpaceWire lanes and discrete IO • Hi-Tech Global FPGA card with Xilinx V6 image • Code Warrior USB tap • Two 1553 I/O channels • Cable insert for four lanes of sRIO at 3.125Gbaud • Two dual UARTs • JTAG/COP • Aurora high-speed connector • Two vertical SATA connectors • Two high-speed USB controllers • One type A and one microAB receptacle • Eight general-purpose I/Os

Daughtercards

Daughtercards
Memory DIMM
SpaceWire
Customizable

RAD750® 6U extended flexible architecture

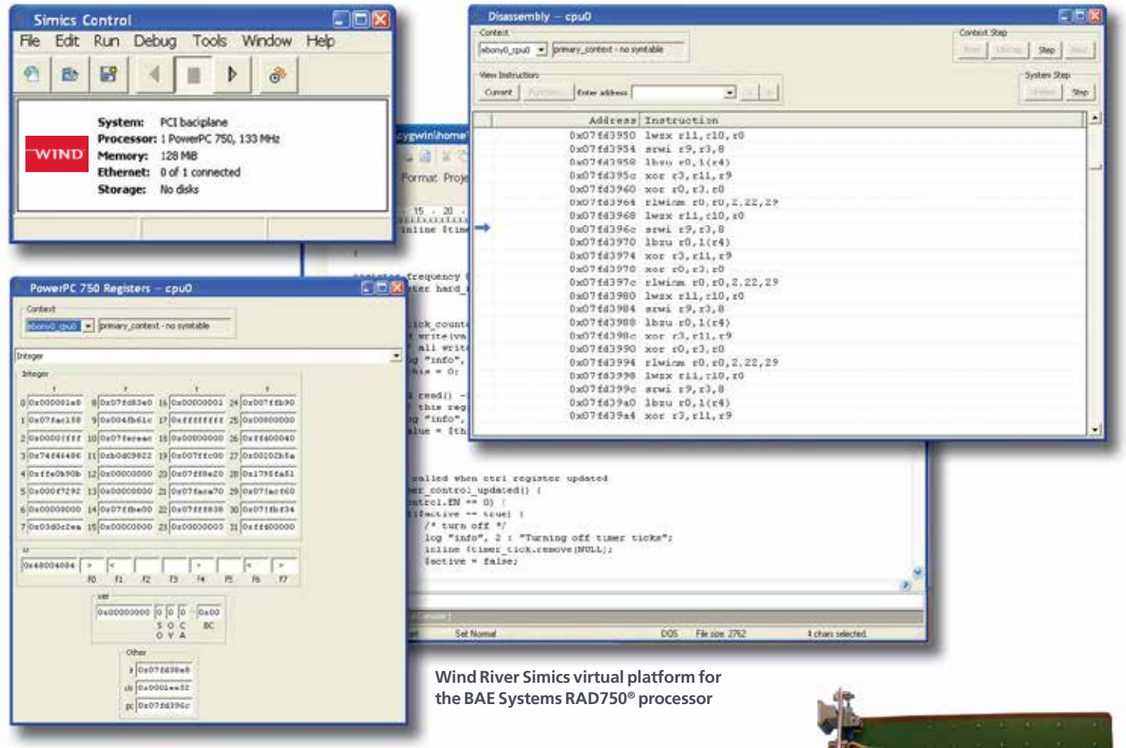


- Triplicated flash with FPGA controller options available

Software tools

Wind River® Simics provides a virtualized instance of the RAD750® component, designed specifically to support software development efforts. This full system simulator includes the RAD750® microprocessor and the devices found on the RAD750® 3U, 6U, and 6U extended boards. The simulator reduces risks and allows software development long before physical hardware is available. This helps ensure that projects are finished on time and within budget.

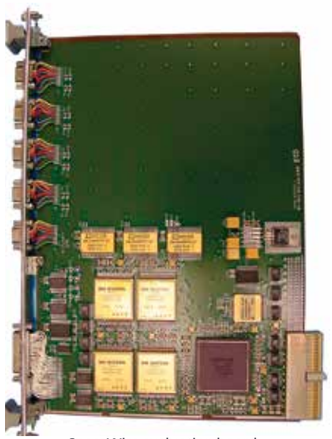
Wind River® Simics is a registered trademark of Wind River.



Wind River Simics virtual platform for the BAE Systems RAD750® processor

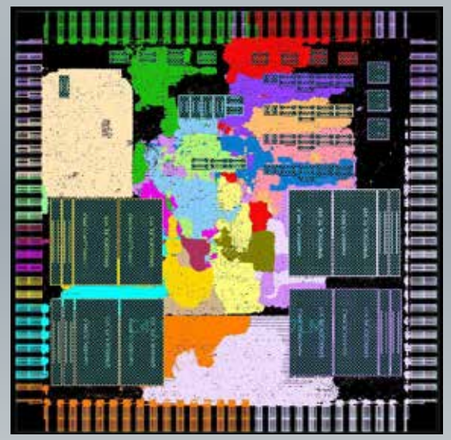
Interface, microcontroller, and evaluation boards

Product name (PN)	Part number (P/N)	Card format	EMC (MIPs)	L2 cache	SRAM	SDRAM	EEPROM	SuROM	Connector	On-card POR	Power control EEPROM	SpaceWire	1553
SpaceWire 4-port router evaluation board	8421831-1	6U	6	No	8 MB	None	None	256 KB EEPROM	CompactPCI	No	No	4-port with router	No

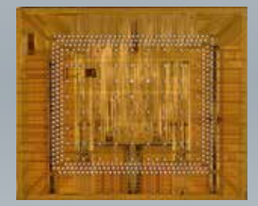


SpaceWire evaluation board

ASIC technologies



Design



Final product

High density, optimized power and performance

Flexible engagement models, state-of-the-art deep sub-micron design flow

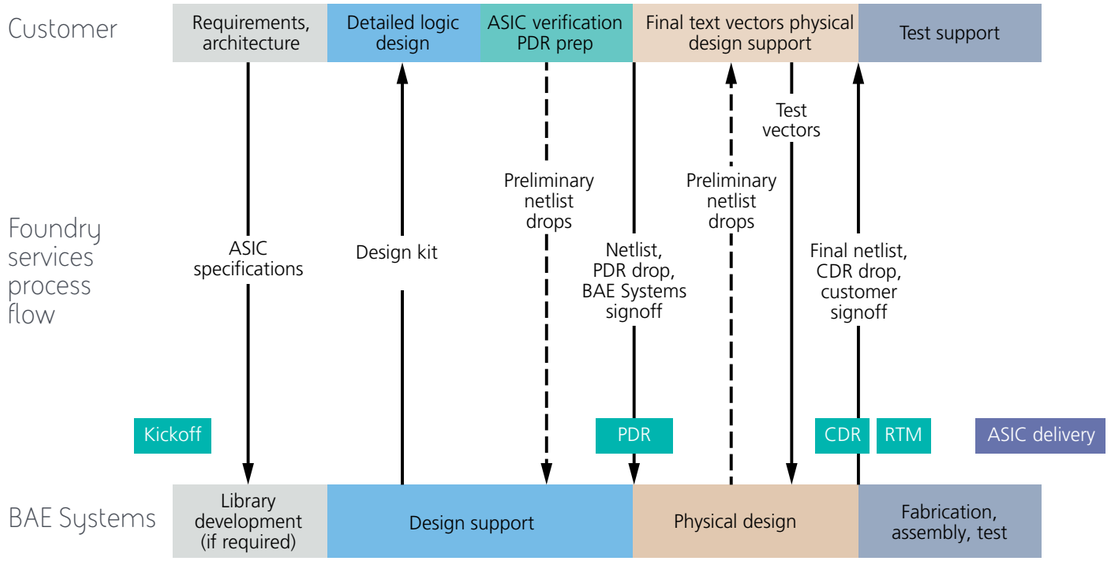
ASIC technology

Technology parameters	RH45® technology	RH14
Technology	SOI	FinFET
Process node (nm)	45	14
Voltages (V)	0.95 I/O Voltages: 1.5 / 1.8 / 2.5 / 3.3	0.8 / 1.8 / 2.5
Wireable gates (millions)	up to 300	up to 800
Maximum core frequency	1.5 GHz	
High-speed logic island max frequency	2 GHz	5GHz
Metal levels	10	
Radiation tolerance — total dose	1 Mrad(Si)	300K rad(s)
ASIC library options		
Standard cell	A	A
Structured ASIC	–	
Mixed signal extensions	A	A
Memory options		
Single port	A	A
Dual port	A	A
Power management options		
Clock gating (by design or through synthesis)	A	A
Multi-vt design libraries	A	A
Low-voltage library extensions	A	A
Package options		
CMOS/LVCMOS	A	A
CCGA	A	A
CQFP	A	A
Number of signal IO supported	up to 1100	
C4 flip chip	A	A
Wire bond	A	A
I/O options		
LVDS	A	D
SERDES	up to 3.125 Gbps	Up to 10 Gbps (D)
SSTL	A	A
HSTL	A	A
Schmitt trigger	A	D
LVCMOS	1.8 V, 2.5 V, 3.3 V	

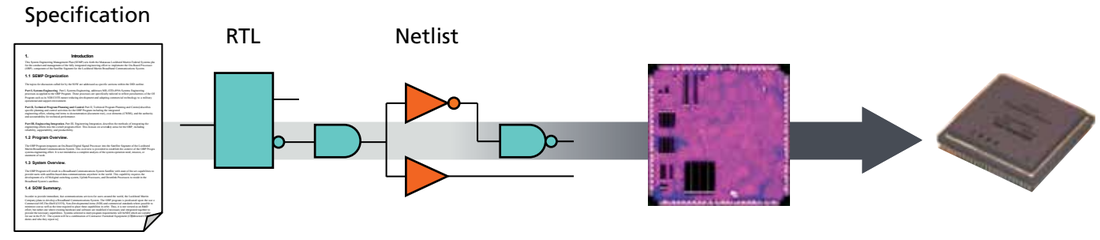
A = Available **P = Planned or in development** **D = In development** **L = Legacy products only**

ASIC design kit

ASIC design flow



ASIC entry points/technology access



ASIC design tools

Supplier	Function
Synopsys	ASIC (standard-cell/gate-array) library cell characterization, logic/physical/test synthesis, physical design, static timing analysis,custom circuit design and layout, formal/LVS/DRC verification, electromigration and voltage drop analysis, SSO, signal integrity, custom circuit simulation (fast SPICE), design for test
Mentor	VHDL/verilog simulation, LVS/DRC verification, DFT insertion and test compression
Cadence	Custom circuit/analog design and layout
TSSI	Manufacturing test pattern conversion

IP cores

IP cores	Description	Further information
OCB	On-chip bus	The OCB (on-chip bus) is a cross-bar network used to connect various on-chip functional blocks, often referred to as cores. The OCB has the following two implementation versions: low-performance OCB for interconnecting cores that do not have a high-bandwidth requirement and for providing isolation of high-bandwidth cores from cores with lesser performance requirements. High performance OCB for interconnecting cores that require high-bandwidth data paths.
OCB	Extension	Extends OCB off-chip and includes OCB Master and OCB Slave
AMCC	Advanced memory controller core	The advanced memory controller core (AMCC) is designed to interface to external memory (SDRAM, SSRAM, SRAM, or ROM). SRAM can refer to non-synchronous devices as well as non-volatile devices such a NVRAM or C-RAM. ROM can refer to any type of read-only memory device (e.g., ROM, PROM, EEPROM, Flash ROM).
AXI to Wishbone Slave only Bridge	Bridge	Bridges an AXI Slave interface to Wishbone Master Interface
mBIST	Built in self-test	The BIST core provides a comprehensive set of design-for-testability features. It contains the circuitry necessary to perform functional, lab, and manufacturing testing of a chip, and may be configured for chips of different sizes and with different testability requirements. Functions supported by the BIST core include clock control, hardware and software reset, logic BIST, array BIST, scan string connection, labscan, mode signal generation, OCD/OCR control signal generation, and manufacturing test modes.
TCB	Test control block	The TCB core supports the following functions: test core, memory BIST support, JTAG support, reset logic, manufacturing test support, oscillator and register control, system clock divide, phase-locked loop (PLL) management, and power management.
D1553	DDC 1553 support	The D1553 core provides the necessary support logic to map a DDC ACE-core into an OCB-based, system-on-chip environment. The DDC ACE-core provides a complete MIL-STD-1553 B solution.
DDC 1553	DDC enhanced Min-ACE	The enhanced mini-ACE family (enhanced mini-ACE, micro-ACE, mini-ACE mark 3, micro-ACE TE) of MIL-STD-1553 terminals enable complete interfaces between a host processor and a 1553 bus. These terminals integrate dual transceiver, protocol logic, and 4K words or 64K words of RAM. The BC/RT/MT versions with 64K words of RAM include built-in RAM parity checking.
DMAC	DMA controller	The DMA controller core provides a simple descriptor-based DMA engine that can perform data transfers between any two address spaces accessible via its OCB interface. The DMA controller will operate on descriptor control blocks stored in linked-list format off the OCB address space. Beyond setting up the DMA descriptors, no other host CPU support is required.
EMC	Embedded microcontroller	The EMC core offers a simple, micro-controlled sequencer that provides flexibility for handling reset-initialization sequences and error-handling functions. The EMC core is a RISC-based micro-controller that provides simple, logical, arithmetic, branch, and vector interrupt capabilities.
FIFO	First in, first out	The EXT_FIFO core provides the capability to map a general FIFO interface (GFI) core transmit and receive ports to an off-chip FIFO interface. It also enables the data-width adjustment from the 4-byte GFI interface to a single-byte external interface
FLASH	Non-volatile flash memory controller	The flash controller provides an interface to the triple modular redundant 8-bit flash memory. It also provides execution of supported flash commands and buffering of flash data and status via a 64-bit SkyBlue interface. The TMR flash controller is able to detect and correct errors on the flash read data path. It supports selectable interrupt conditions, logging of both correctable and uncorrectable TMR errors, and provides power switching control to flash memory.

IP cores	Description	Further information
GFI	Generic FIFO interface	The GFI core enables the transport of data between the OCB and a generic user interface consisting of separate transmit, receive, and configuration ports. The GFI core masters data transfers between the OCB and transmit port using a transmit DMA engine. It also masters data transfers between the OCB and receive port using a receive DMA engine. Both DMA engines are controlled via a linked-list descriptor chain.
GPIO	Generic peripheral input/output	General purpose input and output at the chip or board level.
I2C	Inter-integrated circuit serial bus	I2C is a two-wire, bi-directional serial bus that offers a simple and efficient method of data exchange between devices. It is most suitable for applications requiring occasional communication over a short distance among many devices. The I2C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.
JTAG	Joint test action group	The JTAG slave core provides a test access port (TAP) and associated logic to support a fully compliant IEEE Standard 1149.1a JTAG interface to the OCB. The JTAG slave core consists of four subcores: an OCB master stub subcore, the JTAG OCB/decoder subcore, the JTAG slave/TAP subcore, and the JTAG slave boundary subcore.
MDL	Manchester data link	The MDL core consists of a separate transmitter module and a separate receiver module. The transmitter module (a parallel-to-serial converter) and the receiver module (a serial-to-parallel converter) are used to provide serialized, one-way data transfer between two terminals over the RS-422 physical interface.
MISC	Miscellaneous	The miscellaneous core has a set of registers mapped to the slave OCB interface that provide control and status information. It also provides several primary I/O signals along with sideband signals for connection to other cores within the ASIC.
P60X	60x bus	The 60x bus core is an electronic circuit that transmits and receives data over the 60x bus used by the PowerPC family of processors, a memory controller interface, and an OCB.
PCI	PCI - 32 and 64 bit, tgt, mstr, init.	The PCI core provides a PCI master and target interface and an optional PCI central resource function. The PCI core provides an OCB application interface that is asynchronous to the PCI interface. Internal buffering of data and command queues is provided by the core along with all control necessary to operate the interfaces and buffers. There are 32- and 64-bit versions of this core.
RIF	SpaceWire router interface	The RIF core enables the transport of data between the OCB and the SpaceWire router core. It accomplishes this with separate transmit DMA engine and a receive DMA engine. Each engine is controlled via a linked-list descriptor chain.
PLL	Rad-hard, phase-locked loop	The PLL core is used for clock de-skewing in ASIC chips. The internal ASIC clocks are phase-aligned to a common external system clock. The PLL features include a fully integrated mixed-mode PLL design, wide lock-in range: 30 – 250 MHz, and programmable 1x-10x output-to-input frequency ratio.
SEMC	Embedded microcontroller	High performance version of EMC

IP cores	Description	Further information
SERDES	Serializer/ deserializer	The SERDES product reduces board complexity by converting a wide data bus and clock into a serial data stream transmitted through a twisted pair. It supports a series of industry standard protocols, and up to 3.125 Gbps full duplex.
SRAM	Static random-access memory	The SRAM core is designed to store blocks of data addressed and mapped onto the OCB.
TMR	Flash controller	TMR version of the flash controller
UART	Universal asynchronous receiver/ transmitter	The UART core transmits and receives data through the serial port, allowing for programmability and implementing the requirements of the 16550 UART.
SPI MESH	Serial peripheral interface MESH	A microcontroller that controls four SPI interfaces- programmable from the OCB. It has a master OCB interface to write back data it receives from the SPI ports. It can support up to eight controllers, and a total of 32 SPI interfaces. The interface also supports a bypass mode where the microcontroller is not used.
DDMA-AXI	Dual DMA controller to AXI	The DMA controller core provides a simple descriptor-based DMA engine that is able to perform data transfers between any two address spaces accessible via its AXI interface. The controller will operate on descriptor control blocks that are stored in linked list format off the AXI address space. Beyond setting up the DMA descriptors, no other host CPU support is required

Services

Qualified, trusted and accredited

Design, packaging, assembly, testing, and screening

Services

Services	Description
Design	Expertise in ASIC, FPGA, custom and semi-custom designs. Experienced designers in the areas of digital and mixed signal design, comprehensive logical and physical design methodologies, and the art of identifying and realizing efficient implementations tuned for power-performance and platform execution. Familiarity with design integration for unique and emergent technologies. Flexible engagement models and entry points from specification to GDSII.
FPGA to ASIC conversions	Established FPGA-to-ASIC conversion method, based on experience from internal and external development programs. Mapping of design and constraints handled in a structured manner, exploiting target ASIC technology features. Multiple FPGA to single ASIC conversions available.
Advanced packaging	Broad selection of cost-effective, space-qualified technologies for high-density packaging to meet the needs of high-performance applications. Offers DSCC full military-standard screens. Wide range of qualified flip-chip, wirebond and hermetic ceramic packages available. Memory stacking offered for increased density. Qualified, high-reliability and high-performance ceramic column grid array (CCGA) packages for military and plastic ball grid array (BGA) for commercial applications are available.
Advanced testing	Capabilities include logic and memory testing at wafer and module levels, with full mil-spec temperature test capabilities. Services include test program development through full production including static and dynamic burn-in. Extensive chip diagnostic experience and expertise with scan and other DFT techniques, fault isolation, schmoo plotting and parametric analysis. Support during design is available.
Failure analysis	Expertise in advanced failure analysis techniques. Failure analysis instruments include photo-emission, transmission and scanning electron microscopes and a focused-ion-beam system that supports technology development and semiconductor diagnostics. Destructive physical analysis (DPA), fault localization and characterization, prohibited materials analysis and counterfeit inspection services available.

Quality

- AS9100 quality management system
- Trusted source
- Category 1A
  (Design services, aggregation services, broker services, packaging/assembly services, testing services)
- QML (V, Q, RHA)
  - Class V or Q
    (radiation hardened space qualified)
  - Class K, H, or E
    (hybrid multi-chip module compliant)
- Technology conformance inspections (TCI) and screening per MIL-PRF-38535 and MIL-STD-883

Abbreviations and acronyms

ASIC	Application-specific integrated circuit
ASSP	Application-specific standard product
ATPG	Automatic test pattern generation
AXI	Advanced eXtensible interface
CCGA	Ceramic column grid array
CDR	Critical design review
CGA	Column grid array
cPCI	CompactPCI
CPU	Central processing unit
CQFP	Ceramic quad flat pack
C-RAM	Chalcogenide random access memory
DLA	Defense Logistics Agency
DRC	Design rule check
DMAC	Direct memory access controller
DSCC	Defense Supply Center Columbus
EDU	Engineering development unit
EEPROM	Electrically erasable programmable read-only memory
En-PPCI	Enhance PowerPCI ASIC
FIFO	First-in first-out memory
FP	Flatpack
FPGA	Field-programmable gate array
GVSC1750	Generic VHSIC spaceborne computer - MIL-STD-1750
HSTL	High speed tranceiver logic
I2C	Inter-integrated circuit serial bus
IP core	Intellectual property core
LVDS	Low voltage differential signal
LVS	Layout versus schematic
MIL-STD	Military standard
N/A	Not applicable
NV	Non-volatile
OSC	Oscillator
PCI	Peripheral component interface
PDR	Preliminary design review
P/N	Part number
POR	Power-on reset
Power Ctrl	Power control
PROM	Programmable read-only memory
QML	Qualified manufacturer list
RMAP	Remote memory access protocol
RTL	Register transfer logic
SDRAM	Synchronous dynamic random access memory
SERDES	Serializer/deserializer
Si	Silicon
SMD	Standard microcircuit drawing
SoC	System-on-chip
SPI	Serial peripheral interface bus
SPICE	Simulation program with integrated circuit emphasis
SRAM	Static random access memory
SSRAM	Synchronous static random access memory
SSTL	Stub series terminated logic
SuROM	Start-up read-only memory
VHDL	VHSIC hardware description language
VHSIC	Very-high-speed integrated circuit

Notes

Notes

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