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Wafer Level Chip Scale Package (WLCSP)

1 Introduction

This application note provides guidelines for the handling and assembly of Freescale WLCSP (Wafer Level Chip Scale Package) during printed circuit board (PCB) assembly. PCB design, rework, and package performance information such as Moisture Sensitivity Level (MSL) rating, board level reliability, mechanical, and thermal resistance data are also included for reference.

2 Scope

This document contains generic information that encompasses Wafer Level Chip Scale Packages (WLCSP). Specific information about each device is not provided. To develop a specific solution, actual experience and development efforts are required to optimize the assembly process and application design per individual device requirements, industry standards (such as IPC and JEDEC), and prevalent practices in the assembly environment. For more details about the specific devices contained in this note, visit www.freescale.com or contact the appropriate product application team.

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3 Wafer Level Chip Scale Package (WLCSP)

3.1 Package Description

Wafer Level Chip Scale Package refers to the technology of packaging an integrated circuit at the wafer level, instead of the traditional process of assembling individual units in packages after dicing them from a wafer. This process is an extension of the wafer Fab process, where the device interconnects and protection is accomplished using the traditional fab processes and tools. In the final form, the device is a die with an array pattern of bumps or solder balls attached at an I/O pitch that is compatible with traditional circuit board assembly processes. WLCSP is a true chip-scale packaging (CSP) technology, since the resulting package is of the same size of the die as shown in Figure 1. WLCSP technology differs from other ball-grid array (BGA) and laminate-based CSPs in that no bond wires or interposer connections are required. The key advantages of the WLCSP is the die to PCB inductance is minimized, reduced package size, and enhanced thermal conduction characteristics.

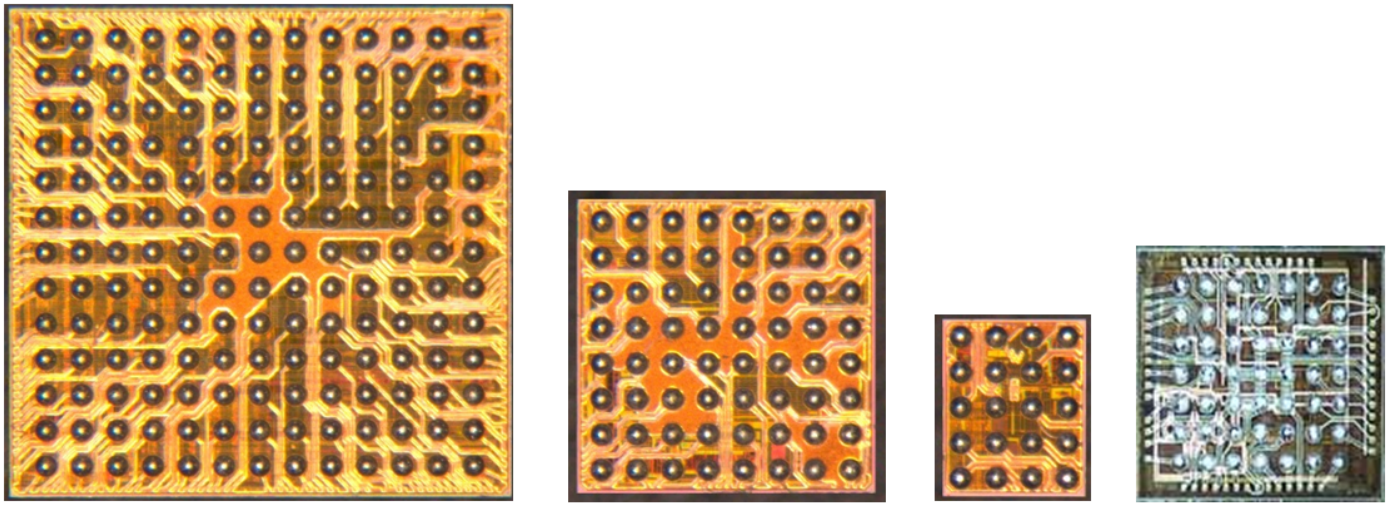

Figure 1. WLCSP Packages Available from Freescale

3.2 Package Dimension

Freescale offers WLCSP size and thicknesses with various options of I/O (solder balls) and a standard ball pitch of 0.40 and 0.50 mm. The physical outlines of WLCSP are dynamic since those depend on actual die size. Refer to Freescale package case outline drawings to obtain detailed dimensions and tolerances, which complies to JEDEC Publication 95, Design Guide 4.18 [1] and JEDEC Standard MO-211. [2] Package size and ball pitch are continually in review, check with the Freescale sales team for more information.

3.3 WLCSP Cross-section

The cross-section drawing in Figure 2 is included to show the representative internal layers of typical WLCSP package with a single redistribution layer (RDL) between two dielectric layers. A typical WLCSP die has a first layer of dielectric, conductive metal RDL to redistribute the signal path from the die peripheral to a solder ball pad, and a second dielectric layer to cover the RDL metal, which in turn is patterned into the solder ball array. The solder ball is a lead-free alloy. Construction is capable to have two RDL metal layers for more complex routing. Over molded construction is also available for high board level reliability requirements.

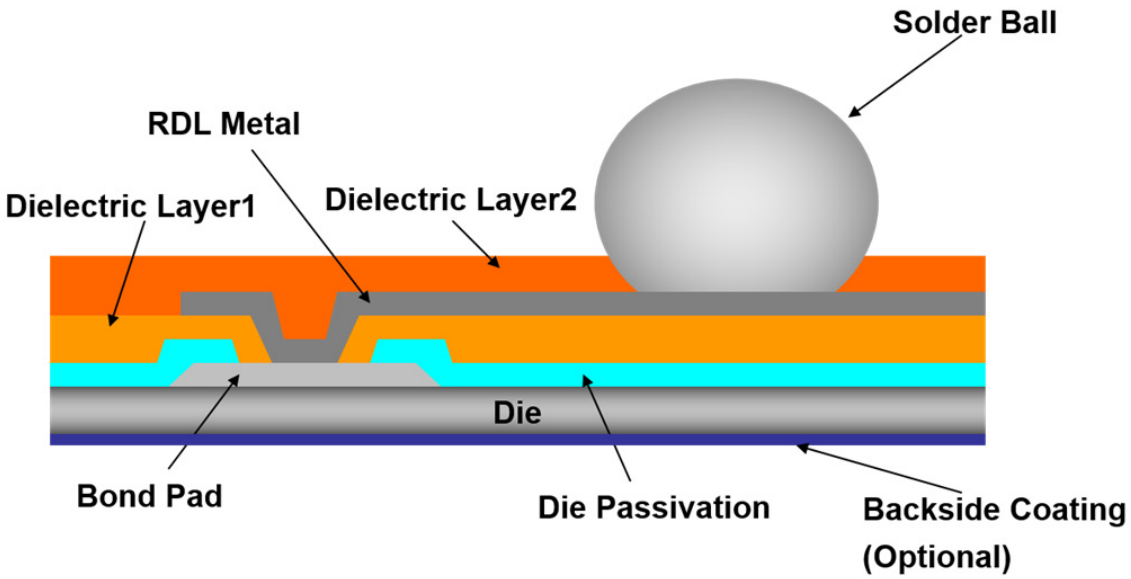

Figure 2. Typical Polymer-RDL WLCSP Construction

3.4 Process Flow

A typical WLCSP process flow is illustrated Figure 3. The illustration displays the process for a single-layer RDL process, with the RDL metal layer between two dielectric layers.

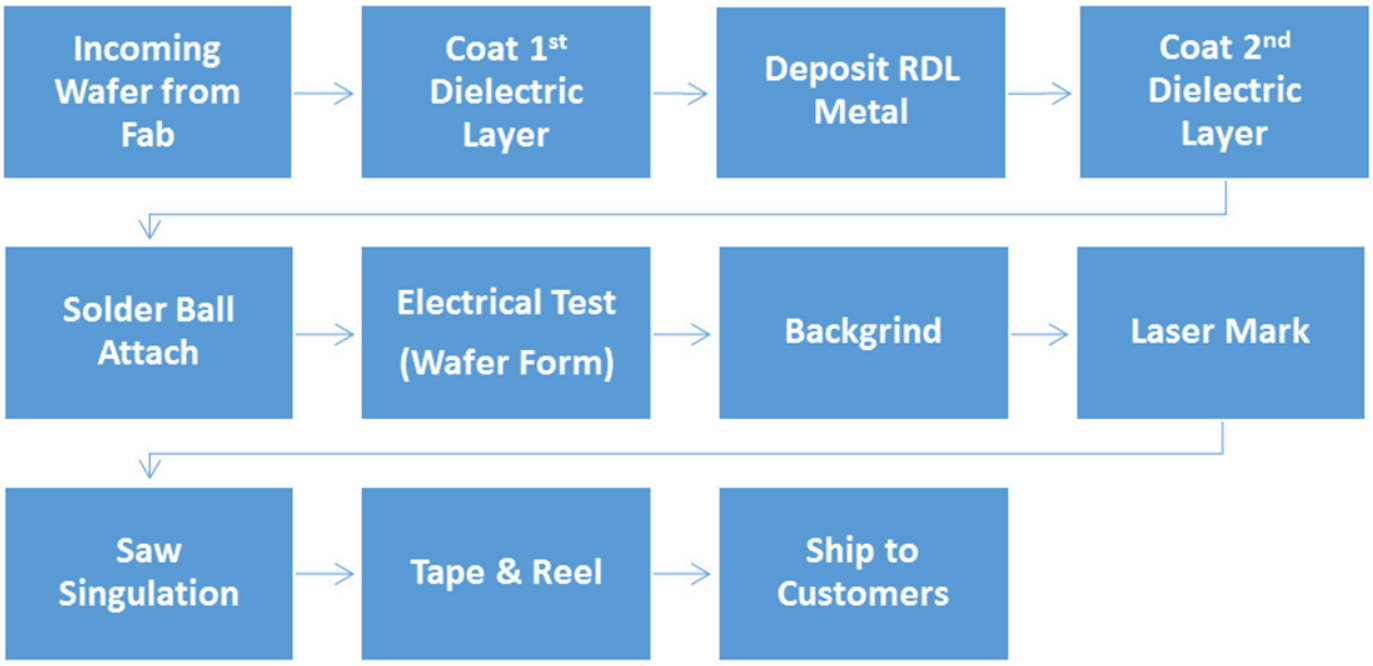

Figure 3. Typical WLCSP Process Flow

4 Printed Circuit Board Guidelines

4.1 PCB Design Guidelines

Proper PCB footprint and stencil designs are critical to ensure high surface mount assembly yields, and electrical and mechanical performance. The design starts with obtaining the correct package drawing. Package case outline drawings are available at www.freescale.com.

Follow the procedures in Downloading the Information from Freescale, Page 12. Figure 4 shows an example of a of a 5.29 x 5.28 mm 120 WLCSP Case Outline drawing.

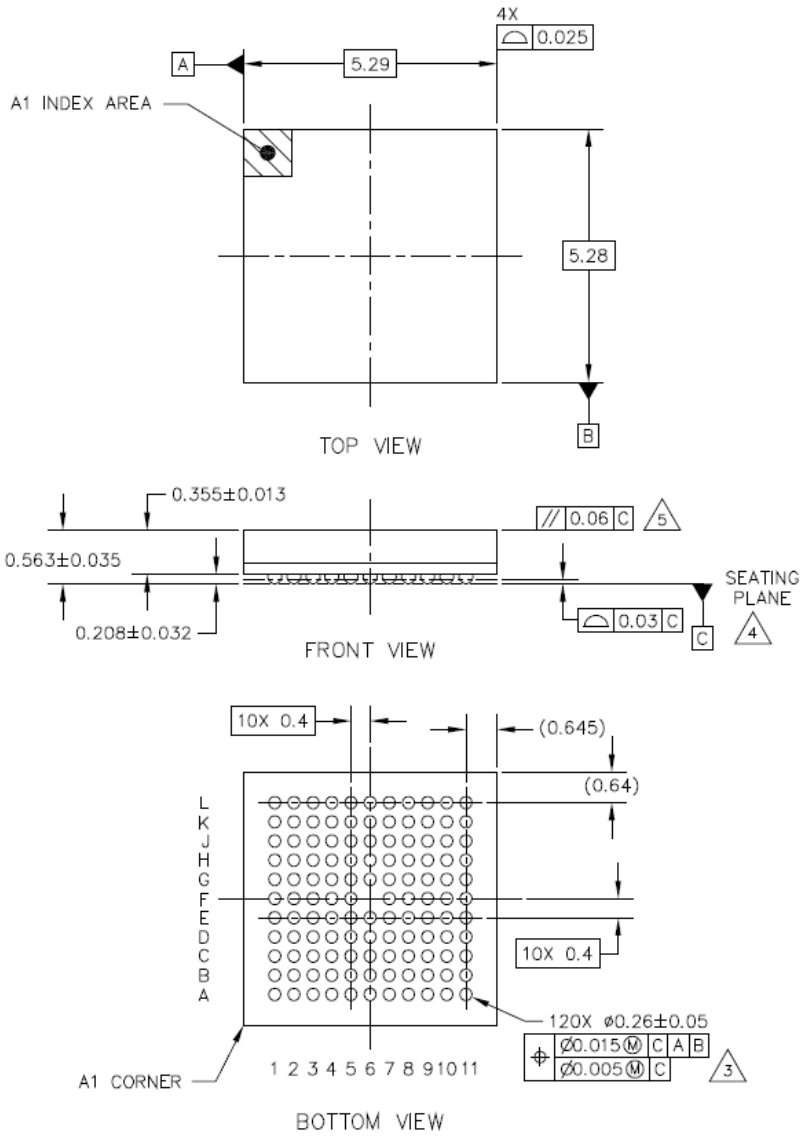

Figure 4. 5.29 x 5.28 mm 120 WLCSP Case Outline (98ASA00311D)

4.2 PCB Pad Design

Freescale follows the generic requirements for Surface Mount Design and Land Pattern standards from the Institute for Printed Circuits (IPC), IPC-7351B. This document and an accompanying land pattern calculator can be purchased from the IPC's web site (http://landpatterns.ipc.org/default.asp) and includes guidelines for BGAs, based on assumed package dimensions.

Many BGA products do not have fully populated arrays to allow for better PCB (printed circuit board) routing. PCB design must ensure the final footprint matches the part.

4.2.1 Pad Diameter

Table 1. Suggested PCB Pad Diameters

Description	0.40 mm Pitch WLCSP	0.50 mm Pitch WLCSP
PCB Pad Shape	Round	Round
PCB Cu Pad Diameter	220 um	280 um

4.2.2 Pad Surface Finish

PCB finish compatible with WLCSP include Organic Solderability Protectant (OSP) and Electroless Nickel Immersion Gold (ENIG, Au < 0.5 um to avoid solder joint embrittlement). Freescale suggests the PCB surface finish shelf life be monitored to ensure the life has not “expired”. Surfaces should always be free of dirt and grease before PCB assembly.

4.2.3 Solder Mask Layer

Solder Mask Defined (SMD) pads are defined by the solder mask opening on the board pad as shown in Figure 5. The opening of the solder mask is smaller than the underlying copper area for soldering to the associated bump. A Non-Solder Mask Defined (NSMD) pad has a solder mask opening larger than the copper pad. There are many factors influencing whether the PCB designer uses SMD or NSMD pads. Either type can successfully be used with WLCSP packages. Freescale recommends using NSMD pads for thermal fatigue and SMD pads for drop test performance. Fillets where the trace connects to the Cu pad are recommended, especially with NSMD pads.

The NSMD solder mask opening diameter is suggested to be 0.10 mm larger than the solderable area (i.e. Cu diameter). However, it is critical to understand the PCB fabrication capabilities of PCB suppliers.

SMD pads (compared to NSMD) have a larger Cu diameter which means more Cu is joined to the PCB laminate. Copper diameter for SMD is 0.10 mm larger than solder mask opening diameter. This increased diameter makes pad cratering on the PCB more difficult, and therefore increases drop/shock life. For SMD at smaller pitches, a key factor of picking the Cu diameter and solder mask diameter is PCB vendor capabilities. Inspection of delivered PCBs for solder mask registration is encouraged.

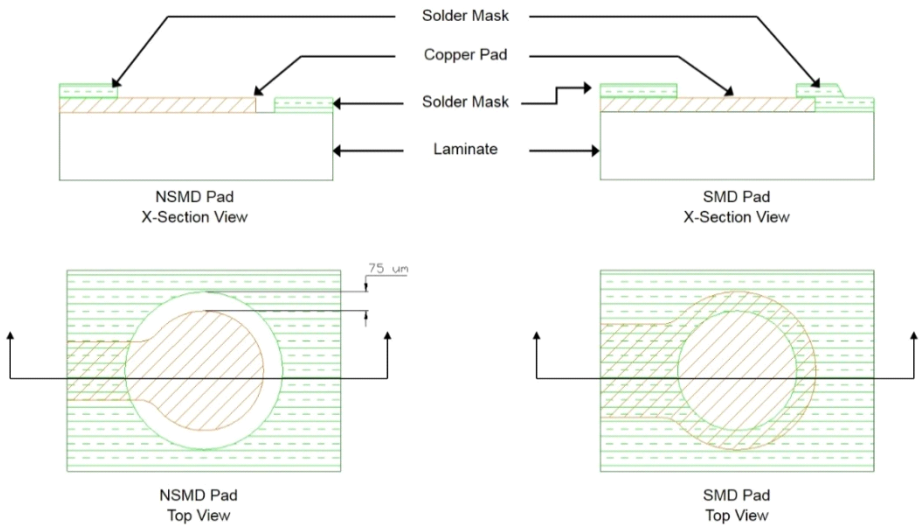

Figure 5. NSMD and SMD Pad Designs for WLCSP PCB Terminal

4.3 Via-In-Pad Structures

The need for via-in-pad structures is generally determined by the design. Via-in-pad designs typically result in voids and inconsistent solder joints after reflow, leading to early failures. These voids are due to trapped air in the via. If via-in-pad structures are used, it is recommended to use filled vias. As with any PCB, the quality and experience of the vendor is very important with via-in-pad designs.

5 Board Assembly

5.1 Assembly Process Flow

A typical Surface Mount Technology (SMT) process flow is shown in Figure 6.

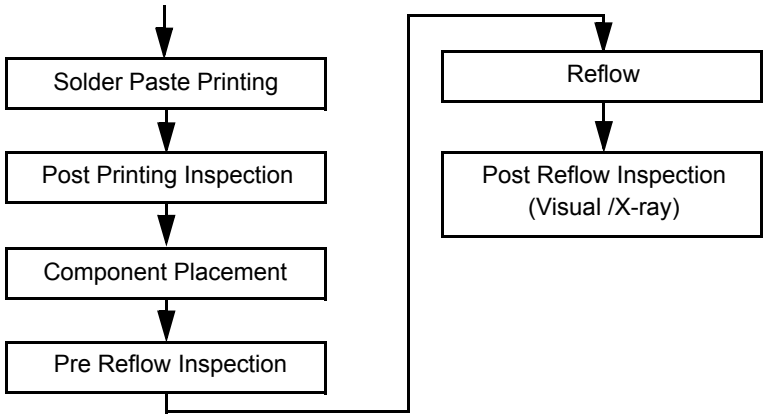

Figure 6. SMT Process Flow

5.2 Solder Stencil / Solder Paste

5.2.1 Stencil Thickness

Solder paste stencil design is critical for good solder joint formation, especially as the ball pitch decreases. The thickness of the stencil and the apertures determine the amount of solder paste deposited onto the printed circuit board land pattern.

Stencils should be laser cut stainless steel with Nickel plating or electroformed Cobalt or Chromium hardened Nickel for repeatable solder paste deposition from ultra-small apertures required by small pitch packages. It is recommended to inspect the stencil openings for burrs and other quality issues prior to use.

Both square and round shaped apertures have been used successfully, however square shaped aperture openings provide more consistent paste printing and transfer efficiency when compared to round openings. Corners may be rounded to prevent clogging.

For 0.50 mm pitch WLCSP devices, 1:1 aperture to pad ratio is recommended for SnAgCu alloys.

For 0.40 mm pitch WLCSP devices, use aperture aspect ratio of >= 0.66, with 0.25 mm x 0.25 mm square openings (25 micron corner radius) for improved solder paste deposition repeatability. Aperture aspect ratio is defined as the aperture opening area divided by the aperture side wall surface area.

A 0.100 mm (4-mil) thick stainless steel stencil is recommended. When these stencil design requirements conflict with other required SMT components in a mixed technology PCB assembly, a step-down stencil process may be utilized in compliance with IPC-7525 [4] design standards.

5.2.2 Solder Paste Properties

Solder paste is one of the most important materials in the SMT assembly process. It is a homogenous mixture of metal alloy, flux, and viscosity modifiers. The metal alloy particles are made in specific size and shape. Flux has a direct effect on soldering and cleaning, and it is used to precondition the surfaces for soldering (by removing minor surface contamination and oxidation).

Solder paste grain size can be useful to manipulate by pitch. Type 4 solder (20 to 38 microns grain size) or finer solder paste is recommended and a low halide (< 100 ppm halides) No-Clean rosin/resin flux system be used to eliminate post-reflow assembly cleaning operations.

5.3 Component Placement

The WLCSP package is comparatively small in size. For better accuracy, it is recommended to use automated fine-pitch placement machines with vision alignment instead of chip-shooters to place the parts. Local fiducials are required on the board to support the vision systems.

Pick and Place systems using mechanical centering are not recommended due to the high potential for mechanical damage to the WLCSP device. Ensure minimal pick-and-place force is used to avoid damage, with all vertical compression forces controlled and monitored. Z-height control methods are recommended over force control. Freescale recommends the use of low-force nozzle options and compliant tip materials to further avoid any physical damage to the WLCSP device. Use only vacuum pencil with compliant tip material whenever manual handling is required.

All assemblers of WLCSP components are encouraged to conduct placement accuracy studies to provide factual local knowledge about compensations needed for this package type. Freescale cannot anticipate the range of placement equipment and settings possible for package placement and therefore cannot make a generic recommendation on how to compensate for WLCSP interchangeability.

5.4 Soldering

Temperature profile is the most important control in reflow soldering and it must be fine-tuned to establish a robust process. The actual profile depends on several factors, including complexity or products, oven type, solder type, temperature difference across the PCB, oven and thermocouple tolerances, etc. All of Freescale's WLCSP devices are qualified at Moisture Sensitivity Level 1 at 260°C. The maximum temperature at the component body should not exceed this level. Actual reflow temperature settings need to be determined by the end-user, based on thermal loading effects and on solder paste vendor recommendations.

5.5 Inspection

The solder joints of WLCSP parts are formed underneath the package. To verify any open or short-circuits (bridging) after reflow, non-destructive vision/optical inspection and X-ray inspection are recommended to verify any open or short-circuit after reflow soldering. Micro-sectioning is another method of inspecting solder joint quality during process optimizations, but it is less suitable to production inspection (due to slow processing). Figure 7 shows the expected x-ray image of soldered component.

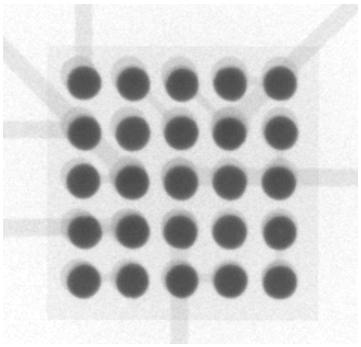

Figure 7. Inspection X-ray of a MAPBGA Package (Similar to WLCSP Image)

6 Repair and Rework Procedure

WLCSP components removed during PCB rework should not be reused for final assemblies. Freescale follows standard component level qualifications for packages/components and these include three solder reflows survivability. A package that has been attached to a PCB and then removed has seen two solder reflows and if the PCB is double sided, the package has seen three solder reflows. Thus the package is at or near the end of the tested and qualified range of known survivability. These removed WLCSP components should be properly disposed of so that they will not mix in with known good WLCSP components.

The rework process for WLCSP devices is similar for typical BGA and CSP packages:

- To remove the faulty component from the board, hot air should be applied from the top and bottom heaters. An air nozzle of correct size should be used to conduct the heat to the WLCSP component such that the vacuum pick up tool can properly remove the component. It is recommended to apply top and bottom heaters simultaneously for 30 seconds at 300 °C and 150 °C, respectively. Many assembly sites have extensive in-house knowledge on rework and their experts should be consulted for further guidance.
- Once the WLCSP component is removed, the site is cleaned and dressed to prepare for the new component placement. A de-soldering station can be used for solder dressing. It should be noted that the applied temperature should not be >245 °C, otherwise the copper pad on the PCB may peel off.
- A mini-stencil with the same stencil thickness, aperture opening and pattern as the normal stencil should be used. Apply a gel or tacky flux using a mini-metal squeegee blade. The printed pads should be inspected to ensure even and sufficient solder paste before component placement.
- A vacuum nozzle is used to pick the new package up, and accurately place it using a vision alignment placement tool. A split light system that displays images of both the WLCSP leads and the footprint on the PCB is recommended.

The replaced component is then soldered to the PCB using a temperature profile similar to the normal reflow soldering process.

7 Board Level Reliability

The board level reliability is usually presented in terms of solder joint life. The solder joint results in this section utilized the board layout guidelines from Section 4.1.

7.1 Testing Details

Solder Joint Reliability (SJR) testing is performed to determine a measure of board level reliability when exposed to thermal cycling. There are several different names for board level reliability (BLR) that customers may see. These include: second level reliability (2nd level reliability), solder joint reliability (SJR), and temperature cycling on board (TCoB).

Information provided here is based on experiments executed on WLCSP devices using a daisy chain BGA configuration. Actual surface mount process and design optimizations are recommended to develop an application specific solution.

SJR temperature cycling conditions may vary widely, depending on the application and specific user. Typically, Freescale SJR testing is performed by temperature range for -40 °C to +125 °C and/or 0 °C to +100 °C.

The preferred test method will vary by market and industry. For automotive, the primary test is a version of IPC-9701A, air temperature cycling. For the consumer market, JEDEC's drop test will be the primary test (JESD22-B111 Drop Test Specification [7]). Telecommunications uses both IPC-9701A and IPC-9702 (monotonic bend). Freescale may not test an electronic package for drop and bend test at all as because of the applications vary for each market and industry

Samples of WLCSP in daisy chain format were used to study the solder joint reliability. BGA pairs were routed together in the WLCSP RDL layer, with a complementary pattern designed on the test PCB to provide one electrical circuit (net) through the package when the package is attached to the test PCB, as illustrated in Figure 8.

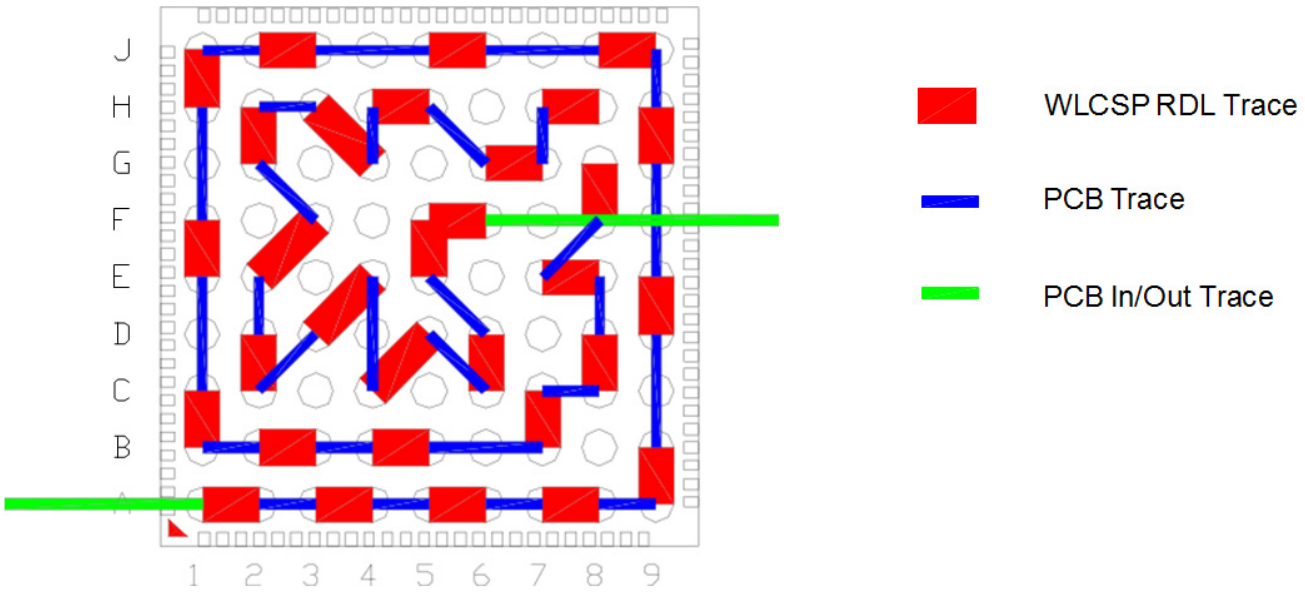

Figure 8. Example WLCSP / PCB Daisy Chain Routing (Not to Scale)

7.2 Board Level Reliability Results

Freescale experimentally gathers board-level reliability data for a variety of packages including temperature cycled Solder Joint Reliability (SJR) and Mechanical Drop Test. To get results from these experiments (including Weibull plots), contact the Freescale sales team. Customers should interpret the Freescale solder joint reliability data to see how well they meet the final application requirements.

7.3 Underfill

Underfilling can significantly increase board level reliability of WLCSP packages. Freescale experiment demonstrated 7X improvement of solder joint reliability life. Careful selection of underfill material is critical for enhancing BLR performance of WLCSP packages since selecting an underfill with too high a CTE can result in worse BLR performance than no underfill.

8 Thermal Characteristics

8.1 General Thermal Performance

Since the thermal performance of the package in the final application depends on a number of factors (i.e. board design, power dissipation of other components on the same board, ambient temperature), the thermal package properties provided by Freescale should only serve as a guideline for the thermal application design. In applications where the thermal performance is considered to be critical, Freescale recommends to run application specific thermal calculations in the design phase to confirm the on-board thermal performance.

8.2 Package Thermal Characteristics

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

Additional factors needing be considered in PCB design and thermal rating of the final application, amongst others are:

- Thermal resistance of the PCB (thermal conductivity of PCB traces, number of thermal vias, thermal conductivity of thermal vias)
- Quality and size of PCB solder joints (effective PCB pad size, potential solder voiding in the thermal path solder joints which may reduce the effective solder area)

The thermal characteristics of the package provide the thermal performance of the package when there are no nearby components dissipating significant amounts of heat. The stated values are meant to define the package thermal performance in a standardized environment.

Thermal properties of the individual products are usually given in the Freescale product data sheets as appropriate. Product Data Sheets are available at www.freescale.com. More detailed thermal properties may be requested by customers.

8.3 Package Thermal Properties - Definition

The thermal performance of a WLCSP package is typically specified by definition of thermal properties such as $R_{\theta JA}$, $R_{\theta JMA}$, $R_{\theta JB}$, $R_{\theta JC}$ and θ_{JT} (in °C/W). Thermal characterization is performed by physical measurements and running complex simulation models under the following conditions.

- Two thermal board types:
  - Single layer board (1s) per JEDEC JESD51-3 & JESD51-5 (exposed pad packages only)
  - Four layer board (2s2p) per JEDEC JESD51-7 and JESD51-5 (exposed pad packages only).
- Four boundary conditions:
  - Natural convection (still air) per JEDEC JESD51-2
  - Forced convection per JEDEC JESD51-6
  - Thermal test board on ring style cold plate method per JEDEC JESD51-8
  - Cold plate method per MIL SPEC-883 method 1012.1

8.3.1 $R_{\theta JA}$: Theta Junction-to-Ambient Natural Convection (Still Air)

Junction-to-ambient thermal resistance (Theta-JA or $R_{\theta JA}$ per JEDEC JESD51-2) is a one-dimensional value measuring the conduction of heat from the junction (hottest temperature on die) to the environment (ambient) near the package in still air environment. The heat generated on the die surface reaches the immediate environment along two paths:

- Convection and radiation off the exposed surface of the package, and
- Conduction into and through the test board followed by convection and radiation off the exposed board surfaces.

8.3.2 $R_{\theta JMA}$: Theta Junction-to-Moving-Air Forced Convection

Junction-to-Moving-Air (Theta-JMA or $R_{\theta JMA}$ per JEDEC JESD51-6) is similar to $R_{\theta JA}$, but it measures the thermal performance of the package mounted on the specified thermal test board exposed to a moving air (at 200 feet/minute) environment.

8.3.3 $R_{\theta JB}$: Theta Junction-to-Board

Junction-to-board thermal resistance (Theta-JB or $R_{\theta JB}$ per JEDEC JESD51-8) measures the horizontal spreading of heat between the junction and the board. The board temperature is measured on the top surface of the board near the package. The measurement uses a high effective thermal conductivity four layer test board (2s2p) per JEDEC JESD51-7. $R_{\theta JB}$ is frequently used by customers to create thermal models considering both package and application board thermal properties.

8.3.4 $R_{\theta}JC$: Theta Junction-to-Case

Junction-to-Case thermal resistance (Theta-JC or $R_{\theta JC}$ per MIL SPEC-883 Method 1012.1) indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method per MIL SPEC-883 Method 1012.1, with the cold plate temperature used for the case temperature. $R_{\theta JC}$ can be used to estimate the thermal performance of a package when the board is adhered to a metal housing or heat sink, or when a complete thermal analysis is done.

8.3.5 ψ_{JT} (Psi JT): Junction-to-Package Top

Junction-to-Package top (Psi JT or ψ_{JT}) indicates the temperature difference between package top and the junction temperature, optionally measured in still air condition (per JEDEC JESD51-2) or forced convection environment (per JEDEC JESD51-6). ψ_{JT} must not be confused with the parameter $R_{\theta JC}$. $R_{\theta JC}$ is the thermal resistance from the device junction to the external surface of the package, with the package surface held at a constant temperature, while ψ_{JT} is the value of the temperature difference between package surface and junction temperature, usually in natural convection.

8.4 Package Thermal Properties

Table 2 shows an example of the thermal characteristics typically shown in a Freescale product data sheet. The example applies to a 5.3x5.3 mm package with 120 I/O in the WLCSP configurations.

Table 2. Thermal parameters comparison (5.3x5.3 mm, 120 I/O)

Rating			Value	Unit	Notes
Junction to Ambient, Natural Convection	Single layer board (1s)	$R_{\theta JA}$	83	°C/W	(1), (2)
Junction to Ambient, Natural Convection	Four layer board (2s2p)	$R_{\theta JA}$	37	°C/W	(1), (2), (3)
Junction to Board		$R_{\theta JB}$	11	°C/W	(4)
Junction to Case		$R_{\theta JC}$	2.4	°C/W	(5)
Junction to Package Top	Natural Convection	ψ_{JT}	3.0	°C/W	(6)

Notes
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESS51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

9 Case Outline Drawing, MCDS and MSL Rating

9.1 Downloading the Information from Freescale

Freescale offers Packaging, Environmental and Compliance information at www.freescale.com in the parametric tables and also in the device information details. Enter the part number in the search box and review the package information details of the specific part.

The complete case outline drawing and the Material Composition Declaration Sheet (MCDS), following the IPC-1752 reporting format, can be downloaded as a PDF file. Information on product specific Moisture Sensitivity Level (MSL) is also available in the part details.

9.2 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) indicates the floor life of the component and its storage conditions and handling precautions after the original container has been opened. The permissible time (from opening the moisture barrier bag until the final soldering process) that a component can remain outside the moisture barrier bag is a measure of the sensitivity of the component to ambient humidity.

Most WLCSP devices are not “plastic encapsulated” hence the JEDEC-JSTD-020 spec specifying MSL rating does not apply and no MSL rating is necessary. The version of WLCSP which have some amount of plastic encapsulation are rated as MSL-1 at 260 °C peak reflow temperature. It is advised to consult the specific data sheet to verify specific MSL of a device.

Table 3. MSL Descriptions

Level Rating	Floor Life	
	Time	Conditions
1	Unlimited	30 °C / 85% RH
2	1 Year	30 °C / 60% RH
2a	4 Weeks	30 °C / 60% RH
3	168 Hours	30 °C / 60% RH
4	72 Hours	30 °C / 60% RH
5	48 Hours	30 °C / 60% RH
5a	24 Hours	30 °C / 60% RH
6	Time on Label (TOL)	30 °C / 60% RH

10 Package Handling

10.1 Handling ESD Devices

Semiconductor Integrated Circuits (ICs) and components are Electrostatic Discharge Sensitive devices (ESDS) and proper precautions are required for handling and processing them. Electrostatic Discharge (ESD) is one of significant factors leading to damage and failure of semiconductor ICs and components, and comprehensive ESD controls to protect ESDS during handling and processing must be considered.

The following industry standards describe detailed requirements for proper ESD controls. Freescale recommends users meet the standards before handling and processing ESDS. Detailed ESD specifications of devices are available in each device data sheet.

- JESD615-A - Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices
- IEC-101/61340-5 - Specification for the Protection of Electronic Devices from Electrostatic Phenomena

10.2 Packing of Devices

WLCSP devices are contained in Tape-and-Reel configurations; Tape-and-Reel is packed for transportation and storage. Packing media are designed to protect devices from electrical, mechanical and chemical damages (as well as moisture absorption), but proper handling and storage of packs are recommended. Improper handling and storage (dropping packs, storage exceeding 40 °C/90 % RH environment, excessive stacking of dry packs, etc.) increases various quality and reliability risks.

- Tape-and-Reel
  - Freescale complies with EIA-481B and EIA-481C for carrier Tape-and-Reel configuration. See Figure 9 and Figure 10.
  - Freescale complies to Pin 1 orientation of devices with EIA-481D
  - Tape-and-Reels are NOT designed to be baked at high temperatures

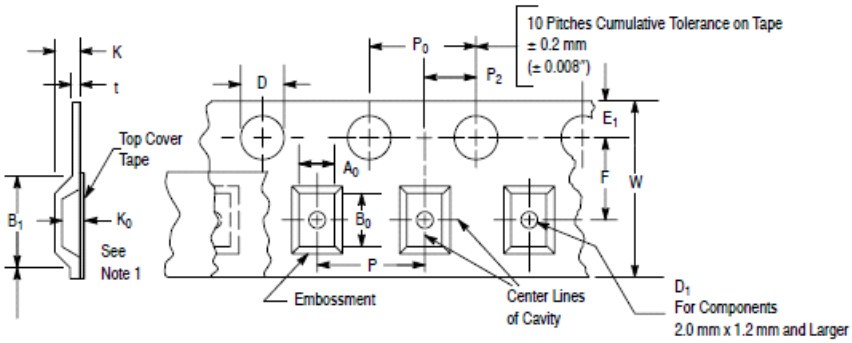

Figure 9. Carrier Tape Specifications

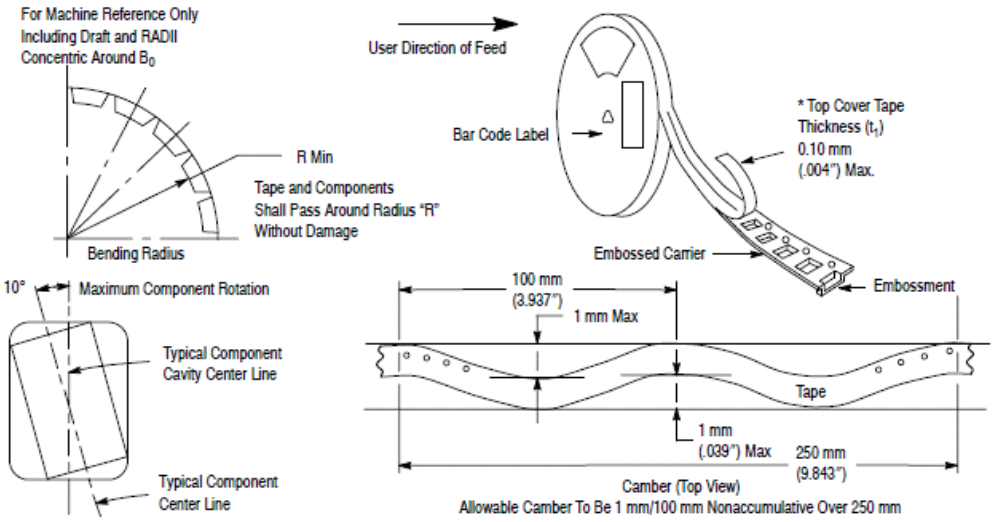

Figure 10. Tape and Reel Example

- Packing
  - Trays and Tape-and-Reels (loaded with devices) are labeled and packed in dedicated boxes with dunnage (packing materials) for the final shipment.
  - Freescale encourages the recycling and reuse of materials whenever possible.
  - Freescale does not use packing media items processed with or containing class 1 Ozone Depleting Substances.
  - Whenever possible, Freescale shall design its packing configurations to optimize volumetric efficiency and package density, to minimize the amount of packing (dunnage) and packaging entering the industrial waste stream.

Freescale complies with the following Environmental Standards Conformance guidelines/directives:

- ISPM 15, Guidelines for Regulating Wood Packaging Material in International Trade.
- European Parliament and Council Directive 94/62/EC of 20 December 1994 on packaging and packaging waste.

11 References

[1] JEDEC Publication 95, Design Guide 4.18, Wafer Level Ball Grid Arrays (WLBGA), Issue. A, September, 20004.

[2] JEDEC MO211, “Die Size Ball Grid Array, Fine Pitch, Thin/Very Thin/Extremely Thin Profile”, June 2004.

[3] ANSI/IPC-A-600G, “Acceptability of Printed Boards”, July 2004.

[4] IPC-7525, “Stencil Design Guidelines”, May 2007.

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12 Revision History

Revision	Date	Description
1.0	3/2009	• Initial release
2.0	8/2009	• Updated content
3.0	5/2012	• Updated content
4.0	8/2015	• Added revision history table • Rewrite

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