

# PROJECT WHIRLWIND

Contract N5ori60

REPORT R-127

## WHIRLWIND I COMPUTER BLOCK DIAGRAMS

VOLUME 2 OF 2 VOLUMES

SERVOMECHANISMS LABORATORY  
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

September 4, 1947

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SPECIAL DEVICES CENTER

UNCLASSIFIED

**PROJECT  
WHIRLWIND**  
(DEVICE 24-X-3)

REPORT R-127

**WHIRLWIND I COMPUTER  
BLOCK DIAGRAMS**

VOLUME 2 OF 2 VOLUMES

Submitted to the  
SPECIAL DEVICES CENTER  
OFFICE OF NAVAL RESEARCH  
Under Contract N5ori60

Report by  
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Cambridge 39, Massachusetts

Project DIC 6345

September 4, 1947

## FOREWORD

This report is a description of the Whirlwind electronic digital computers under development at the Servomechanisms Laboratory of M. I. T. for the Office of Naval Research. The arithmetic nature and the physical nature of the computers are covered briefly, and the block diagrams for the prototype computer WWI are discussed in some detail.

The report consists of two volumes: Volume 1 contains the text and Volume 2 the drawings.

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58	B-37075	Program Timing Matrix
59	C-37064	Storage Chassis Arrangement
60	B-37057	Flip-flop Storage Section
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62	B-37061	Flip-flop Storage Control
63	C-37072	Arithmetic Element
64	B-37056	Section of A-Register
65	C-37063	Accumulator Sections
66	C-37096	Accumulator Sections
67	B-37069	B-Register Sections
68	B-37097	B-Register Sections
69	B-37074	Step Counter
70	B-37065	Check Register
71	A-30874	Program Timing
72	B-37080	Timing for Add
73	B-37081	Timing for Clear and Add
74	B-37082	Timing for Subtract
75	B-37083	Timing for Clear and Subtract
76	B-37084	Timing for Multiply and Roundoff
77	B-37085	Timing for Multiply and Hold Full Product
78	B-37094	Timing for Divide
79	B-37086	Timing for Transfer to Storage
80	B-37088	Timing for Shift Right
81	B-37089	Timing for Shift Left
82	B-37090	Timing for Subprogram
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84	B-37092	Timing for Transfer Digits
85	B-37093	Timing for Special Add
86	B-37087	Timing for Store & Display
87	B-37001	Parallel Digit Computer Codes

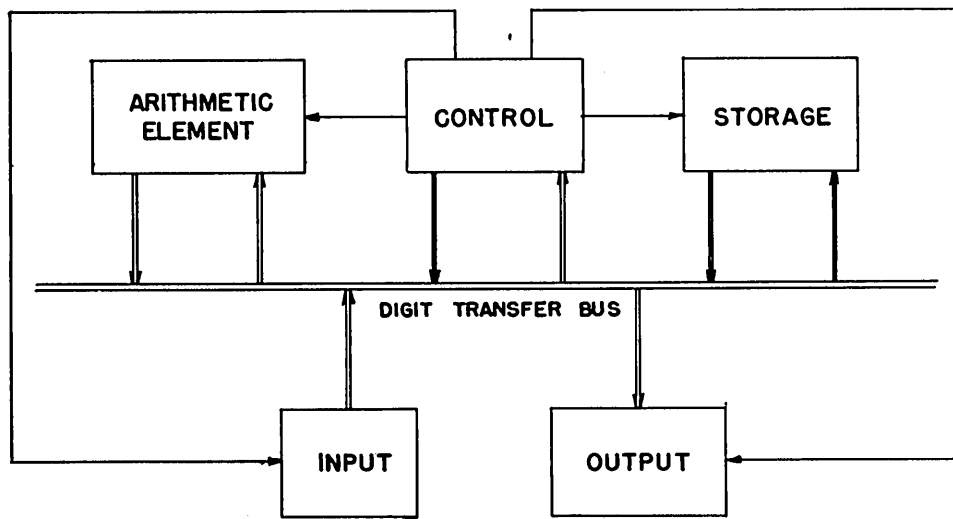


Figure 1  
GENERAL BLOCK DIAGRAM

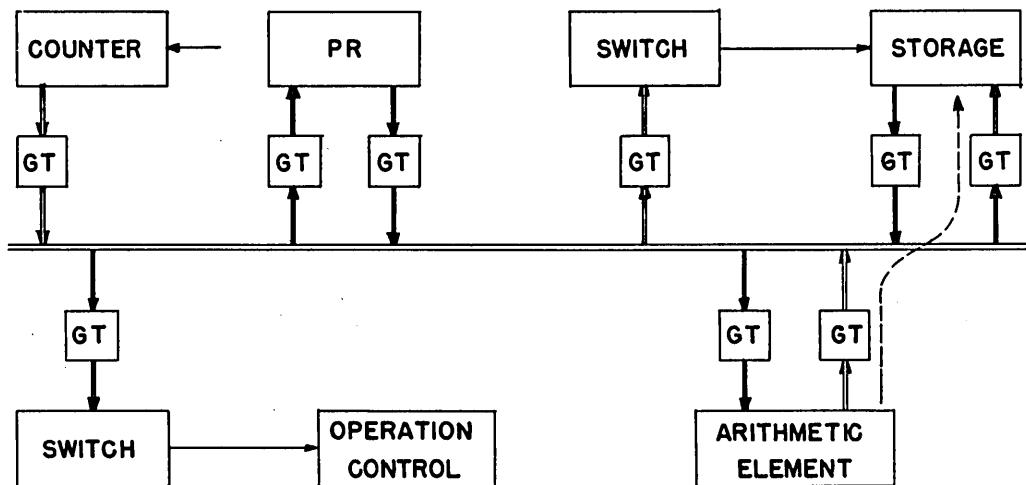


Figure 2  
STORE RESULT

ORIGIN OF ORDERS

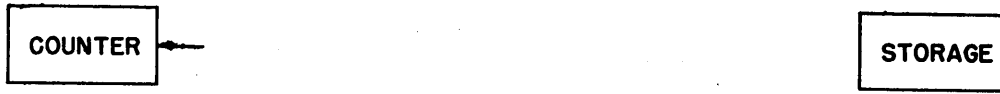


Figure 3  
ORIGIN OF ORDERS

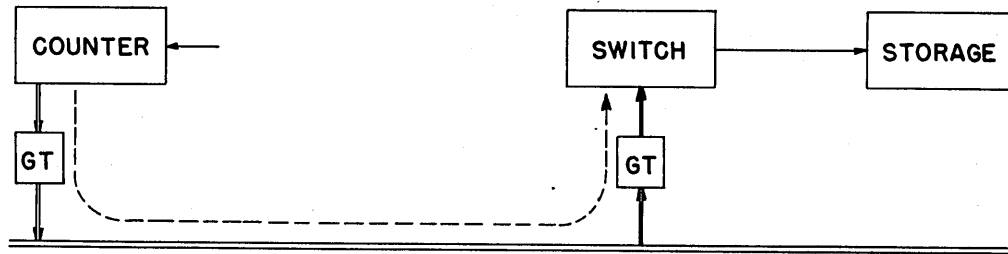


Figure 4  
SETUP ORDER

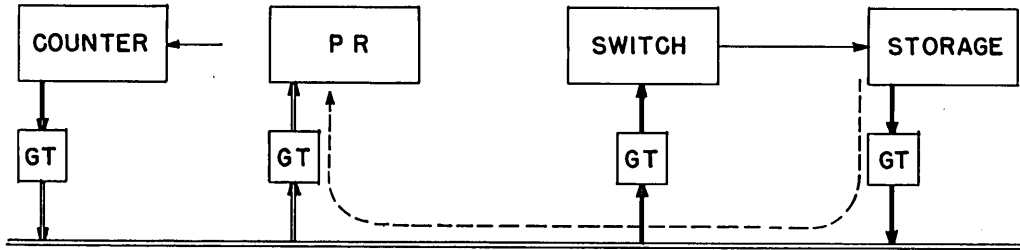


Figure 5  
READ OUT ORDER

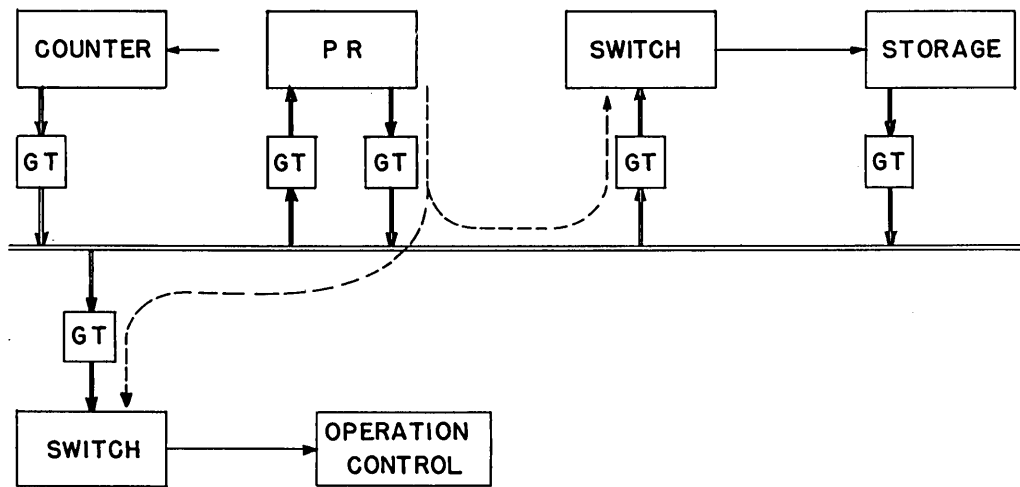


Figure 6  
SETUP OPERATION



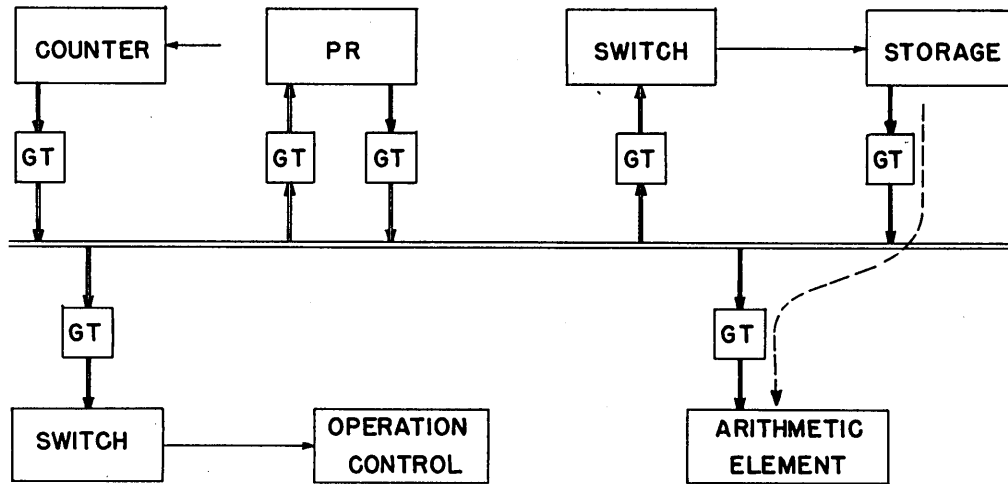


Figure 7  
PERFORM OPERATION

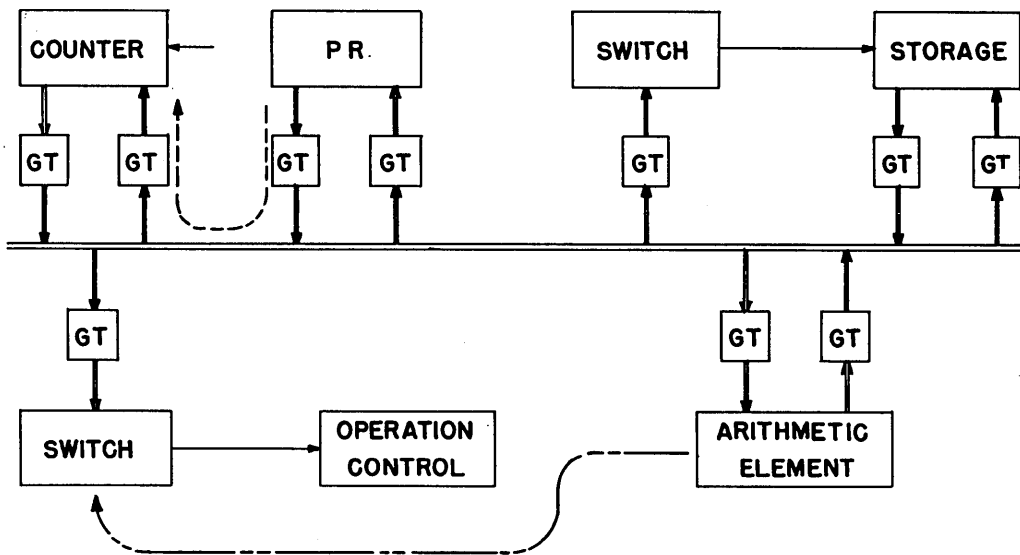


Figure 8  
SUBPROGRAM

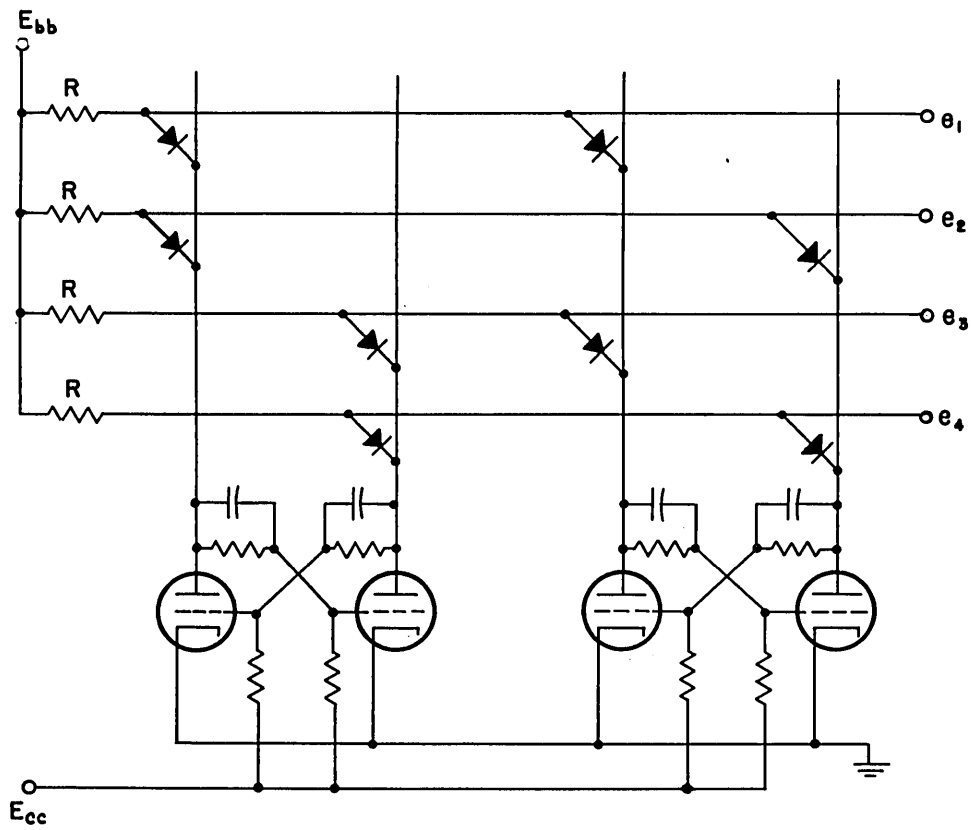


Figure 9  
ELECTRONIC SWITCH

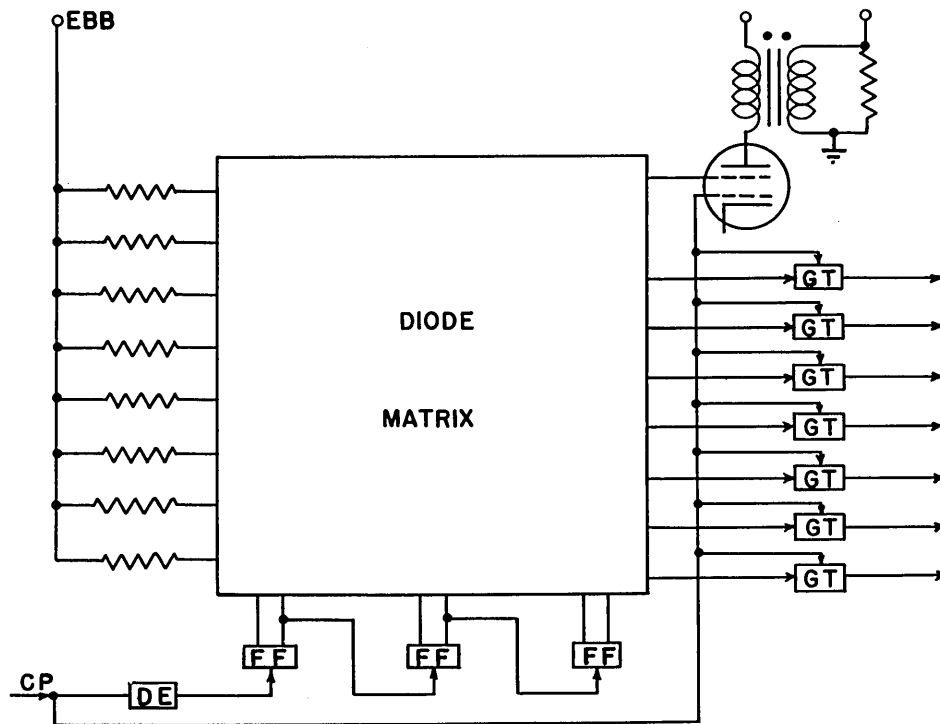


Figure 10  
TIME PULSE DISTRIBUTOR

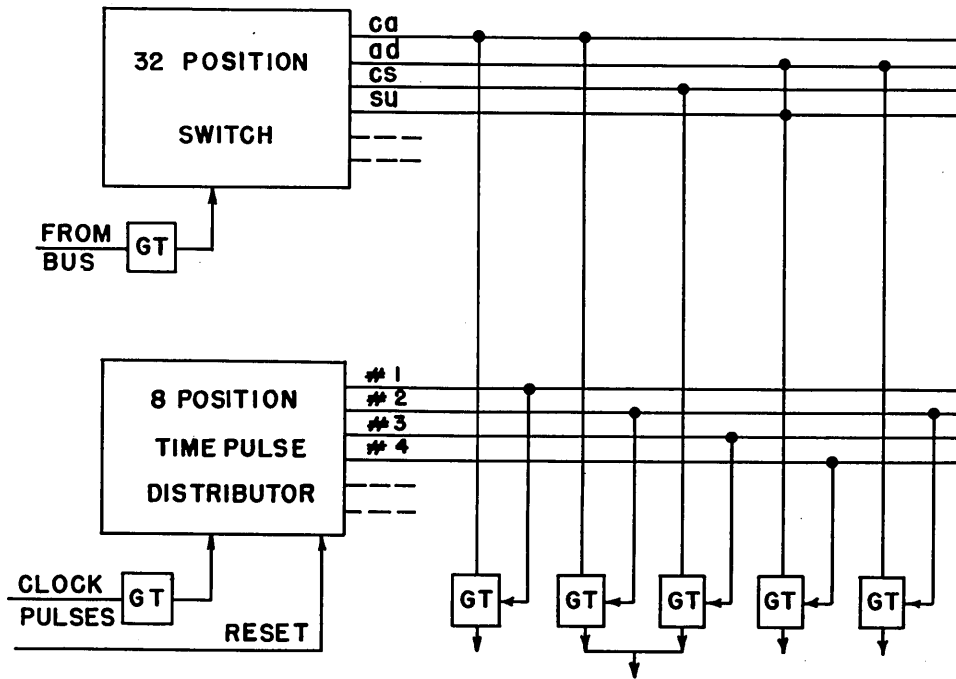


Figure 11  
CONTROL

$$\begin{array}{r}
 3546 \\
 1371 \\
 \hline
 4817 \\
 +1 \\
 \hline
 4917
 \end{array}$$

Figure 12  
DECIMAL ADDITION

```

      11011010
      10110110
      -----
      01101100
      1 1 1
      -----
      101001000
      1 1
      -----
      100000000
      1 1
      -----
      110010000
  
```

Figure 13  
BINARY ADDITION

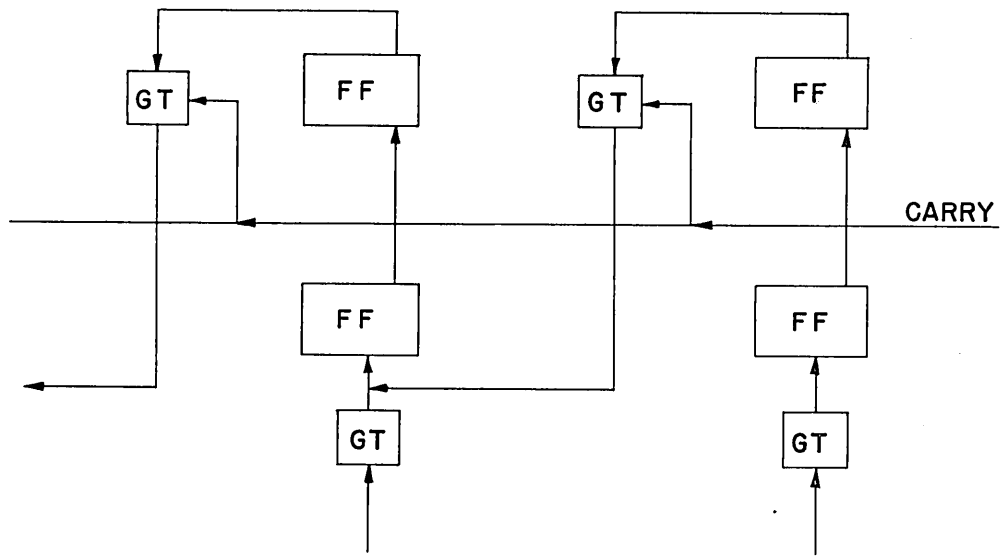


Figure 14  
A BINARY ADDER

	DECIMAL	BINARY
POSITIVE NUMBER	223	11011111
NEGATIVE "	- 223	- 11011111
10's COMPLEMENT	1 777	1 00100001
9's "	1 776	1 00100000

Figure 15  
NEGATIVE NUMBERS

BINARY		DECIMAL
+010110110	= $N_1$	= 182
-011010010	= $-N_2$	= -210
		<u>-28</u>
010110110	= $N_1$	
<u>100101101</u>	= $2^7 - N_2 - 1$	
111100011	= $2^7 - (N_2 - N_1) - 1$	
-000011100	= $N_1 - N_2$	= -28
010110110	= $N_1$	= 182
-010010010	= $N_2$	= -146
		<u>+36</u>
010110110	= $N_1$	
<u>101101101</u>	= $2^7 - N_2 - 1$	
1000100011	= $N_1 - N_2 + 2^7 - 1$	
END AROUND CARRY		
<u>+1</u>		
000100100	= $N_1 - N_2$	= +36

Figure 16  
SUBTRACTION USING 9'S COMPLEMENTS

3 5 6	MULTIPLICAND
6 2 7	MULTIPLIER
<u>4 2</u>	
3 5	
<u>2 1</u>	
2 4 9 2	PARTIAL PRODUCT
1 2	
1 0	
<u>6</u>	
9 6 1 2	PARTIAL PRODUCT
3 6	
3 0	
<u>1 8</u>	
2 2 3 2 1 2	PRODUCT

Figure 17  
DECIMAL MULTIPLICATION

REPRESENTS POWERS OF 2

MULTIPLICATION TABLE:

1 x 1 = 1  
1 x 0 = 0  
0 x 0 = 0

ADDITION:

1 + 1 = 10  
1 + 0 = 1  
0 + 0 = 0

BINARY COLUMNS  $\approx 3\frac{1}{3} \times$  DECIMAL COLUMNS  
ONLY DIGITS 1 AND 0 REQUIRED IN EQUIPMENT

Figure 18  
BINARY NOTATION

10110	MULTIPLICAND	22
10011	MULTIPLIER	19
10110		198
10110		22
1000010	PARTIAL PRODUCT	418
00000		
1000010	PARTIAL PRODUCT	
00000		
01000010	PARTIAL PRODUCT	
10110		
110100010	= 418 PRODUCT	

Figure-19

BINARY MULTIPLICATION

STEP 1	<table style="border-collapse: collapse;"> <tr><td style="text-align: right; padding-right: 10px;">10110</td><td>MULTIPLICAND</td></tr> <tr><td style="text-align: right; border-bottom: 1px solid black;">10011</td><td>MULTIPLIER</td></tr> <tr><td style="text-align: right; padding-right: 10px;">10110</td><td>PARTIAL PRODUCT</td></tr> </table>	10110	MULTIPLICAND	10011	MULTIPLIER	10110	PARTIAL PRODUCT				
10110	MULTIPLICAND										
10011	MULTIPLIER										
10110	PARTIAL PRODUCT										
STEP 2	<table style="border-collapse: collapse;"> <tr><td style="text-align: right; padding-right: 10px;">10110</td><td>MULTIPLICAND</td></tr> <tr><td style="text-align: right; border-bottom: 1px solid black;">1001</td><td>SHIFTED MULTIPLIER</td></tr> <tr><td style="text-align: right; padding-right: 10px;">10110</td><td>SHIFTED PARTIAL PRODUCT</td></tr> <tr><td style="text-align: right; padding-right: 10px;">10110</td><td></td></tr> <tr><td style="text-align: right; border-bottom: 1px solid black;">1000010</td><td>PARTIAL PRODUCT</td></tr> </table>	10110	MULTIPLICAND	1001	SHIFTED MULTIPLIER	10110	SHIFTED PARTIAL PRODUCT	10110		1000010	PARTIAL PRODUCT
10110	MULTIPLICAND										
1001	SHIFTED MULTIPLIER										
10110	SHIFTED PARTIAL PRODUCT										
10110											
1000010	PARTIAL PRODUCT										
STEP 3	<table style="border-collapse: collapse;"> <tr><td style="text-align: right; padding-right: 10px;">10110</td><td>MULTIPLICAND</td></tr> <tr><td style="text-align: right; border-bottom: 1px solid black;">100</td><td>SHIFTED MULTIPLIER</td></tr> <tr><td style="text-align: right; padding-right: 10px;">1000010</td><td>SHIFTED PARTIAL PRODUCT</td></tr> <tr><td style="text-align: right; padding-right: 10px;">00000</td><td></td></tr> <tr><td style="text-align: right; border-bottom: 1px solid black;">1000010</td><td>PARTIAL PRODUCT</td></tr> </table>	10110	MULTIPLICAND	100	SHIFTED MULTIPLIER	1000010	SHIFTED PARTIAL PRODUCT	00000		1000010	PARTIAL PRODUCT
10110	MULTIPLICAND										
100	SHIFTED MULTIPLIER										
1000010	SHIFTED PARTIAL PRODUCT										
00000											
1000010	PARTIAL PRODUCT										
STEP 4	<table style="border-collapse: collapse;"> <tr><td style="text-align: right; padding-right: 10px;">10110</td><td>MULTIPLICAND</td></tr> <tr><td style="text-align: right; border-bottom: 1px solid black;">10</td><td>SHIFTED MULTIPLIER</td></tr> <tr><td style="text-align: right; padding-right: 10px;">1000010</td><td>SHIFTED PARTIAL PRODUCT</td></tr> <tr><td style="text-align: right; padding-right: 10px;">00000</td><td></td></tr> <tr><td style="text-align: right; border-bottom: 1px solid black;">01000010</td><td>PARTIAL PRODUCT</td></tr> </table>	10110	MULTIPLICAND	10	SHIFTED MULTIPLIER	1000010	SHIFTED PARTIAL PRODUCT	00000		01000010	PARTIAL PRODUCT
10110	MULTIPLICAND										
10	SHIFTED MULTIPLIER										
1000010	SHIFTED PARTIAL PRODUCT										
00000											
01000010	PARTIAL PRODUCT										
STEP 5	<table style="border-collapse: collapse;"> <tr><td style="text-align: right; padding-right: 10px;">10110</td><td>MULTIPLICAND</td></tr> <tr><td style="text-align: right; border-bottom: 1px solid black;">1</td><td>SHIFTED MULTIPLIER</td></tr> <tr><td style="text-align: right; padding-right: 10px;">01000010</td><td>SHIFTED PARTIAL PRODUCT</td></tr> <tr><td style="text-align: right; padding-right: 10px;">10110</td><td></td></tr> <tr><td style="text-align: right; border-bottom: 1px solid black;">110100010</td><td>PRODUCT</td></tr> </table>	10110	MULTIPLICAND	1	SHIFTED MULTIPLIER	01000010	SHIFTED PARTIAL PRODUCT	10110		110100010	PRODUCT
10110	MULTIPLICAND										
1	SHIFTED MULTIPLIER										
01000010	SHIFTED PARTIAL PRODUCT										
10110											
110100010	PRODUCT										

Figure 20

MODIFIED BINARY MULTIPLICATION

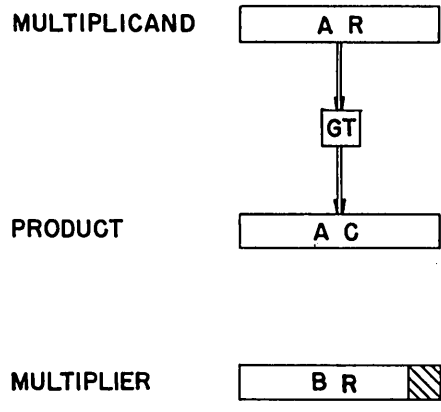


Figure 21  
MULTIPLICATION I

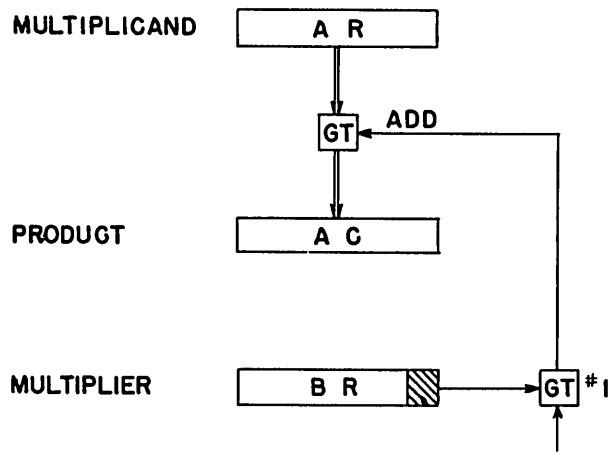


Figure 22  
MULTIPLICATION II



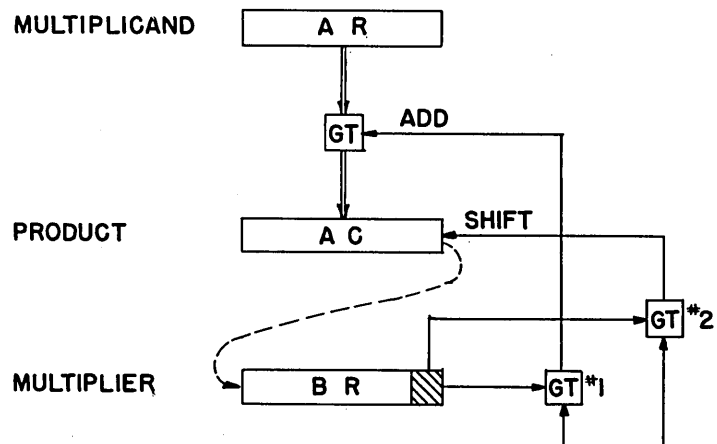


Figure 23  
MULTIPLICATION III

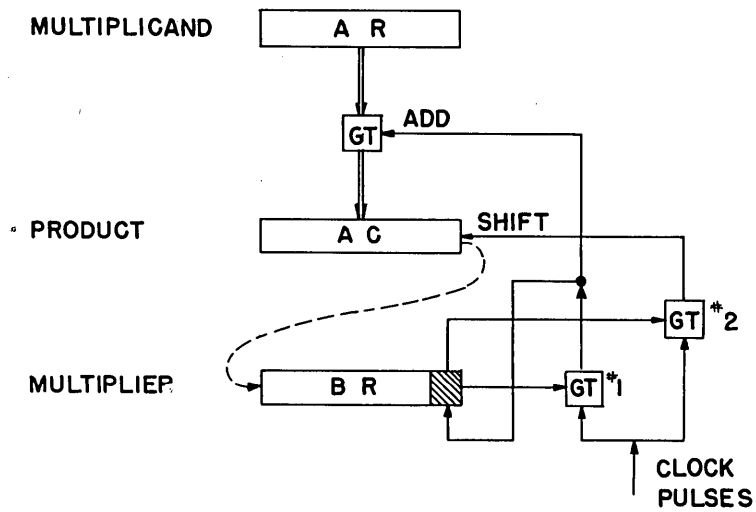


Figure 24  
MULTIPLICATION IV

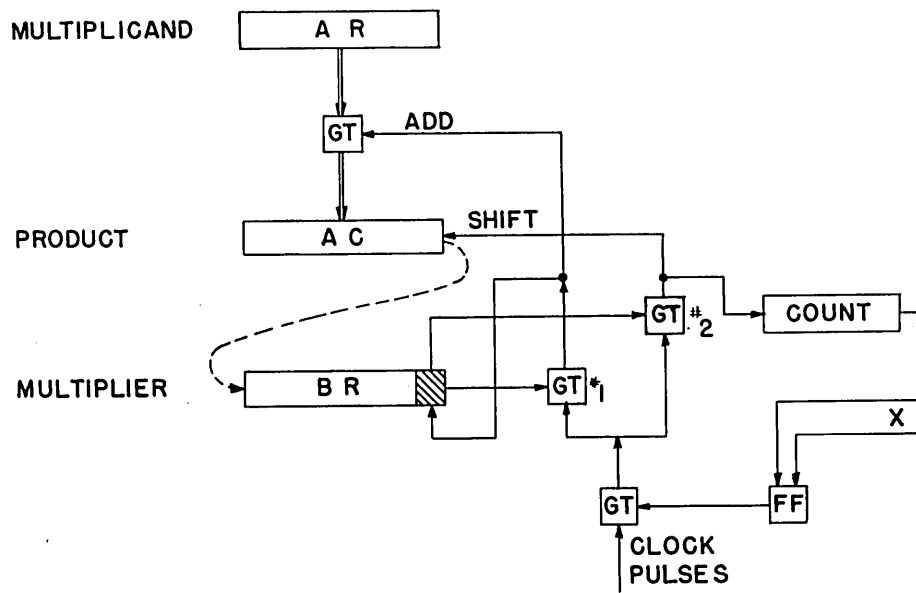


Figure 25  
MULTIPLICATION V

DECIMAL

1734	6148
	5
1735	1

173	46148
	5
173	9

BINARY

11010	1010
	1
11011	
1101	01010
	1
1101	1

Figure 26  
ROUNDING OFF

```

      1 4 2
28 | 3 9 7 6
   - 2 8
   -----
     1 1 7 6
     - 2 8
     -----
     - 1 6 2 4
     + 2 8
     -----
     1 1 7 6
     - 2 8
     -----
       8 9 6
       - 2 8
       -----
       6 1 6
       - 2 8
       -----
       3 3 6
       - 2 8
       -----
       5 6
       - 2 8
       -----
       - 2 2 4
       + 2 8
       -----
         5 6
         - 2 8
         -----
         2 8
         - 2 8
         -----
         0
         - 2 8
         -----
         - 2 8
         + 2 8
         -----
         0

```

```

SUBTRACT 1
POS. REMAINDER
SUBTRACT 2
OVERCAST
RESTORE -1
SHIFT 1 NET SUBTRACTION
SUBTRACT 1
POS. REMAINDER
SUBTRACT 2
POS. REM.
SUBTRACT 3
POS. REM.
SUBTRACT 4
POS. REM.
SUBTRACT 5
OVERCAST
RESTORE -1
SHIFT 4 NET SUBTRACTION
SUBTRACT 1
POS. REM.
SUBTRACT 2
POS. REM.
SUBTRACT 3
OVERCAST
RESTORE -1
REMAINDER 0 2 NET SUB.

```

Figure 27  
DECIMAL DIVISION

```

      0.1 0 1 1 0
0.101 | 0.0 1 1 1 0
      1.0 1 0 1 1
      -----
      1.1 1 0 0 1
      1.1 0 0 1 1
      -----
      0.1 0 1 0 0
      1 0.0 0 1 1 1
      -----
      0.0 1 0 0 0
      0.1 0 0 0 0
      -----
      1.0 1 0 1 1
      1.1 1 0 1 1
      -----
      1.1 0 1 1 1
      0.1 0 1 0 0
      -----
      1 0.0 1 0 1 1
      -----
      0.0 1 1 0 0
      0.1 1 0 0 0
      -----
      1.0 1 0 1 1
      1 0.0 0 0 1 1
      -----
      0.0 0 1 0 0
      0.0 1 0 0 0
      -----
      1.0 1 0 1 1
      1.1 0 0 1 1

```

```

SUBTRACT
NEG. REMAINDER 0 IN QUOTIENT
SHIFT LEFT
ADD
END AROUND CARRY
POS. REMAINDER 1 IN QUOTIENT
SHIFT LEFT
SUBTRACT
NEG. REMAINDER 0 IN QUOTIENT
SHIFT LEFT
ADD
END AROUND CARRY
POS. REMAINDER 1 IN QUOTIENT
SHIFT LEFT
SUBTRACT
END AROUND CARRY
POS. REMAINDER 1 IN QUOTIENT
SHIFT LEFT
SUBTRACT
NEG. REMAINDER 0 IN QUOTIENT

```

Figure 28  
BINARY DIVISION

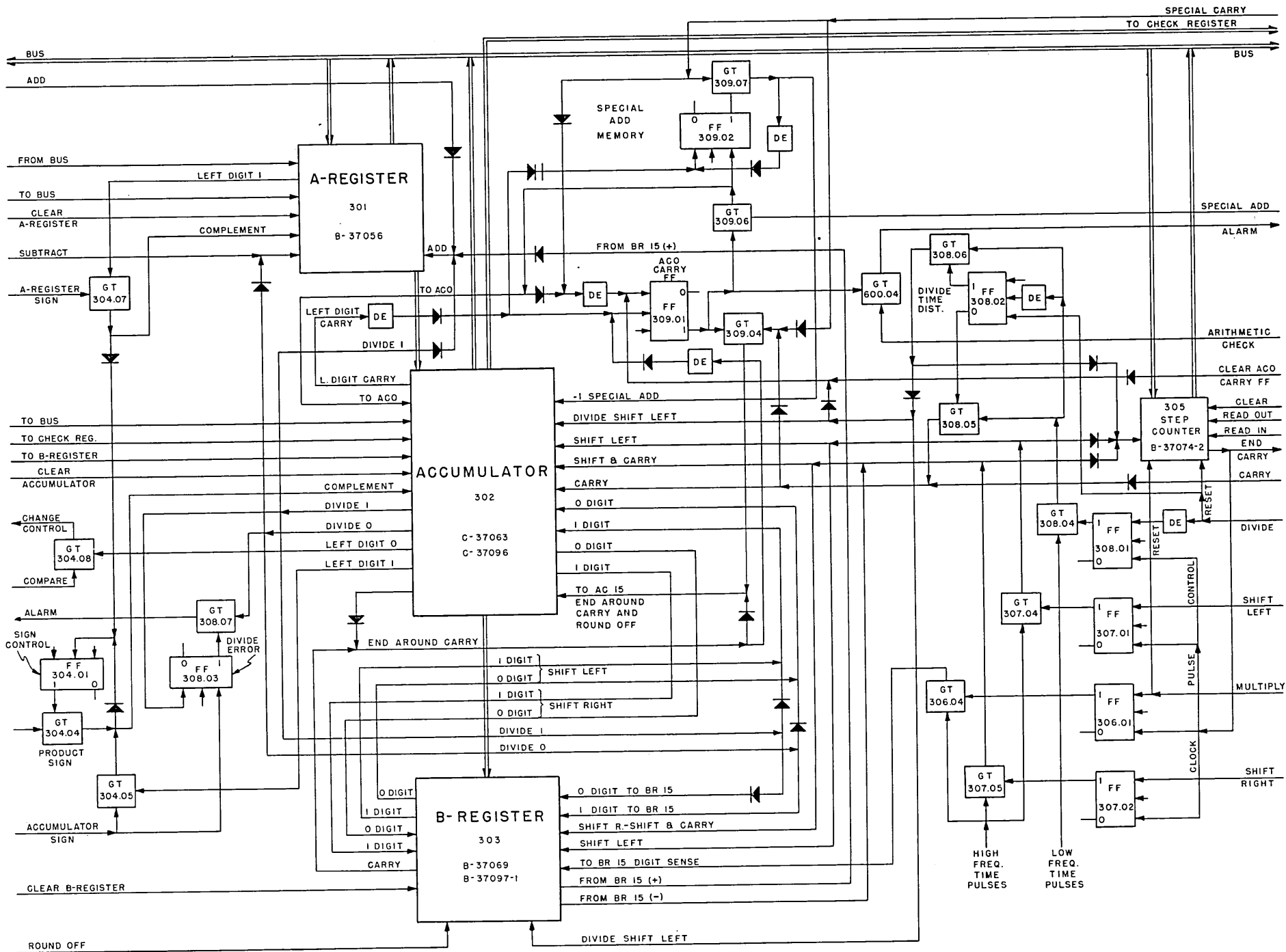


Figure 29  
ARITHMETIC ELEMENT

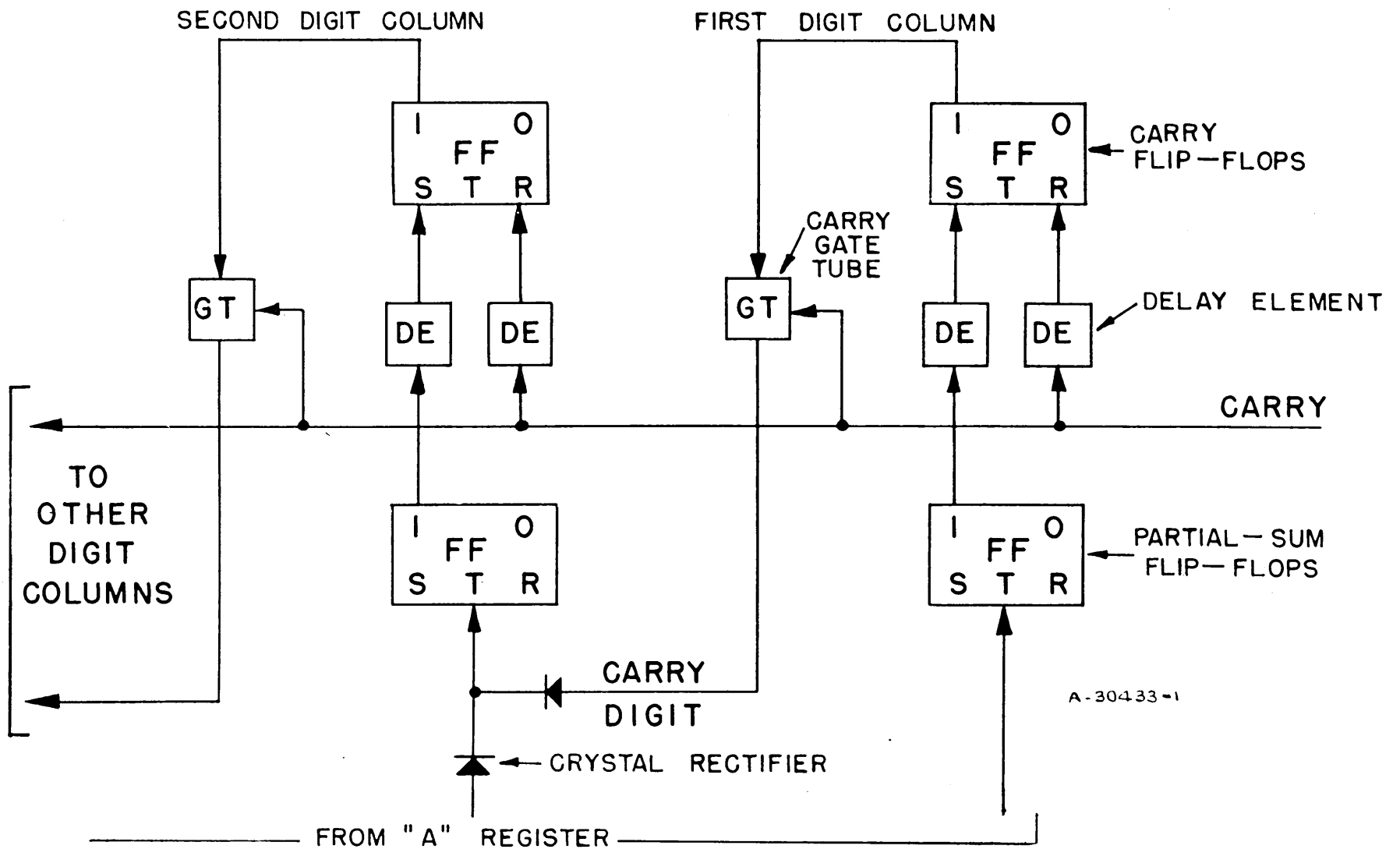


Figure 30  
ACCUMULATOR

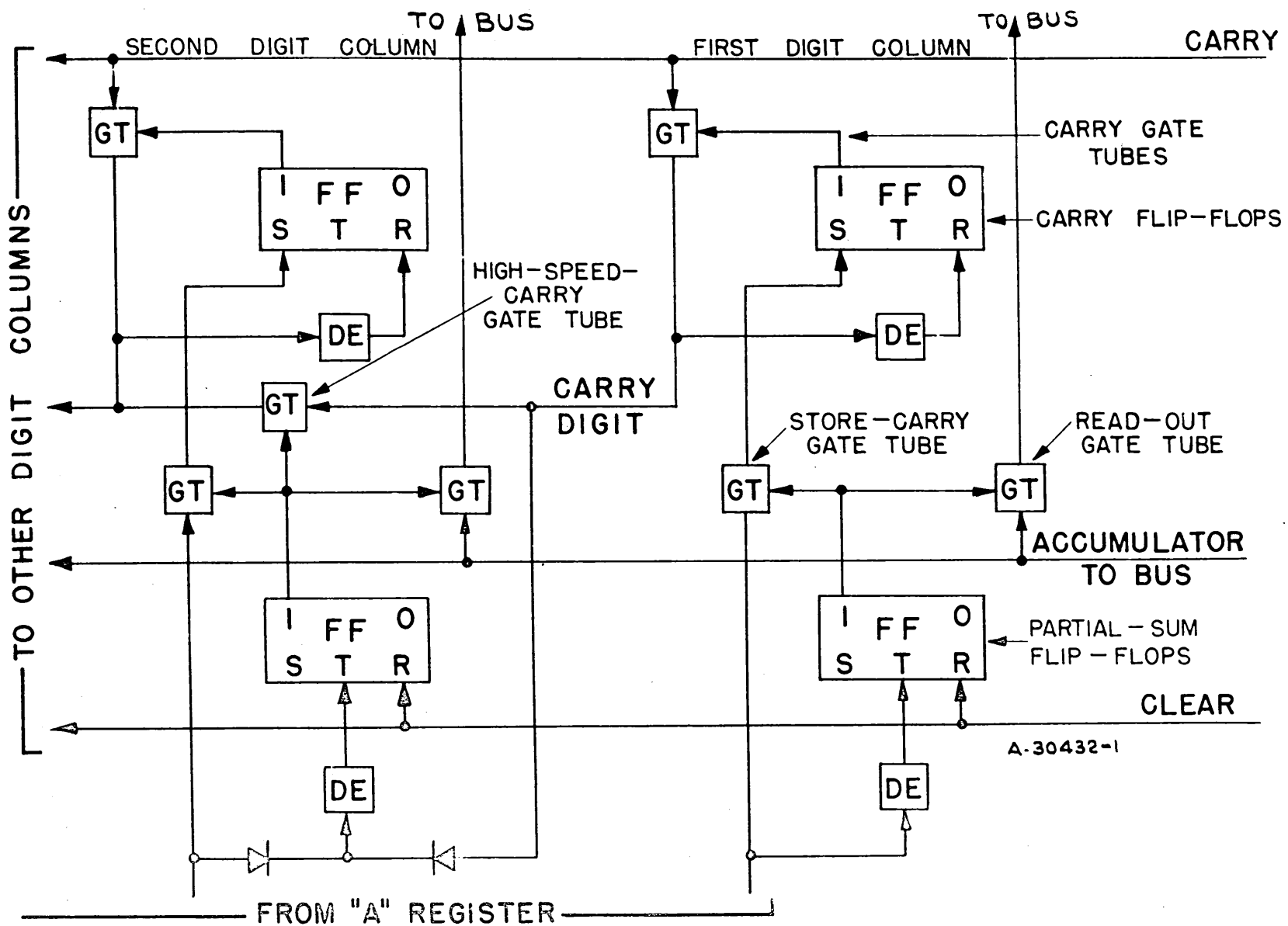


Figure 31  
ACCUMULATOR

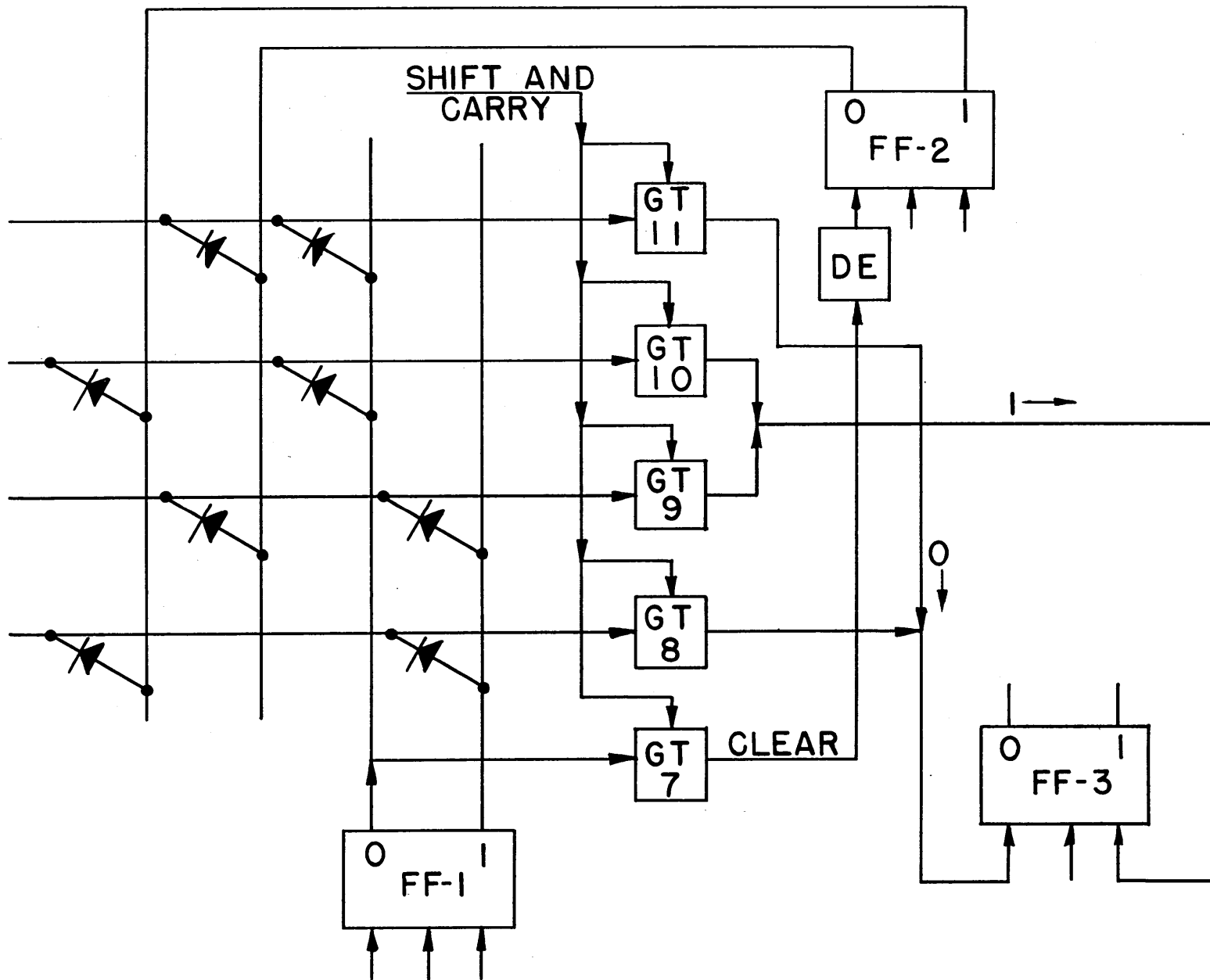


Figure 32  
SHIFT AND CARRY

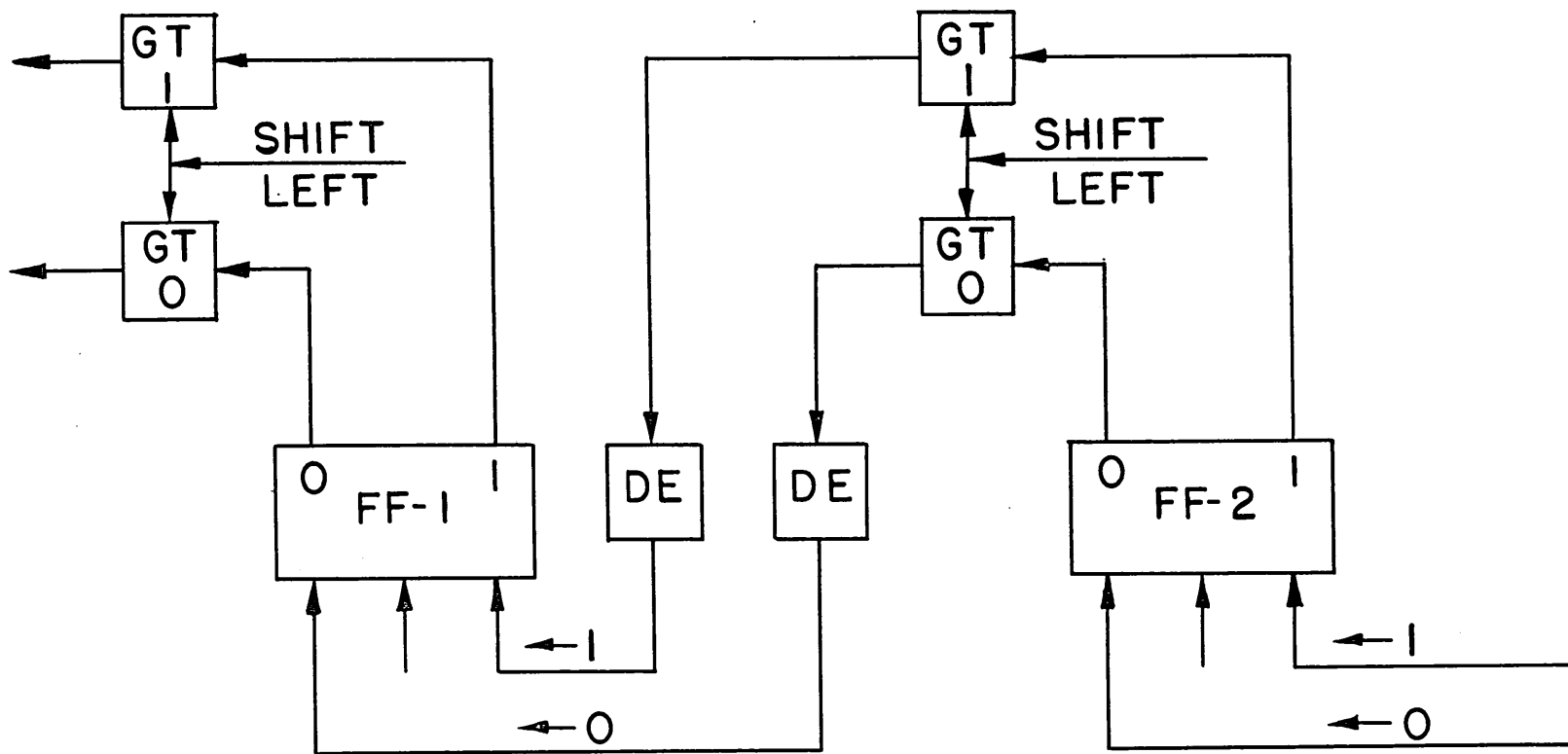


Figure 33  
SHIFT LEFT



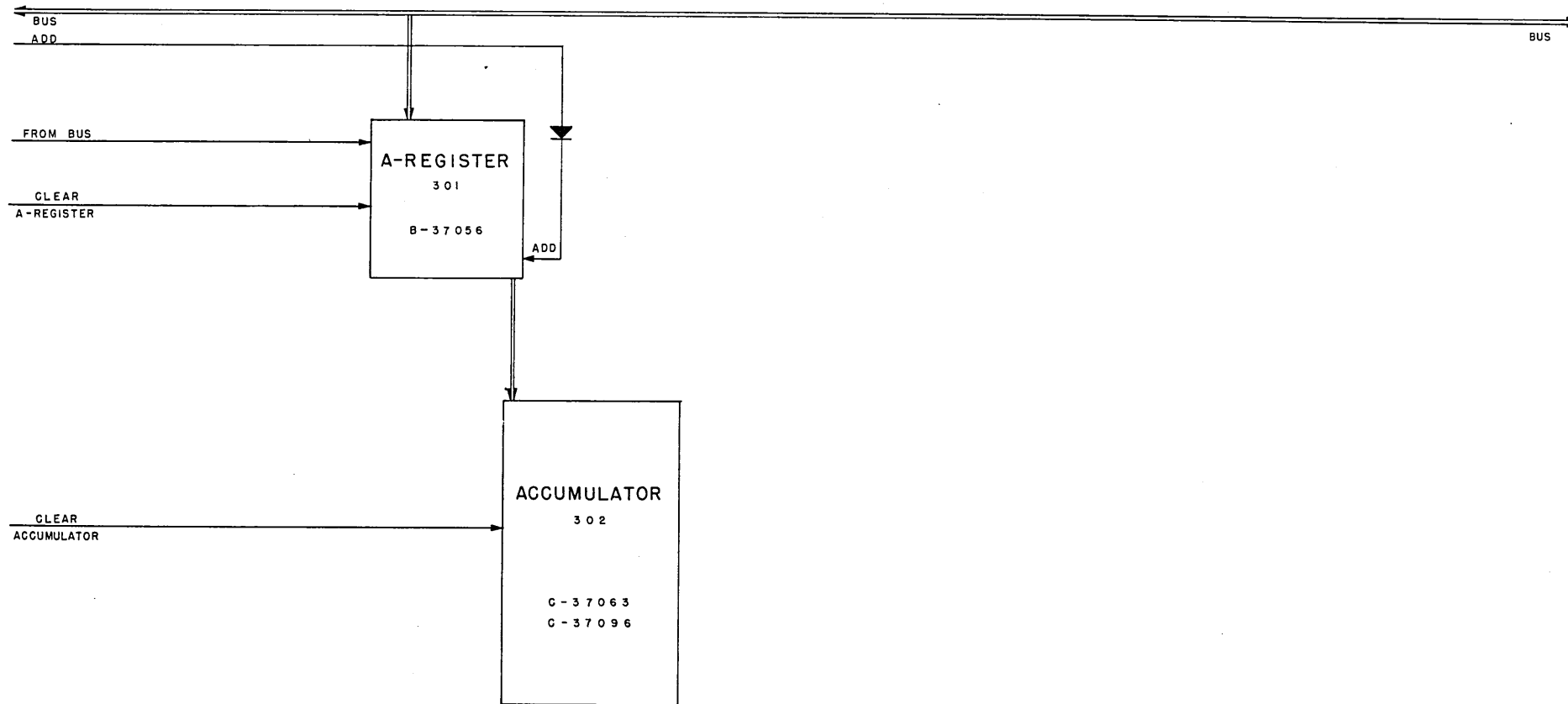


Figure 34  
CLEAR AND ADD

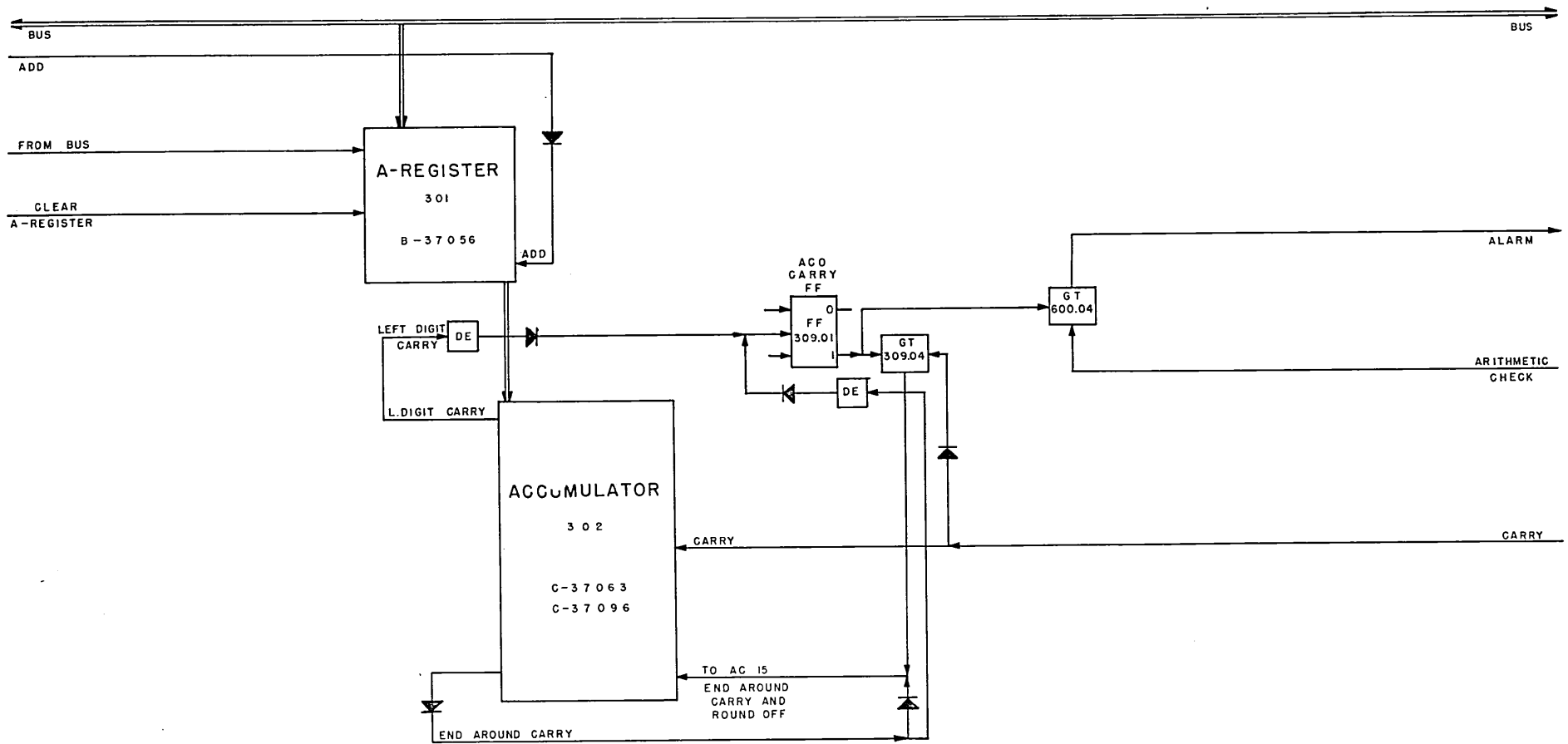


Figure 35  
ADD

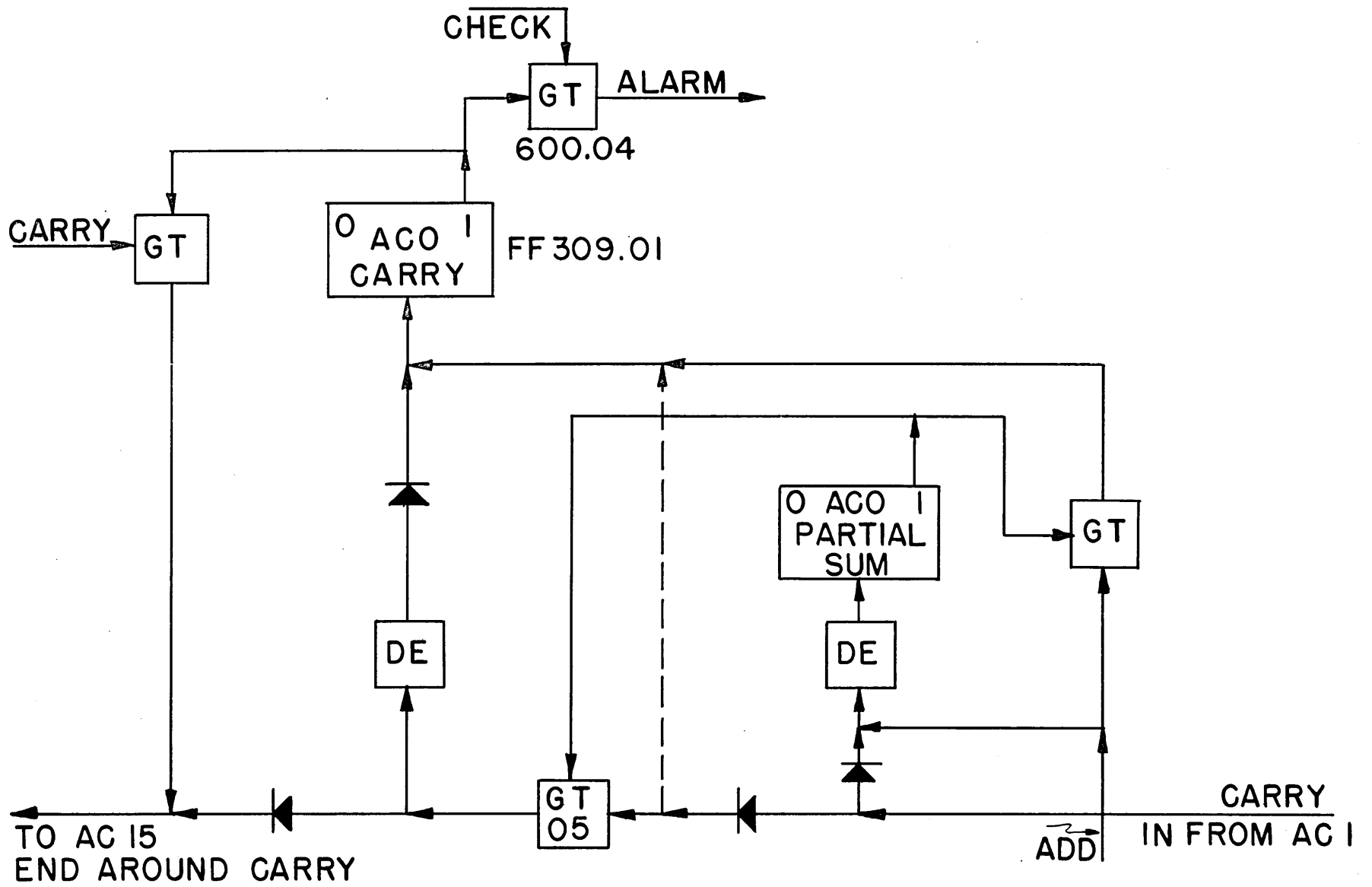


Figure 36  
ARITHMETIC CHECK

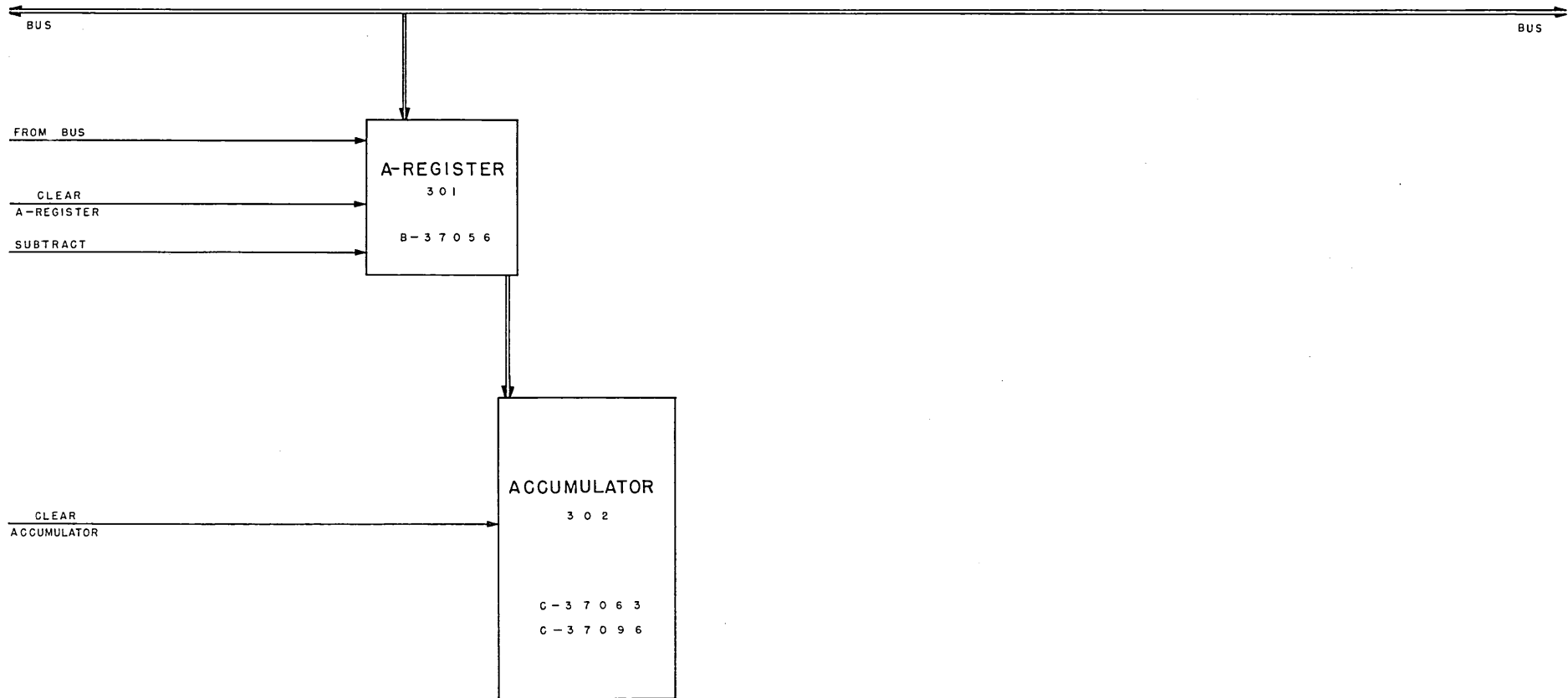


Figure 37  
CLEAR AND SUBTRACT

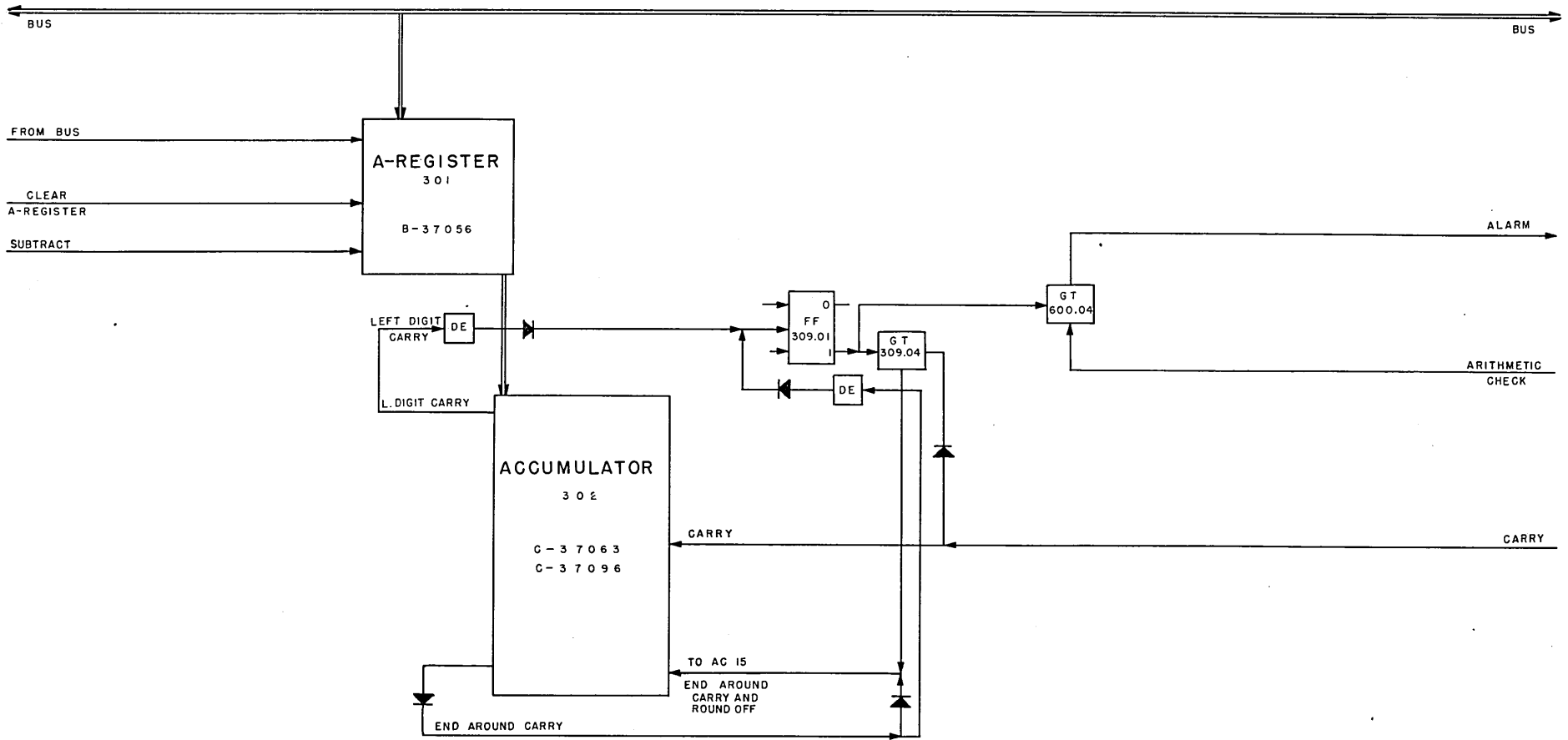


Figure 38  
SUBTRACT

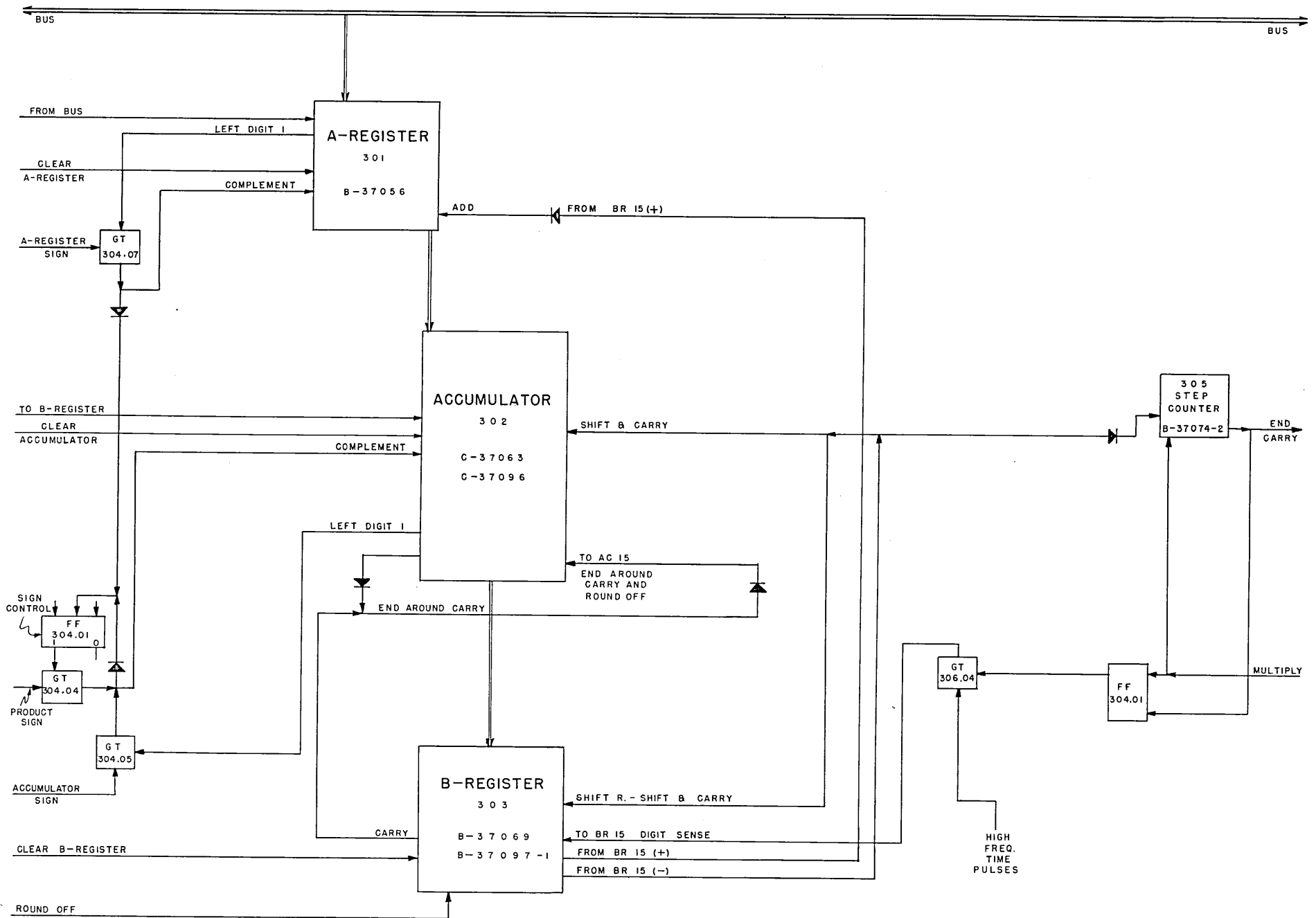


Figure 39  
 MULTIPLY AND ROUND OFF  
 MULTIPLY AND HOLD FULL PRODUCT

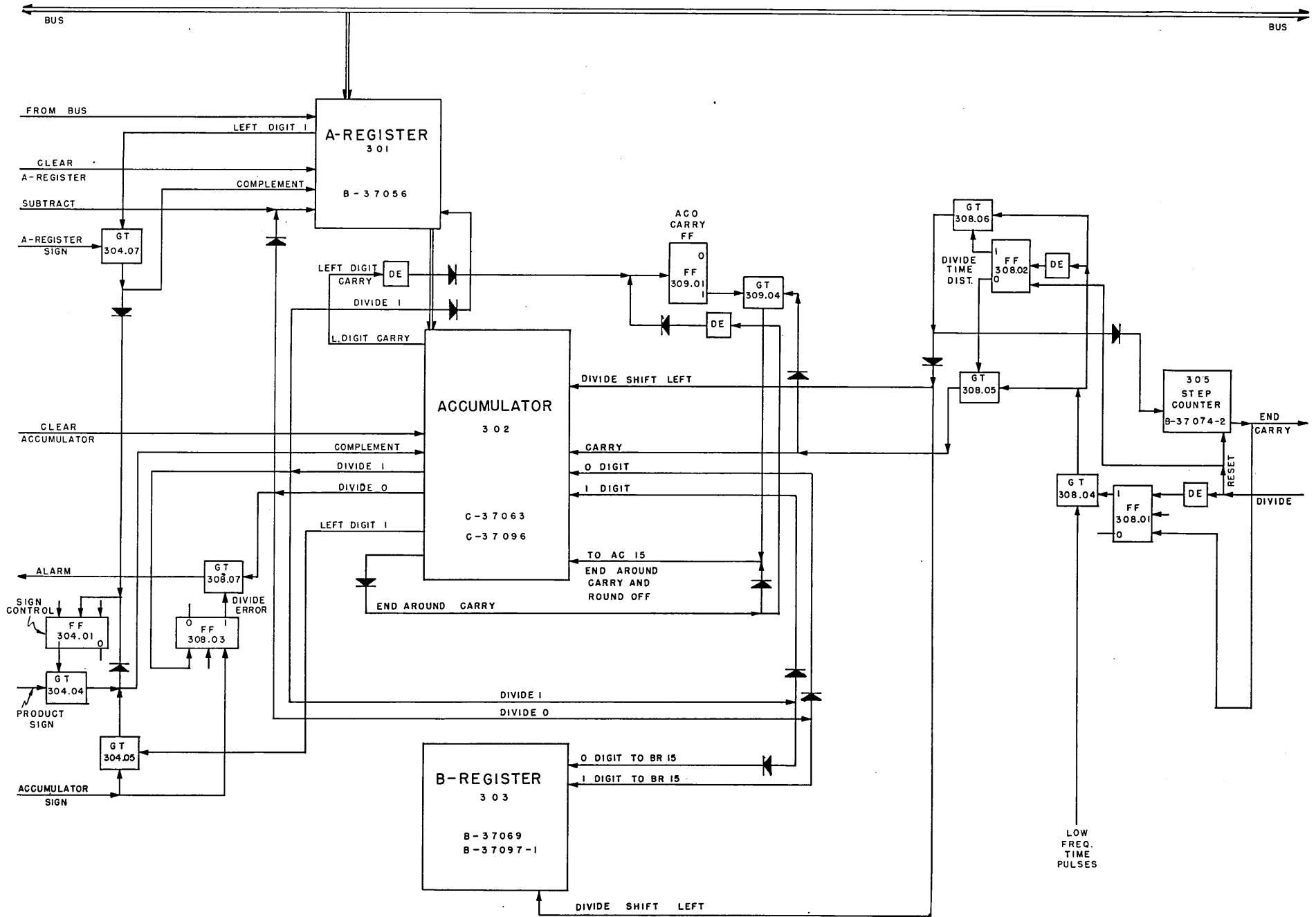


Figure 40  
DIVIDE

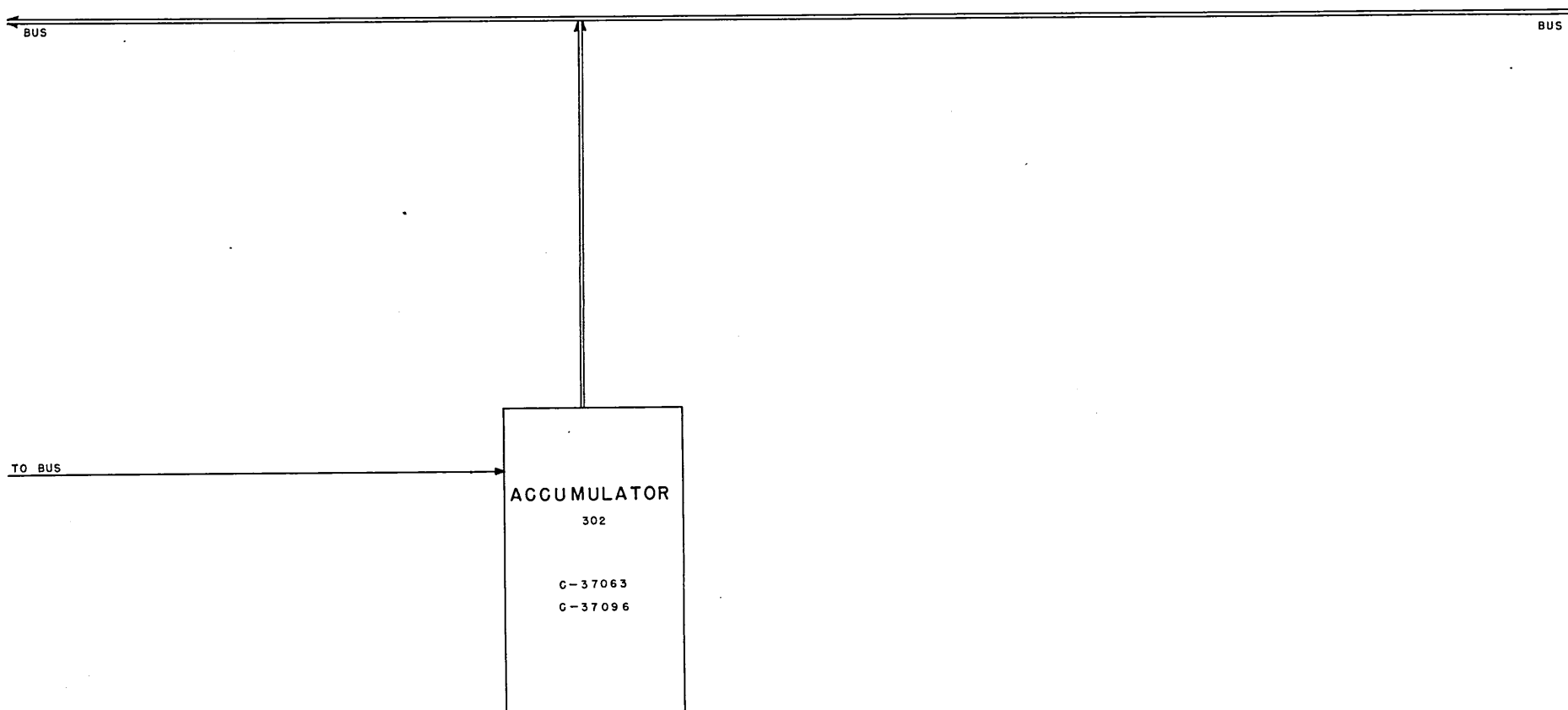


Figure 41  
TRANSFER TO STORAGE  
TRANSFER DIGITS  
STORE AND DISPLAY



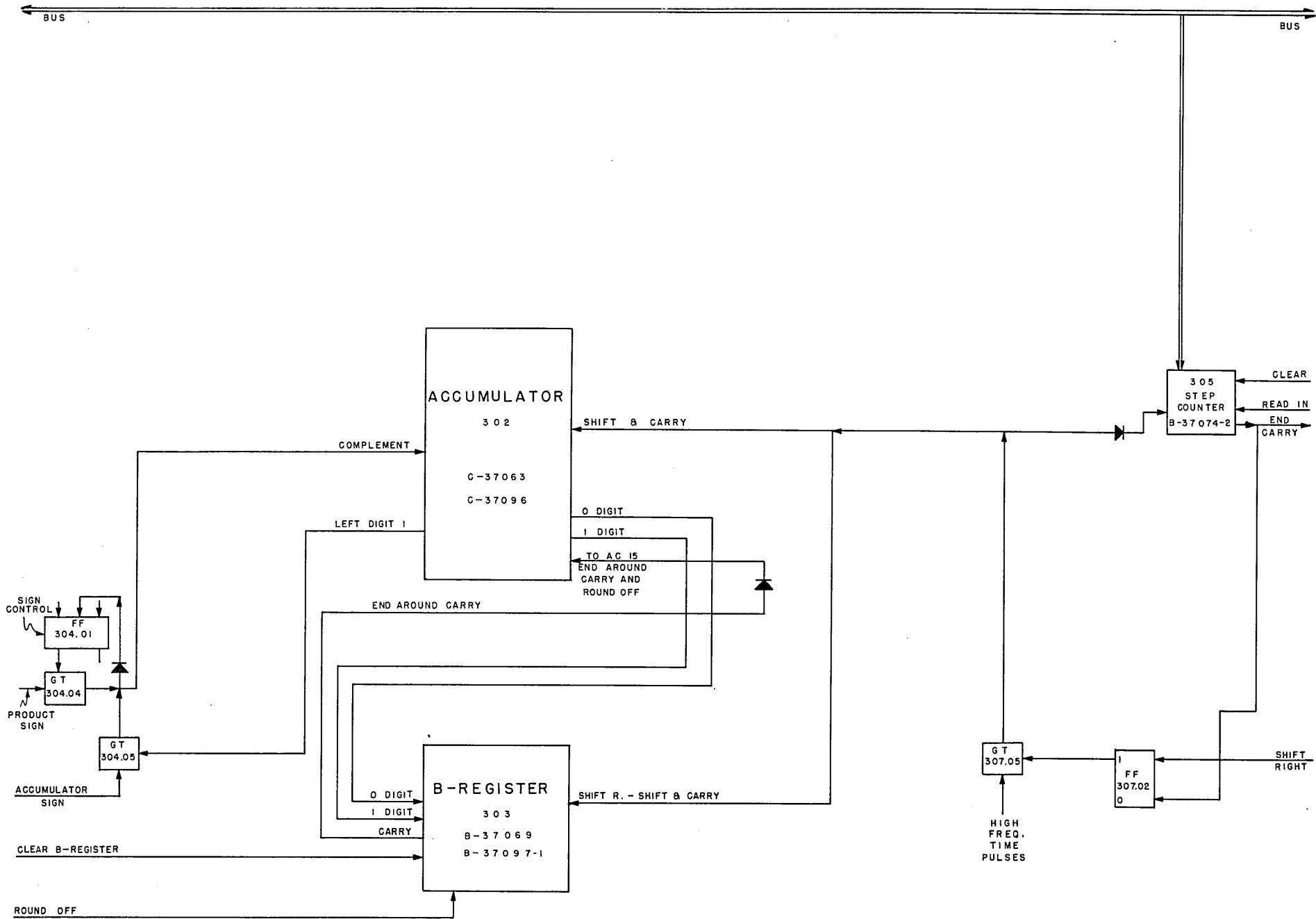


Figure 42  
SHIFT RIGHT

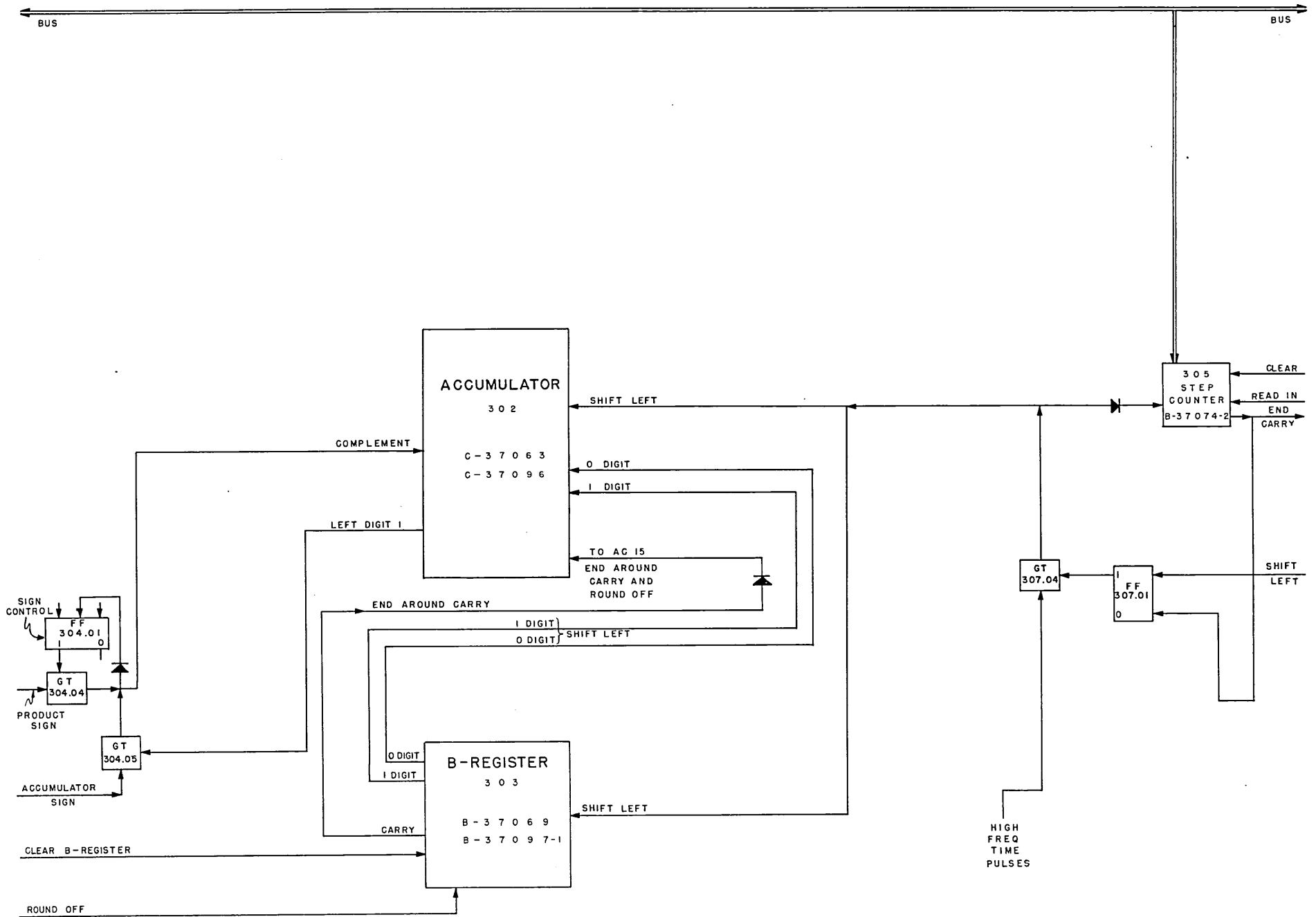


Figure 43  
SHIFT LEFT

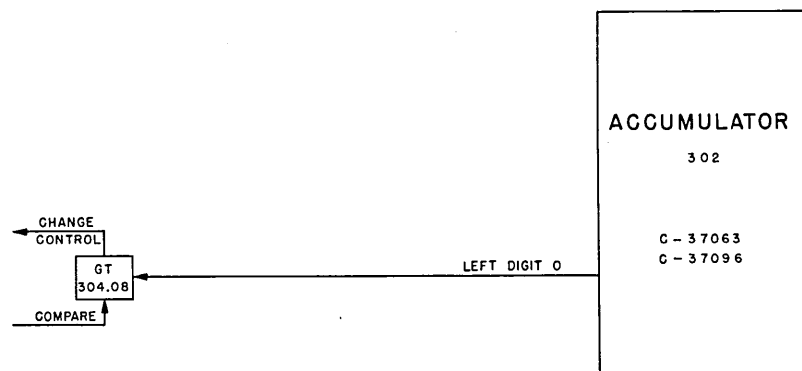


Figure 44  
CONDITIONAL PROGRAM

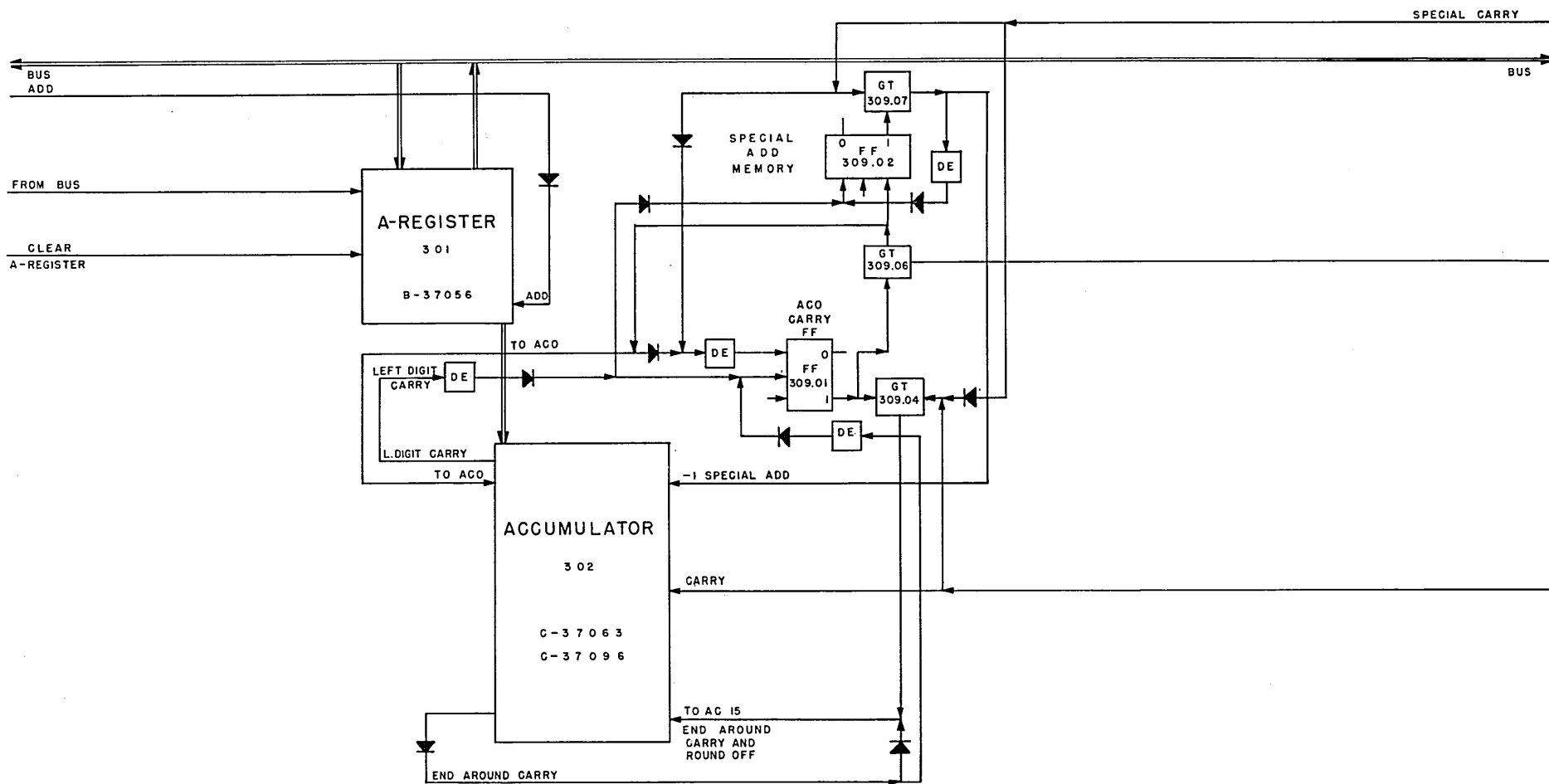
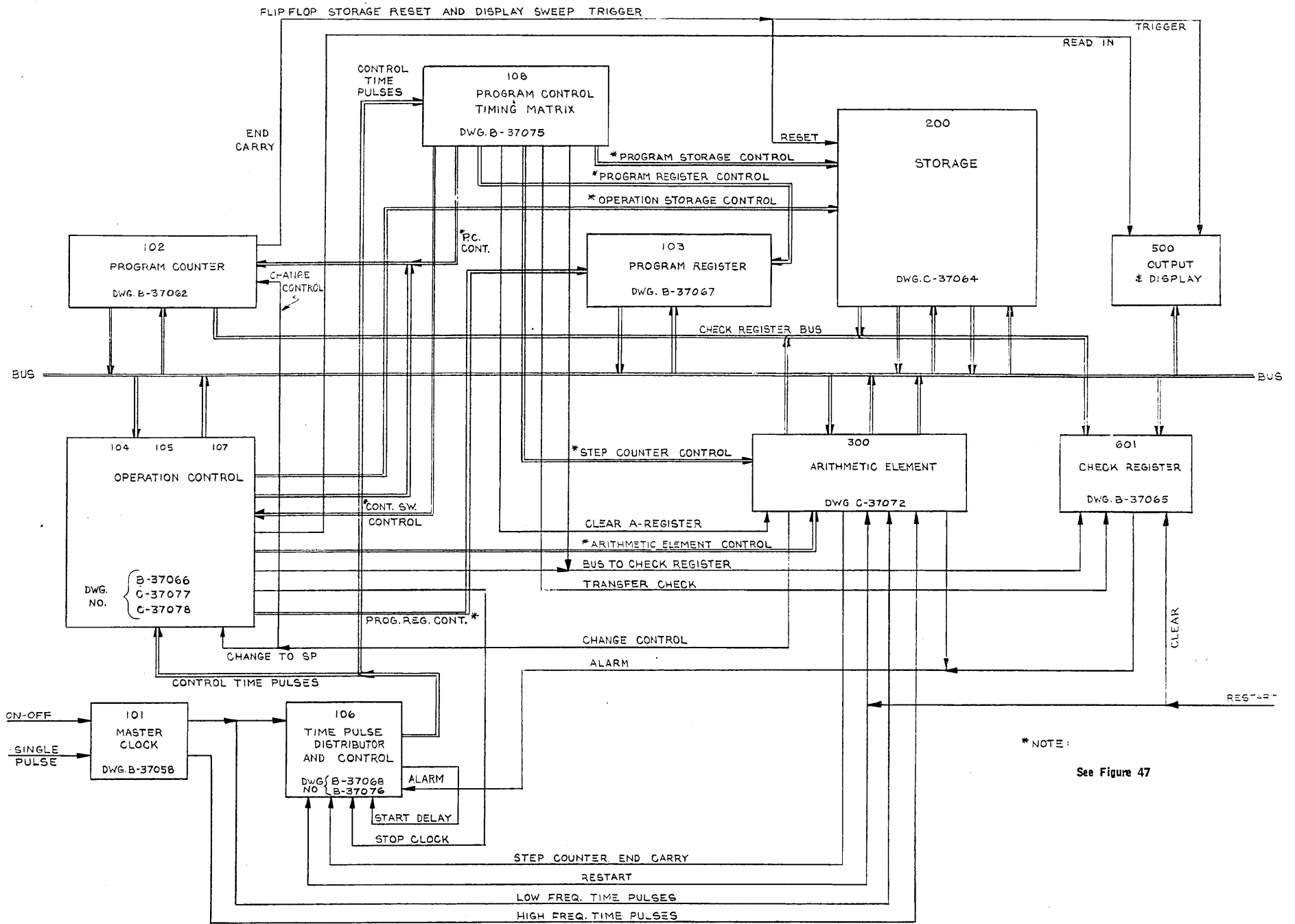


Figure 45  
SPECIAL ADD



\* NOTE:  
See Figure 47

Figure 46  
SYSTEM BLOCK DIAGRAM

ARITHMETIC ELEMENT CONTROL

- |                                   |           |
|-----------------------------------|-----------|
| 1. Bus to A-Register              | GT 301.01 |
| 2. A-Register to Bus              | GT 301.02 |
| 3. Subtract: A-Register to Accum. | GT 301.04 |
| 4. Add: A-Register to Accumulator | GT 301.05 |
| 5. Accumulator to Bus             | GT 302.02 |
| 6. Accumulator to Check Register  | GT 302.03 |
| 7. Accumulator to B-Register      | GT 302.04 |
| 8. Carry                          | GT 302.20 |
| 9. Roundoff                       | GT 303.08 |
| 10. Product Sign                  | GT 304.04 |
| 11. Accumulator Sign              | GT 304.05 |
| 12. A-Register Sign               | GT 304.07 |
| 13. Compare                       | GT 304.08 |
| 14. Multiply                      | FF 306.01 |
| 15. Shift Left                    | FF 307.01 |
| 16. Shift Right                   | FF 307.02 |
| 17. Divide                        | FF 308.01 |
| 18. Special Add                   | GT 309.06 |
| 19. Arithmetic Check              | GT 600.04 |
| 20. Clear Accumulator             |           |
| 21. Clear B-Register              |           |
| 22. Special Carry                 |           |

PROGRAM COUNTER CONTROL

- |                          |           |
|--------------------------|-----------|
| 1. In from Bus           | GT 102.01 |
| 2. Out to Bus            | GT 102.02 |
| 3. Out to Check Register | GT 102.03 |
| 4. Add Pulse             |           |
| 5. Clear                 |           |

PROGRAM REGISTER CONTROL

- |                |           |
|----------------|-----------|
| 1. In from Bus | GT 103.01 |
| 2. Out to Bus  | GT 103.02 |
| 3. Clear       |           |

CONTROL SWITCH CONTROL

- |                |           |
|----------------|-----------|
| 1. In from Bus | GT 104.01 |
| 2. Out to Bus  | GT 104.02 |
| 3. Clear       |           |

STEP COUNTER CONTROL

- |                |           |
|----------------|-----------|
| 1. In from Bus | GT 305.01 |
| 2. Out to Bus  | GT 305.02 |
| 3. Clear       |           |

PROGRAM STORAGE CONTROL

- |                              |           |
|------------------------------|-----------|
| 1. Bus to Storage Switch     | GT 201.01 |
| 2. Storage Switch to Bus     | GT 201.02 |
| 3. Storage Readout           | GT 203.02 |
| 4. Storage Switch Clear      |           |
| 5. Storage to Check Register | GT 203.03 |

OPERATION STORAGE CONTROL

- |                          |           |
|--------------------------|-----------|
| 1. In from Bus           | GT 203.01 |
| 2. Storage Readout       | GT 203.02 |
| 3. Out to Check Register | GT 203.03 |
| 4. Storage Clear         |           |

NOTE: See Figure 46

Figure 47  
CONTROL FUNCTIONS

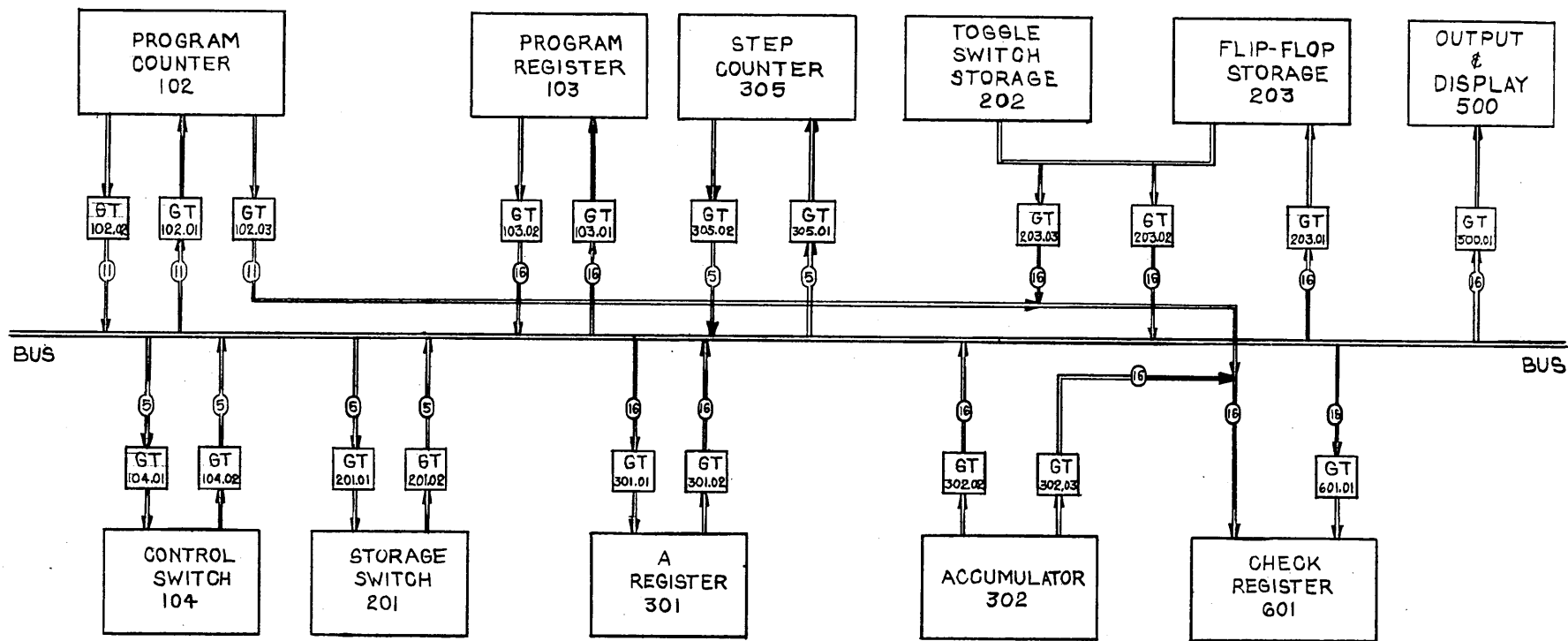
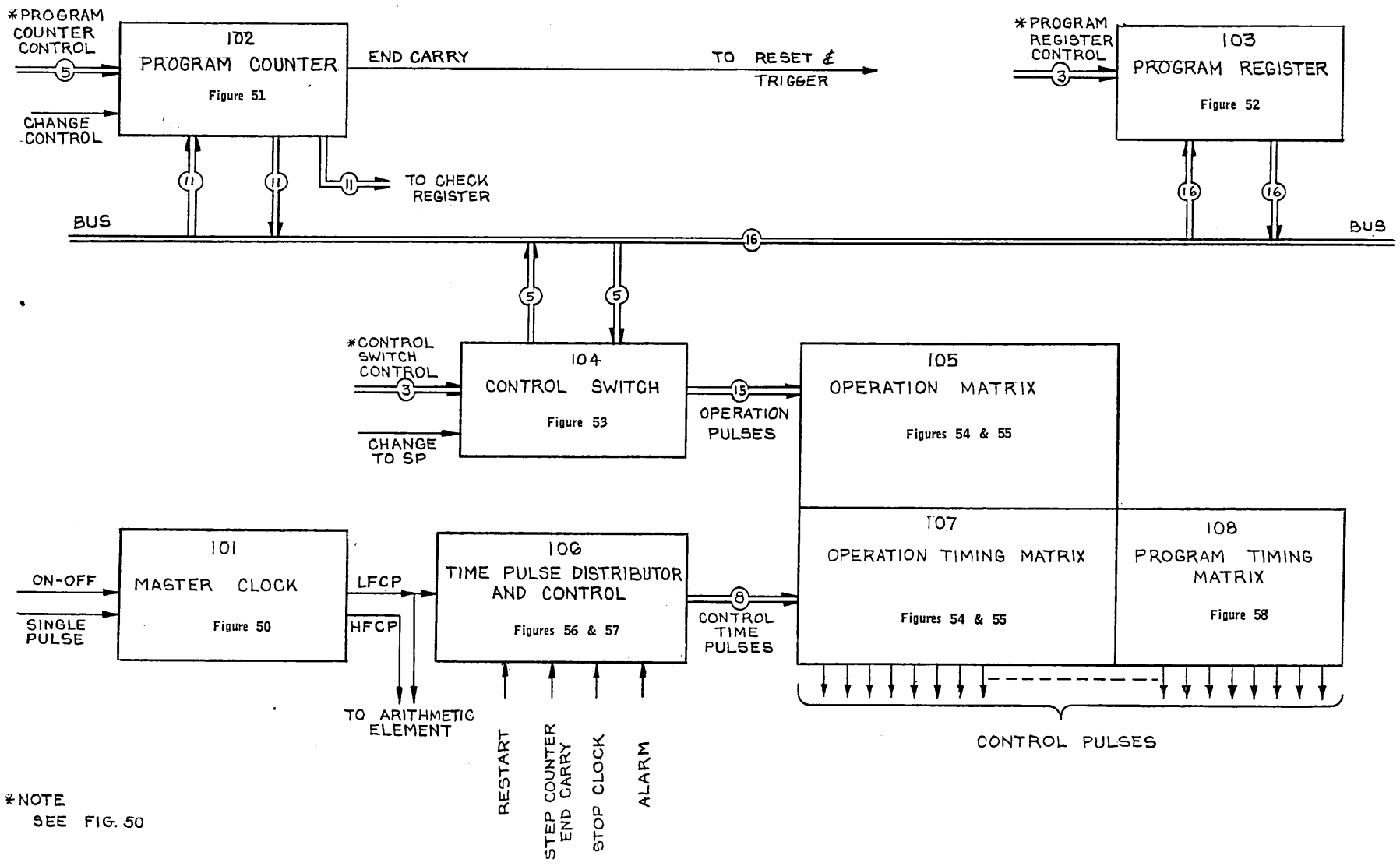


Figure 48  
BUS CONNECTIONS



\*NOTE  
SEE FIG. 50

Figure 49  
CONTROL



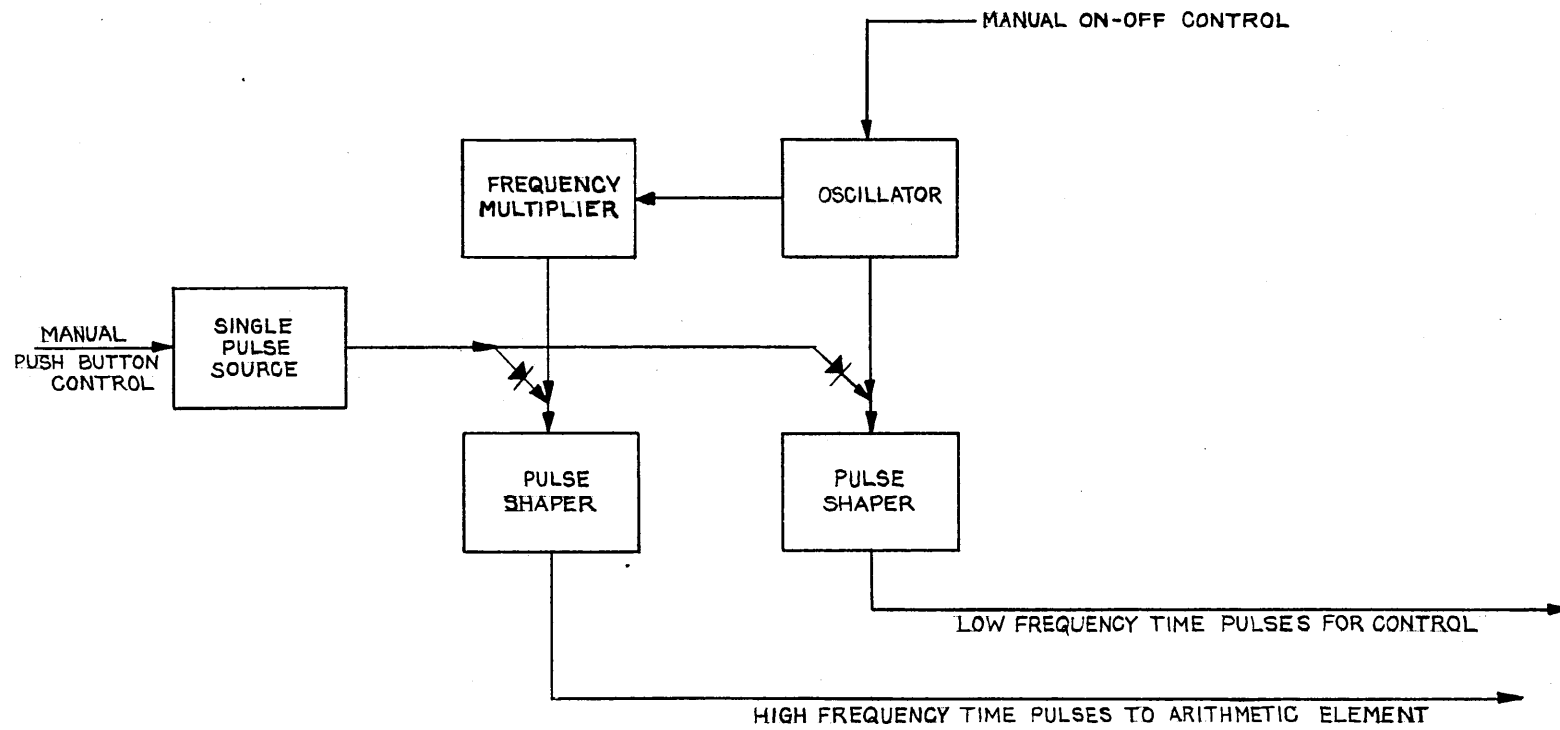


Figure 50  
MASTER CLOCK

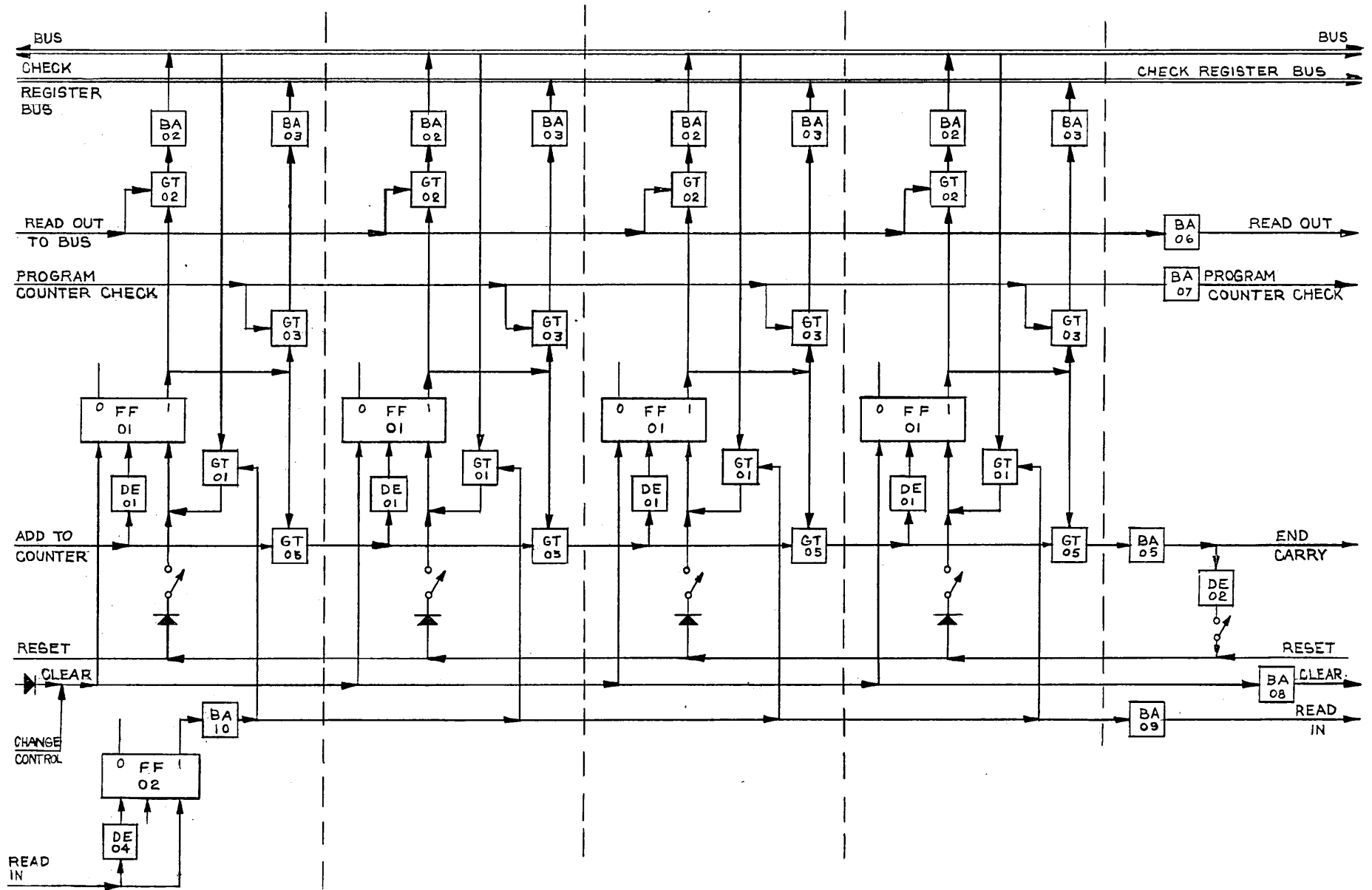


Figure 51  
PROGRAM COUNTER

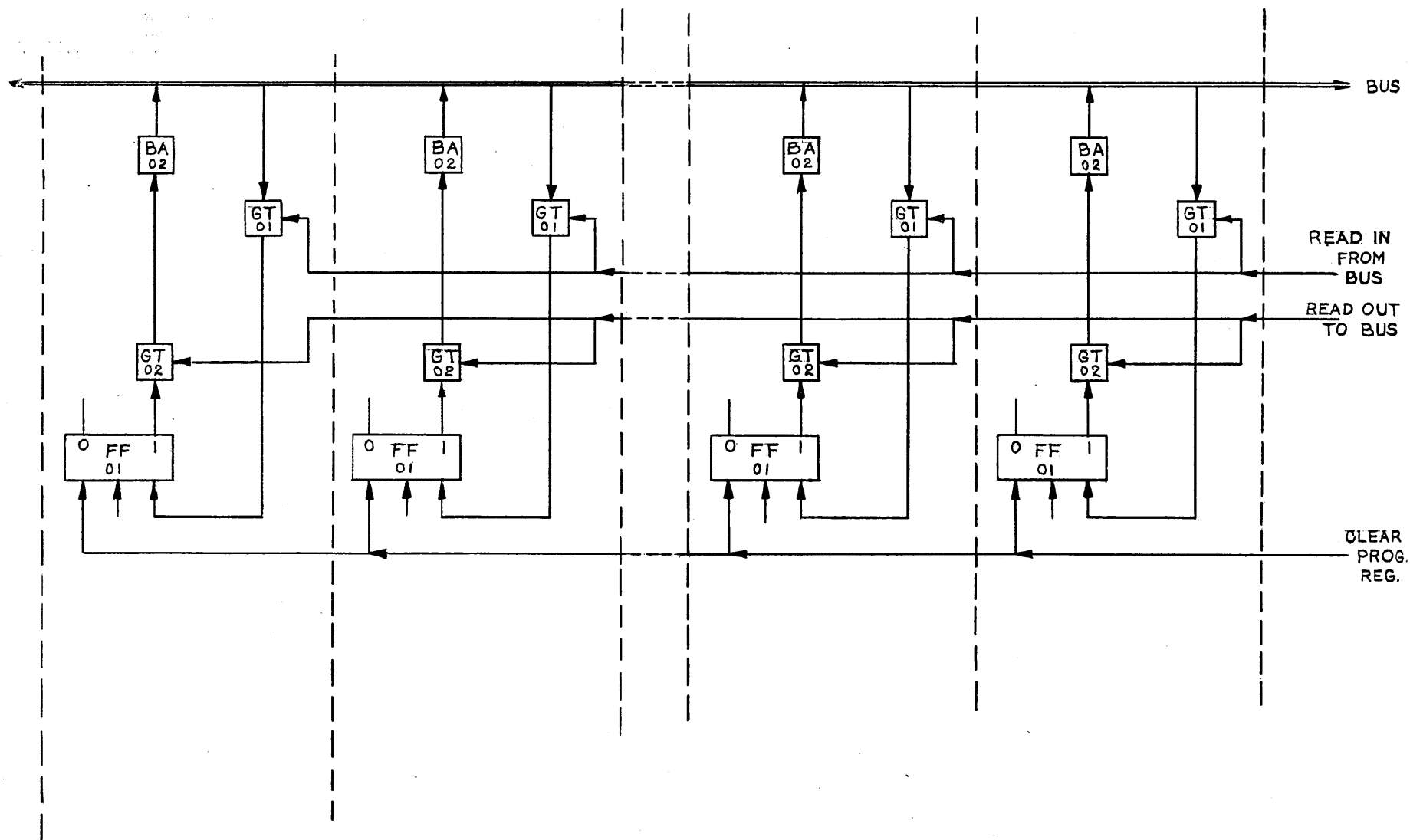


Figure 52  
PROGRAM REGISTER

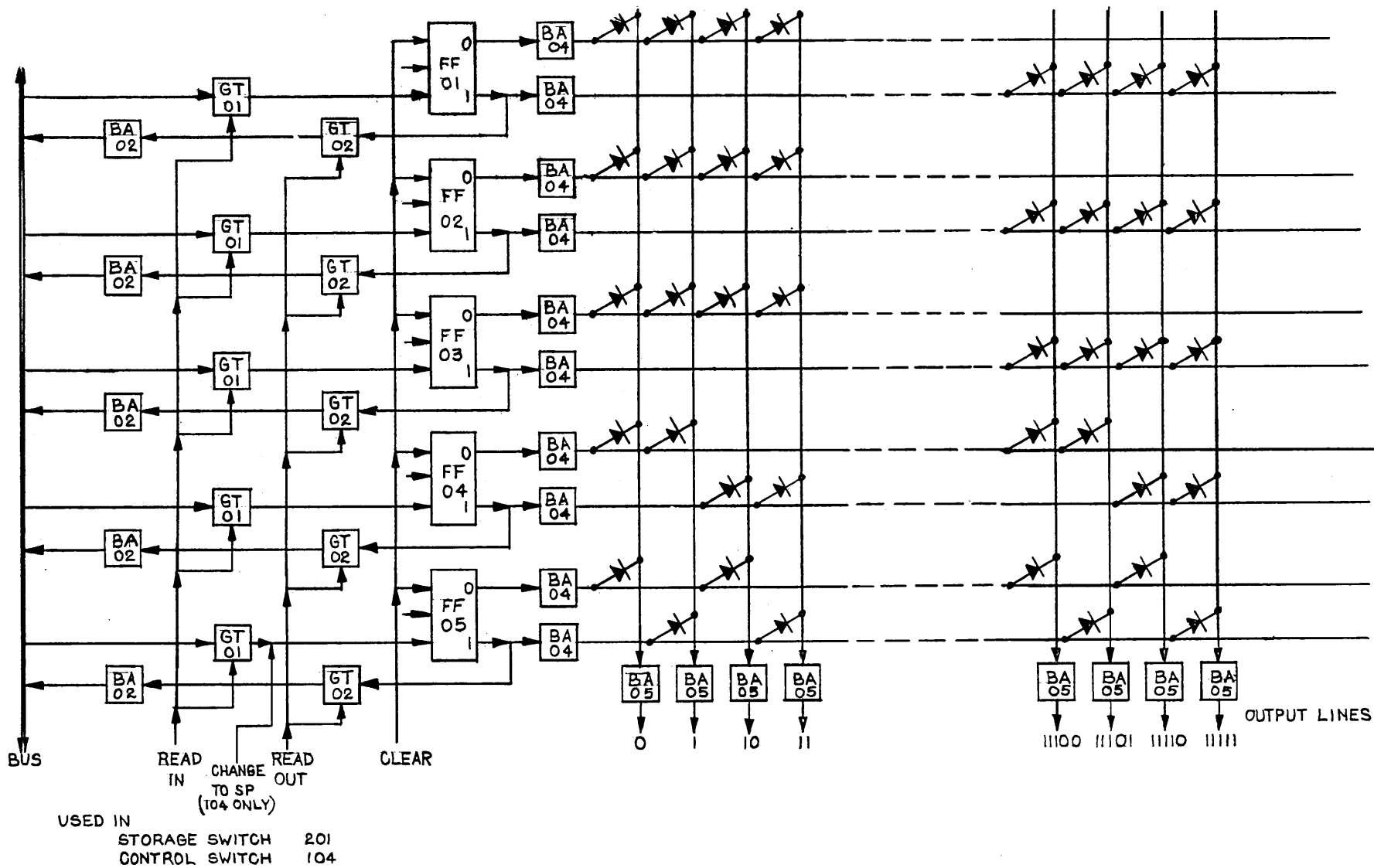


Figure 53  
 CONTROL SWITCH

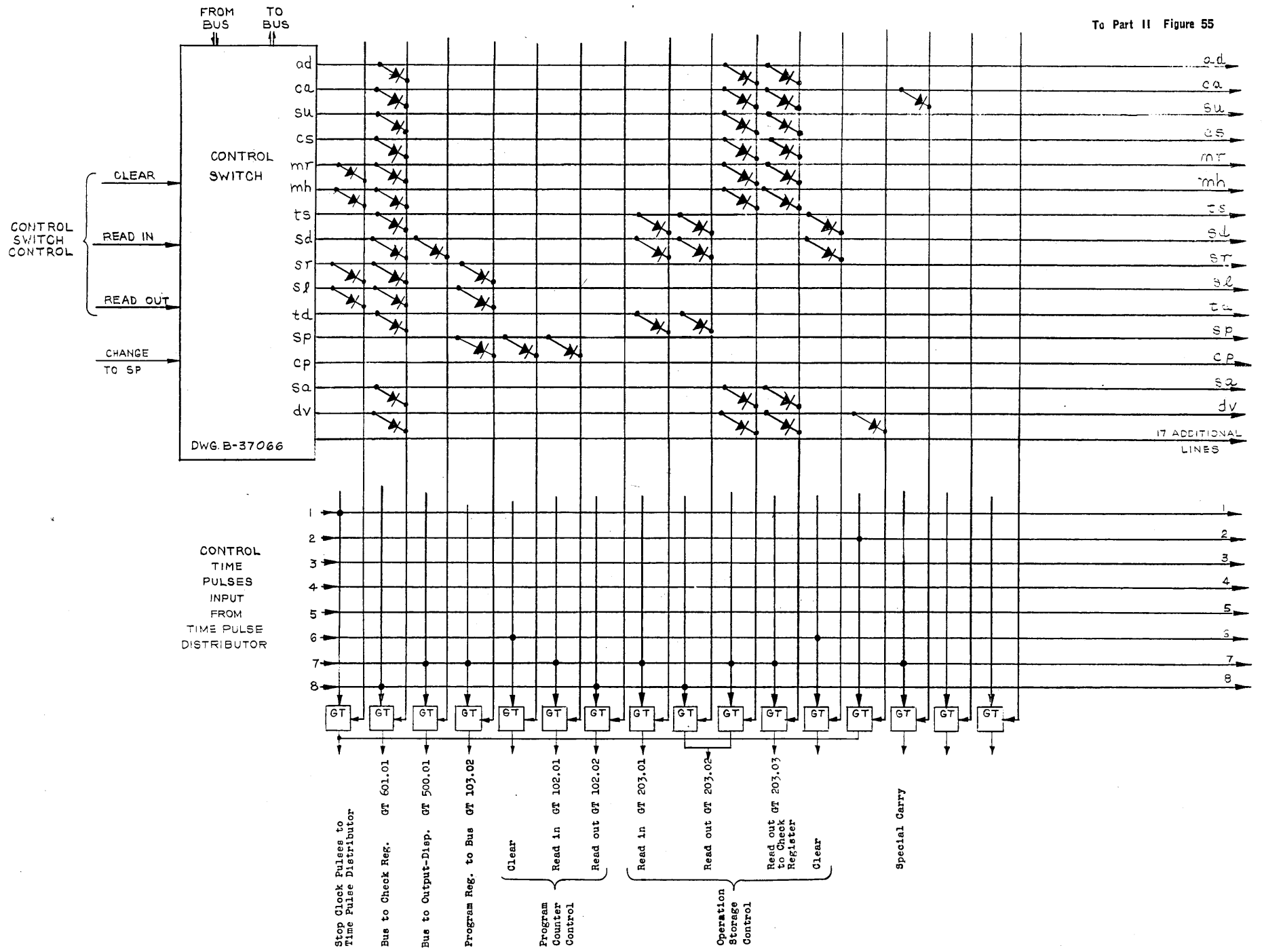


Figure 54  
OPERATION MATRIX I

FROM PART I  
Dwg. C-37077

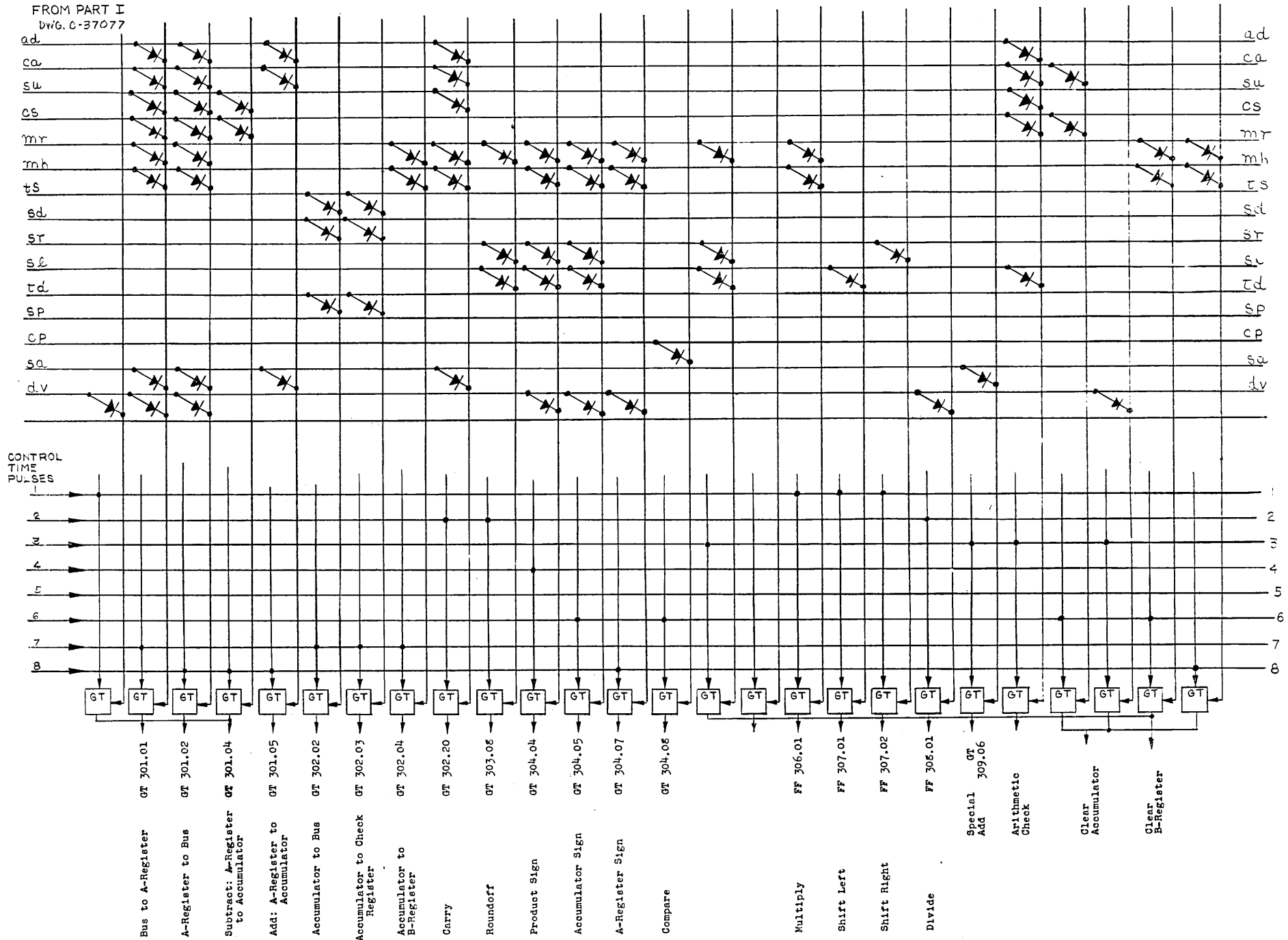


Figure 55  
OPERATION MATRIX II

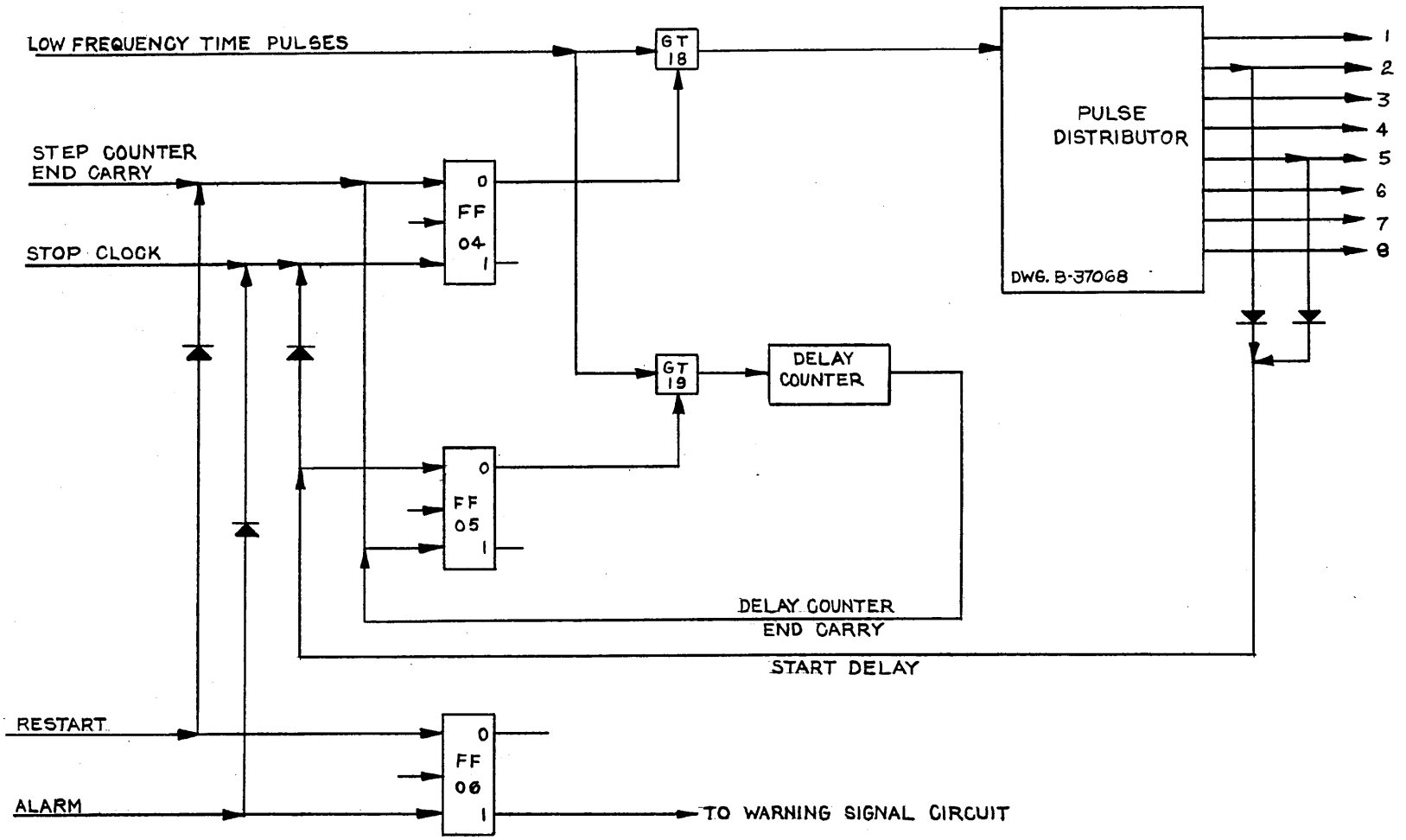


Figure 56  
 TIME PULSE DISTRIBUTOR CONTROL

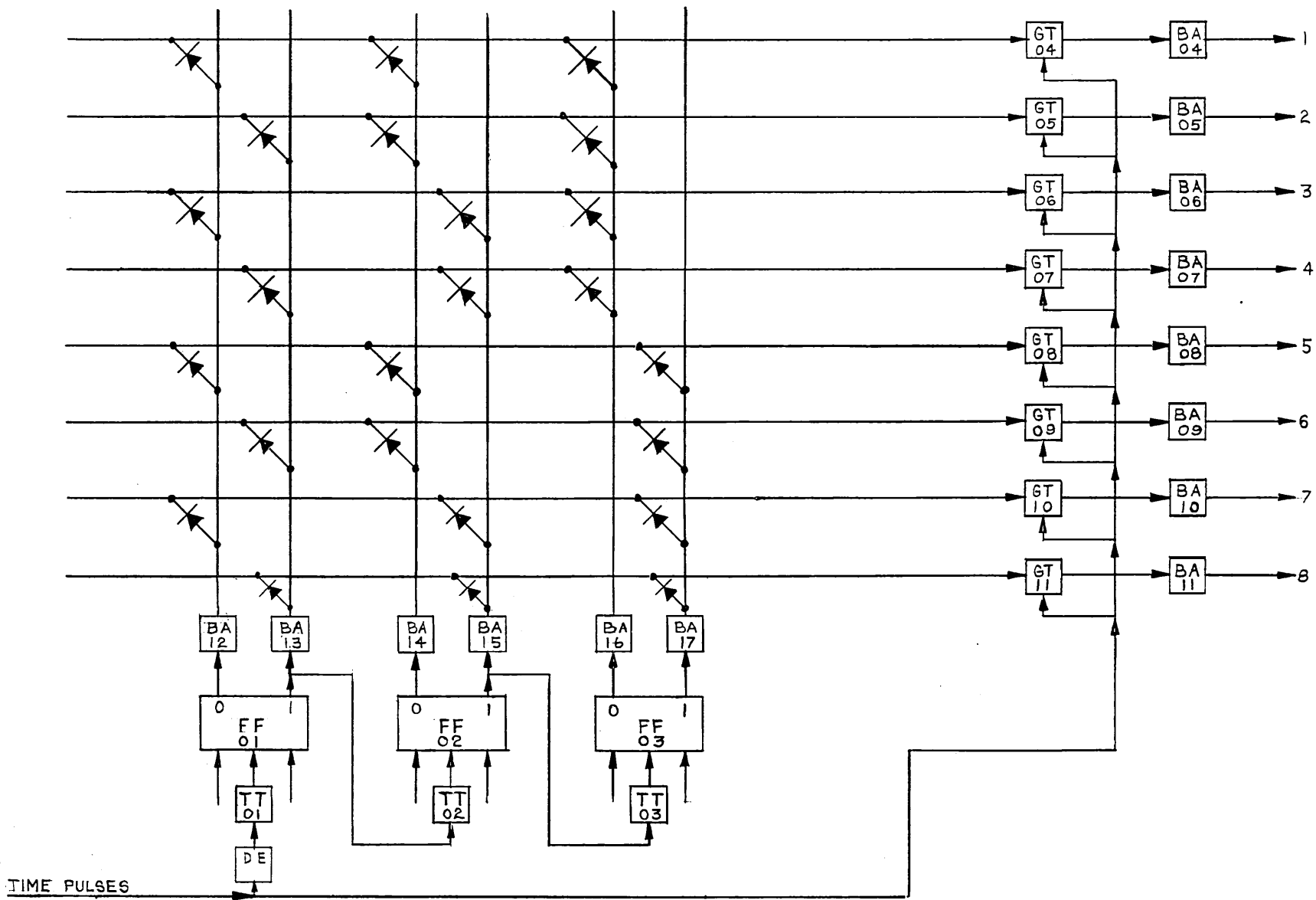


Figure 57  
PULSE DISTRIBUTOR



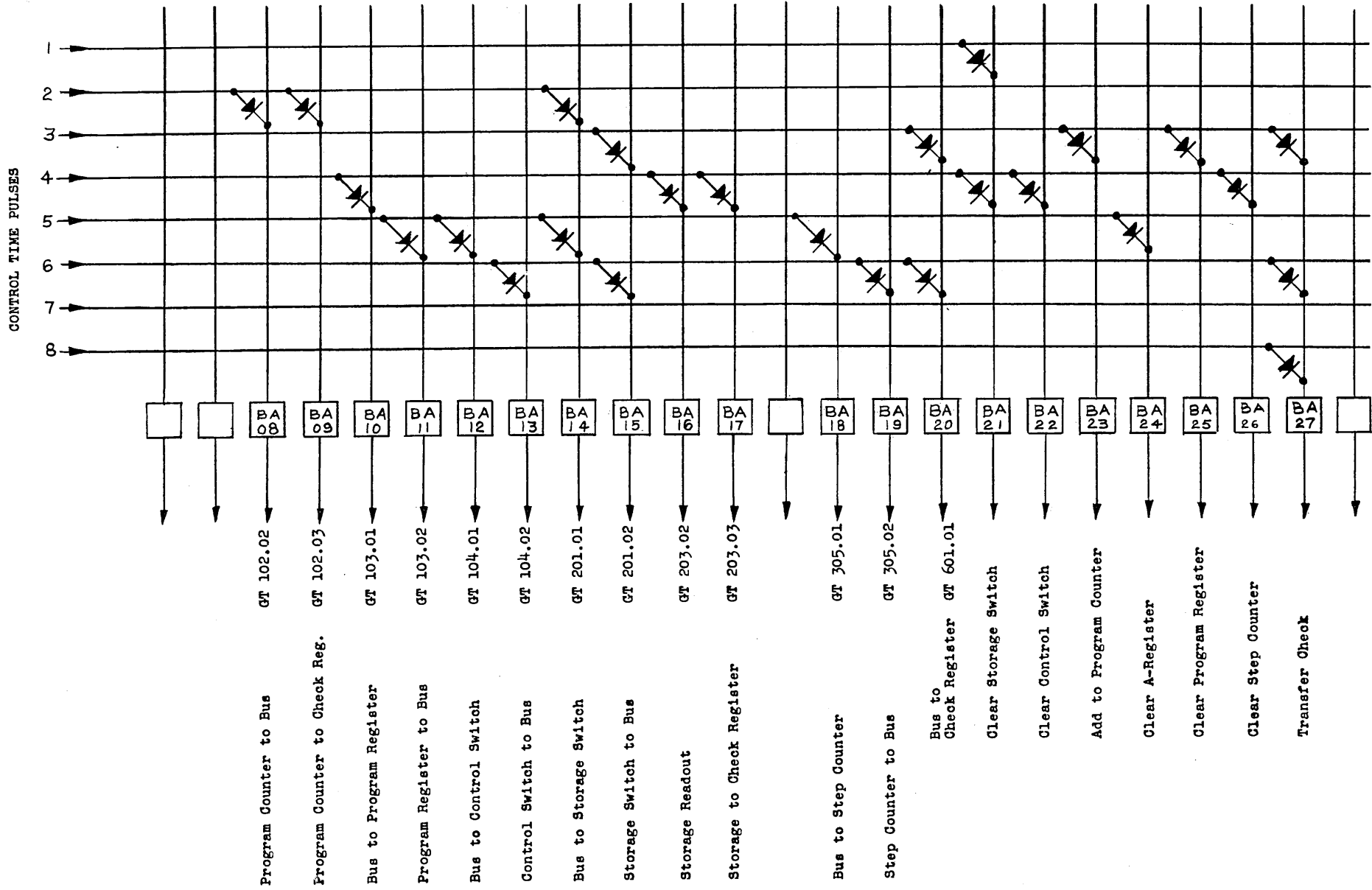


Figure 58  
PROGRAM TIMING MATRIX

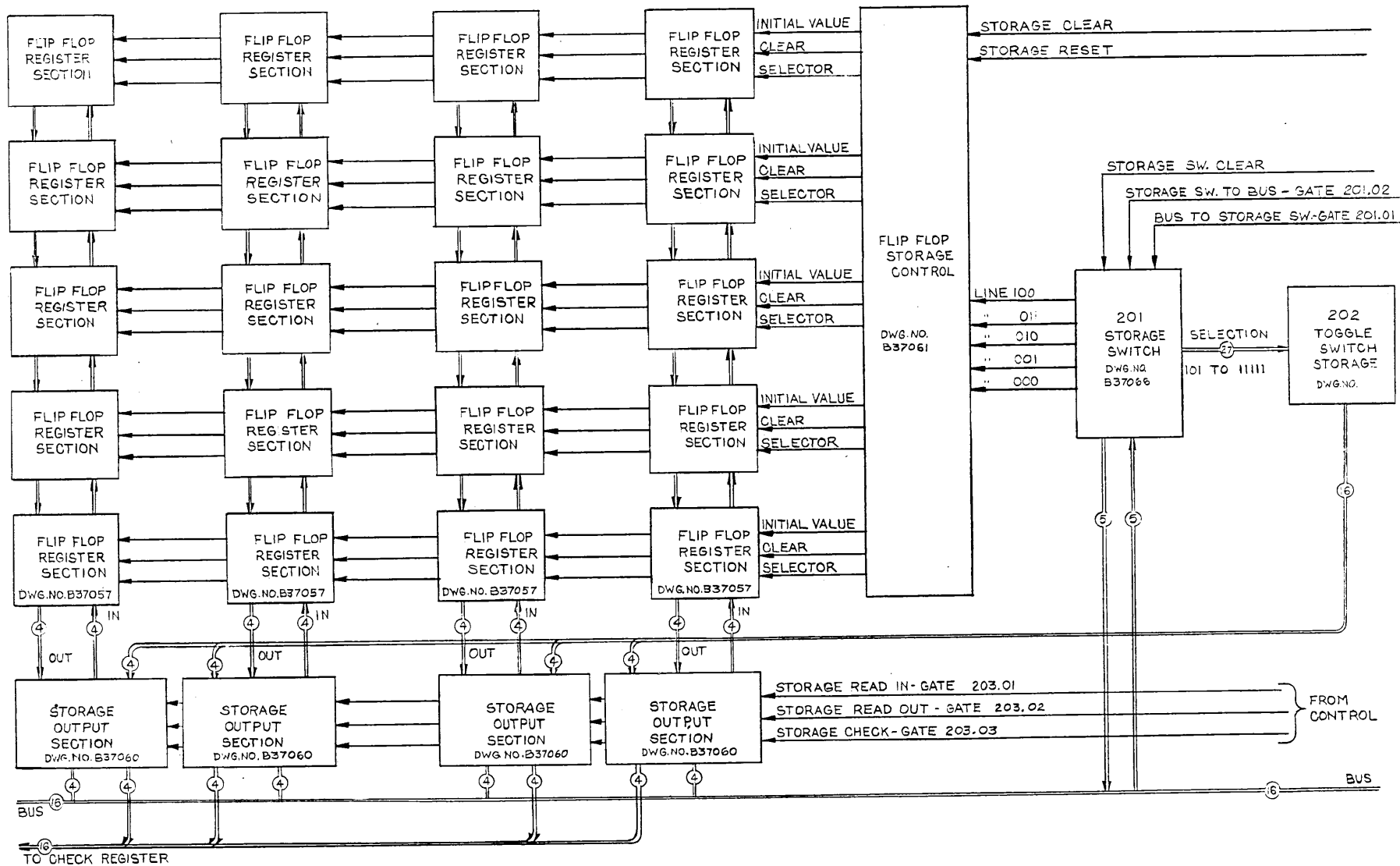
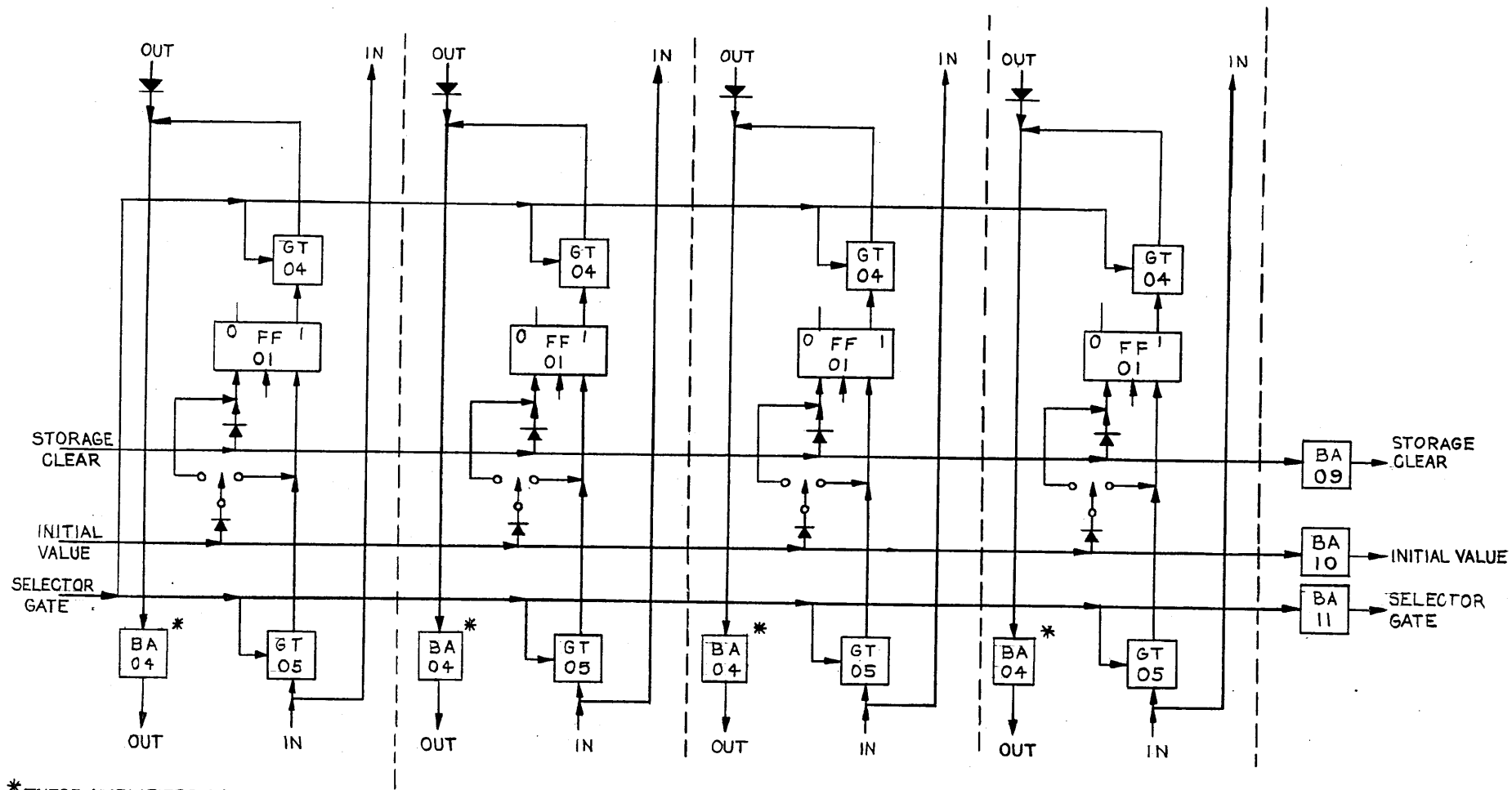


Figure 59

STORAGE CHASSIS ARRANGEMENT



\* THESE AMPLIFIERS IN  
BOTTOM SECTION ONLY.

Figure 60  
FLIP-FLOP STORAGE SECTION

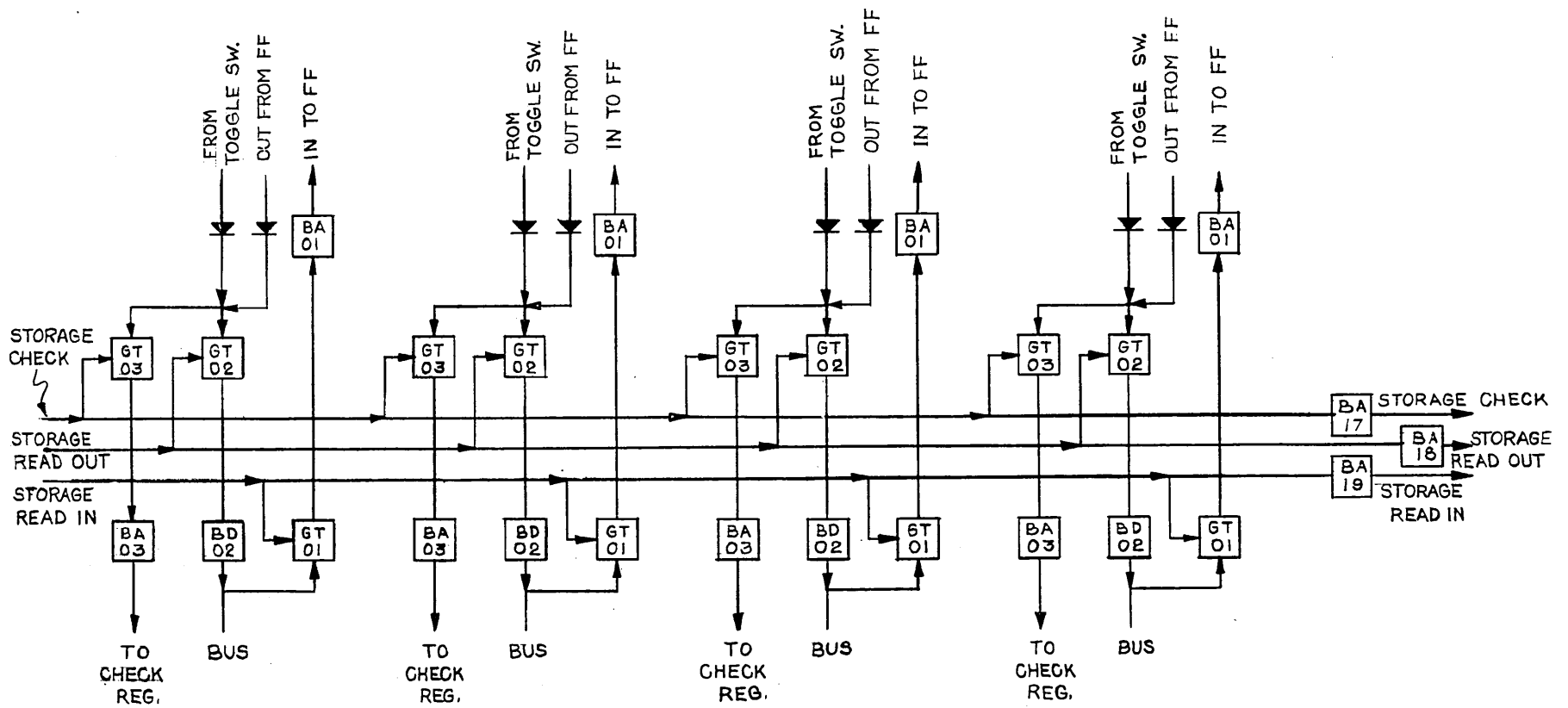


Figure 61  
STORAGE OUTPUT SECTION

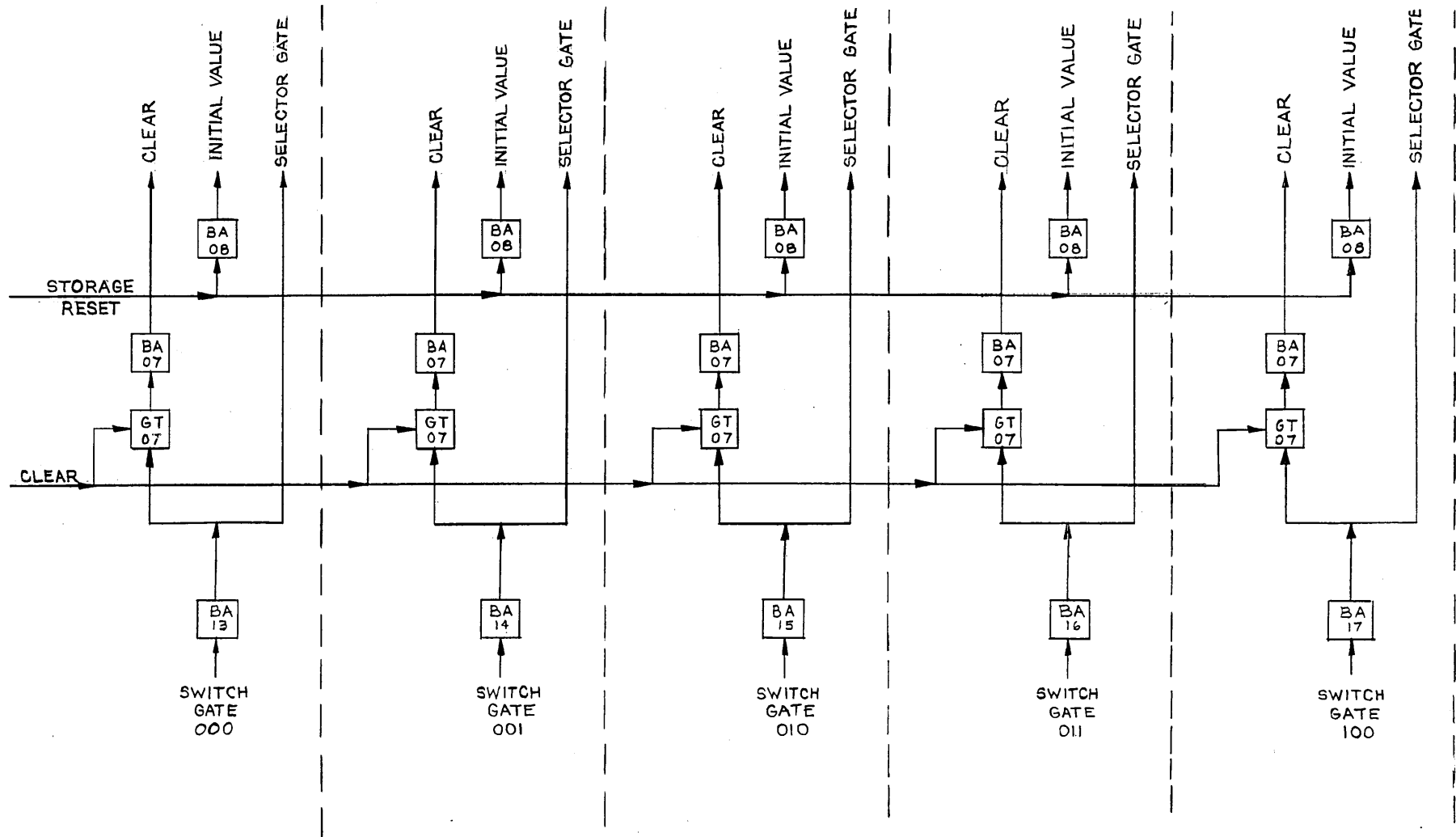


Figure 62  
 FLIP-FLOP STORAGE CONTROL

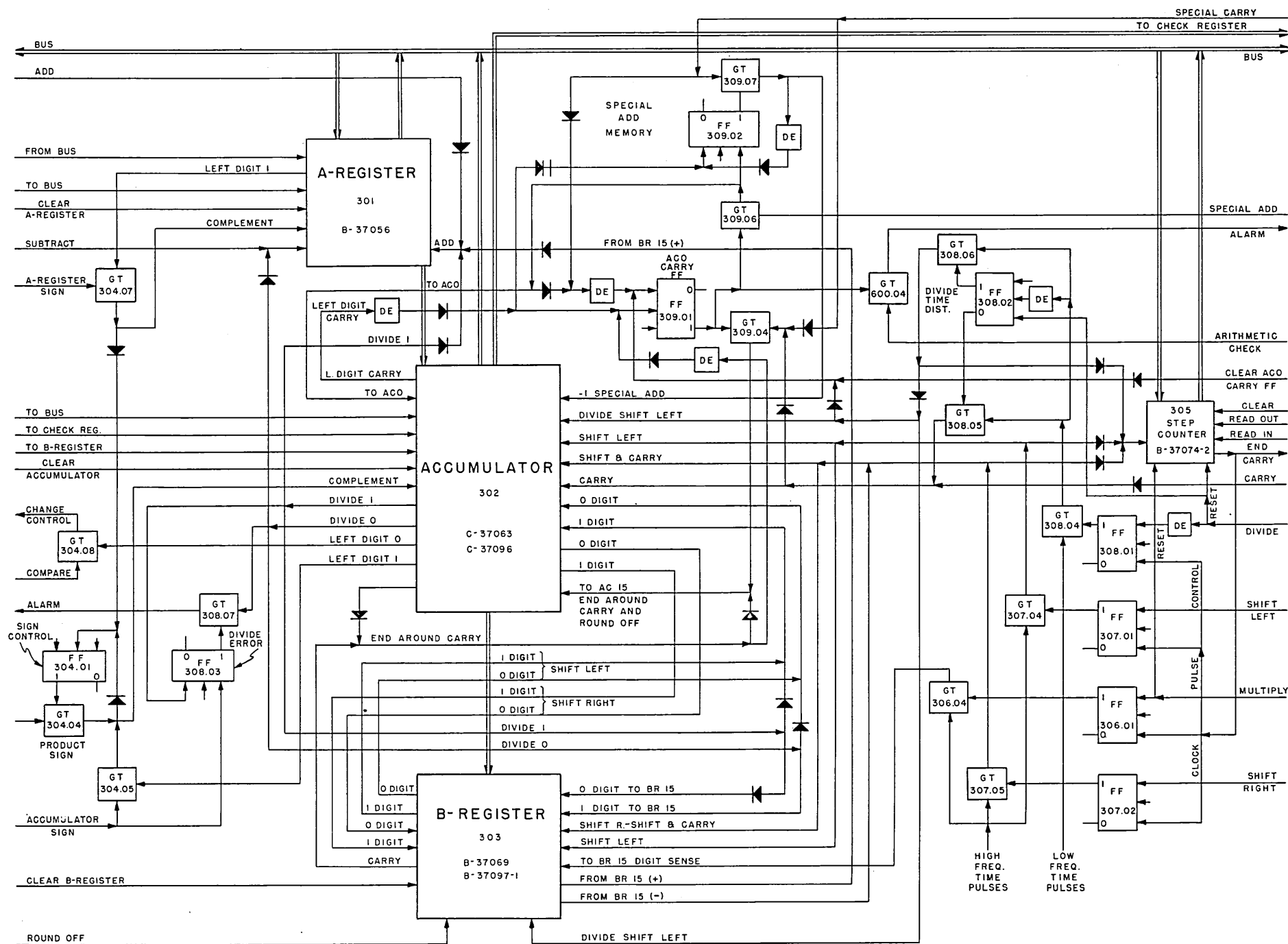


Figure 63  
ARITHMETIC ELEMENT

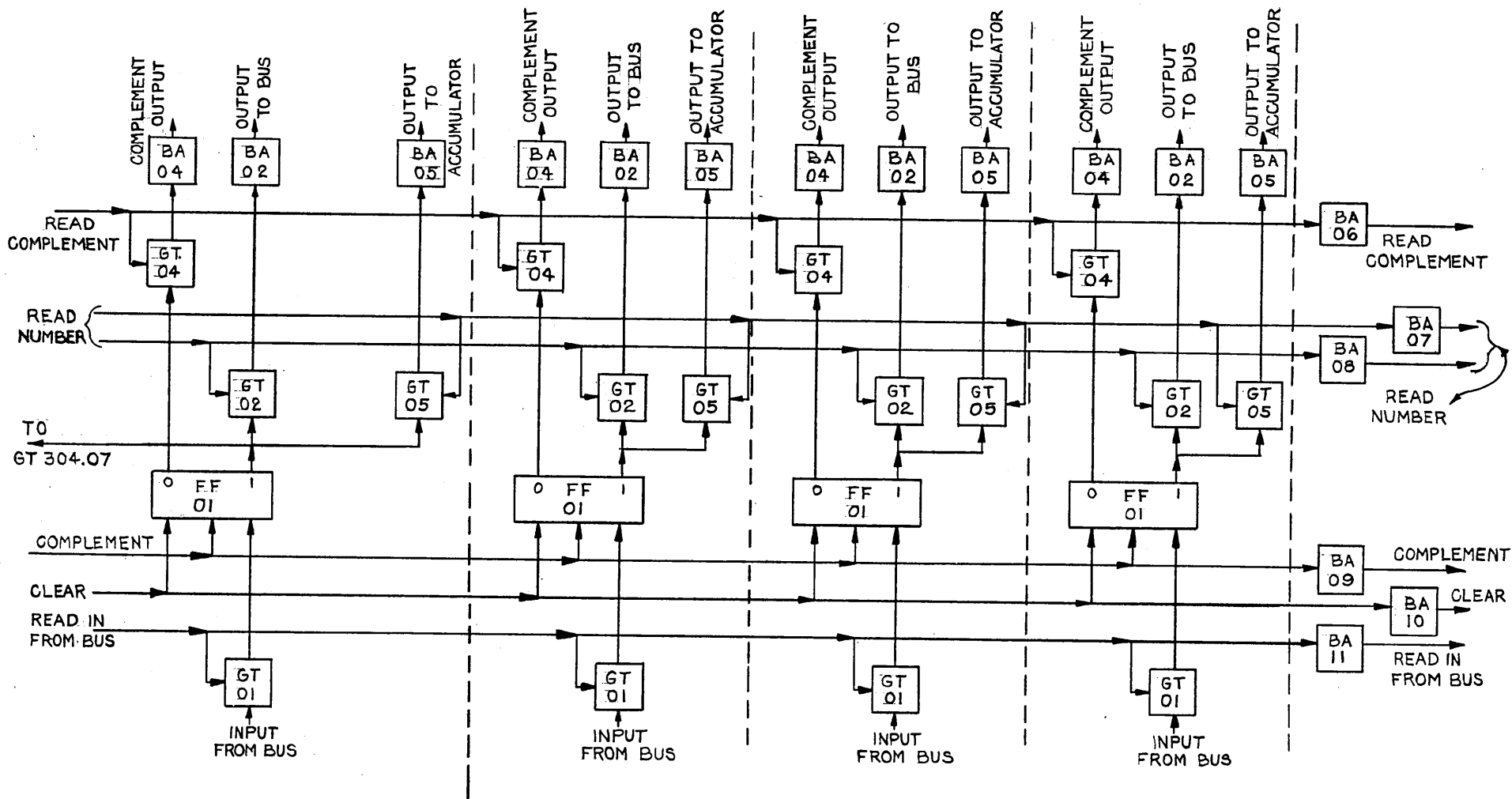


Figure 64  
SECTION OF A-REGISTER

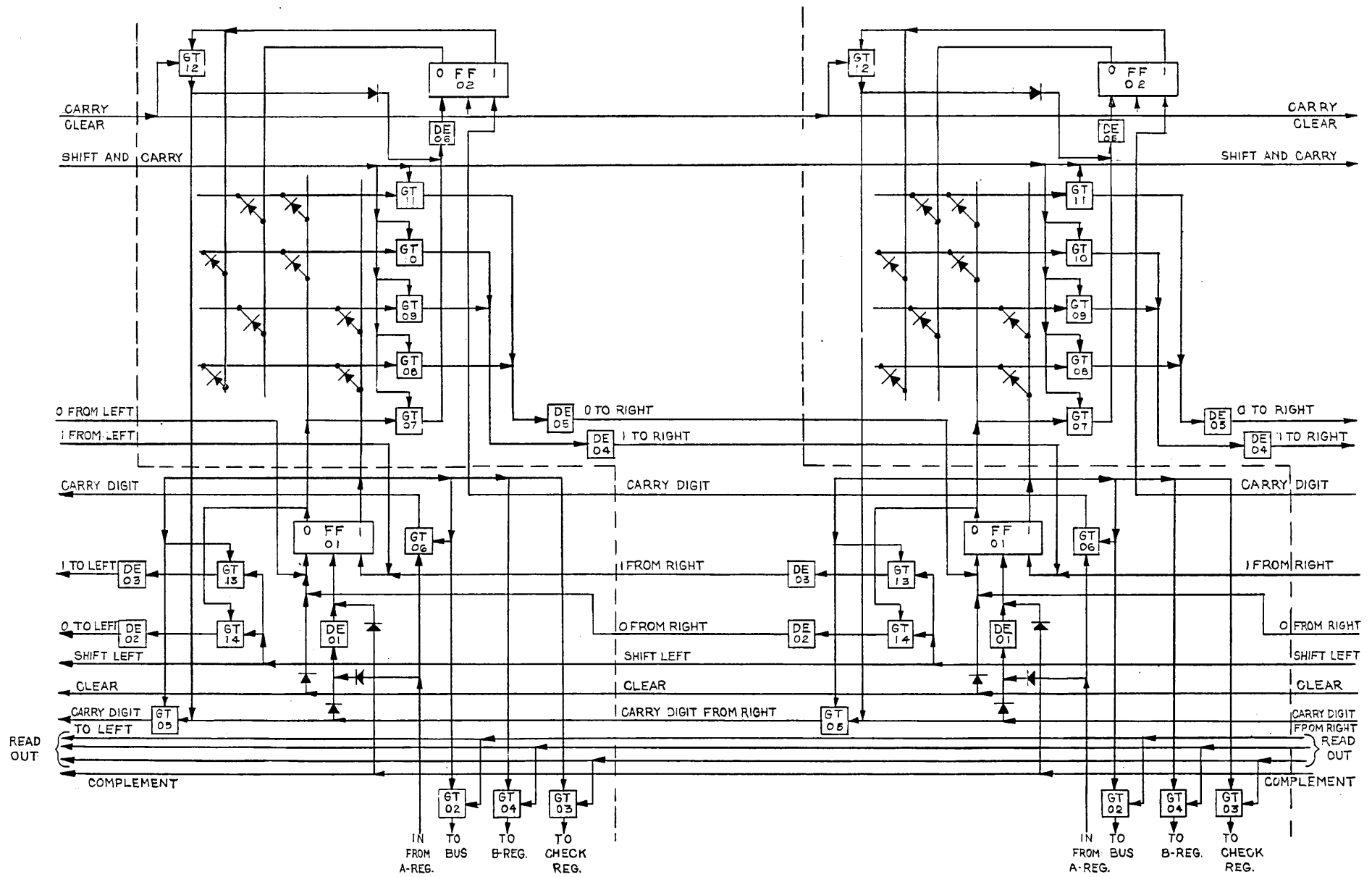


Figure 65  
ACCUMULATOR SECTIONS



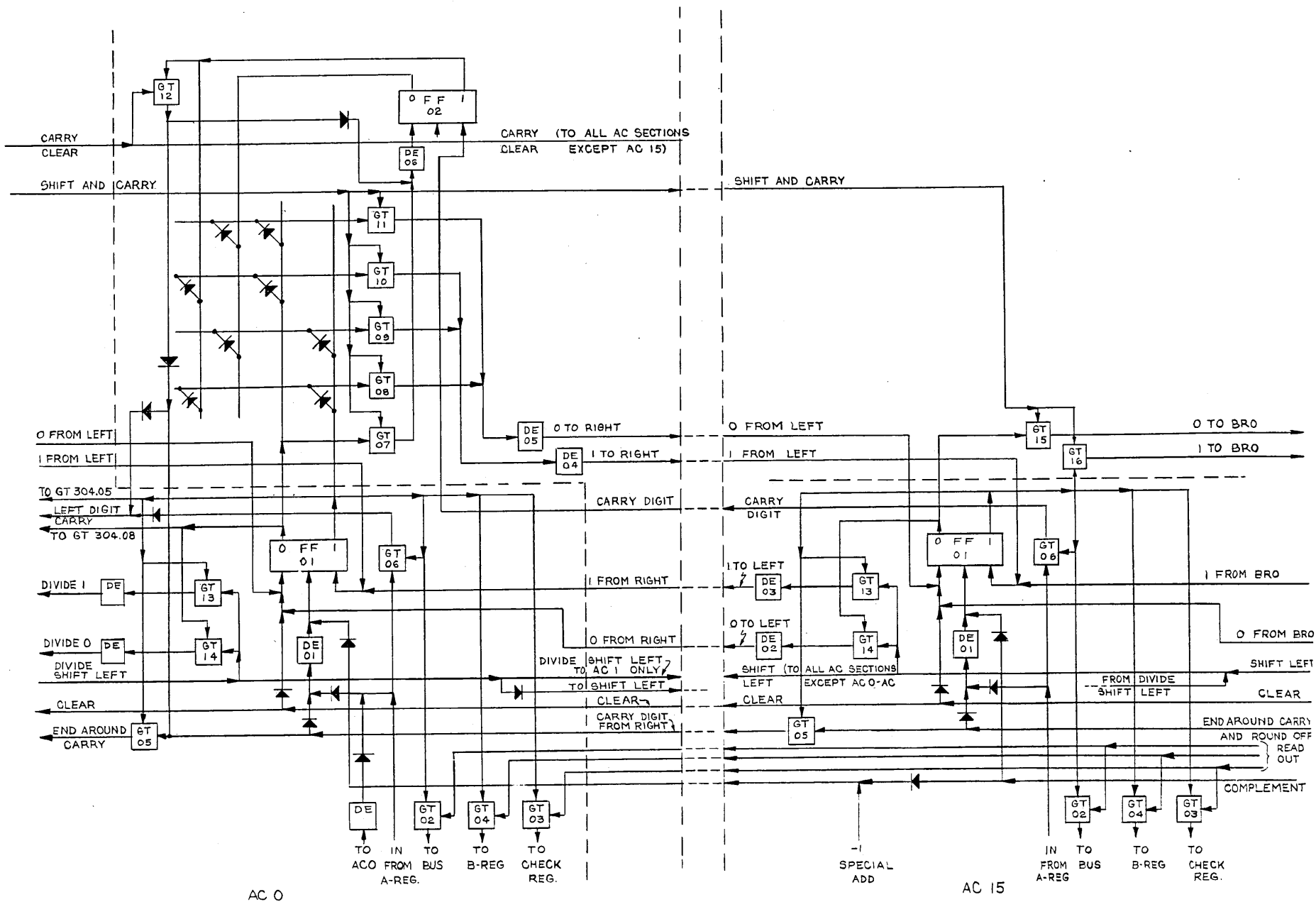


Figure 66  
ACCUMULATOR SECTIONS AC0-AC15

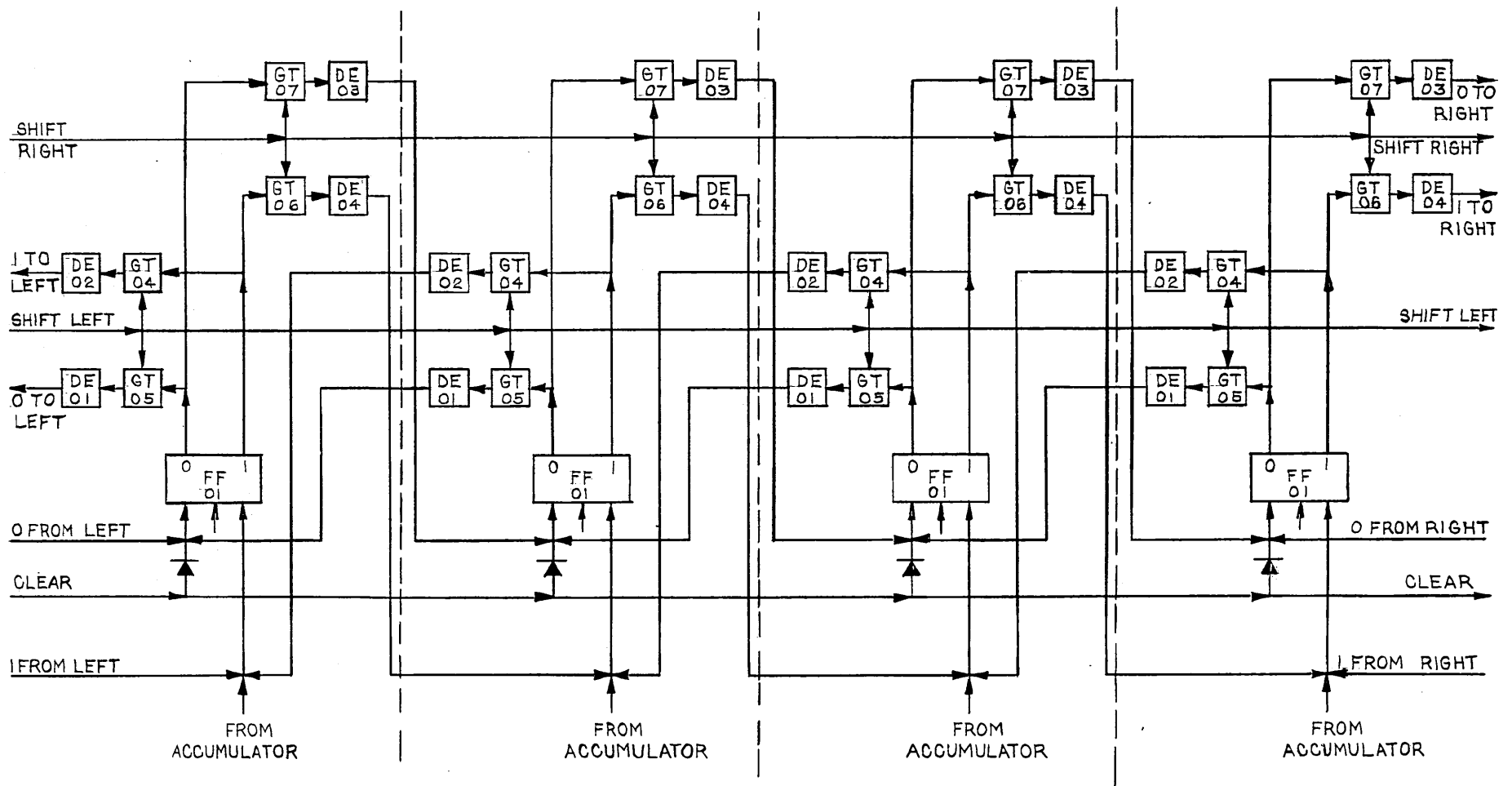


Figure 67  
B-REGISTER SECTIONS

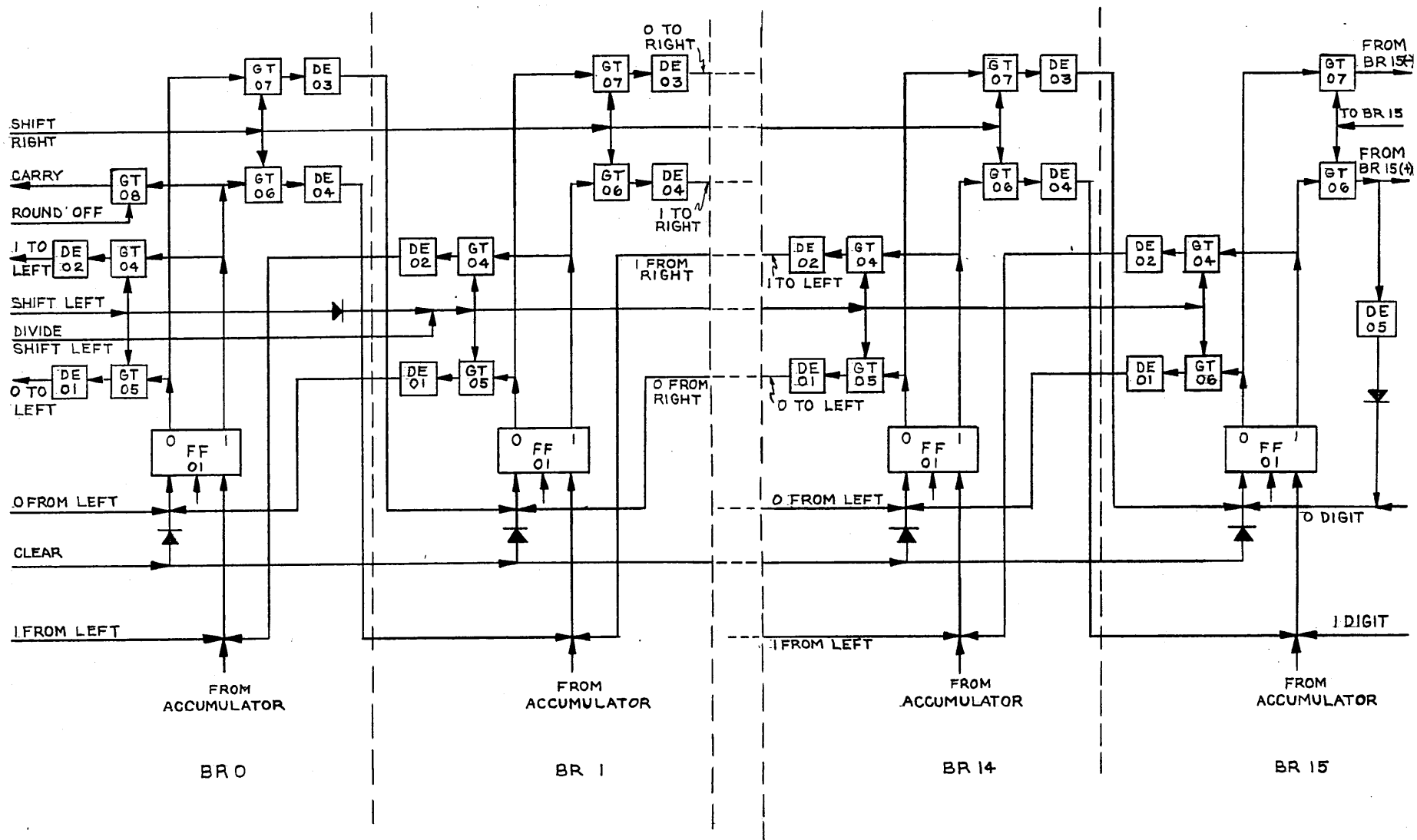


Figure 68  
 B-REGISTER SECTIONS BR 0, 1, 14, 15

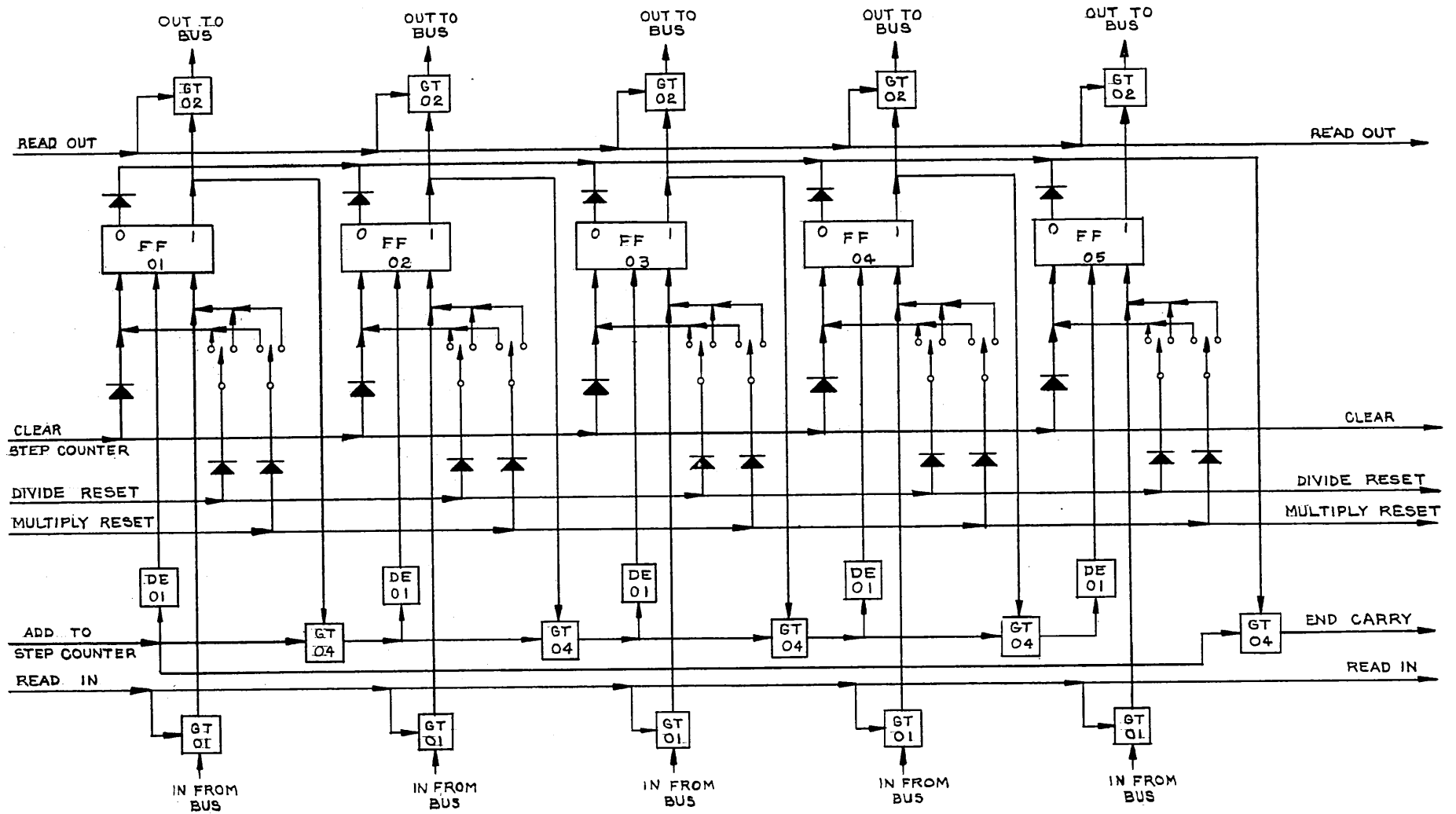


Figure 69  
STEP COUNTER

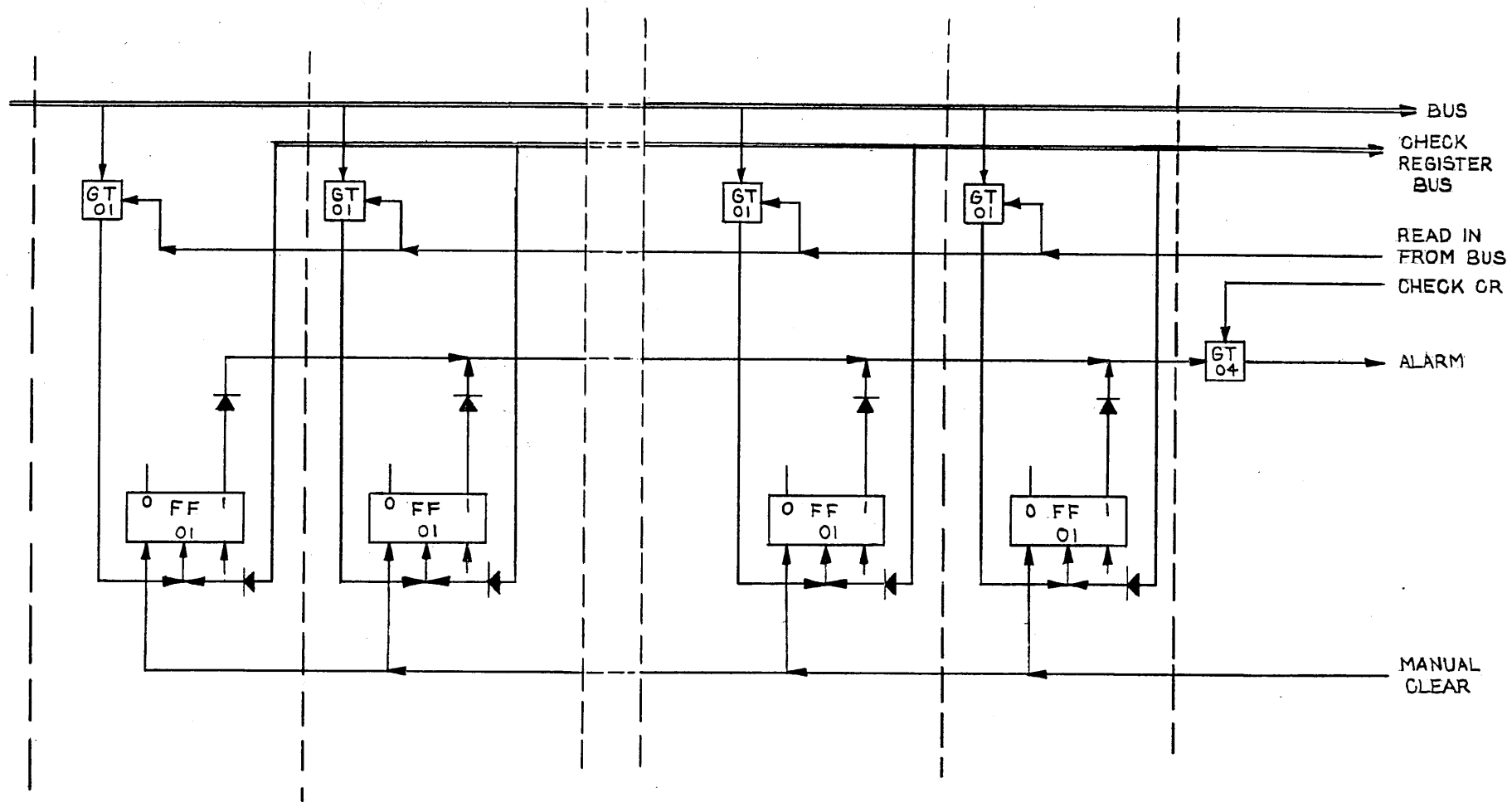


Figure 70  
CHECK REGISTER

**CONTROL TIME PULSES**

1 2 3 4 5 6 7 8 1 2 3 4

PROGRAM COUNTER TO BUS . . . . . GT 102.02  
 PROG. COUNTER TO CHECK REGISTER. . . . . GT 102.03  
 BUS TO PROGRAM REGISTER . . . . . GT 103.01  
 PROGRAM REGISTER TO BUS . . . . . GT 103.02  
 BUS TO CONTROL SWITCH . . . . . GT 104.01  
 CONTROL SWITCH TOBUS. . . . . GT 104.02  
 BUS TO STORAGE SWITCH . . . . . GT 201.01  
 STORAGE SWITCH TOBUS . . . . . GT 201.02  
 STORAGE READOUT . . . . . GT 203.02  
 STORAGE TO CHECK REGISTER . . . . . GT 203.03  
 BUS TO STEP COUNTER . . . . . GT 305.01  
 STEP COUNTER TO BUS . . . . . GT 305.02  
 BUS TO CHECK REGISTER . . . . . GT 601.01  
 START DELAY COUNTER . . . . .  
 ADD TO PROGRAM COUNTER . . . . .  
 CLEAR CONTROL SWITCH . . . . .  
 CLEAR STORAGE SWITCH . . . . .  
 CLEAR A-REGISTER . . . . .  
 CLEAR PROGRAM REGISTER . . . . .  
 CLEAR STEP COUNTER . . . . .  
 TRANSFER CHECK . . . . .

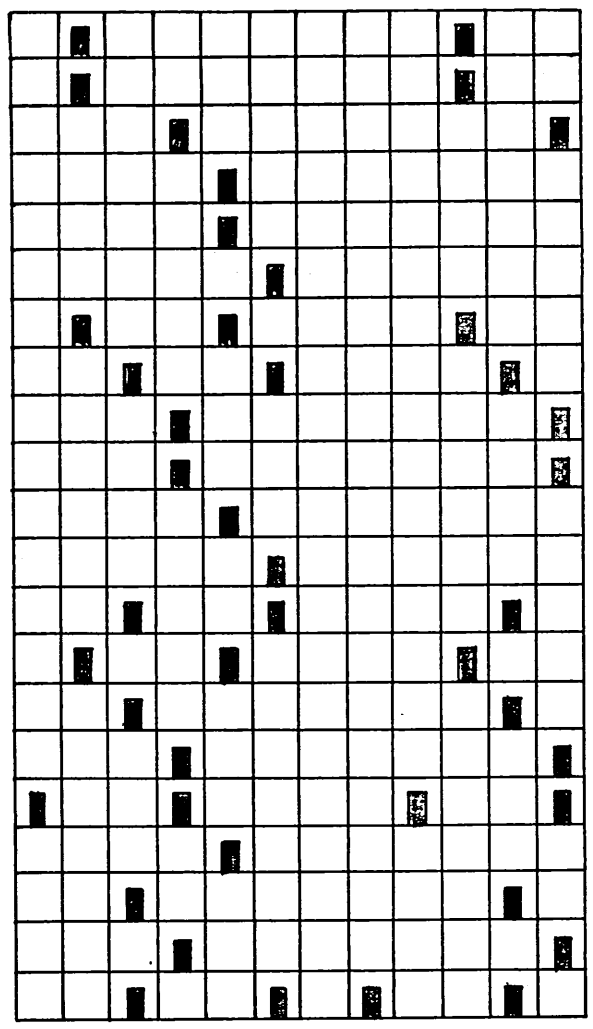


Figure 71  
**PROGRAM TIMING**

CONTROL TIME PULSES  
1 2 3 4 5 6 7 8 1 2 3 4

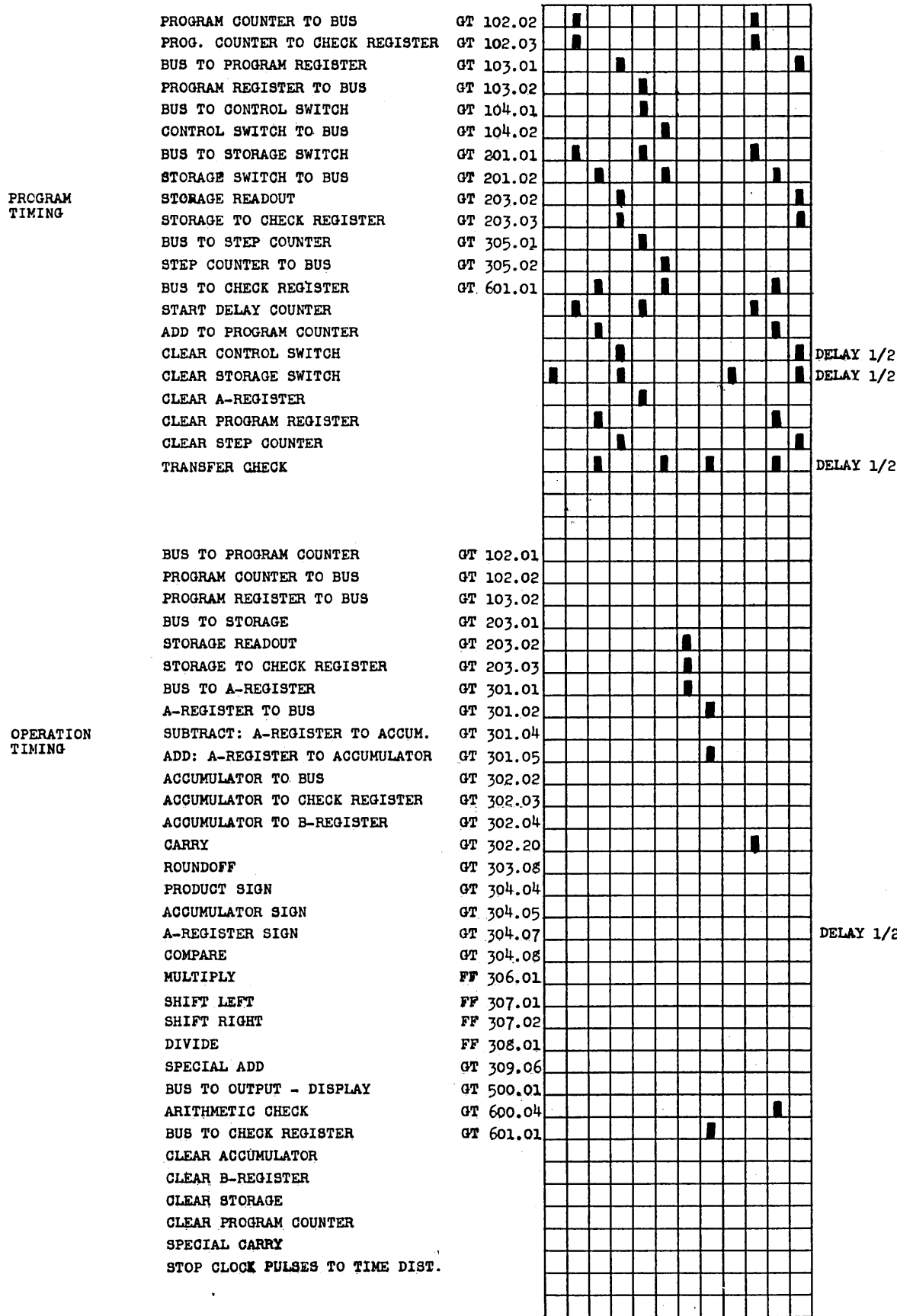


Figure 72

TIMING FOR ADD

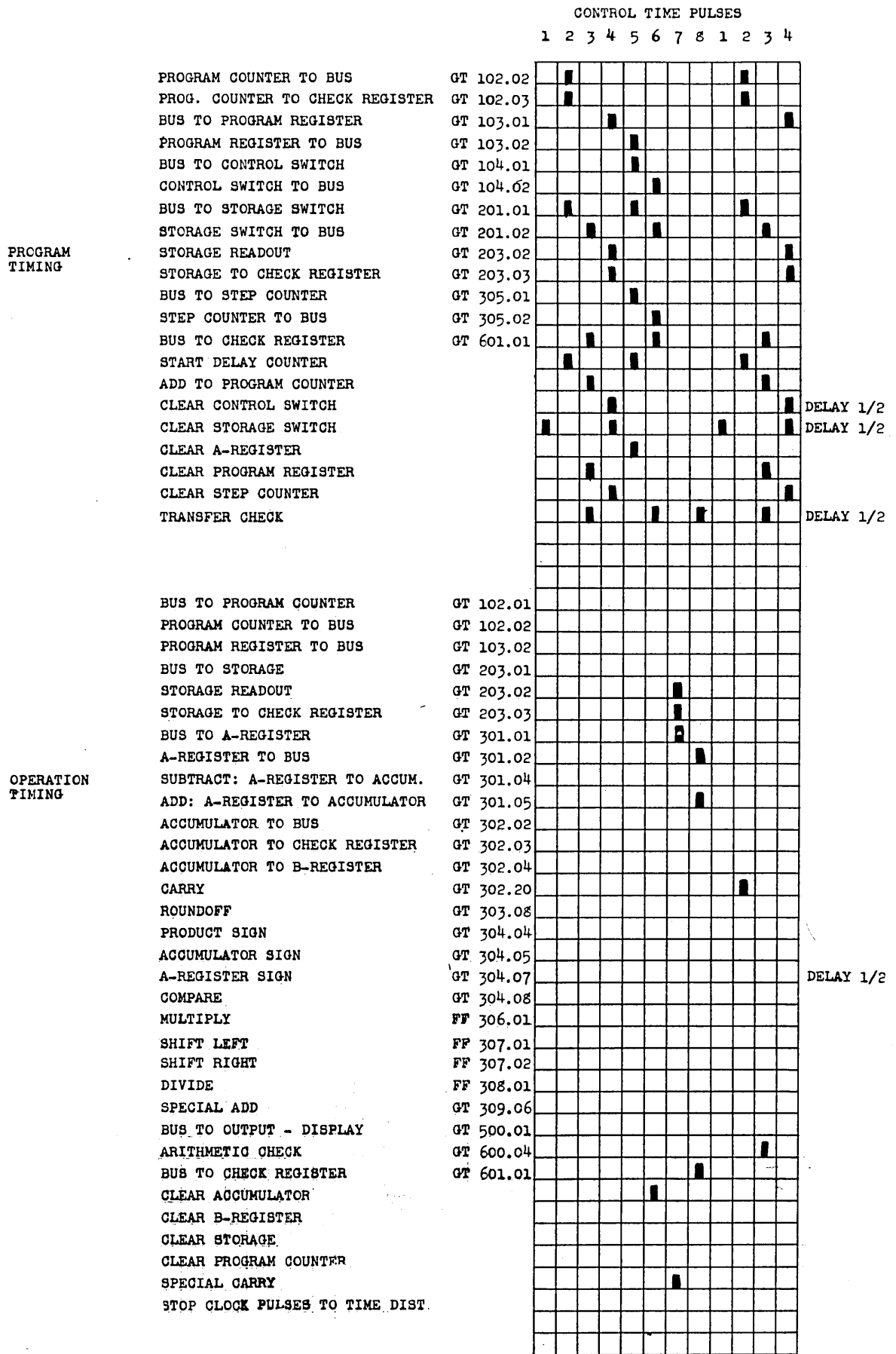


Figure 73  
TIMING FOR CLEAR AND ADD

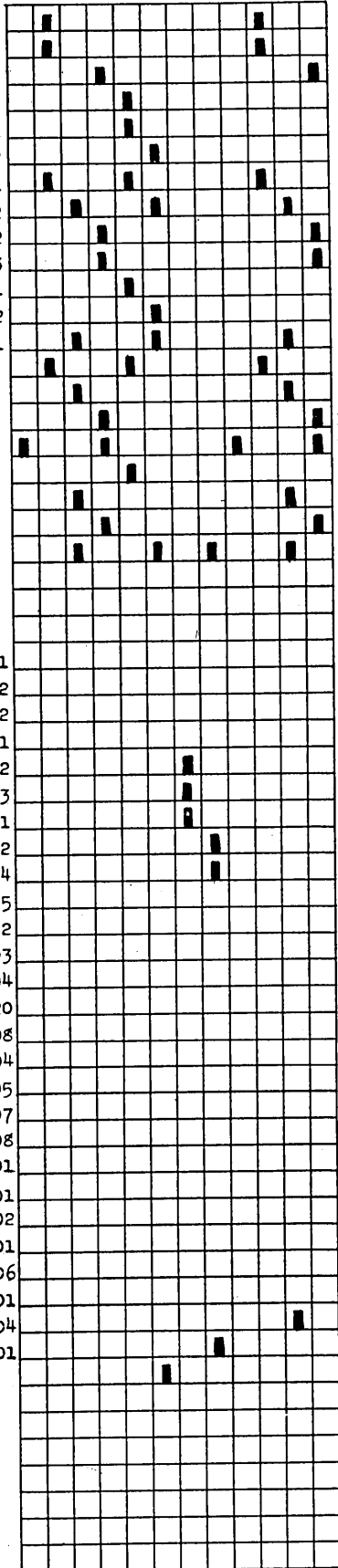




CONTROL TIME PULSES  
1 2 3 4 5 6 7 8 1 2 3 4

PROGRAM  
TIMING

PROGRAM COUNTER TO BUS GT 102.02  
 PROG. COUNTER TO CHECK REGISTER GT 102.03  
 BUS TO PROGRAM REGISTER GT 103.01  
 PROGRAM REGISTER TO BUS GT 103.02  
 BUS TO CONTROL SWITCH GT 104.01  
 CONTROL SWITCH TO BUS GT 104.02  
 BUS TO STORAGE SWITCH GT 201.01  
 STORAGE SWITCH TO BUS GT 201.02  
 STORAGE READOUT GT 203.02  
 STORAGE TO CHECK REGISTER GT 203.03  
 BUS TO STEP COUNTER GT 305.01  
 STEP COUNTER TO BUS GT 305.02  
 BUS TO CHECK REGISTER GT 601.01  
 START DELAY COUNTER  
 ADD TO PROGRAM COUNTER  
 CLEAR CONTROL SWITCH  
 CLEAR STORAGE SWITCH  
 CLEAR A-REGISTER  
 CLEAR PROGRAM REGISTER  
 CLEAR STEP COUNTER  
 TRANSFER CHECK



DELAY 1/2  
DELAY 1/2

DELAY 1/2

OPERATION  
TIMING

BUS TO PROGRAM COUNTER GT 102.01  
 PROGRAM COUNTER TO BUS GT 102.02  
 PROGRAM REGISTER TO BUS GT 103.02  
 BUS TO STORAGE GT 203.01  
 STORAGE READOUT GT 203.02  
 STORAGE TO CHECK REGISTER GT 203.03  
 BUS TO A-REGISTER GT 301.01  
 A-REGISTER TO BUS GT 301.02  
 SUBTRACT: A-REGISTER TO ACCUM. GT 301.04  
 ADD: A-REGISTER TO ACCUMULATOR GT 301.05  
 ACCUMULATOR TO BUS GT 302.02  
 ACCUMULATOR TO CHECK REGISTER GT 302.03  
 ACCUMULATOR TO B-REGISTER GT 302.04  
 CARRY GT 302.20  
 ROUNDOFF GT 303.08  
 PRODUCT SIGN GT 304.04  
 ACCUMULATOR SIGN GT 304.05  
 A-REGISTER SIGN GT 304.07  
 COMPARE GT 304.08  
 MULTIPLY FF 306.01  
 SHIFT LEFT FF 307.01  
 SHIFT RIGHT FF 307.02  
 DIVIDE FF 308.01  
 SPECIAL ADD GT 309.06  
 BUS TO OUTPUT - DISPLAY GT 500.01  
 ARITHMETIC CHECK GT 600.04  
 BUS TO CHECK REGISTER GT 601.01  
 CLEAR ACCUMULATOR  
 CLEAR B-REGISTER  
 CLEAR STORAGE  
 CLEAR PROGRAM COUNTER  
 SPECIAL CARRY  
 STOP CLOCK PULSES TO TIME DIST.

DELAY 1/2

Figure 75  
TIMING FOR CLEAR AND SUBTRACT

OPERATION: MULTIPLY AND ROUND OFF    **mf**

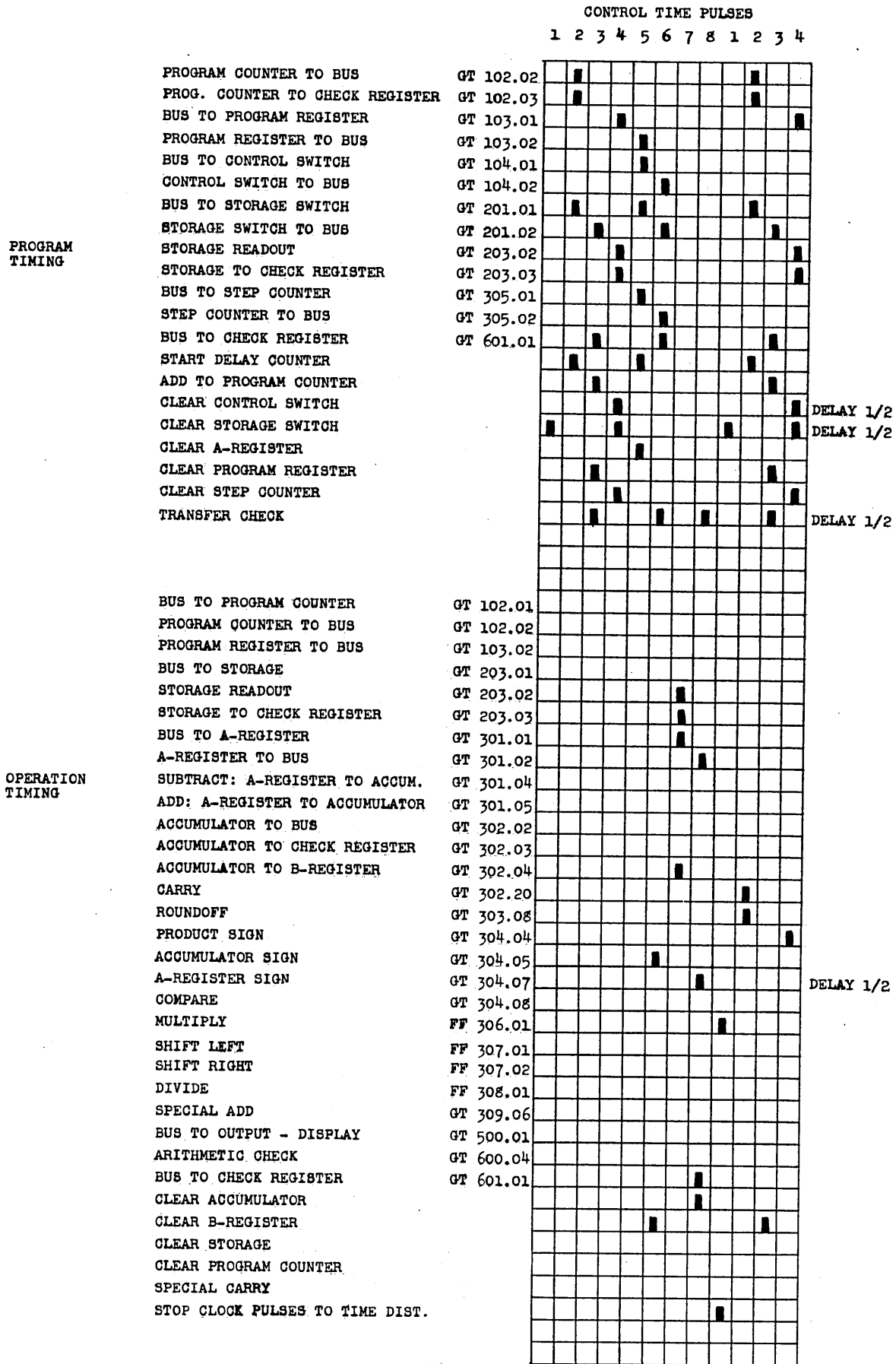


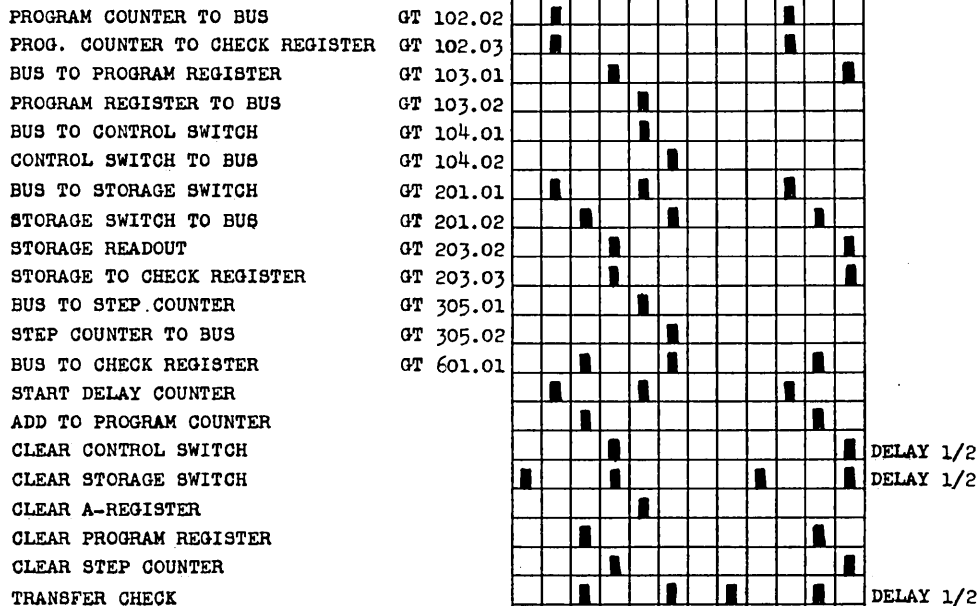
Figure 76

TIMING FOR MULTIPLY AND ROUND OFF

CONTROL TIME PULSES

1 2 3 4 5 6 7 8 1 2 3 4

PROGRAM  
TIMING



OPERATION  
TIMING

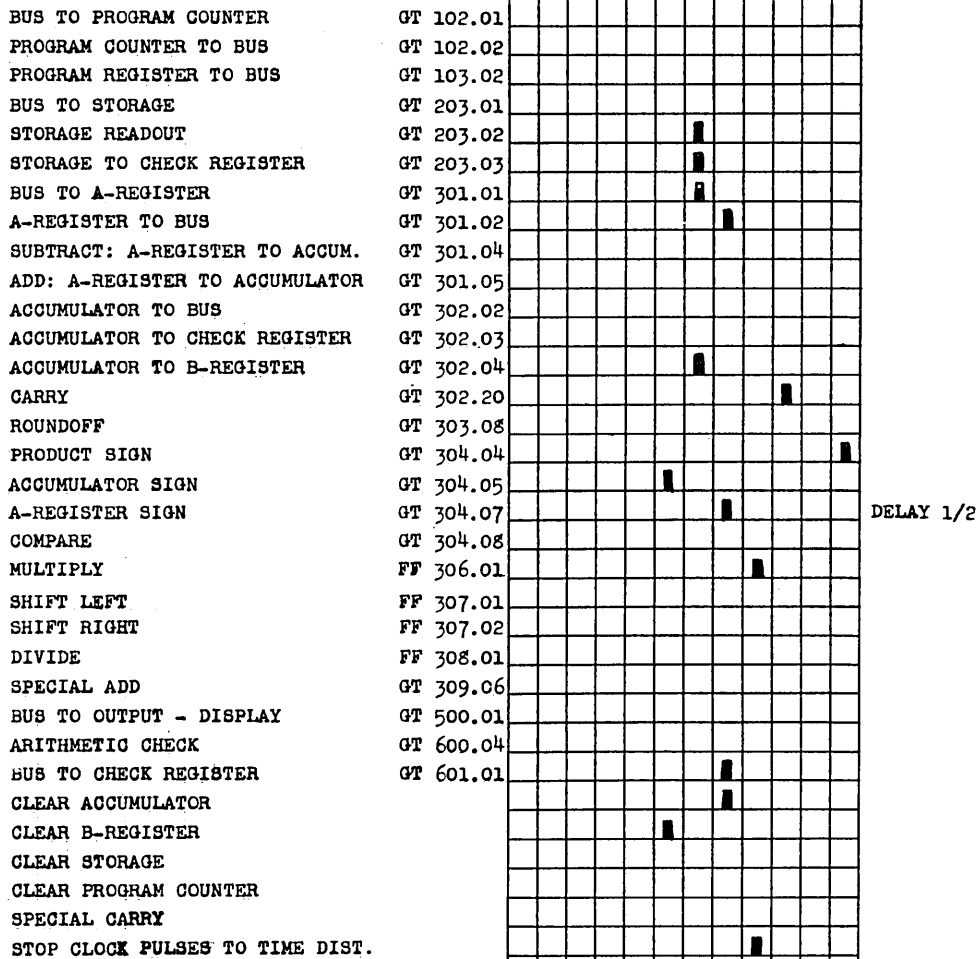


Figure 77

TIMING FOR MULTIPLY AND HOLD FULL PRODUCT

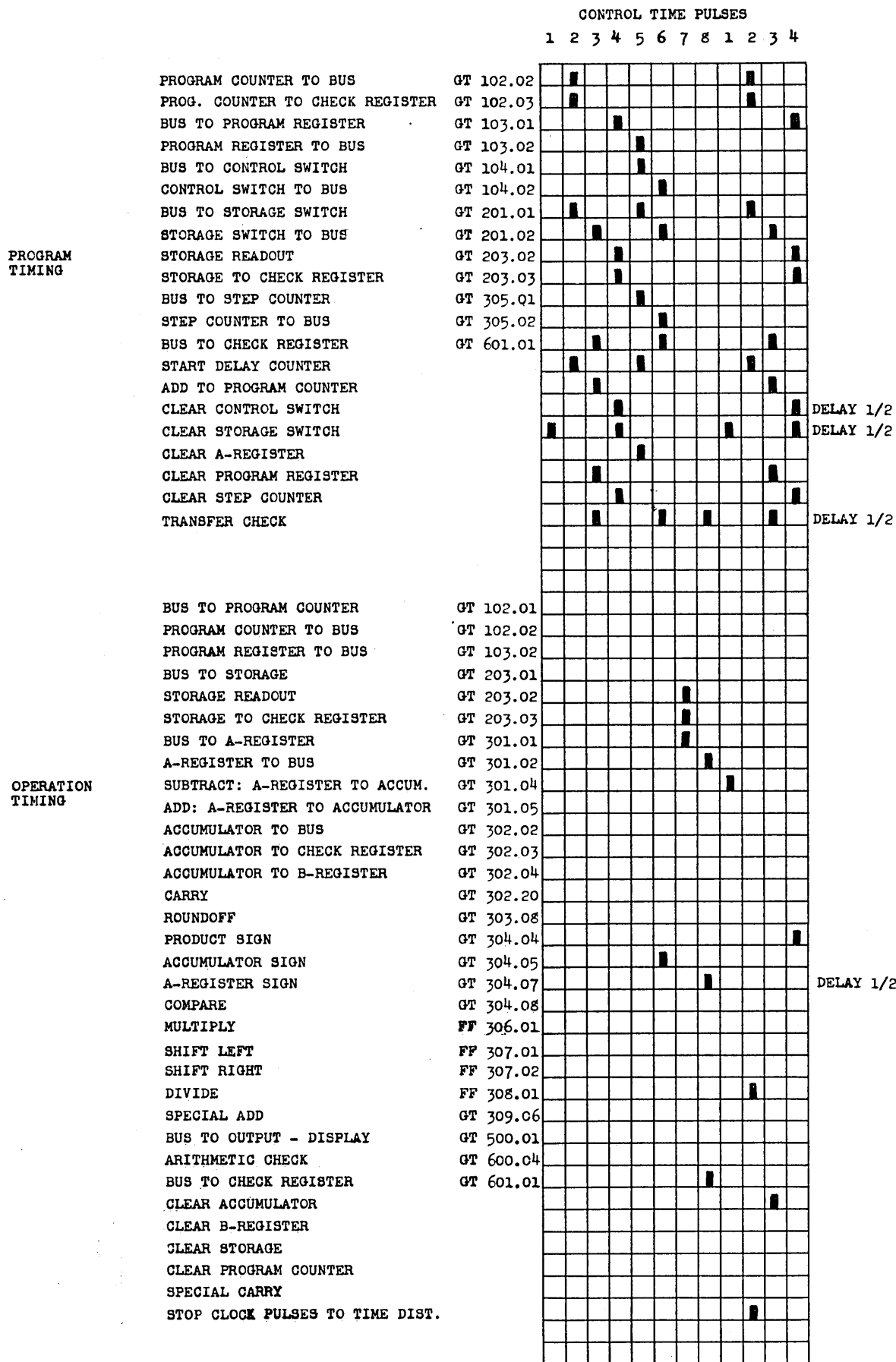


Figure 78

TIMING FOR DIVIDE

CONTROL TIME PULSES

1 2 3 4 5 6 7 8 1 2 3 4

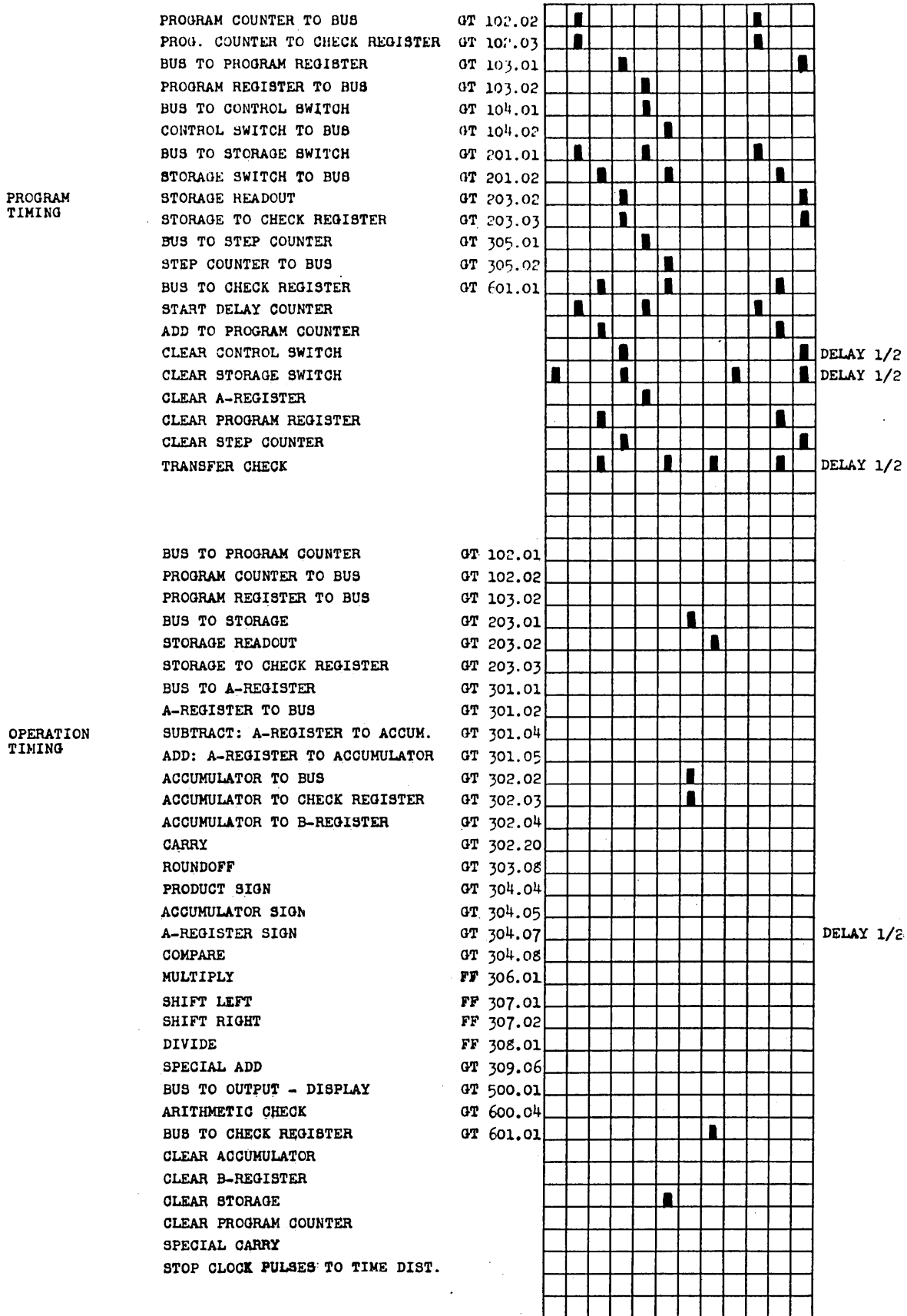


Figure 79

TIMING FOR TRANSFER TO STORAGE

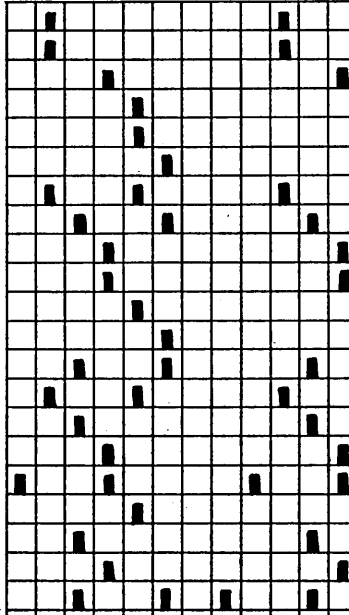
OPERATION: SHIFT RIGHT sr

CONTROL TIME PULSES

1 2 3 4 5 6 7 8 1 2 3 4

PROGRAM  
TIMING

PROGRAM COUNTER TO BUS	GT 102.02
PROG. COUNTER TO CHECK REGISTER	GT 102.03
BUS TO PROGRAM REGISTER	GT 103.01
PROGRAM REGISTER TO BUS	GT 103.02
BUS TO CONTROL SWITCH	GT 104.01
CONTROL SWITCH TO BUS	GT 104.02
BUS TO STORAGE SWITCH	GT 201.01
STORAGE SWITCH TO BUS	GT 201.02
STORAGE READOUT	GT 203.02
STORAGE TO CHECK REGISTER	GT 203.03
BUS TO STEP COUNTER	GT 305.01
STEP COUNTER TO BUS	GT 305.02
BUS TO CHECK REGISTER	GT 601.01
START DELAY COUNTER	
ADD TO PROGRAM COUNTER	
CLEAR CONTROL SWITCH	
CLEAR STORAGE SWITCH	
CLEAR A-REGISTER	
CLEAR PROGRAM REGISTER	
CLEAR STEP COUNTER	
TRANSFER CHECK	

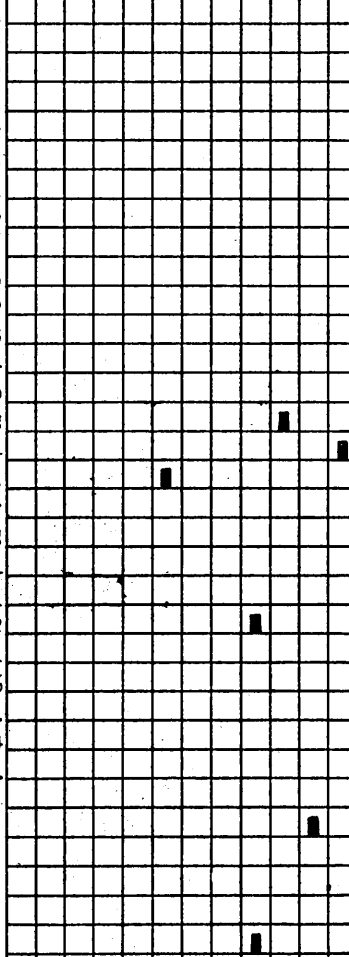


DELAY 1/2  
DELAY 1/2

DELAY 1/2

OPERATION  
TIMING

BUS TO PROGRAM COUNTER	GT 102.01
PROGRAM COUNTER TO BUS	GT 102.02
PROGRAM REGISTER TO BUS	GT 103.02
BUS TO STORAGE	GT 203.01
STORAGE READOUT	GT 203.02
STORAGE TO CHECK REGISTER	GT 203.03
BUS TO A-REGISTER	GT 301.01
A-REGISTER TO BUS	GT 301.02
SUBTRACT. A-REGISTER TO ACCUM.	GT 301.04
ADD: A-REGISTER TO ACCUMULATOR	GT 301.05
ACCUMULATOR TO BUS	GT 302.02
ACCUMULATOR TO CHECK REGISTER	GT 302.03
ACCUMULATOR TO B-REGISTER	GT 302.04
CARRY	GT 302.20
ROUND OFF	GT 303.08
PRODUCT SIGN	GT 304.04
ACCUMULATOR SIGN	GT 304.05
A-REGISTER SIGN	GT 304.07
COMPARE	GT 304.08
MULTIPLY	FF 306.01
SHIFT LEFT	FF 307.01
SHIFT RIGHT	FF 307.02
DIVIDE	FF 308.01
SPECIAL ADD	GT 309.06
BUS TO OUTPUT - DISPLAY	GT 500.01
ARITHMETIC CHECK	GT 600.04
BUS TO CHECK REGISTER	GT 601.01
CLEAR ACCUMULATOR	
CLEAR B-REGISTER	
CLEAR STORAGE	
CLEAR PROGRAM COUNTER	
SPECIAL CARRY	
STOP CLOCK PULSES TO TIME DIST	



DELAY 1/2

Figure 80

TIMING FOR SHIFT RIGHT

CONTROL TIME PULSES

1 2 3 4 5 6 7 8 1 2 3 4

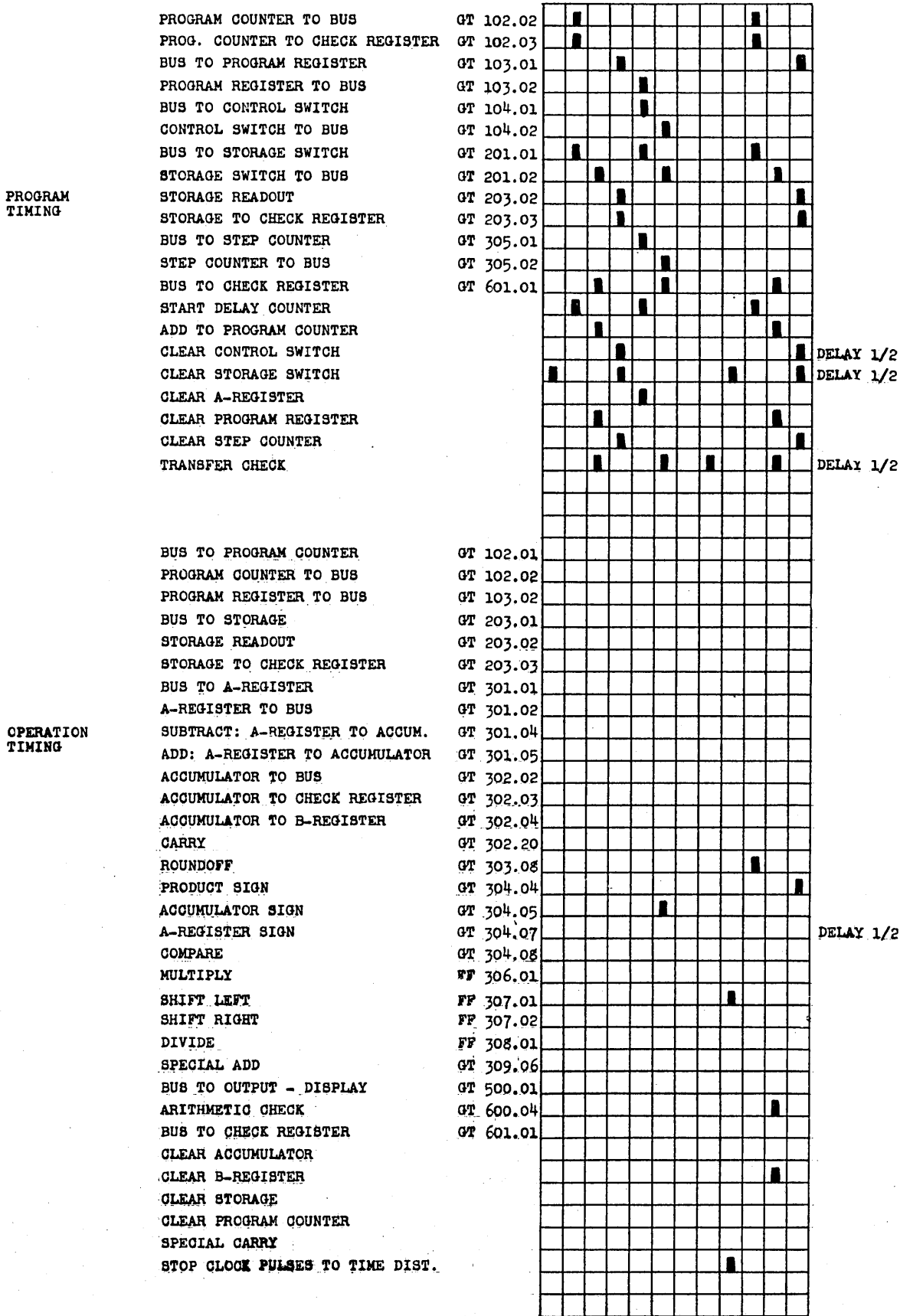


Figure 81

TIMING FOR SHIFT LEFT

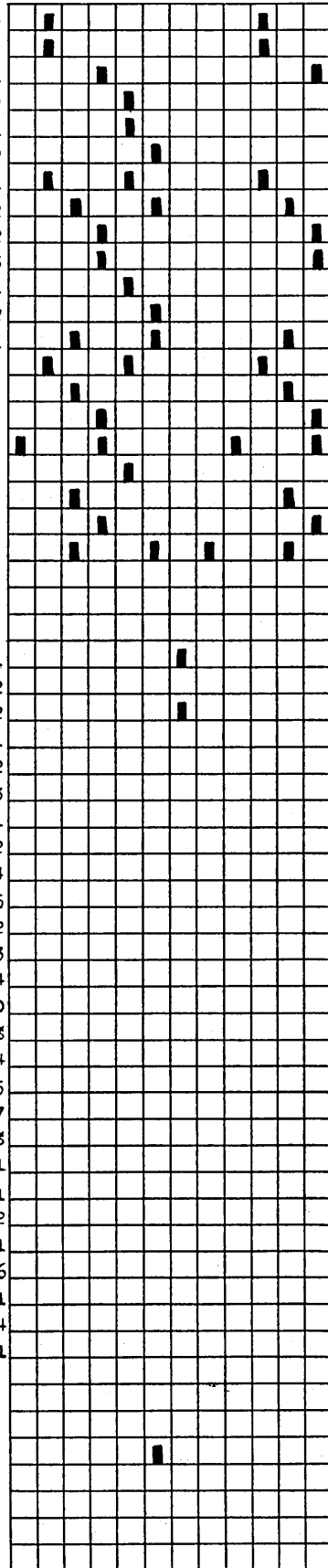


CONTROL TIME PULSES

1 2 3 4 5 6 7 8 1 2 3 4

PROGRAM  
TIMING

PROGRAM COUNTER TO BUS GT 102.02  
 PROG. COUNTER TO CHECK REGISTER GT 102.03  
 BUS TO PROGRAM REGISTER GT 103.01  
 PROGRAM REGISTER TO BUS GT 103.02  
 BUS TO CONTROL SWITCH GT 104.01  
 CONTROL SWITCH TO BUS GT 104.02  
 BUS TO STORAGE SWITCH GT 201.01  
 STORAGE SWITCH TO BUS GT 201.02  
 STORAGE READOUT GT 203.02  
 STORAGE TO CHECK REGISTER GT 203.03  
 BUS TO STEP COUNTER GT 305.01  
 STEP COUNTER TO BUS GT 305.02  
 BUS TO CHECK REGISTER GT 601.01  
 START DELAY COUNTER  
 ADD TO PROGRAM COUNTER  
 CLEAR CONTROL SWITCH  
 CLEAR STORAGE SWITCH  
 CLEAR A-REGISTER  
 CLEAR PROGRAM REGISTER  
 CLEAR STEP COUNTER  
 TRANSFER CHECK



DELAY 1/2  
 DELAY 1/2  
 DELAY 1/2

OPERATION  
TIMING

BUS TO PROGRAM COUNTER GT 102.01  
 PROGRAM COUNTER TO BUS GT 102.02  
 PROGRAM REGISTER TO BUS GT 103.02  
 BUS TO STORAGE GT 203.01  
 STORAGE READOUT GT 203.02  
 STORAGE TO CHECK REGISTER GT 203.03  
 BUS TO A-REGISTER GT 301.01  
 A-REGISTER TO BUS GT 301.02  
 SUBTRACT: A-REGISTER TO ACCUM. GT 301.04  
 ADD: A-REGISTER TO ACCUMULATOR GT 301.05  
 ACCUMULATOR TO BUS GT 302.02  
 ACCUMULATOR TO CHECK REGISTER GT 302.03  
 ACCUMULATOR TO B-REGISTER GT 302.04  
 CARRY GT 302.20  
 ROUND OFF GT 303.08  
 PRODUCT SIGN GT 304.04  
 ACCUMULATOR SIGN GT 304.05  
 A-REGISTER SIGN GT 304.07  
 COMPARE GT 304.08  
 MULTIPLY FF 306.01  
 SHIFT LEFT FF 307.01  
 SHIFT RIGHT FF 307.02  
 DIVIDE FF 308.01  
 SPECIAL ADD GT 309.06  
 BUS TO OUTPUT - DISPLAY GT 500.01  
 ARITHMETIC CHECK GT 600.04  
 BUS TO CHECK REGISTER GT 601.01  
 CLEAR ACCUMULATOR  
 CLEAR B-REGISTER  
 CLEAR STORAGE  
 CLEAR PROGRAM COUNTER  
 SPECIAL CARRY  
 STOP CLOCK PULSES TO TIME DIST.

DELAY 1/2

Figure 82

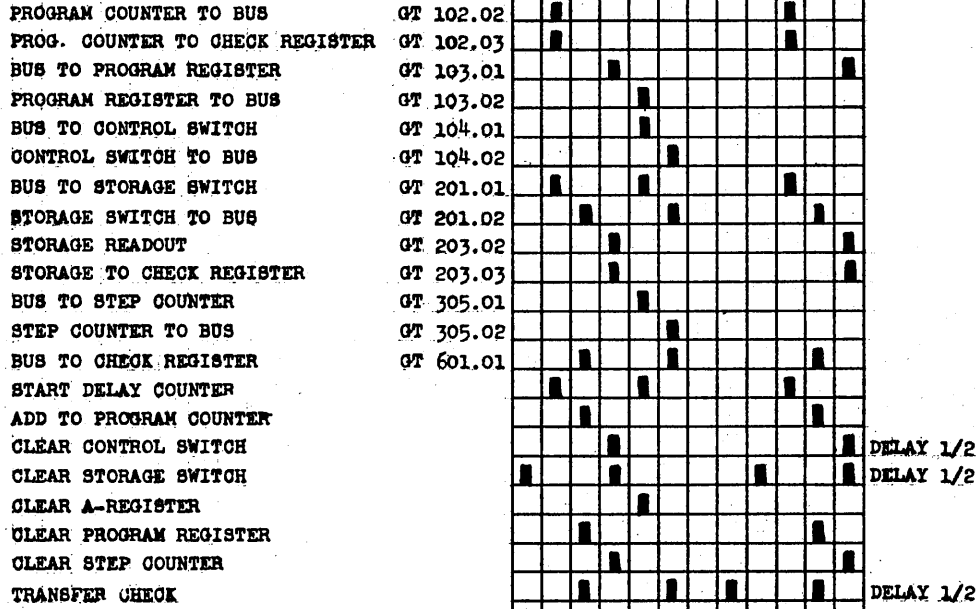
TIMING FOR SUBPROGRAM



CONTROL TIME PULSES

1 2 3 4 5 6 7 8 1 2 3 4

PROGRAM TIMING



OPERATION TIMING

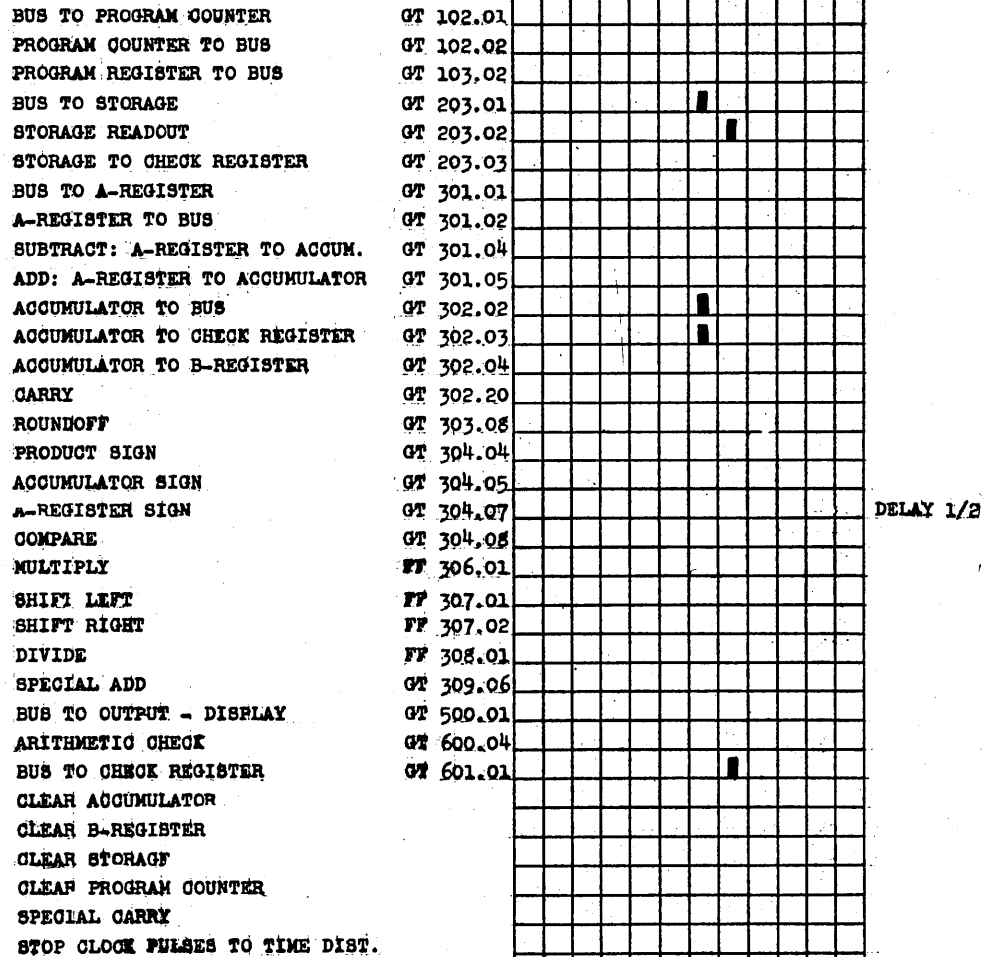


Figure 84

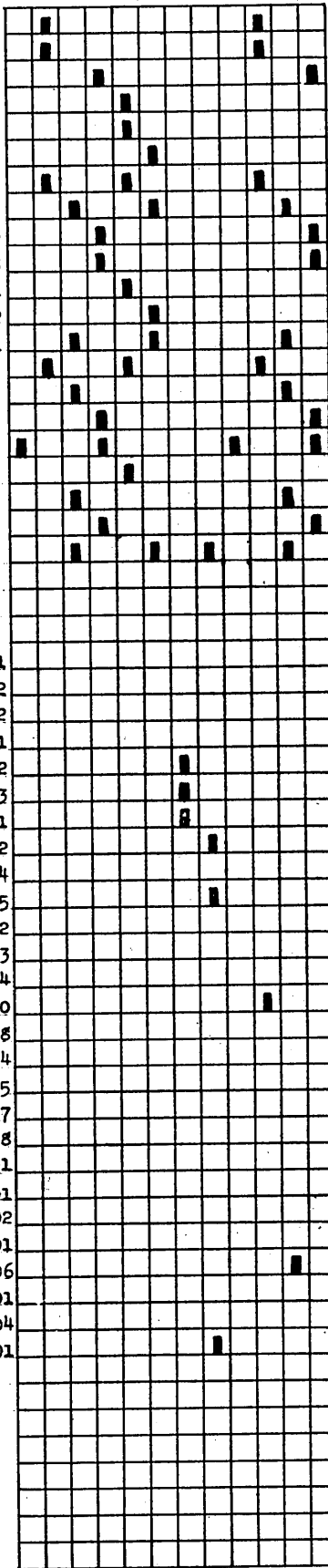
TIMING FOR TRANSFER DIGITS

CONTROL TIME PULSES

1 2 3 4 5 6 7 8 1 2 3 4

PROGRAM TIMING

PROGRAM COUNTER TO BUS GT 102.02  
 PROG. COUNTER TO CHECK REGISTER GT 102.03  
 BUS TO PROGRAM REGISTER GT 103.01  
 PROGRAM REGISTER TO BUS GT 103.02  
 BUS TO CONTROL SWITCH GT 104.01  
 CONTROL SWITCH TO BUS GT 104.02  
 BUS TO STORAGE SWITCH GT 201.01  
 STORAGE SWITCH TO BUS GT 201.02  
 STORAGE READOUT GT 203.02  
 STORAGE TO CHECK REGISTER GT 203.03  
 BUS TO STEP COUNTER GT 305.01  
 STEP COUNTER TO BUS GT 305.02  
 BUS TO CHECK REGISTER GT 601.01  
 START DELAY COUNTER  
 ADD TO PROGRAM COUNTER  
 CLEAR CONTROL SWITCH  
 CLEAR STORAGE SWITCH  
 CLEAR A-REGISTER  
 CLEAR PROGRAM REGISTER  
 CLEAR STEP COUNTER  
 TRANSFER CHECK



DELAY 1/2  
 DELAY 1/2

DELAY 1/2

OPERATION TIMING

BUS TO PROGRAM COUNTER GT 102.01  
 PROGRAM COUNTER TO BUS GT 102.02  
 PROGRAM REGISTER TO BUS GT 103.02  
 BUS TO STORAGE GT 203.01  
 STORAGE READOUT GT 203.02  
 STORAGE TO CHECK REGISTER GT 203.03  
 BUS TO A-REGISTER GT 301.01  
 A-REGISTER TO BUS GT 301.02  
 SUBTRACT: A-REGISTER TO ACCUM. GT 301.04  
 ADD: A-REGISTER TO ACCUMULATOR GT 301.05  
 ACCUMULATOR TO BUS GT 302.02  
 ACCUMULATOR TO CHECK REGISTER GT 302.03  
 ACCUMULATOR TO B-REGISTER GT 302.04  
 CARRY GT 302.20  
 ROUND OFF GT 303.08  
 PRODUCT SIGN GT 304.04  
 ACCUMULATOR SIGN GT 304.05  
 A-REGISTER SIGN GT 304.07  
 COMPARE GT 304.08  
 MULTIPLY FF 306.01  
 SHIFT LEFT FF 307.01  
 SHIFT RIGHT FF 307.02  
 DIVIDE FF 308.01  
 SPECIAL ADD GT 309.06  
 BUS TO OUTPUT - DISPLAY GT 500.01  
 ARITHMETIC CHECK GT 600.04  
 BUS TO CHECK REGISTER GT 601.01  
 CLEAR ACCUMULATOR  
 CLEAR B-REGISTER  
 CLEAR STORAGE  
 CLEAR PROGRAM COUNTER  
 SPECIAL CARRY  
 STOP CLOCK PULSES TO TIME DIST.

DELAY 1/2

Figure 85

TIMING FOR SPECIAL ADD

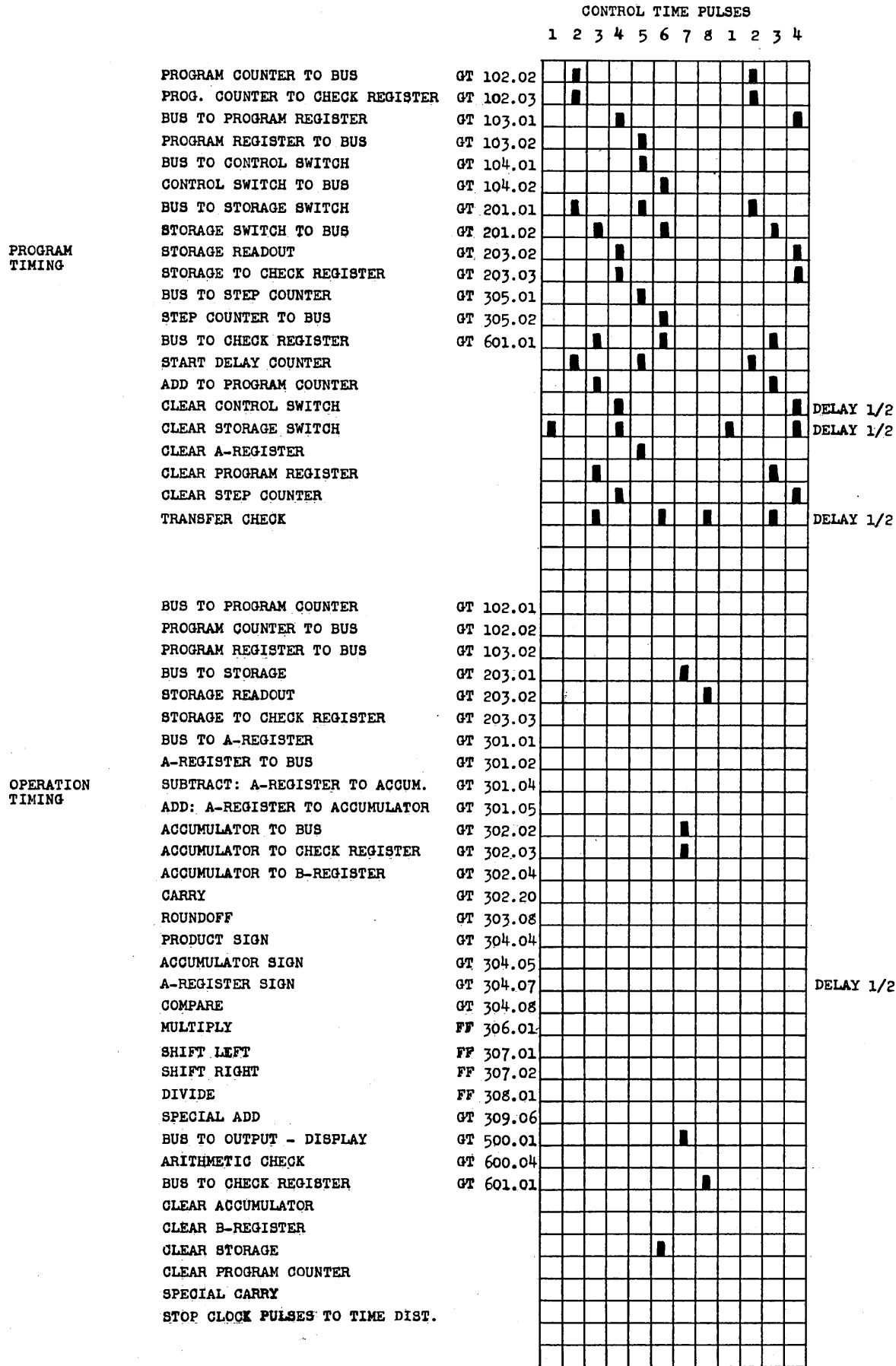


Figure 86  
TIMING FOR STORE AND DISPLAY

UNIT CODE NUMBERS

100 Control

101 Master Clock  
 102 Program Counter  
 103 Program Register  
 104 Control Switch  
 105 Operation Matrix  
 106 Time Pulse Distributor  
 107 Operation Timing Matrix  
 108 Program Timing Matrix  
 109 Repeat Switch - (Removed from System)

200 Storage

201 Switch  
 202 Toggle Switch Storage  
 203 Flip Flop Storage

300 Arithmetic Element

301 A-Register  
 302 Accumulator  
 303 B-Register  
 304 Sign Control  
 305 Step Counter  
 306 Multiply  
 307 Shift  
 308 Divide

400 Input

500 Output

600 Checking

601 Check Register

LETTER SYMBOLS

AC Accumulator  
 BA Buffer Amplifier  
 BC Binary Coder  
 BD Bus Driver  
 DE Delay Element  
 ES Electronic Switch  
 FD Frequency Divider  
 FF Flip Flop  
 GT Gate Tube Circuit  
 IC Intensity Control Circuit  
 PF Pulse Forming Circuit  
 ST Storage Tube  
 TG Trigger Pulse Generator  
 TP Timing Pulse Generator  
 TT Trigger Tube

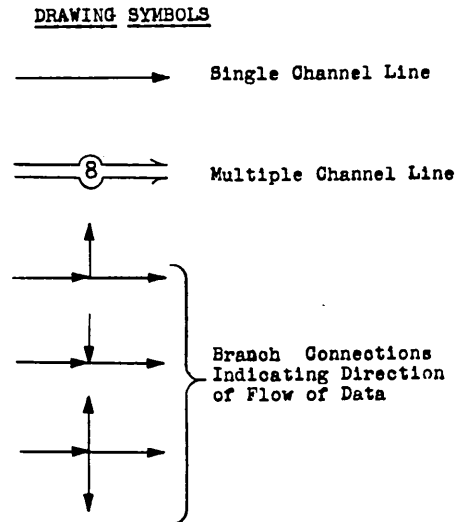


Figure 87  
 PARALLEL DIGIT COMPUTER CODES

USN

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