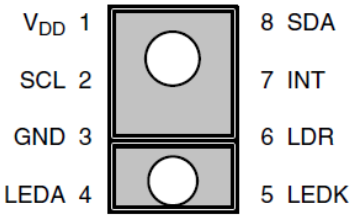
Description

HALS3300 is an optical digital heart rate sensor, 525nm green LED and driver in a single 8-pin package.

The sensor incorporates with a fast, two-wire I^2C bus (up to 800kHz) to communicate with micro-controller or embedded system. Its excellent background light rejection allows the device to operate in environments from sunlight to dark rooms.

The heart rate sensing is realized by using an 525nm green light LED with current driver, a reflection light detector for the PPG signal from the human body, as well as heart rate algorithm.

PACKAGE
MODULE–8
(TOP VIEW)



Package Drawing is Not to Scale

Typical heart rate measurement samples the reflected PPG signal at a frequency of 25Hz, then the resulting light intensity signal can be transferred to the host controller by I2C interface and the heart rate is calculated by the controller utilizing the algorithm.

The device can be used in a health wearable devices, such as sport band or smart watch. Its signal can also be analyzed to indicate the detach of the device.

Features

- **Heart Rate Sensor: 525nm wavelength PPG signal and provide algorithm**
- **HRS: Programmable green light intensity and analog gain**
- **HRS sensor with reduced background noise**
- **ALS cancellation**
- **I^2C interface(up to 800kHz)**
- **Low power consumption**

- **Wide Input Voltage: From 2.3V to 3.6V**
- **Package size:3.94mm×2.36mm×1.35mm**
- **Pb free and ROHS compliant**

Function Block Diagrams

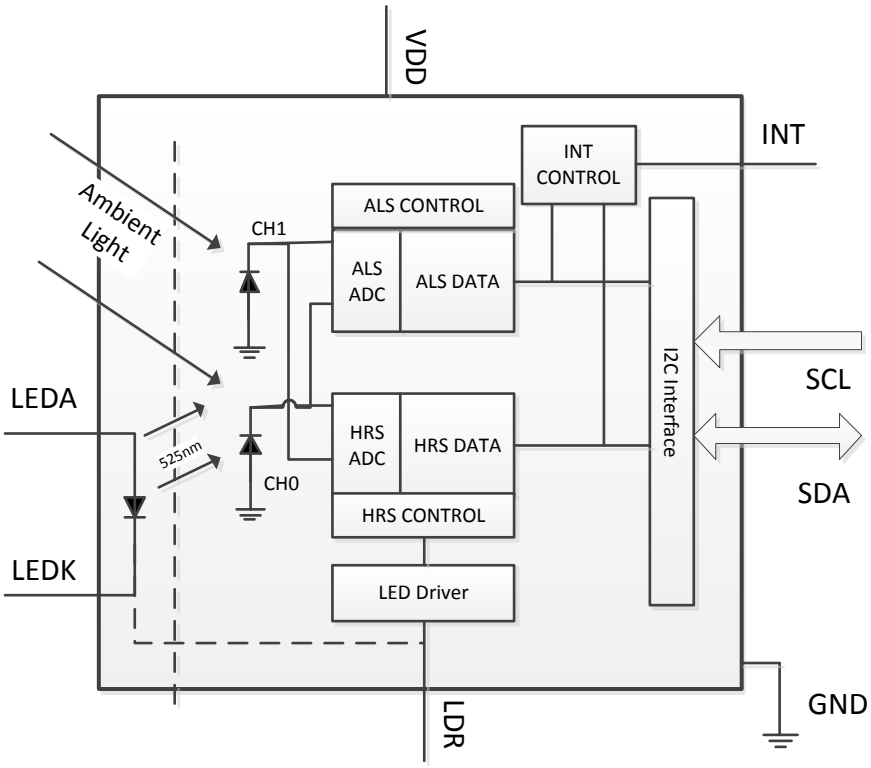


Figure 1. Function Block Diagrams

Note:

1. LEDK and LDR terminals are shorted internally in the package, to be compatible with most PCB designs for sensors with internal LED driver.
2. For PCB traces connecting to LEDK and LDR, they can be shorted or leave float, but not connect to ground.

Applications

- Sport Bands
- Smart Watch
- Children Watch
- Wearable Health Devices
- Sensor Application

Terminal Functions

PIN	Name	Type	Description
1	VDD		Power supply voltage
2	SCL	I	I^2C serial clock input terminal-clock signal for I^2C serial data
3	GND		Power supply ground
4	LEDA	I	LED anode
5	LEDK	O	LED cathode, connect to LDR pin internally.
6	LDR	I	LED driver for Green LED, connect to LEDK pin internally.
7	INT	O	Interrupt-open drain
8	SDA	I/O	I^2C serial data I/O terminal-serial data I/O for I^2C –open drain

Specifications

Absolute Maximum Ratings(T_a=25℃, unless otherwise specified)

Parameter	Symbol		Unit
Supply voltage	V_{DD}	4.0	V
Digital output voltage range	V_O	-0.5 to 4.0	V
Digital output current	I_O	-1 to 10	mA
Analog voltage range	LDR	-0.5 to 5.5	V
Storage temperature	T_{stg}	-40 to 85	℃
ESD tolerance(HBM)		3000	V

Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	2.3	3	3.6	V
Supply voltage accuracy	-10		10	%
Operating free-air temperature, T_a	-30		85	℃

Operating Characteristics(V_{DD}=3.3V,Ta=25℃, HRS sample time 40ms, unless otherwise specified, ALS resolution is 14bit, HRS resolution is 14bit)

Parameter	Min	Typ.	Max	Unit	Description
I_{DD}	---	0.01	0.1	μA	Supply current: Sleep mode
	---	110	115	μA	Supply current, HRS on
	---	2.6	2.8	mA	LEDA current ,HRS on
V_{OLSDA}	0		0.4	V	SDA output low voltage: 3mA sink current

V_{OLINT}	0		0.4	V	INT output low voltage: 3mA sink current
I_{LEAK}	---	0.03	0.05	μA	Leakage current, SDA pin
	---	0.01	0.05	μA	Leakage current, SCL pin
	---	0.02	0.05	μA	Leakage current, INT pin
	---	0.01	0.05	μA	Leakage current, LDR pin
V_{IL}			0.55	V	SCL, SDA input low voltage
V_{IH}	1.25			V	SCL, SDA input high voltage

Electrical Characteristics(V_{DD}=V_{LEDA}=3.3V , T_a=25℃, unless otherwise specified, HRS resolution is 14bit)

Parameter	Test Conditions	Min	Typ.	Max	Units
Dark ALS ADC count	E_e=0,AGAIN=1	0	3	5	counts
ALS ADC integration time		---	100	---	ms
HRS ADC conversion time			25		ms
HRS Cycle Wait Time		0	12.5	800	ms
LED current, I_{LED} [2]	PDRIVE=00		12.5		mA
	PDRIVE=01		20		
	PDRIVE=10		30		
	PDRIVE=11		40		

Notes:

1. The 525nm LED with peak 525nm and spectral half-width $\Delta\lambda^{1/2}$=20nm is used for final mass product testing.
2. No reflective surface above the module.
3. No glass or aperture above the module. Tested value is the average of 5 consecutive reading.

AC Electrical Characteristics(V_{DD}= 3V,T_a=25℃,unless otherwise specified)

Parameter	Symbol	Min.	TYP	Max.	Units
Clock Frequency	f_{SCL}	0		800	kHz
Bus free time between start and stop condition	t_{BUF}	1.3			μs
Hold time(repeated) START condition After this period, the first clock pulse is generated	t_{HDSTA}	0.6			μs
Set-up time for a repeated START condition	t_{SUSTA}	0.6			μs
Set-up time for STOP condition	t_{SUSTO}	0.6			μs
Data hold time	t_{HDDAT}	0			μs
Data setup time	t_{SUDAT}	100			ns
SCL clock low period	t_{LOW}	1.3			μs
SCL clock high period	t_{HIGH}	0.6			μs
Clock/data fall time	t_F			300	ns
Clock/data rise time	t_R			300	ns
Input pin capacitance	C_i			10	pF

Note：Specified by design and characterization.

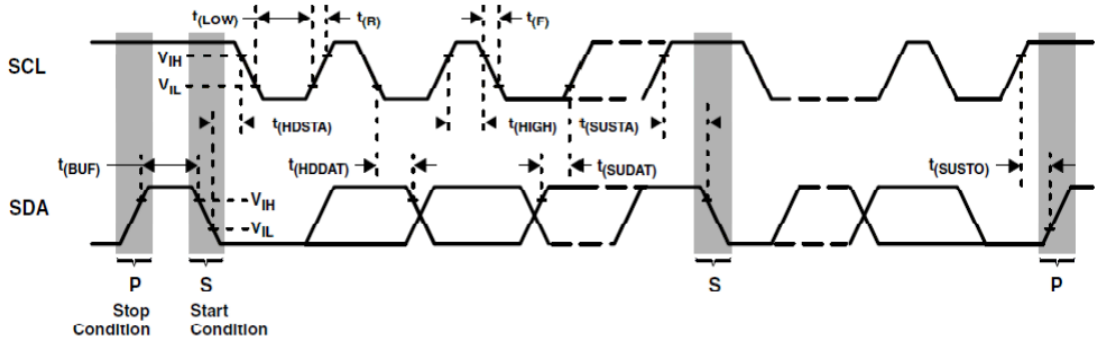


Figure 2. Timing Diagram

Application Note

Heart rate sensor

Heart rate measurement is accomplished by measuring the reflected amount of green energy from the internal green LED. Light rays emitting from the internal green LED, reflecting back from the skin of human, and being absorbed by the photo-diode. The internal green LED is driven by the integrated current driver. The LED current driver provides a regulated current sink on the LDR terminal that eliminated the need for an external current limiting resistor. The PDRIVE(PDRIVE[1] register 0x01,bit 3, PDRIVE[0] register 0x0C,bit 6) register setting sets the sink current from 12.5mA to 40mA. The heart rate engine uses a novel technique to suppress background noise effectively. Then the HRS ADC converts a value and stores the result in (CH0DATAx) register

I^2C Protocol

Interface and control are accomplished through an I^2C serial compatible interface to a set of registers that provide access to device control functions and output data. The address of HALS3300 is 0x44, the device also supports the 7-bit I^2C addressing protocol.

HALS3300 supports the standard writing and reading protocol. The register index will automatically increase by 1 after the addressed register has been accessed (read or write).

A Acknowledge (0)

P Stop Condition

R Read (1)

S Start Condition

W Write (0)

Sr Repeated Start Condition

■ Master-to- Slave

□ Slave-to-Master

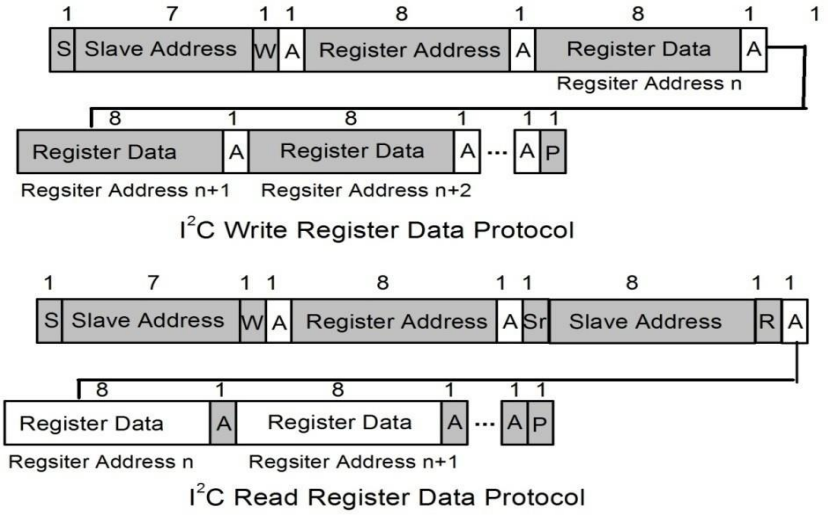


Figure 2. I^{2}C Protocols

Register Set

The device is controlled and monitored by data registers accessible through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The register set is summarized in Table 1.

Table 1. Register Address

Address	name	R/W	function	Recommend Value
0x00	ID	R/W	Device ID	0x21
0x01	Enable	R/W	Enable HRS	0x68
0x08	C1DATAM	RO	CH1 data register bit 10~3	0x00
0x09	C0DATAM	RO	CH0 data register bit 15~8	0x00
0x0A	C0DATAH	RO	CH0 data register bit 7~4	0x00
0x0C	PDRIVER	R/W	HRS LED driver/PON/PDRIVE[0]	0x68
0x0D	C1DATAH	RO	CH1 data register bit 17~11	0x00
0x0E	C1DATAL	RO	CH1 data register bit 2~0	0x00
0x0F	C0DATAL	RO	CH1 data register bit 17~16 and 3~0	0x00
0x16	RES	R/W	ALS and HRS resolution	0x66
0x17	HGAIN	R/W	HRS gain	0x10

ID Register(0x00)

The ID Register(read-only) provides the value for the part number.

Table 2. ID Register

BITS	FIELD	Description
7:0	ID	0x21

ENABLE Register(0x01)

The ENABLE register is used to enable and disable ALS and HRS functions.

Table 3. ENABLE Register

BITS	FIELD	Description
7	HEN	HRS enable. This bit activates the HRS function. Writing a 1 enables. Writing a 0 disables
6:4	HWT	HRS wait time
		000:wait time between each conversion cycle is 800 ms
		001:wait time between each conversion cycle is 400 ms
		010:wait time between each conversion cycle is 200 ms
		011:wait time between each conversion cycle is 100 ms
		100:wait time between each conversion cycle is 75 ms
		101:wait time between each conversion cycle is 50 ms
		110:wait time between each conversion cycle is 12.5 ms
		111:wait time between each conversion cycle is 0 ms
3	PDRIVE[1]	Bit1 for LED drive current setup, see also Register 0xOC Bit6.
		00: set current 12.5mA
		01: set current 20mA
		10: set current 30mA
		11: set current 40mA
2:0	Reserved	Reserved

CH1 Data register(0x08,0x0D,0x0E)

Table 4. ALS Data Register

BITS	ADDRESS	REGISTER	Description
7:0	0x08	C1DATA[10:3]	CH1 data register
6:0	0x0D	C1DATA[17:11]	CH1 data register
2:0	0x0E	C1DATA[2:0]	CH1 data register

CH0 Data Register(0x09,0x0A,0x0F)

Table 5. HRS Data Register

BITS	ADDRESS	REGISTER	Description
7:0	0x09	C0DATA[15:8]	CH0 data register
3:0	0x0A	C0DATA[7:4]	CH0 data register
5:4 3:0	0x0F	C0DATA[17:16] C0DATA[3:0]	CH0 data register

HRS LED Driver Set Register (0x0C)

Table 6. HRS LED Driver Set Register

BIT	FIELD	Description
7	Reserved	Reserved
6	PDRIVE[0]	Bit0 for LED drive current setup, see also Register 0x01 Bit3.
		00: set current 12.5mA
		01: set current 20mA
		10: set current 30mA
		11: set current 40mA
5	PON	Write 1 active OSC, write 0 disable OSC. Generate PD signal to analog(0 for work, 1 for Power down)
4	Reserved	Reserved
3:0	Reserved	Reserved

RESOLUTION Register(0x16)

The RESOLUTION register is used to control resolution of ALS ADC and HRS ADC.

Table 7. Resolution Register

BIT	FIELD	Description
7:4	Reserved	
3:0	ALS_RES	ALS ADC resolution. Generate TSEL to analog in ALS mode. 0000: 8 bits 0001 9 bits 0010: 10 bits 0011: 11 bits 0100: 12 bits 0101: 13 bits 0110: 14 bits 0111: 15 bits 1000: 16 bits 1001: 17 bits others: 18 bits

HGAIN Register(0x17)

The HGAIN register is used to control the gain of HRS ADC.

Table 8. HGAIN Register

BIT	FIELD	Description	
7:5	Reserved	Reserved	
4:2	HGAIN	FIELD VALUE	HRS gain
		000	×1
		001	×2
		010	×4
		011	×8
		Other	×64
1:0	Reserved	Reserved	

Application Information

A typical application for HALS3300 is shown in Figure 3. The I^2C signals and the Interrupt are open-drain outputs and require pull-up resistor (R_P). It is recommended use 1.5 kΩ resistor when running at 400kbps. Pin INT can be disconnected in typical HRS application mode .

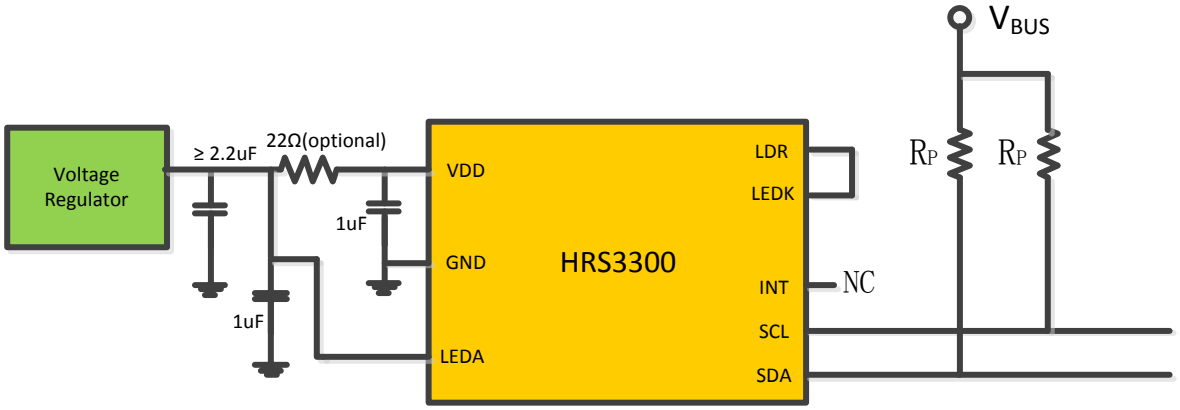


Figure 3. Typical Application Schematic Diagram

The 1uF decoupling capacitor between VDD and GND must be placed close to the sensor package , recommended distance in 0.5mm .

PCB Pad Layout

Suggest PCB pad layout guidelines for the surface module are shown in Figure4. Flash Gold is recommended surface finish for the landing pads.

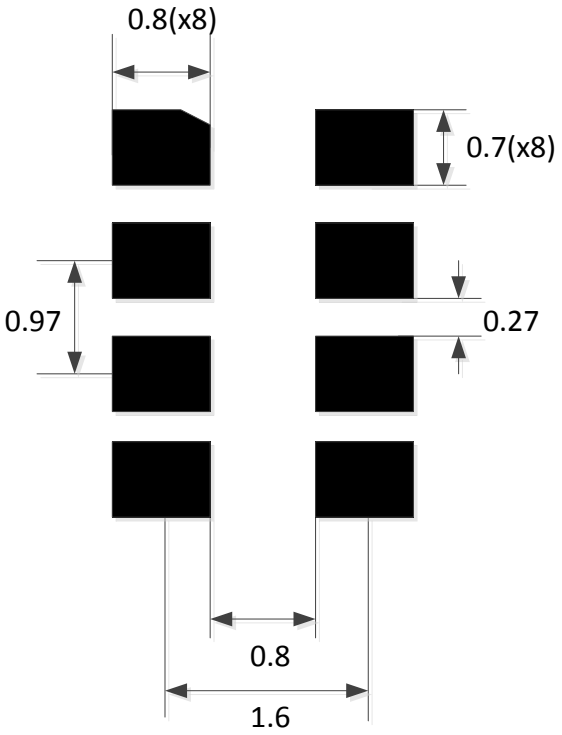


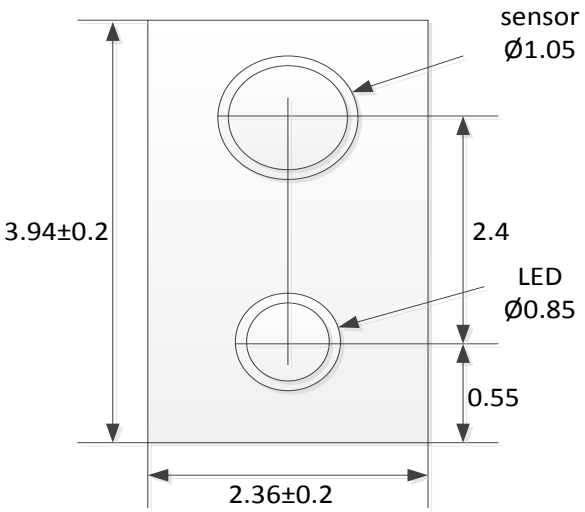
Figure 4. Suggested Module PCB layout

Note: All linear dimensions are in mm

Package Information

MODULE

Top View



Bottom View

Side View

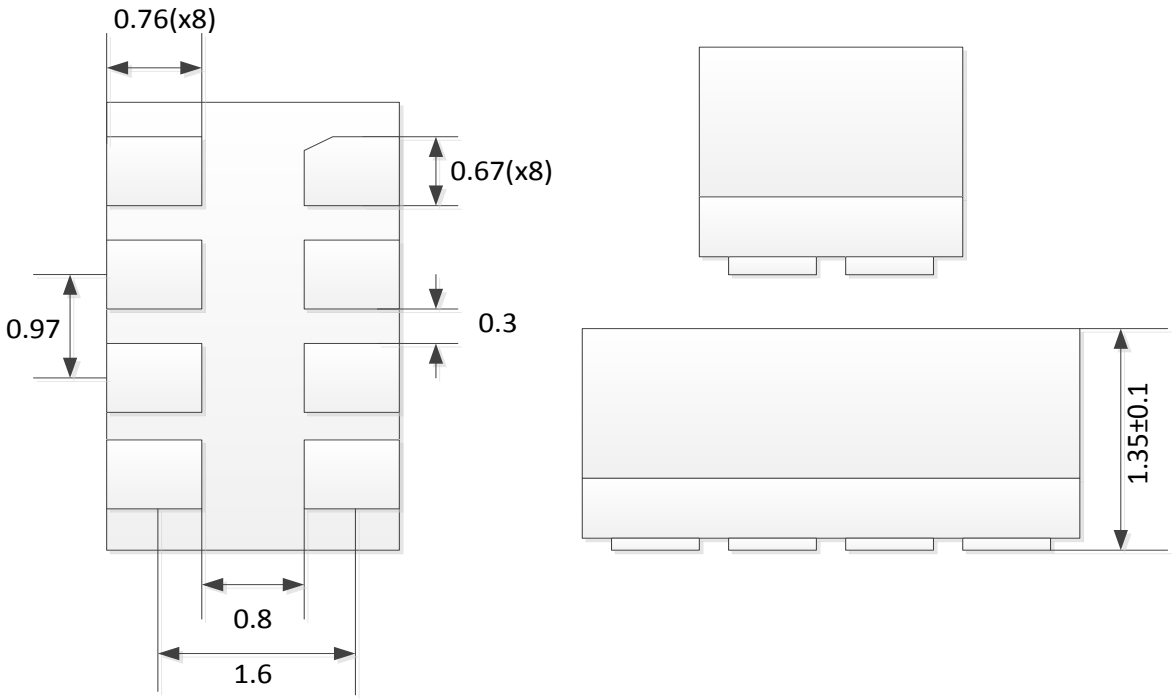


Figure 5. Package information

Notes: All linear dimensions are in mm. Dimension tolerance is ±0.05mm unless otherwise noted.

Soldering Information

The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The process, equipment, and material used in these test are detailed below. The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Table 9. Solder Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5℃/sec
Soak time	t_{soak}	2 to 3 minutes
Time above 217℃ (T_1)	t_1	Max 60 sec
Time above 230℃ (T_1)	t_2	Max 50 sec
Time above T_{peak}-10℃ (T_3)	t_3	Max 10 sec
Peak temperature in reflow	T_{peak}	260℃
Temperature gradient in cooling		Max-5℃/sec

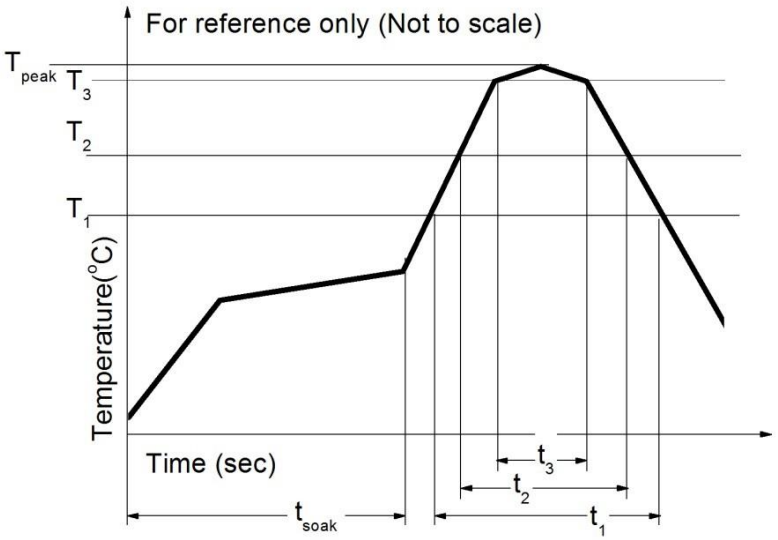


Figure 6. Solder reflow profile graph